Low Voltage Stepper Motor Driver

Features

- **Operating voltage: from 1.8 to 10V**
- **Maximum output current: 1.3A$_{rms}$**
- **$R_{DS(ON)}$ HS + LS = 0.4Ω typ.**
- **Microstepping up to 1/256th of a step**
- **Current control with programmable off-time**
- **Full protection set**
  - **Non-dissipative overcurrent protection**
  - **Short-circuit protection**
  - **Thermal shutdown**
- **Energy saving and long battery life with standby consumption less than 80nA**

Applications

Battery-powered stepper motor applications such as:

- **Pop-up camera control for smartphones**
- **Point of sale (POS) devices**
- **Portable printers**
- **PC peripherals and accessories**
- **Robotics**
- **Toys**
- **Reflex cameras**

General Description

The G2069 is a stepper motor driver which integrates, in a small QFN3X3-16 package, both control logic and a low $R_{DS\ (on)}$ power stage.

The integrated controller implements PWM current control with fixed OFF time and a microstepping resolution up to 1/256th of a step.

The device is designed to operate in battery-powered scenarios and can be forced into a zero-consumption state, allowing a significant increase in battery life.

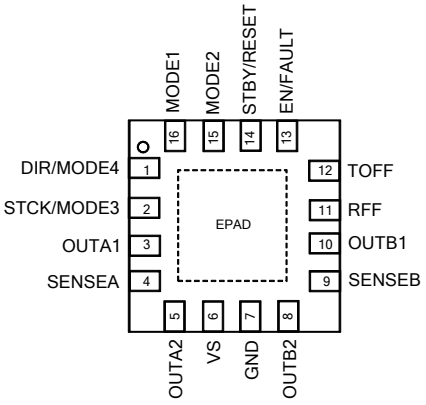
The device offers a complete set of protection features including overcurrent, overtemperature and short-circuit protection.

Ordering Information

ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE (Green)
G2069Q41U	2069	-40°C to +85°C	QFN3X3-16

Note: Q4: QFN3X3-16
1: Bonding Code
U : Tape & Reel
Green : Lead Free / Halogen Free.

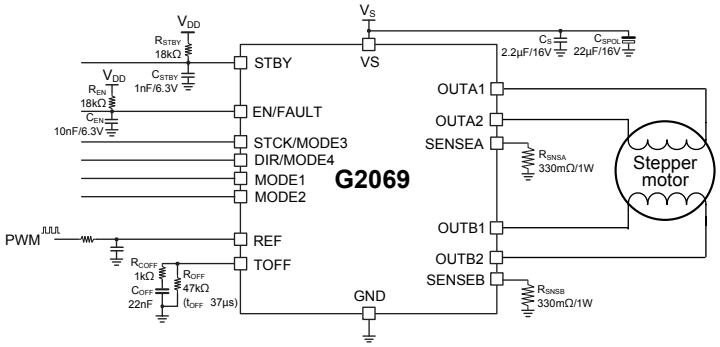
Pin Configuration



G2069 QFN3X3-16

Note: Recommend connecting the Thermal Pad to the Ground for excellent power dissipation.

Typical application schematic



Absolute Maximum Ratings

Supply voltage (V_S) . . . . . -0.3V to 11V
Logic input voltage (V_{IN}) . . . . . -0.3V to 5.5V
Output-to-sense voltage drop ($V_{OUT} – V_{SENSE}$) . . . . . .up to 12V
Supply-to-output voltage drop ($V_S – V_{OUT}$) . . .up to 12V
Sense pin voltage (V_{SENSE}). . . . . .-1V to 1V
Reference voltage input (V_{REF}) . . . . . -0.3V to 1V
Continuous power stage output current (each bridge) ($I_{OUT,RMS}$) . . . . . 0.3A_{rms}
Thermal Resistance of Junction to Ambient, (θ_{JA})
QFN3X3-16 . . . . . .TBD°C/W
Continuous Power Dissipation (T_A = +25°C)
QFN3X3-16. . . . . .TBDW

Operative junction temperature ($T_{j,OP}$) . . . . . -40°C to 150°C
Storage junction temperature ($T_{j,STG}$) . . . . . -55°C to 150°C
ESD (HBM) 2kV
ESD (CDM) 500V

Recommended operating conditions

Supply voltage (V_S) . . . . . 1.8V to 10V
Logic input voltage (V_{IN}) . . . . . 0V to 5V
Reference voltage input (V_{REF}) . . . . . -0.1V to0.5V
Logic inputs positive/negative pulse width (t_{INw}) 300ns

Electrical Characteristics

(V_S =5V, Tj=25°C unless otherwise specified.)

The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply						
V_S turn-on voltage	$V_{Sth\ (ON)}$	VS rising from 0V	1.45	1.65	1.79	V
V_S turn-off voltage	$V_{Sth(OFF)}$	VS falling from 5V	1.3	1.45	1.65	V
V_S hysteresis voltage	$V_{Sth(HYS)}$		---	180	---	mV
V_S supply current	I_S	No commutations EN='0' R_{OFF}=160kΩ	---	960	1300	µA
		No commutations EN='1' R_{OFF}=160kΩ	---	1500	1950	
V_S standby current	$I_{S,STBY}$	STBY=0 V	---	10	80	nA
Standby low logic level input voltage	V_{STBYL}		---	---	0.9	V
Standby high logic level input voltage	V_{STBYH}		1.48	---	---	V
Power stage						
Total ON resistance HS+LS	$R_{DS\ (ON)HS+LS}$	V_S=10V, I_{OUT}=1.3A	---	0.4	0.65	Ω
		V_S=10V, I_{OUT}=1.3A, T_j=125°C(1)	---	0.53	0.87	
		V_S=3V, I_{OUT}=0.4A	---	0.53	0.8	
Leakage current	I_{DSS}	OUTx=V_S	---	---	1	µA
		OUTx=GND	-1	---	---	
Freewheeling diode forward voltage	V_{DF}	I_D=1.3A	---	0.9	---	V
Rise time	t_{rise}	V_S=10V;unloaded outputs	---	10	---	ns
Fall time	t_{fall}	V_S=10V;unloaded outputs	---	10	---	ns
Dead time	t_{DT}		---	50	---	ns
Current control						
Sensing offset	$V_{SNS,OFFSET}$	V_{REF}=0.5V; Internal reference 20% V_{REF}	-15	---	+15	mV
Total OFF time	t_{OFF}	R_{OFF}=10kΩ	---	9	---	µs
		R_{OFF}=160kΩ	---	125	---	µs
Internal oscillator precision ($f_{OSC}/f_{OSC,ID}$)	Δf_{OSC}	R_{OFF} =20kΩ	-20	---	+20	%
Total OFF time jittering	$t_{OFF,jitter}$	R_{OFF} =10kΩ	---	---	2	%
Slow decay time	$t_{OFF,SLOW}$		---	5/8 ×t_{OFF}	---	µs
Fast decay time	$t_{OFF,FAST}$		---	3/8 ×t_{OFF}	---	µs

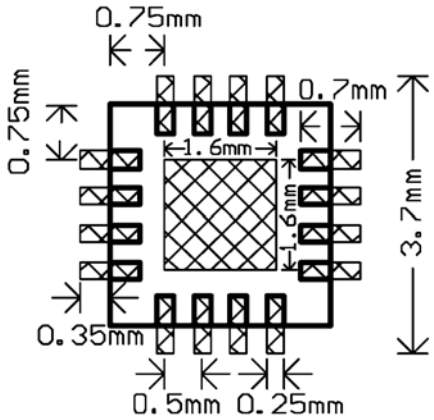
Electrical Characteristics (Continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logic IOs						
High logic level input voltage	V_{IH}		1.6	---	---	V
Low logic level input voltage	V_{IL}		---	---	0.6	V
FAULT open drain release voltage	$V_{RELEASE}$		---	---	0.4	V
EN Low logic level output voltage	V_{OL}	I_{EN}=4mA	---	---	0.4	V
STBY pull-down resistance	R_{STBY}		---	36	---	kΩ
EN pull-down current	I_{PDEN}		---	10.5	---	µA
EN input propagation delay	t_{ENd}	From EN falling edge to OUT high impedance	---	55	---	ns
MODEx input hold time	t_{MODEho}	From STBY edge, see Figure 6	100	---	---	µs
MODEx input setup time	t_{MODEsu}	From STBY edge, see Figure 6	1	---	---	µs
DIR input hold time	t_{DIRh}	From STCK rising edge, see Figure 5	100	---	---	ns
DIR input setup time	t_{DIRsu}	From STCK rising edge, see Figure 5	100	---	---	ns
STCK high time	t_{STCKH}	See Figure 5	100	---	---	ns
STCK low time	t_{STCKL}	See Figure 5	100	---	---	ns
STCK inputs frequency	f_{STCK}	See Figure 5	---	---	1	MHz
Protections						
Thermal shutdown threshold	T_{jSD}		---	160	---	°C
Thermal shutdown hysteresis	$T_{jSD,Hyst}$		---	40	---	°C
Overcurrent threshold	I_{OC}	See Figure 15. Power stage resistance versus temperature	---	2	---	A

1. Based on characterization data on a limited number of samples, not tested during production.

Minimum Footprint PCB Layout Section

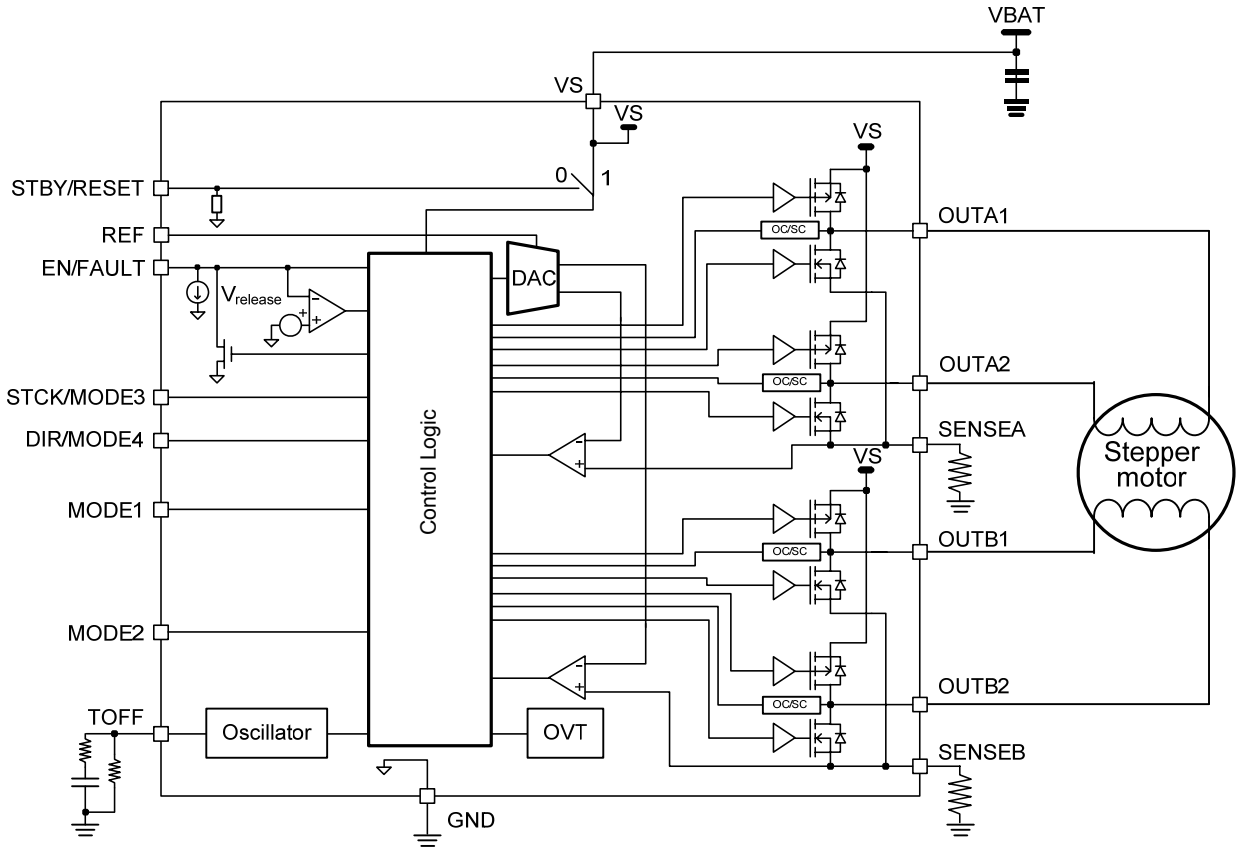
QFN3X3-16



Pin Description

PIN	NAME	TYPE	FUNCTION
1	DIR/MODE4	Logic input	Direction input, Step mode selection input 4.
2	STCK/MODE3	Logic input	Step clock input, Step mode selection input 3.
3	OUTA1	Power output	Power bridge output side A1.
4	SENSEA	Power output	Sense output of the bridge A.
5	OUTA2	Power output	Power bridge output side A2.
6	VS	Supply	Device supply voltage.
7	GND	Ground	Device ground.
8	OUTB2	Power output	Power bridge output side B2.
9	SENSEB	Power output	Sense output of the bridge B.
10	OUTB1	Power output	Power bridge output side B1.
11	REF	Analog input	Reference voltage for the PWM current control circuitry.
12	TOFF	Analog input	Internal oscillator frequency adjustment.
13	EN/FAULT	Logic input/ Open drain output	This is the power stage enable (when low, the power stage is turned off) and is forced low through the integrated open-drain MOSFET when a failure occurs.
14	STBY/RESET	Logic input	When forced low, the device is forced into low consumption mode.
15	MODE2	Logic input	Step mode selection input 2.
16	MODE1	Logic input	Step mode selection input 1.

Block diagram



Functional description

The G2069 is a stepper motor driver integrating a microstepping sequencer (up to 1/256th of a step), two PWM current controllers and a power stage composed of two fully-protected full-bridges.

Standby and power-up

The device provides a low consumption mode which is set forcing the STBY\RESET input below the V_{STBYL} threshold.

When the device is in standby status, the power stage is disabled (outputs are in high impedance) and the supply to the integrated control circuitry is cut off. When the device exits the standby status, all of the control circuitry is reset to power-up condition.

At power-up, power-down and when leaving the standby condition, the EN/FAULT pin is forced low until the internal circuitry stabilize.

Microstepping sequencer

The value of the MODEx inputs is latched at power-up and when the device exits the STBY condition. After this, the input value is unimportant and the MODE3 and MODE4 inputs start operating as step-clock and direction input.

The only exception is the MODE1=MODE2=LOW condition; in this case the system is forced into full-step mode. The previous condition is restored as soon as the MODE1 and MODE2 inputs switch to a different combination.

An example of mode selection is shown in Figure 5. STCK and DIR timing.

At each STCK rising edge, the sequencer of the device is increased (DIR input high) or decreased (DIR input low) of a module selected through the MODEx inputs as listed in Table 1. Step mode selection through MODEx inputs.

The sequencer is a 10-bit counter that sets the reference value of the PWM current controller and the direction of the current for both of the H bridges.

Table 1. Step mode selection through MODEx inputs

MODE3 (STCK)	MODE4(DIR)	MODE1	MODE2	Step mode
0	0	0	0	**Full-step**
0	0	0	1	1/32nd step
0	0	1	0	1/128th step
0	0	1	1	1/256th step
0	1	0	0	**Full-step - 1/32nd step** (1)
0	1	0	1	1/4th step
0	1	1	0	1/256th step
0	1	1	1	1/64th step
1	0	0	0	**Full-step - 1/128nd step** (1)
1	0	0	1	1/256th step
1	0	1	0	1/2 step
1	0	1	1	1/8th step
1	1	0	0	**Full-step - 1/256th step** (1)
1	1	0	1	1/64th step
1	1	1	0	1/8th step
1	1	1	1	1/16th step

1.This driving mode is automatically bypassed by the MODE1=MODE2=0 if it is kept after the device quit the standby condition.

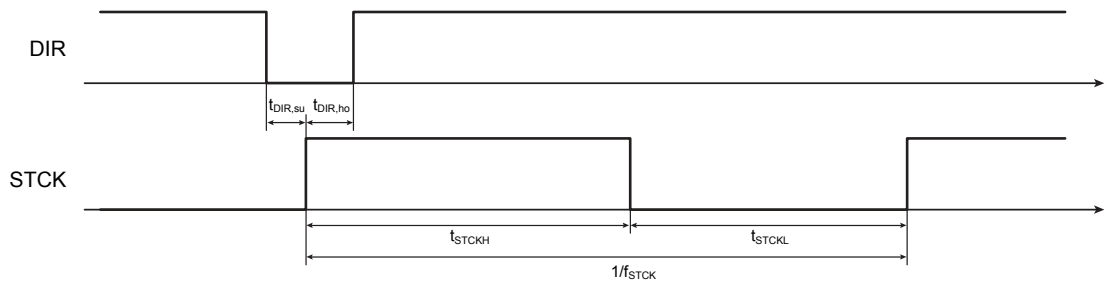


Figure 1. STCK and DIR timing

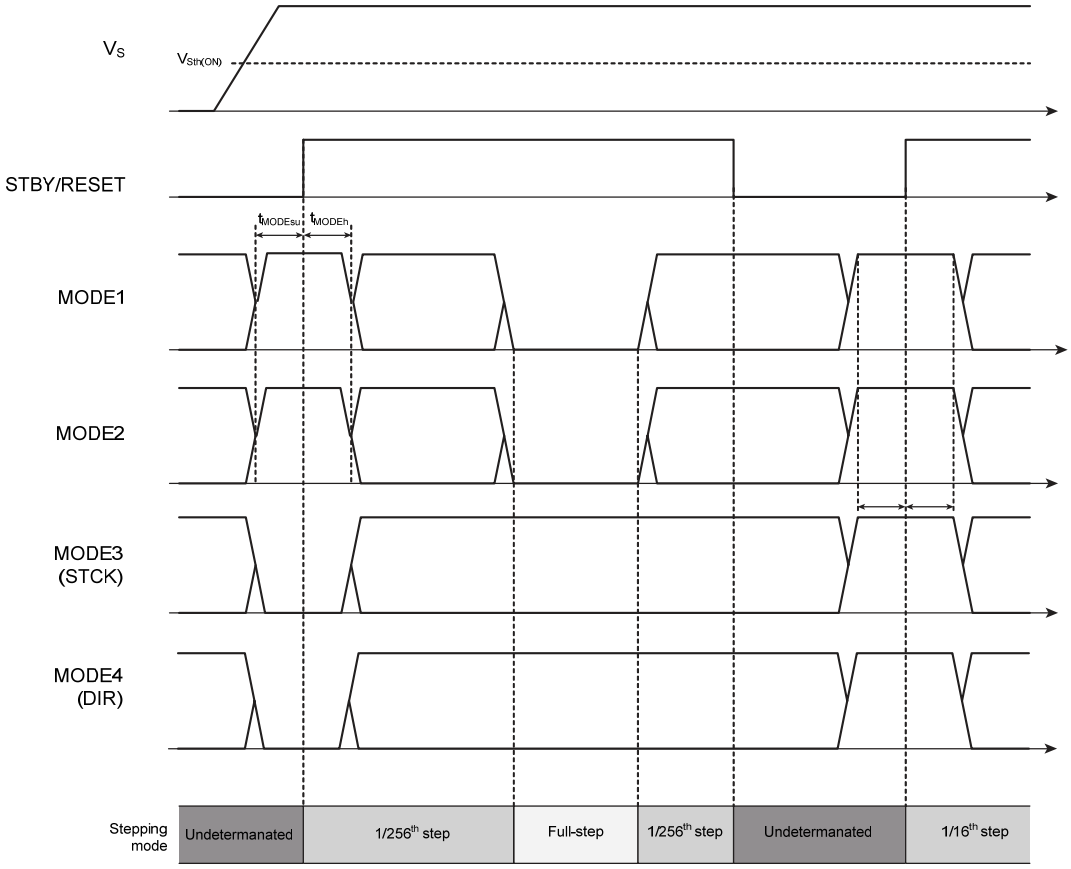


Figure 2. Mode selection example

When the full-step mode is set, the reference value of the PWM current controller and the direction of the current for both H bridges as listed in Table 2. Step mode selection through MODEx inputs.

Table 2. Target reference and current direction according to sequencer value (full-step mode)

Sequencer value										Phase A		Phase B	
										Reference voltage	Current direction	Reference voltage	Current direction
0	0	X	X	X	X	X	X	X	X	100% × V_{REF}	A1 → A2	100% × V_{REF}	B1 → B2
0	1	X	X	X	X	X	X	X	X	100% × V_{REF}	A1 → A2	100% × V_{REF}	B1 ← B2
1	0	X	X	X	X	X	X	X	X	100% × V_{REF}	A1 ← A2	100% × V_{REF}	B1 ← B2
1	1	X	X	X	X	X	X	X	X	100% × V_{REF}	A1 ← A2	100% × V_{REF}	B1 → B2

When the step mode is different from the full-step mode the values listed in Table 3. Target reference and current direction according to sequencer value (not full-step mode) are used.

Table 3. Target reference and current direction according to sequencer value (not full-step mode)

Sequencer value										Phase A		Phase B	
										Reference voltage	Current direction	Reference voltage	Current direction
0	0	0	0	0	0	0	0	0	0	Zero (power bridge disabled)	---	100%×V_{REF}	B1 → B2
0	0	N								Sin(N/256×π/2)×V_{REF}	A1 → A2	Cos(N/256×π/2)×V_{REF}	B1 → B2
0	1	0	0	0	0	0	0	0	0	100%×V_{REF}	A1 → A2	Zero (power bridge disabled)	---
0	1	N								Sin(π/2+N/256×π/2)×V_{REF}	A1 → A2	Cos(π/2+N/256×π/2)×V_{REF}	B1 ← B2
1	0	0	0	0	0	0	0	0	0	Zero (power bridge disabled)	---	100%×V_{REF}	B1 ← B2
1	0	N								Sin(N/256×π/2)×V_{REF}	A1 ← A2	Cos(N/256×π/2)×V_{REF}	B1 ← B2
1	1	0	0	0	0	0	0	0	0	100%×V_{REF}	A1 ← A2	Zero (power bridge disabled)	---
1	1	N								Sin(π/2+N/256×π/2)×V_{REF}	A1 ← A2	Cos(π/2+N/256×π/2)×V_{REF}	B1 → B2

The following table shows the target reference and sequencer values for 1/2-, 1/4- and 1/8-step operation. Higher microstepping resolutions follow the same pattern. The reset state (home state) for all stepping mode is entered at power-up or when the device exits the standby status.

Table 4. Example

1/2 step	1/4 step	1/8 step	VREF phase A	VREF phase B	Sequencer value
1	1	1	0%	100%	0000000000 home state
		2	19.509%	98.079%	0000100000
	2	3	38.268%	92.388%	0001000000
		4	55.557%	83.147%	0001100000
2	3	5	70.711%	70.711%	0010000000
		6	83.147%	55.557%	0010100000
	4	7	92.388%	38.268%	0011100000
		8	98.079%	19.509%	0011100000
3	5	9	100%	0%	0100000000
		10	98.079%	-19.509%	0100100000
	6	11	92.388%	-38.268%	0101000000
		12	83.147%	-55.557%	0101100000
4	7	13	70.711%	-70.711%	0110000000
		14	55.557%	-83.147%	0110100000
	8	15	38.268%	-92.388%	0111000000
		16	19.509%	-98.079%	1000100000
5	9	17	0%	-100%	1000000000
		18	-19.509%	-98.079%	1000100000
	10	19	-38.268%	-92.388%	1001000000
		20	-55.557%	-83.147%	1001100000
6	11	21	-70.711%	-70.711%	1010000000
		22	-83.147%	-55.557%	1010100000
	12	23	-92.388%	-38.268%	1011000000
		24	-98.079%	-19.509%	1011100000
7	13	25	-100%	0%	1100000000
		26	-98.079%	19.509%	1100100000
	14	27	-92.388%	38.268%	1101000000
		28	-83.147%	55.557%	1101100000
8	15	29	-70.711%	70.711%	1110000000
		30	-55.557%	83.147%	1110100000
	16	31	-38.268%	92.388%	1111000000
		32	-19.509%	98.079%	1111100000

Note: The positive number means that the output current is flowing from OUTx1 to OUTx2, vice versa for a negative value.

PWM current control

The device implements two independent PWM current controllers, one for each full bridge.

The voltage of the sense pins (V_{SENSEA} and V_{SENSEB}) is compared to the respective internal reference generated based on the sequencer value (see Table 9. Target reference and current direction according to sequencer value(full-step mode) and Table 10. Target reference and current direction according to sequencer value (not full-step mode).

When V_{SENSEX}>V_{REFX}, the integrated comparator is triggered, the OFF time counter is started and the decay sequence is performed.

The decay sequence starts turning on both the low sides of the full bridge. When 5/8^{ths} of the programmed OFF time ($t_{OFF,SLOW}$) has expired, the decay sequence performs a quasi-synchronous fast decay.

Table 5. ON, slow decay and fast decay states

Current direction(1)	ON	Slow decay	Fast decay (quasi-synch)
Zero (power bridge disabled)	HSX1=OFF LSX1=OFF HSX2=OFF LSX2=OFF	HSX1=OFF LSX1=OFF HSX2=OFF LSX2=OFF	HSX1=OFF LSX1=OFF HSX2=OFF LSX2=OFF
X1 → X2	**HSX1=ON** LSX1=OFF HSX2=OFF **LSX2=ON**	HSX1=OFF **LSX1=ON** HSX2=OFF **LSX2=ON**	HSX1=OFF **LSX1=ON** HSX2=OFF LSX2=OFF
X1 ← X2	HSX1=OFF **LSX1=ON** **HSX2=ON** LSX2=OFF	HSX1=OFF **LSX1=ON** HSX2=OFF **LSX2=ON**	HSX1=OFF LSX1=OFF HSX2=OFF **LSX2=ON**

1.The current direction is set according to Table 2. Target reference and current direction according to sequencer value (full-step mode) Table 3. Target reference and current direction according to sequencer value (not full-step mode) .

Detailed Description

The reference voltage value, VREF, must be selected according to the load current target value (peak value) and sense resistor value.

Equation 1

$$V_{REF} = R_{SNSX} \times I_{LOAD,peak} \quad (1)$$

In choosing the sense resistor value, two main issues must be taken into account:

- The sense resistor dissipates energy and provides dangerous negative voltages on the SENSE pins during current recirculation. For this reason the resistance of this component should be kept low (using multiple resistors in parallel will help to obtain the required power rating with standard resistors).
- The lower the R_{SNSx} value, the higher the peak current error due to noise on the V_{REF} pin and the input offset of the current sense comparator. Values of R_{SNSx} that are too low must be avoided.

OFF time adjustment

The total OFF time (slow decay + fast decay) is adjusted through an external resistor connected between the TOFF pin and ground, as shown in Figure 5. PWM current control sequence. A small RC series must be inserted in parallel with the regulator resistor in order to increase the stability of the regulation circuit according to Table 5. ON, slow decay and fast decay states indications.

The relationship between the OFF time and the external resistor value is shown in Figure 3. OFF time regulation circuit. The value typically ranges from 10µs to 150µs.

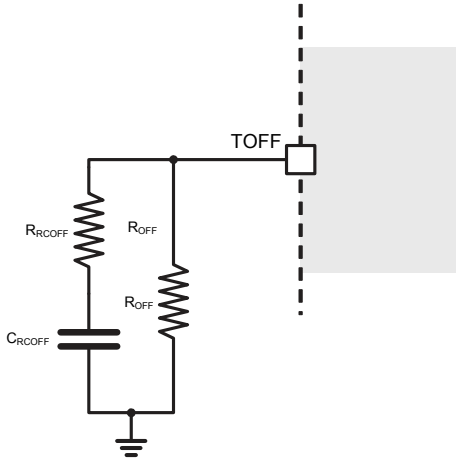


Figure 3. OFF time regulation circuit

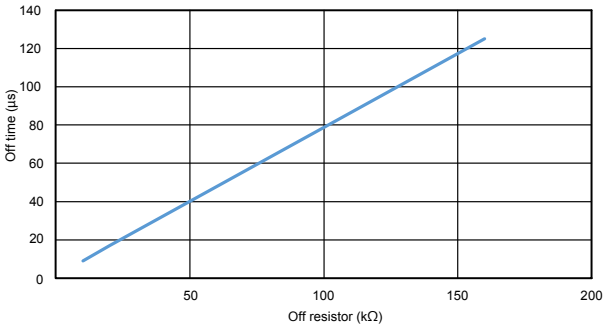


Figure 4. OFF time vs. ROFF value

Table 6. Recommended R_{RCOFF} and C_{RCOFF} values according to R_{OFF}

ROFF	RRCOFF	CRCOFF
10kΩ≤ROFF<82kΩ	1kΩ	22nF
82kΩ≤ROFF≤160kΩ	2.2kΩ	22nF

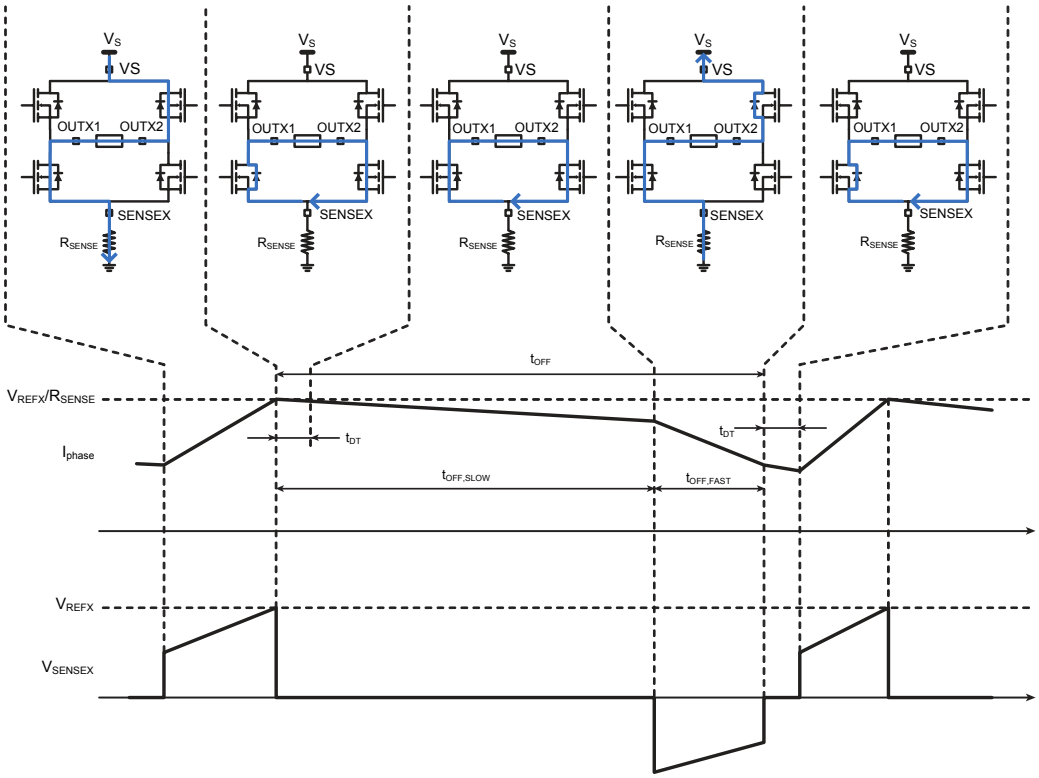


Figure 5. PWM current control sequence

Overcurrent and short-circuit protection

The device embeds circuitry protecting each power output against the overload and short circuit conditions (short-circuit to ground, short-circuit to VS and short-circuit between outputs).

When the overcurrent or short-circuit protection is triggered, the power stage is disabled and the EN/FAULT input is forced low through the integrated open-drain MOSFET discharging the external C_{EN} capacitor (refer to Figure 6. Overcurrent and short-circuit protection management).

The power stage is kept disabled and the open-drain MOSFET is kept ON until the EN/FAULT input falls below the $V_{RELEASE}$ threshold, then the C_{EN} capacitor is charged through the external R_{EN} resistor.

The total disable time after an overcurrent event can be set sizing properly the external network connected to the EN/FAULT pin (refer to Figure 6. Overcurrent and short-circuit protection management):
Equation 2

$$t_{DIS} = t_{discharge} + t_{charge} \quad 2$$

But t_{charge} is normally much higher than $t_{discharge}$, thus we can consider the following:
Equation 3

$$t_{DIS} = R_{EN} \times C_{EN} \times \ln \frac{(V_{DD} - R_{EN} \times I_{PDEN}) - V_{RESEASE}}{(V_{DD} - R_{EN} \times I_{PDEN}) - V_{IH}} \quad 3$$

where VDD is the pull-up voltage of the REN resistor.

Thermal shutdown

The device embeds circuitry protecting it from the overtemperature conditions.

When the thermal shutdown temperature is reached, the power stage is disabled and the EN/FAULT input is forced low through the integrated open-drain MOSFET (refer to Figure 7. Thermal shutdown management).The protection and the EN/FAULT output are released when the IC temperature returns below a safe operating value (T_{jSD} - $T_{jSD,Hyst}$).

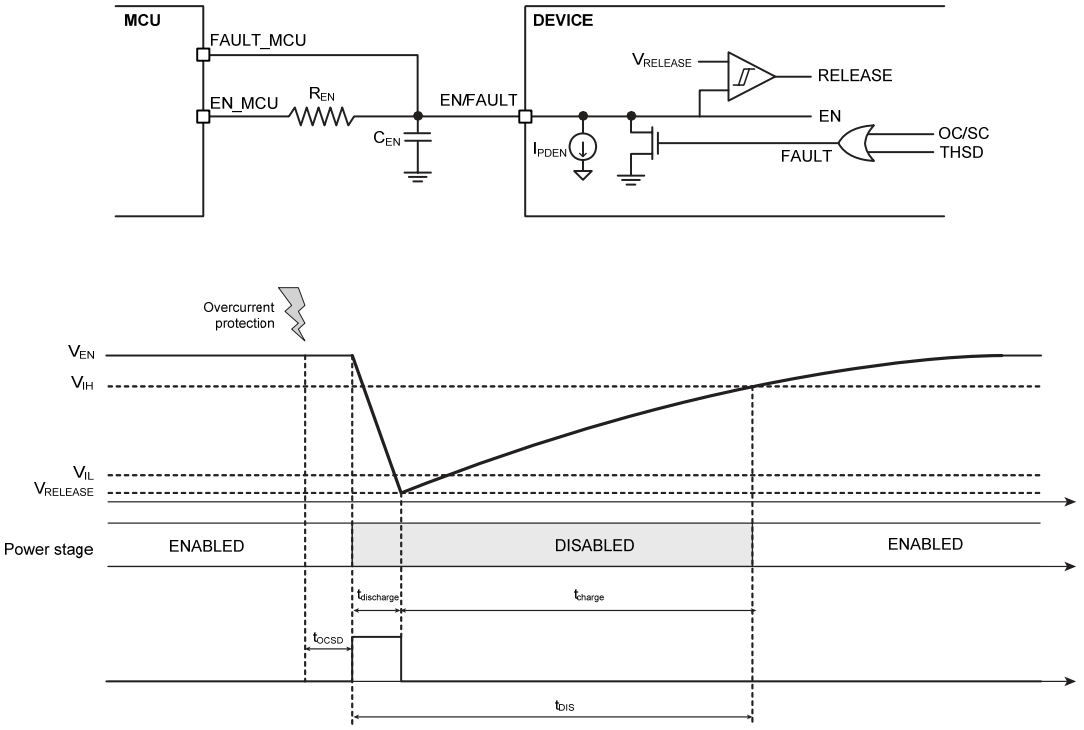


Figure 6. Overcurrent and short-circuit protection management

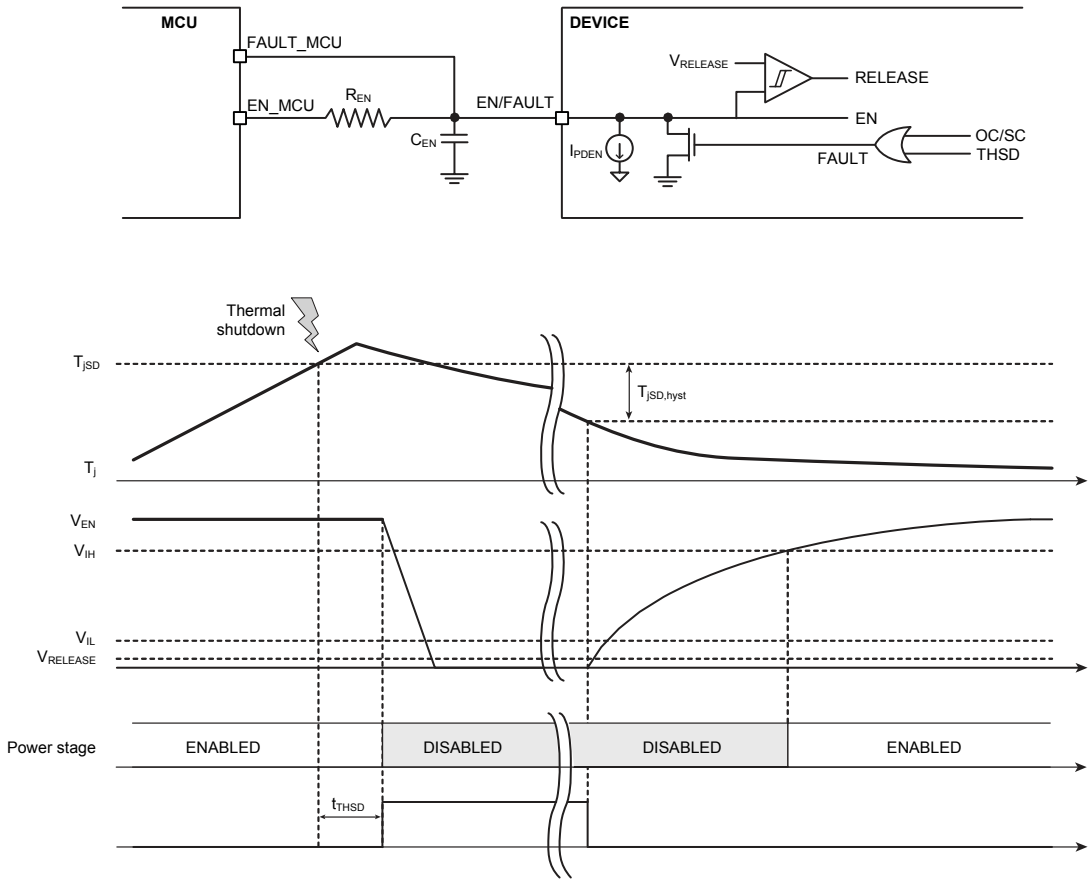
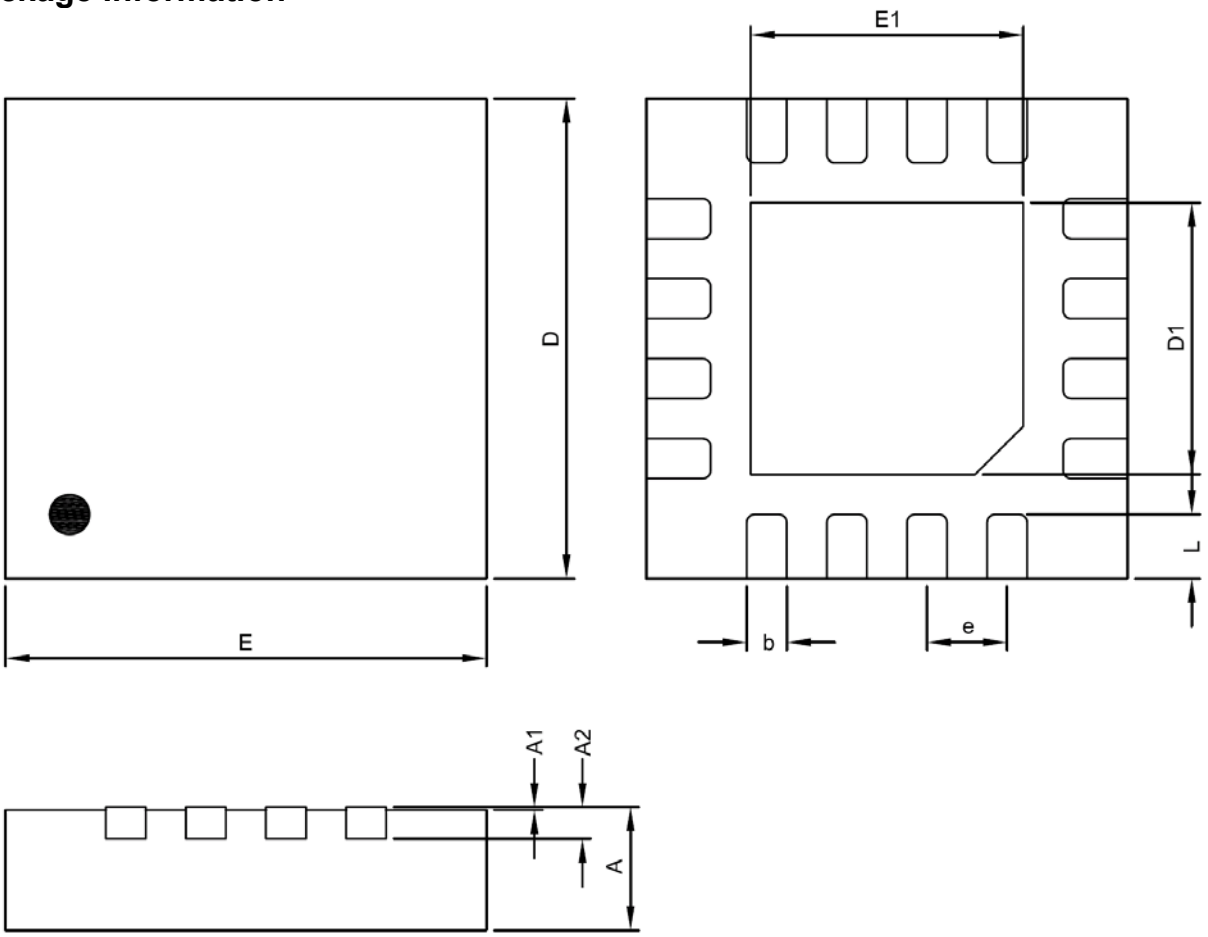


Figure 7. Thermal shutdown management

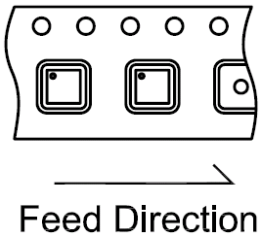
Package Information



QFN3X3-16 Package

Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.90	1.00	0.0315	0.0354	0.0394
A1	0.00	- - -	0.05	0.0000	- - -	0.0020
A2	0.20 REF			0.0079 REF		
D	2.95	3.00	3.05	0.1161	0.1181	0.1201
E	2.95	3.00	3.05	0.1161	0.1181	0.1201
D1	1.60	1.70	1.80	0.0630	0.0669	0.0689
E1	1.60	1.70	1.80	0.0630	0.0669	0.0689
b	0.18	0.25	0.30	0.0071	0.0098	0.0118
e	0.50 BSC			0.0197 BSC		
L	0.35	0.40	0.45	0.0138	0.0157	0.0177

Taping Specification



PACKAGE	Q'TY/BY REEL
QFN3X3-16	3,000 ea