G2156

4 Channels, High Efficiency, Synchronous Step Down

Features

- **Continuous Loading: 3A (Buck1), 1A (Buck2, 3 and 4)**
- **1MHz Switching Frequency**
- **0.8V ± 2% Voltage Reference Over Temperature**
- **External Enable/Sequencing Pins**
- **Power Good Output**
- **Cycle by Cycle Current Limit, Thermal and Overload protection.**
- **Thermally Enhanced 4mm × 4mm 32-pin QFN**

Applications

- **Set Top Boxes**
- **Blue-ray DVD**

General Description

The G2156 device features four synchronous 5.5V input range high efficiency buck converters. The converters are designed to simplify its application while giving the designer the option to optimize their usage according to the target application.

The converters can operate in 5V systems and have integrated power transistors. The output voltage can be set externally using a resistor divider to any value between 0.8V and close to the input supply. Each converter features enable pin that allows a delayed start-up for sequencing purposes. The current mode control allows a simple RC compensation.

The switching frequency of the converters can operate 1 MHz.

The G2156 features a supervisor circuit that monitors each converter output. The PGOOD pin is asserted once sequencing is done, all PG signals are reported and a selectable end of reset time lapses. The polarity of the PGOOD signal is active high.

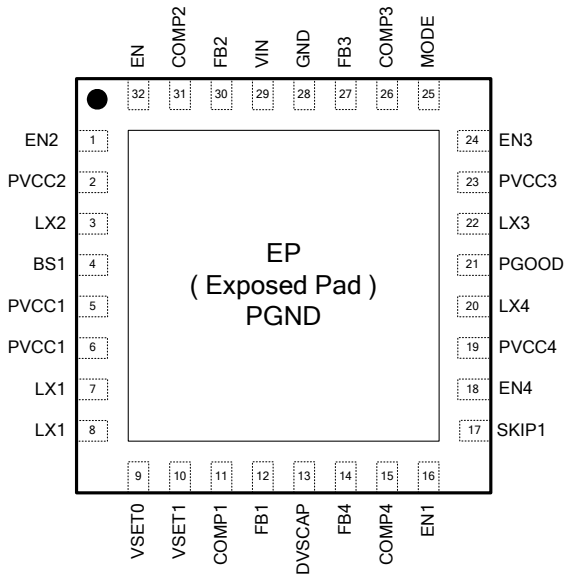
The G2156 Buck1/3/4 also features a light load pulse skipping mode, PSM mode allows for a reduction on the input power supplied to the system when the host processor is in stand-by (low activity) mode. SKIP1 PIN is setting Buck1/3/4 skipping mode.

Ordering Information

ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE (Green)
G2156K11U	2156	-40°C to +85°C	TQFN4X4-32

Note: K1: TQFN4X4-32
1: Bonding Code
U: Tape & Reel
Green : Lead Free / Halogen Free

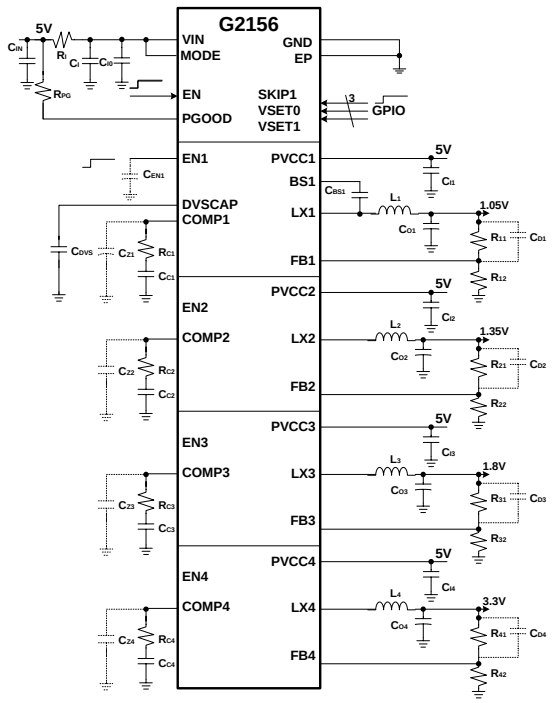
Pin Configuration



G2156 TQFN4X4-32

Note: Recommend connecting the Thermal Pad to the Ground for excellent power dissipation.

Typical Application Circuit



Absolute Maximum Ratings

VIN, PVCC1/2/3/4 Power Input Voltage
. . . . . -0.3V to +6.5V
ENx, FBx, COMPx, SSx, LXx, PGOOD,SKIP1, VSET1, VSET0 Pin Input/Output Voltage. . …. . .-0.3V to +6.5V
'BS1 – LX1 ' Voltage . . . . . -0.3V to +6.5V
LX1/2/3/4 Pin 10ns Transient . . . . -3V to +8.5V
Thermal Resistance Junction to Ambient, (θ_{JA})*
TQFN4X4-32 . . . . . 52°C/W
Continuous Power Dissipation (T_A = +25°C)*
TQFN4X4-32. . . . . 2.4W
Thermal Resistance Junction to Board (θ_{JB})
TQFN4X4-32. . . . . .32°C/W
Thermal Resistance Junction to Case, (θ_{Jc})
TQFN4X4-32. . . . . 28°C/W
Operation Temperature . . . . . -40°C to +85°C
Storage Temperature . . . . . -55°C to +150°C
ESD Susceptibility (HBM) 2kV
ESD Susceptibility (MM) 200V

Operation Conditions

Power supply voltage. . . . . .2.95V to +6.0V
ENx,SSx, MODE PIN input voltage . . . . . .0 to VIN
Operating ambient temperature (T_A). .-20°C to +85°C

* The package is placed on a 4-layer PCB (1oz) with 1via. Please refer to EV Board PCB Layout Section

1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Device are ESD sensitive. Handling precaution recommended. The Human Body model is a 100pF capacitor discharged through a 1.5KΩ resistor into each pin.

Electrical Characteristics

(V_{IN}=5V, T_A=25°C)

The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SUPPLY VOLTAGE (VIN PIN)						
VIN Operating input Voltage	V_{VIN}		2.95	---	6	V
Internal under voltage lockout threshold1	$V_{UVLO1(H2L)}$	hys. 200mV	---	2.65	2.8	V
Shutdown supply current	I_{SHDN}	EN = 0V, 25°C, 2.95V ≤ VIN ≤6V	---	2	5	μA
Quiescent current	I_{Q1}	EN = VIN, VIN = 5V, Temp.=25°C, ENx =0V	---	200	300	μA
CONTROL BLOCK(EN ,EN1/2/3/4 , MODE, SKIP1, VSET1/0)						
EN Operating input Voltage	V_{EN}	With Pull Up Resistance	0	---	VIN	V
EN threshold	V_{EN_L2H}	Rising	1.3	--	VIN	V
	V_{EN_H2L}	Falling	0	--	0.5	V
EN Pull Up Resistance	R_{EN}	VIN=5V	---	2.5	---	MΩ
EN1/2/3/4 Operating input Voltage	V_{EN1234}	With Pull Up Current	0	---	VIN	V
EN1/2/3/4 threshold	V_{EN1234_L2H}	Rising	1.55	--	VIN	V
	V_{EN1234_H2L}	Falling	0	--	1.25	V
EN1234 Pull Up Current	I_{EN1234}	VIN=5V	---	1	---	μA
MODE Operating input Voltage	V_{mode}	Without Pull up/down Resistance	0	---	VIN	V
MODE threshold	V_{EN1234_L2H}	Rising	0.8*VIN	--	VIN	V
	V_{EN1234_H2L}	Falling	0	--	0.2*VIN	V
SKIP1,VSET1/0 Operating input Voltage	V_{SKIP}	With Pull down 1MΩ at EN=H	0	---	VIN	V
SKIP1,VSET1/0 threshold	V_{SKIP_L2H}	Rising	1.3	--	VIN	V
	V_{SKIP_H2L}	Falling	0	--	0.5	V
VOLTAGE REFERENCE (FB1/2/3/4 PIN)						
Voltage Reference	$V_{FB1/2/3/4}$	2.95V ≤ VIN ≤ 6.0V	-2%	0.8	+2%	V

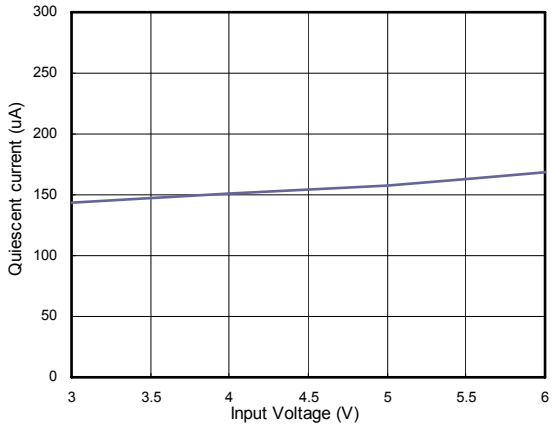
Electrical Characteristics (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
MOSFET						
CH1 High side switch resistance	R_{ON_HS}	BS1-LX1=5.0V	---	90	---	mΩ
CH1 Low side switch resistance	R_{ON_LS}	PVCC1=5.0V	---	55	---	mΩ
CH2/3/4 High side switch resistance	R_{ON_HS}	PVCC2/3/4=5.0V	---	150	---	mΩ
CH2/3/4 Low side switch resistance	R_{ON_LS}	PVCC2/3/4=5.0V	---	120	---	mΩ
ERROR AMPLIFIER						
Error amplifier trans-conductance (gm)	GM_1	VIN=5V	---	130	---	μmhos
Error amplifier source/sink	I_{ERROR_MAX}	V(COMP)=1.0V, 100mV overdrive	---	±16	---	μA
COMP1 to ILX1 gm	GM_{COMP1}		---	8	---	A/V
COMP2/3/4 to ILX2/3/4 gm	$GM_{COMP2/3/4}$		---	3	---	A/V
CURRENT LIMIT						
CH1 Current limit threshold	I_{LIMIT1}		4	5	---	A
CH2/3/4 Current limit threshold	$I_{LIMIT2/3/4}$		2.0	2.5	---	A
Thermal Shutdown						
Thermal Shutdown Temperature	T_{TSD}	Latch , reset by EN H to L	---	150	---	°C
OSCILLATOR						
Frequency of CH1/2/3/4	F_{req}		0.8	1	1.2	MHz
LX1/2/3/4 (LX PIN)						
CH1 Minimum off width	$TOFF_{MIN}$		---	60	---	ns
CH2/3/4 Minimum on width	TON_{MIN}		---	60	---	ns
LX Current sensing delay width	LX_{MIN}		---	60	---	ns
LX Rise/Fall Time	$LX_{TR/TF}$		---	1.5	---	V/ ns
BOOT (BS1 PIN)						
BOOT Charge Resistance	R_{BS}		---	25	---	Ω
Soft Start Time						
CH1/2/3/4 Soft Start Time	T_{SSx}		---	1	---	mS
POWER GOOD (PGOOD PIN)						
FBx threshold	VPG_{LF}	FBx falling (Fault)	---	85	---	% Vref
	VPG_{LR}	FBx rising (Good)	---	95	---	% Vref
	VPG_{HR}	FBx rising (Fault)	---	107.5	---	% Vref
	VPG_{HF}	FBx falling (Good)	---	105	---	% Vref
Hysteresis		FBx falling	---	10	---	% Vref
Output high leakage	IPG_{LEAK}	FBx = VREF, V(PG) = 5.5V	---	2	---	nA
On resistance	R_{PG}		---	15	---	Ω
Minimum VIN for valid output		V(PG) < 0.5V at 100μA	---	1.2	1.6	V
PGOOD detect Delay	$T_{PG(L2H)}$	all FBx > 95%*Vref	15	19.6	---	mS
	$T_{PG(H2L)}$	FBx < 85%*Vref and SSOKx=H	80	125	180	μS
Over Load Protection(OLP) detect Delay	T_{OLP}	FBx < 85%*Vref and SSOKx=H	---	10	---	mS

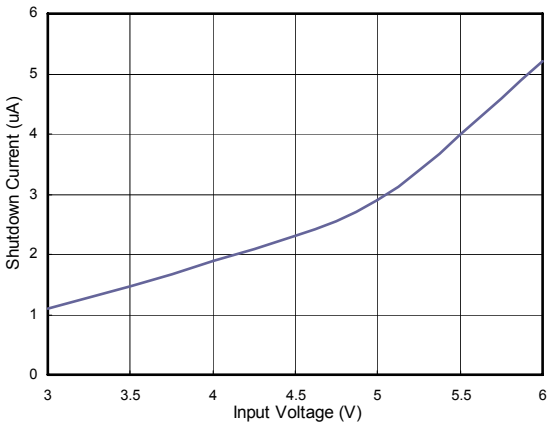
Typical Performance Characteristics

(V_{IN}= 5V, T_A=25°C, unless otherwise noted.)

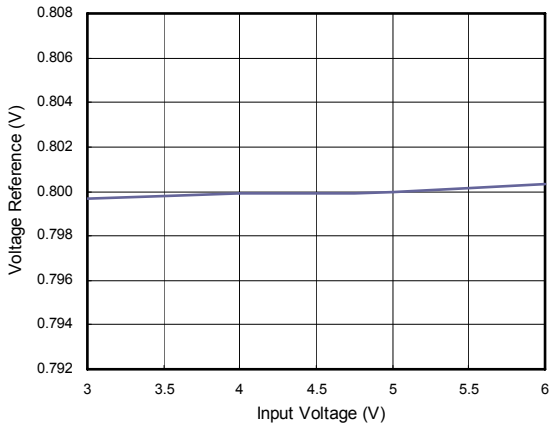
Quiescent Current vs. Input Voltage



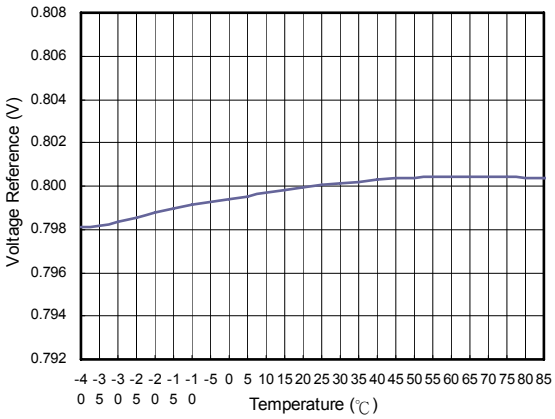
Shutdown Current vs. Input Voltage



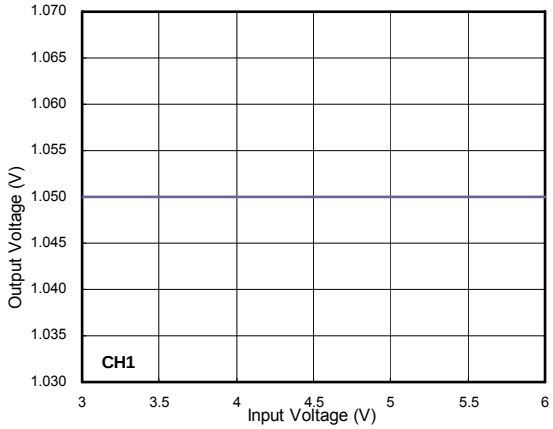
Voltage Reference vs. Input Voltage



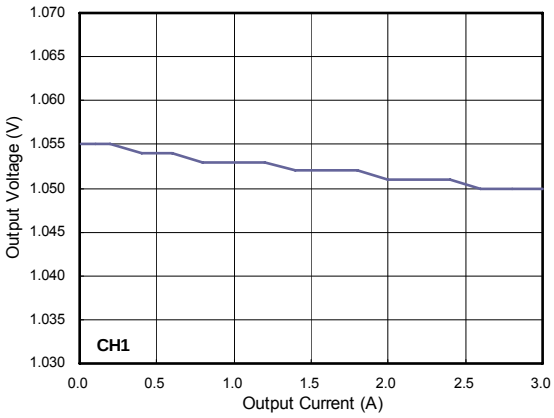
Voltage Reference vs. Temperature



Output Voltage vs. Input Voltage

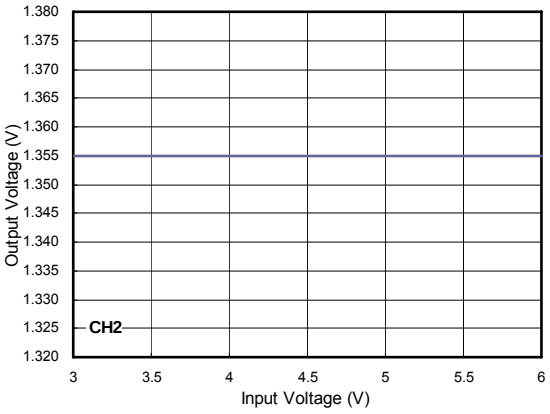


Output Voltage vs. Output Current

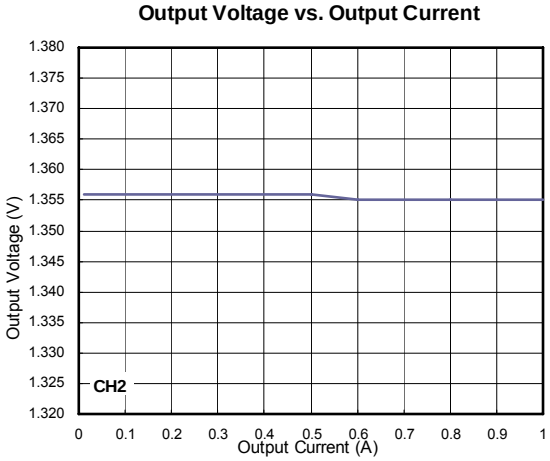


Typical Performance Characteristics (continued)

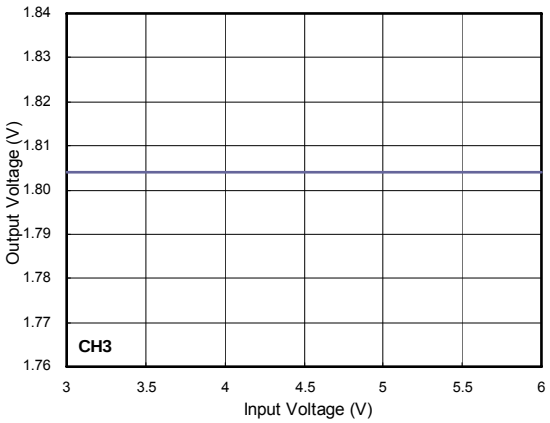
Output Voltage vs. Input Voltage



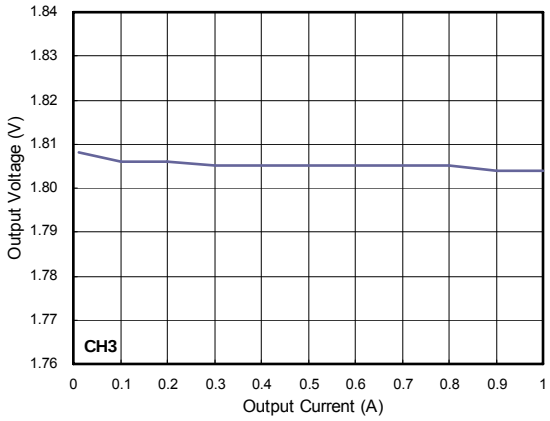
Output Voltage vs. Output Current



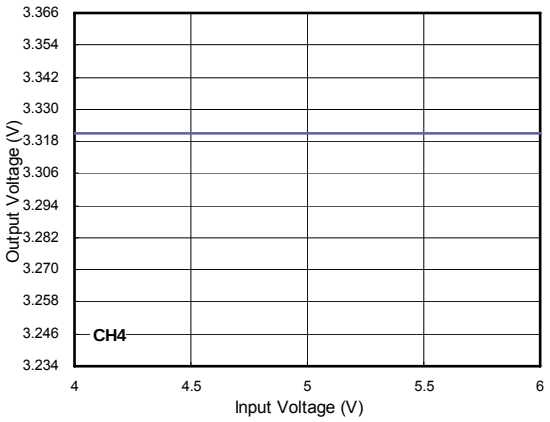
Output Voltage vs. Input Voltage



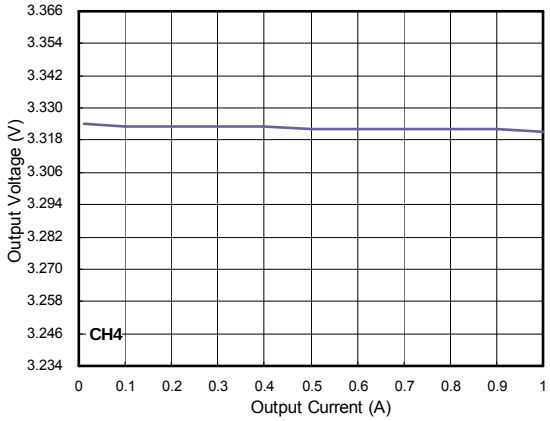
Output Voltage vs. Output Current



Output Voltage vs. Input Voltage

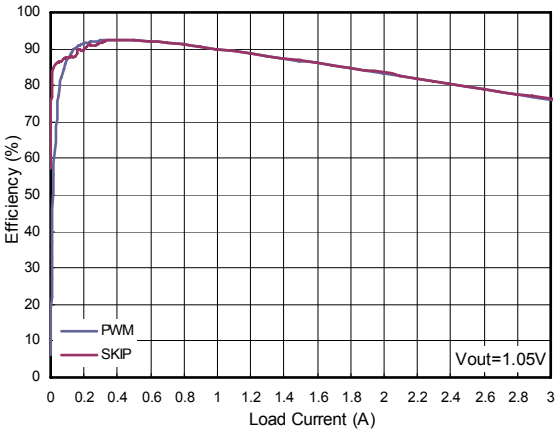


Output Voltage vs. Output Current

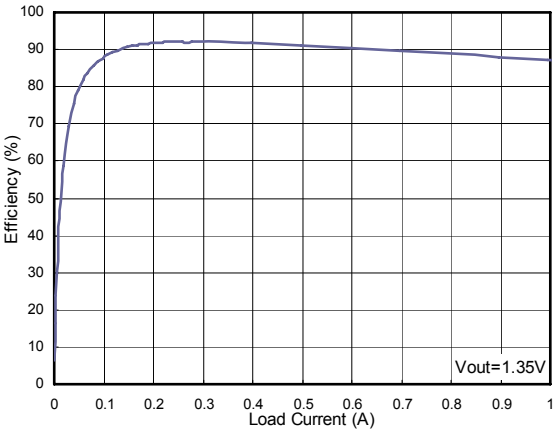


Typical Performance Characteristics (continued)

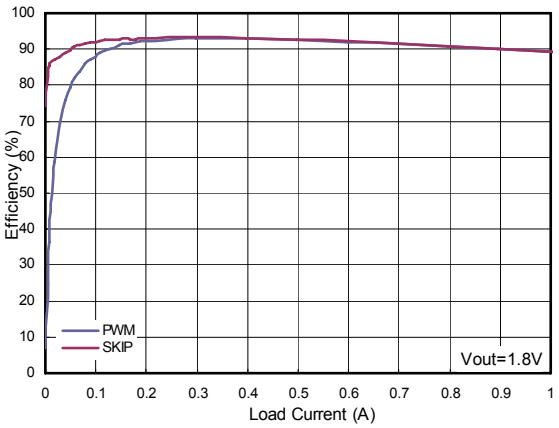
Efficiency-CH1



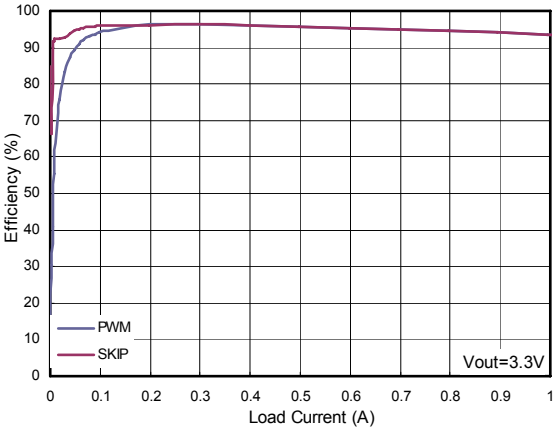
Efficiency-CH2



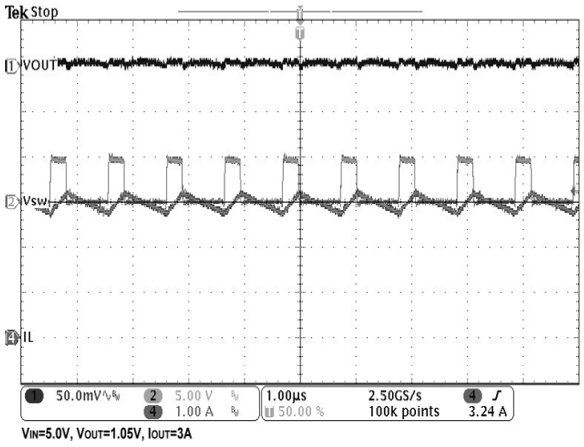
Efficiency-CH3



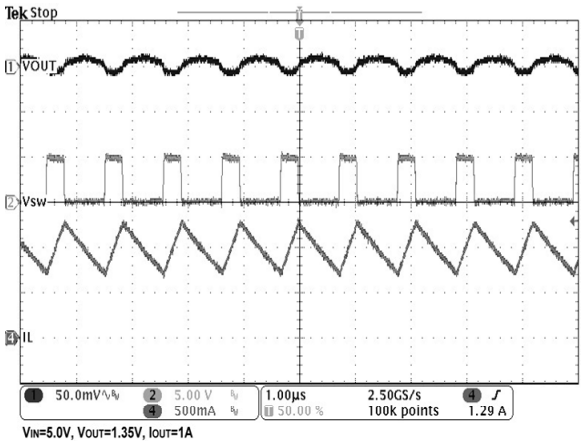
Efficiency-CH4



Steady-state Waveform-CH1

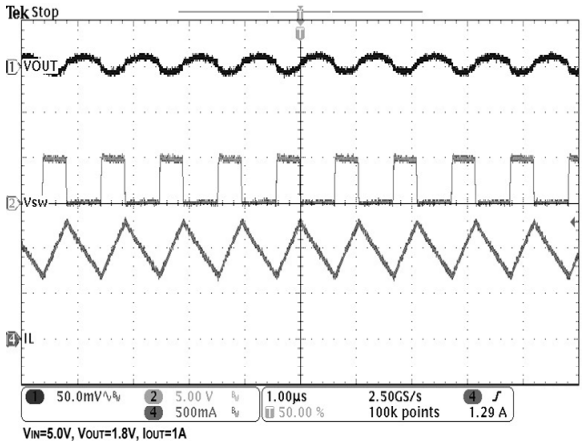


Steady-state Waveform-CH2



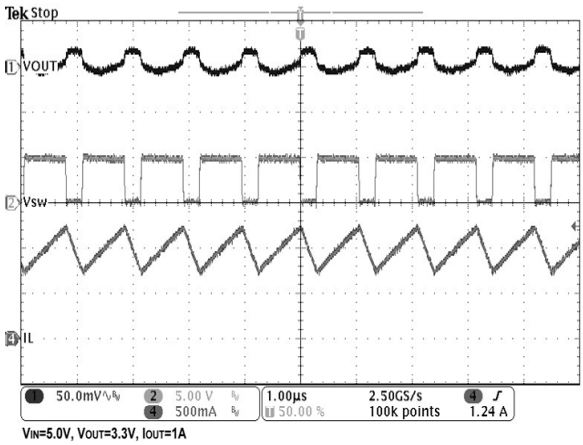
Typical Performance Characteristics (continued)

Steady-state Waveform-CH3



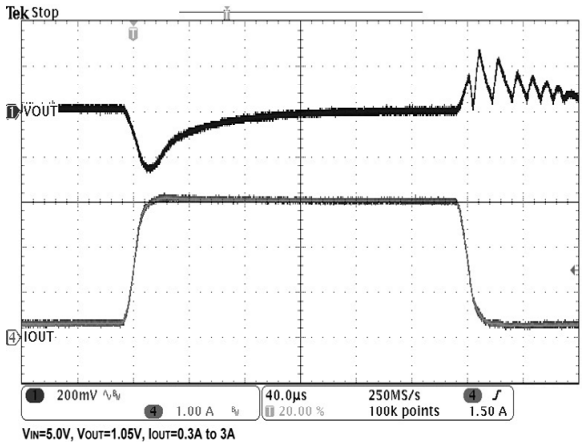
VIN=5.0V, VOUT=1.8V, IOUT=1A

Steady-state Waveform-CH4



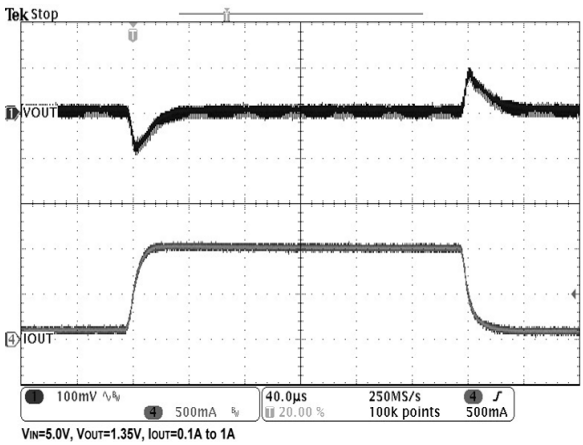
VIN=5.0V, VOUT=3.3V, IOUT=1A

Load Transient-CH1



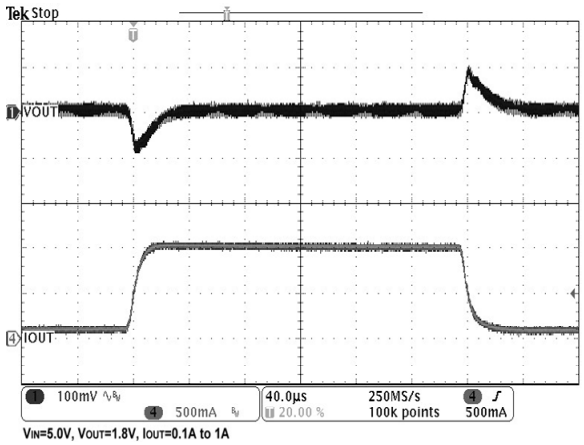
VIN=5.0V, VOUT=1.05V, IOUT=0.3A to 3A

Load Transient-CH2



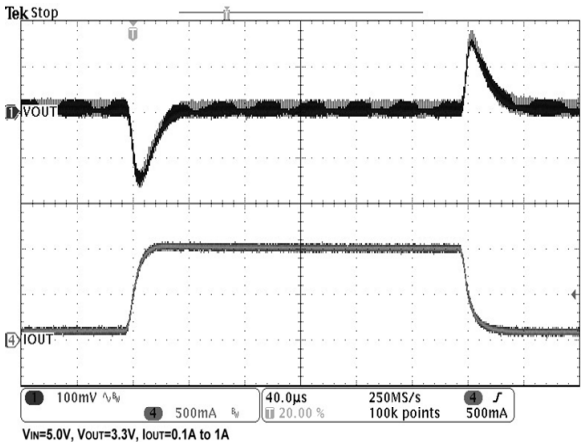
VIN=5.0V, VOUT=1.35V, IOUT=0.1A to 1A

Load Transient-CH3



VIN=5.0V, VOUT=1.8V, IOUT=0.1A to 1A

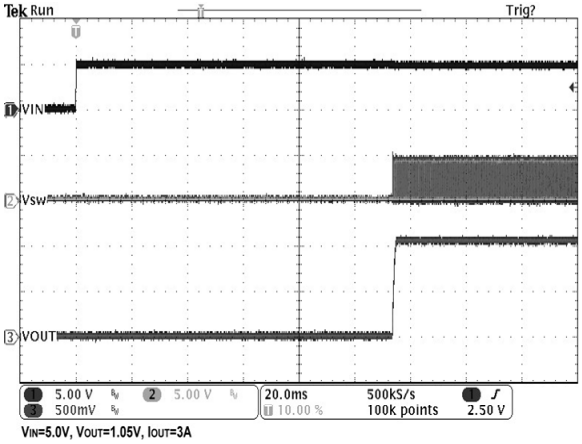
Load Transient-CH4



VIN=5.0V, VOUT=3.3V, IOUT=0.1A to 1A

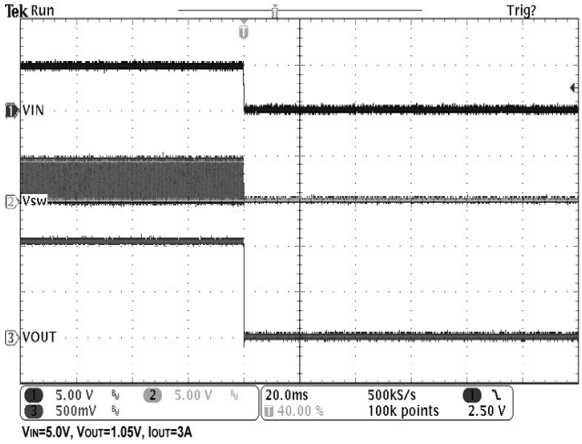
Typical Performance Characteristics (continued)

Power On Waveform-CH1



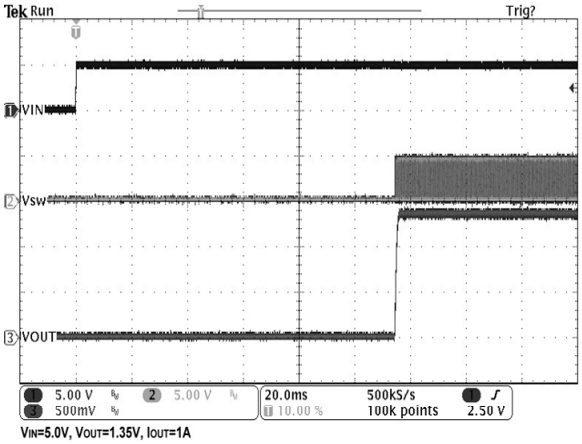
VIN=5.0V, VOUT=1.05V, IOUT=3A

Power Off Waveform-CH1



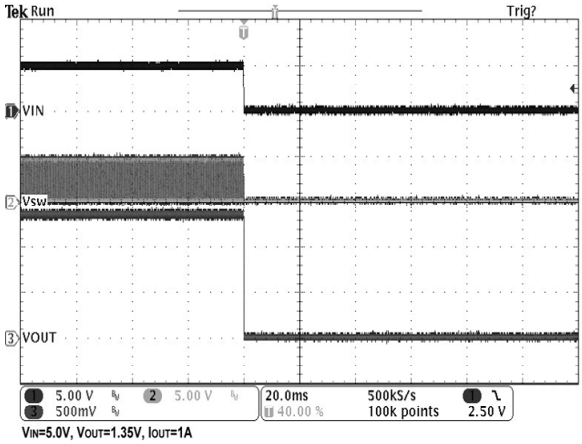
VIN=5.0V, VOUT=1.05V, IOUT=3A

Power On Waveform-CH2



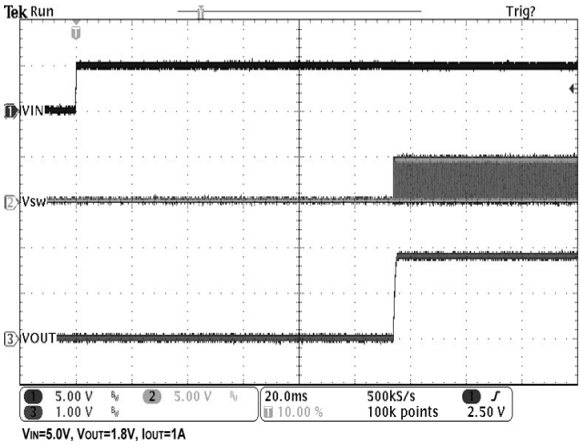
VIN=5.0V, VOUT=1.35V, IOUT=1A

Power Off Waveform-CH2



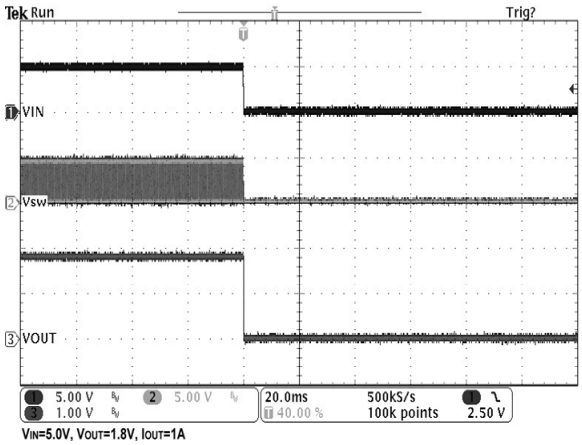
VIN=5.0V, VOUT=1.35V, IOUT=1A

Power On Waveform-CH3



VIN=5.0V, VOUT=1.8V, IOUT=1A

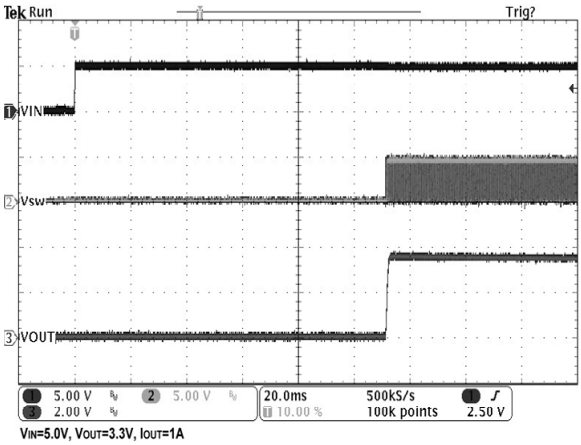
Power Off Waveform-CH3



VIN=5.0V, VOUT=1.8V, IOUT=1A

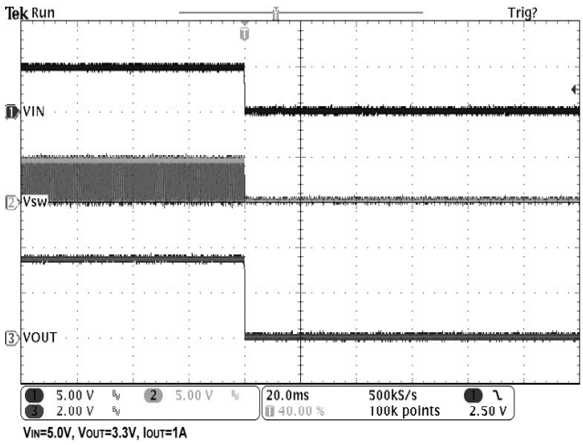
Typical Performance Characteristics (continued)

Power On Waveform-CH4



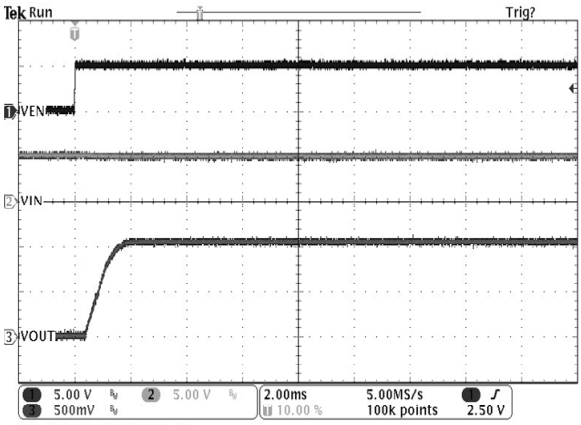
VIN=5.0V, VOUT=3.3V, IOUT=1A

Power Off Waveform-CH4



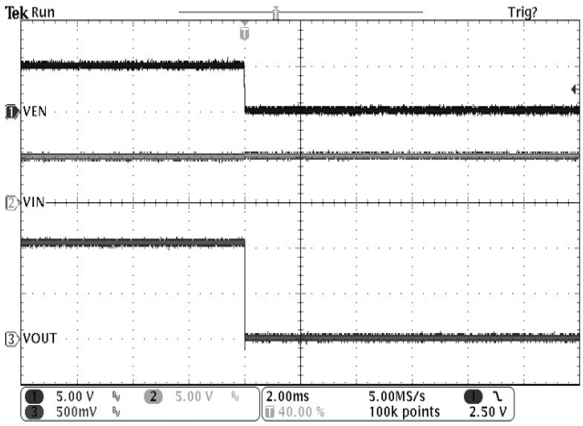
VIN=5.0V, VOUT=3.3V, IOUT=1A

Start-Up Waveform-CH1



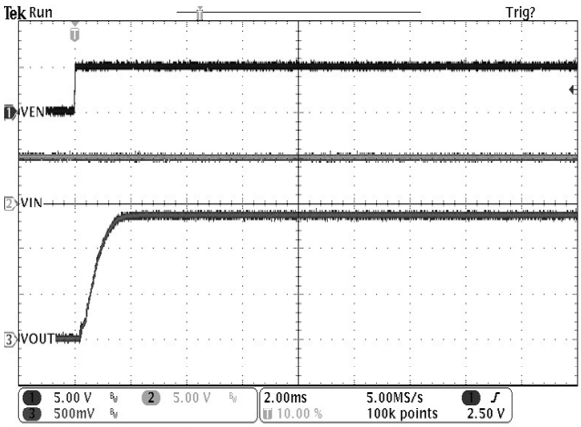
VIN=5.0V, VOUT=1.05V, IOUT=3A

Shutdown Waveform-CH1



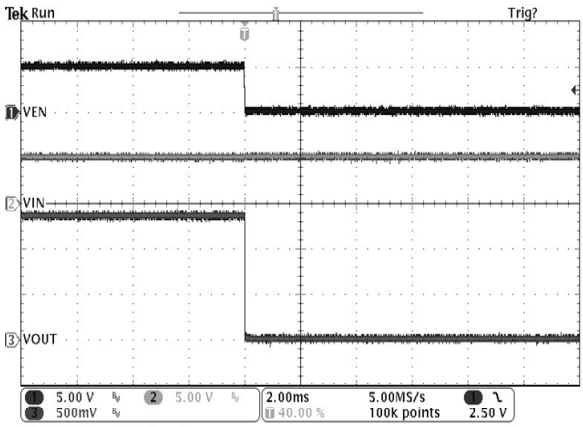
VIN=5.0V, VOUT=1.05V, IOUT=3A

Start-Up Waveform-CH2



VIN=5.0V, VOUT=1.35V, IOUT=1A

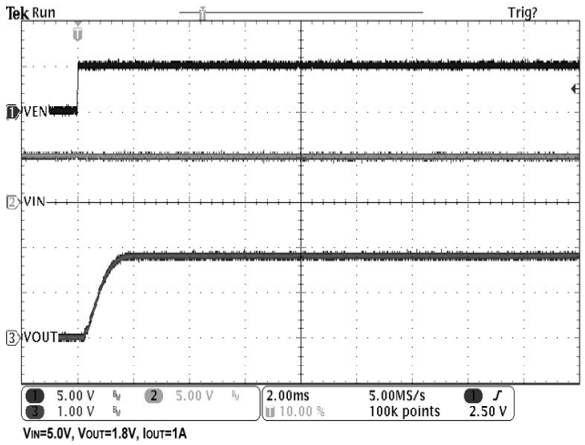
Shutdown Waveform-CH2



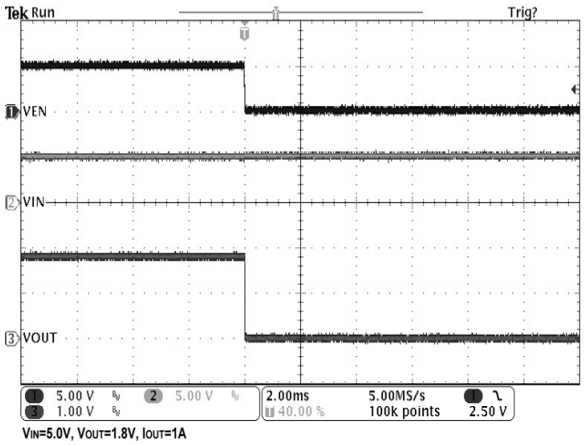
VIN=5.0V, VOUT=1.35V, IOUT=1A

Typical Performance Characteristics (continued)

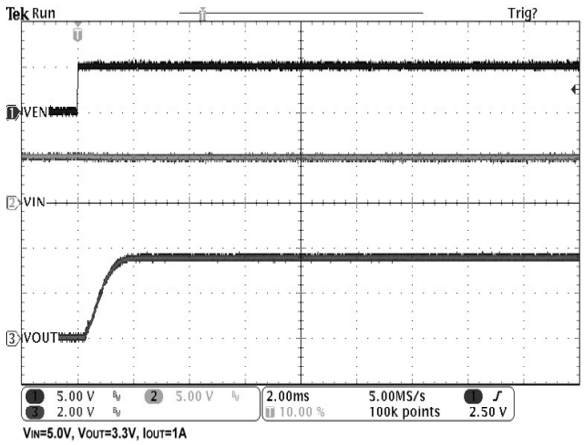
Start-Up Waveform-CH3



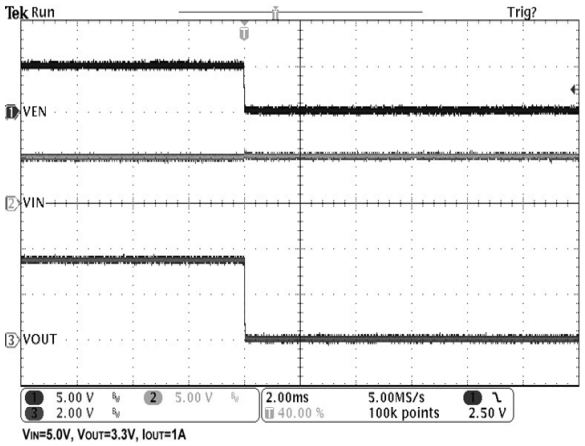
Shutdown Waveform-CH3



Start-Up Waveform-CH4

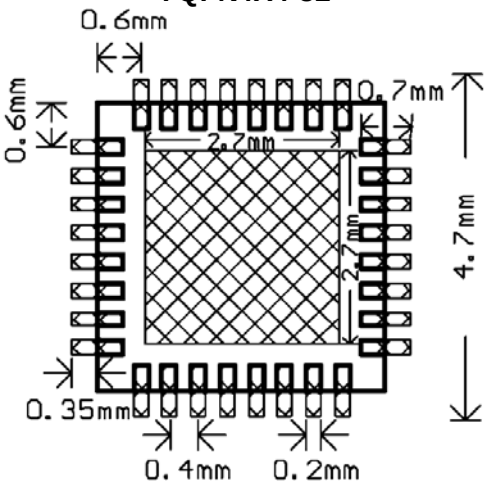


Shutdown Waveform-CH4



Minimum Footprint PCB Layout Section

TQFN4X4-32

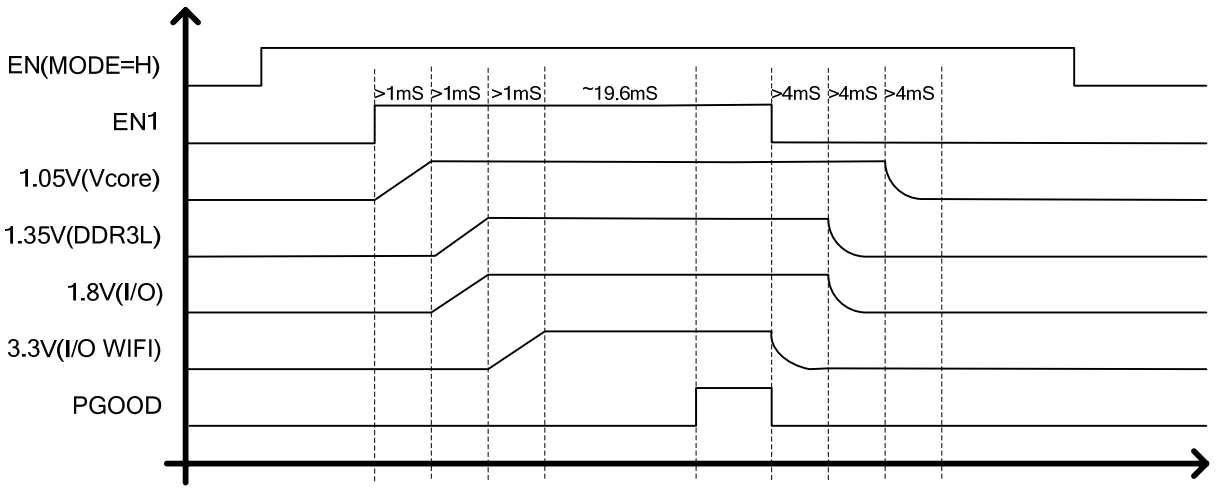


Power ON/OFF Timing Sequence setting :

The G2156 have selectable power on/off sequence as set by the MODE pin (Table 1).

Table 1. Truth Table for CH1, CH2, CH3 ,CH4 Power ON/OFF Sequence

MODE	Power ON	Power OFF
GND	EN Pin must be high level to enable CHIP Bias Circuit CH1,CH2,CH3 and CH4 are independence, the channel on/off can be controlled by ENx Pin	
VIN	CH1 → CH2&CH3 →CH4 → PGOOD	PGOOD → CH4 → CH2&3 →CH1
	EN Pin must be high level to enable CHIP Bias Circuit CH1,CH2,CH3 and CH4 are dependence, the channel on/off can be controlled by EN1 Pin	



CH1 DVS (Dynamic Voltage Scaling**) setting :**

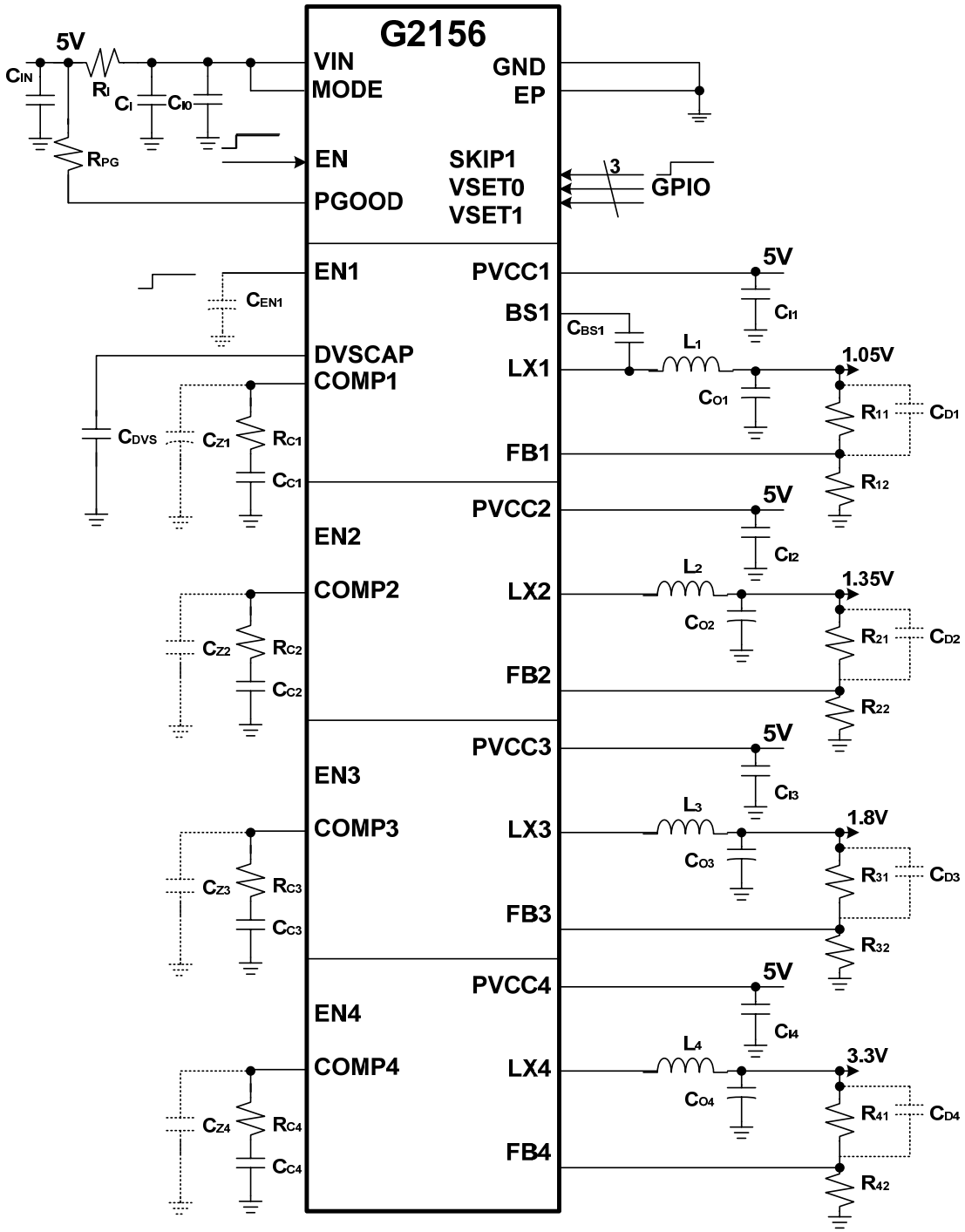
The G2156 have selectable CH1 output voltage as set by the VSET1 and VSET0 pin (Table 2).

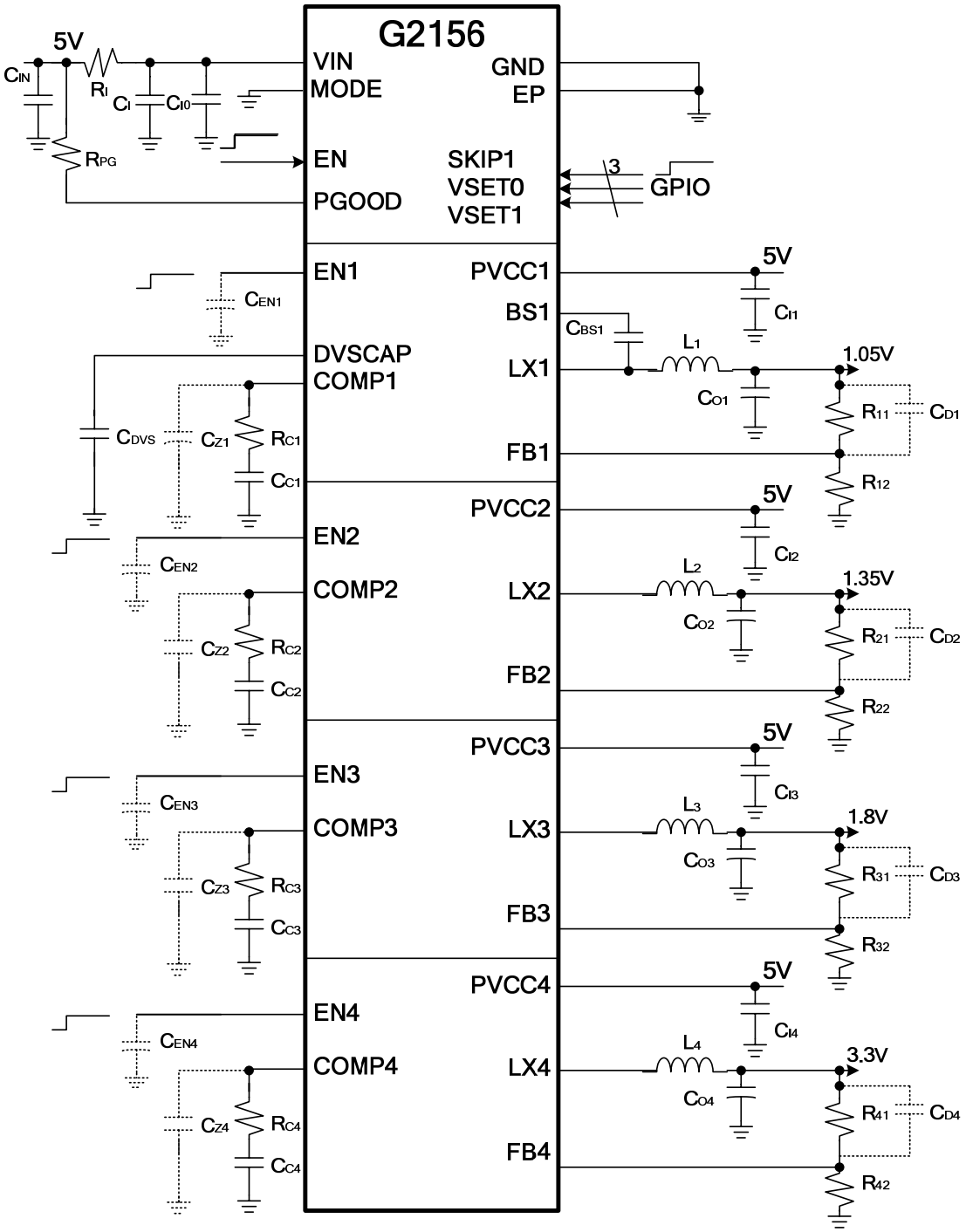
Table 2. Truth Table for CH1 output voltage (R11=50KΩ, R12=160KΩ,)

VSET1	VSET0	CH1 output voltage	CH1 FB1 voltage
GND	GND	1.05V	0.8V
	VIN	1.15V	0.876V
VIN	GND	1.25V	0.953V
	VIN	1.31V	0.998V

Typical Performance Characteristics

Condition: VIN=PVCC1/2/3/4=5V, C_{IN}=22µF, C_I=1µF, C_{I0}=0.1µF, R_I=10Ω,
$C_{EN1/2/3/4}$=0.1µF, L1=2.2µH, L2=L3=L4=2.2µH,
$C_{I1/2/3/4}$=10µF, C_{BS1}=0.1µF, C_{DVS}=10nF, C_{O1}=22µF,C_{O2}=10µF, C_{O3}=10µF,C_{O4}=10µF
R_{C1}=20KΩ, C_{C1}=2.2nF, R_{C2}=39KΩ, C_{C2}=220pF, R_{C3}=39KΩ, C_{C3}=220pF, R_{C4}=39KΩ, C_{C4}=220pF
R11=50KΩ, R12=160KΩ, R21=110KΩ, R22=160KΩ,
R31=200KΩ, R32=160KΩ, R41=500KΩ, R42=160KΩ, R_{PG}=100KΩ
C_{D1}=N.C, C_{D2}= N.C, C_{D3}= N.C, C_{D4}= N.C, C_{Z1}=N.C, C_{Z2}= N.C, C_{Z3}= N.C, C_{Z4}= N.C




G2156
5V
CIN
RI
CI
CI0
RPG
VIN
MODE
EN
PGOOD
GND
EP
SKIP1
VSET0
VSET1
3
GPIO
EN1
CEN1
DVSCAP
COMP1
CDVS
CZ1
RC1
CC1
PVCC1
BS1
CBS1
L1
LX1
CO1
FB1
CI1
1.05V
R11
CD1
R12
EN2
CEN2
COMP2
CZ2
RC2
CC2
PVCC2
L2
LX2
CO2
FB2
CI2
1.35V
R21
CD2
R22
EN3
CEN3
COMP3
CZ3
RC3
CC3
PVCC3
L3
LX3
CO3
FB3
CI3
1.8V
R31
CD3
R32
EN4
CEN4
COMP4
CZ4
RC4
CC4
PVCC4
L4
LX4
CO4
FB4
CI4
3.3V
R41
CD4
R42

Pin Description

PIN NO.	SYMBOL	DESCRIPT
1	EN2	Enable pin, internal pull-up current source.
2	PVCC2	Input supply voltage 2.95V to 6.0V for CH2
3	LX2	The source of the internal high side power MOSFET, and drain of the internal low side (synchronous) rectifier MOSFET.
4	BS1	A bootstrap capacitor is required between BS1 and LX1. The output is forced to switch off until the capacitor is refreshed.
5,6	PVCC1	Input supply voltage 2.95V to 6.0V for CH1
7,8	LX1	The source of the internal high side power MOSFET, and drain of the internal low side (synchronous) rectifier MOSFET.
9	VSET0	CH1 DVS (Dynamic Voltage Scaling) setting pin (ref. Table2)
10	VSET1	CH1 DVS (Dynamic Voltage Scaling) setting pin (ref. Table2)
11	COMP1	Error amplifier output, and input to the output switch current comparator. Connect frequency compensation components to this pin.
12	FB1	Inverting node of the trans-conductance (gm) error amplifier.
13	DVSCAP	CH1 DVS Capacitor.
14	FB4	Inverting node of the trans-conductance (gm) error amplifier.
15	COMP4	Error amplifier output, and input to the output switch current comparator. Connect frequency compensation components to this pin.
16	EN1	Enable pin, internal pull-up current source.
17	SKIP1	SKIP1=VIN sets CH1/3/4 in auto-skip mode, SKIP1=GND sets CH1/3/4 in force PWM mode
18	EN4	Enable pin, internal pull-up current source.
19	PVCC4	Input supply voltage 2.95V to 6.0V for CH4
20	LX4	The source of the internal high side power MOSFET, and drain of the internal low side (synchronous) rectifier MOSFET.
21	PGOOD	An open drain output, asserts low if output voltage is low due to thermal shutdown, over-current, under-voltage or ENx shut down.
22	LX3	The source of the internal high side power MOSFET, and drain of the internal low side (synchronous) rectifier MOSFET.
23	PVCC3	Input supply voltage 2.95V to 6.0V for CH3
24	EN3	Enable pin, internal pull-up current source.
25	MODE	MODE=GND : CH1,2,3,4 independence enable MODE=VIN : On sequence : CH1→CH2/3→CH4 →PGOOD, Off sequence : PGOOD →CH4→ CH2/3→CH1
26	COMP3	Error amplifier output, and input to the output switch current comparator. Connect frequency compensation components to this pin.
27	FB3	Inverting node of the trans-conductance (gm) error amplifier.
28	GND	Analog Ground should be electrically connected to GND close to the device.
29	VIN	Input supply voltage 2.95V to 6.0V, If the voltage on this capacitor is below the minimum required by the VIN UVLO.
30	FB2	Inverting node of the trans-conductance (gm) error amplifier.
31	COMP2	Error amplifier output, and input to the output switch current comparator. Connect frequency compensation components to this pin.
32	EN	Enable pin, enable CHIP Bias circuit
EP	PGND1/2/3/4	Exposed PAD should be soldered to PCB and connected to GND

Block Diagram

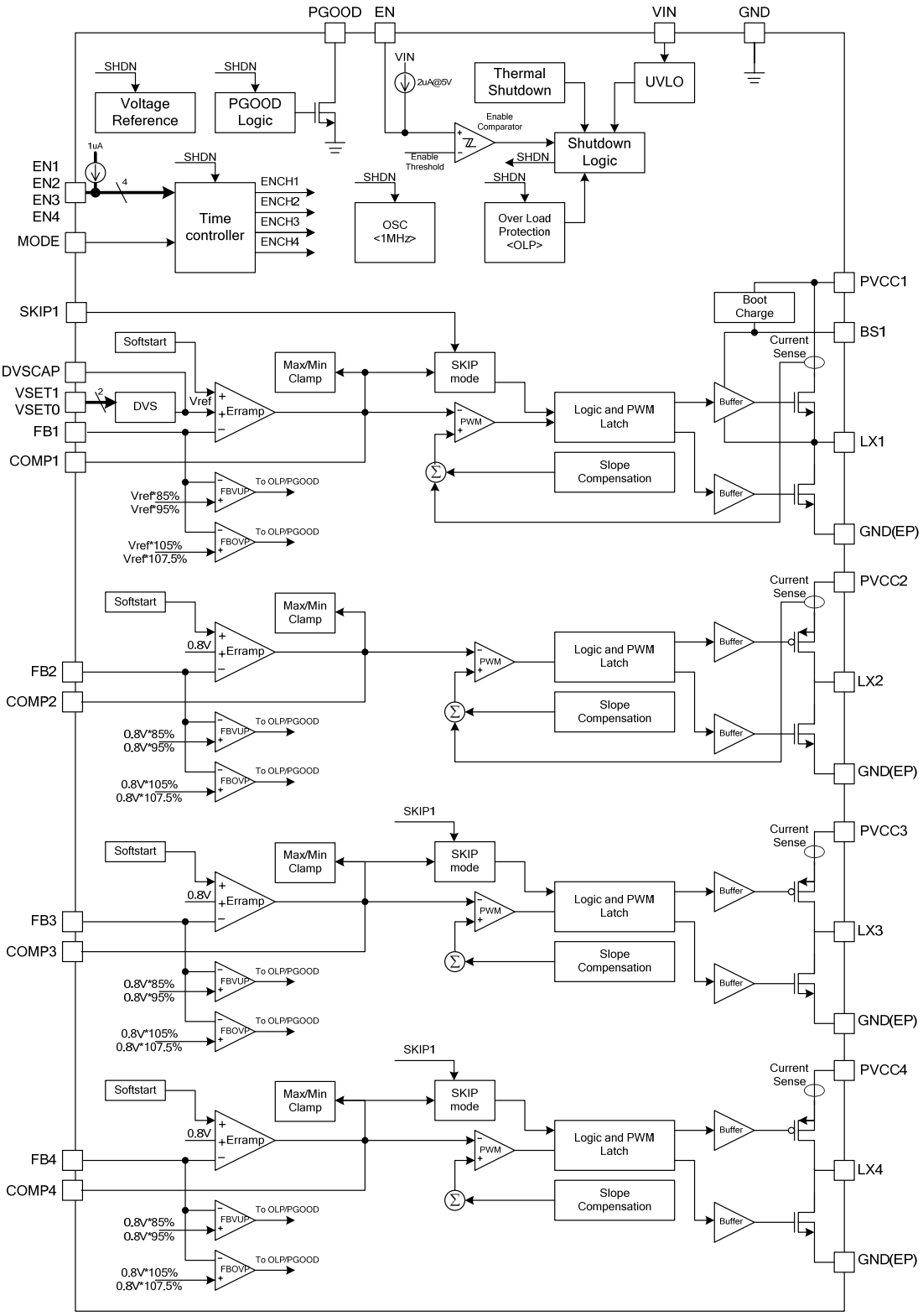


Figure1. Block Diagram of G2156

Application Information

Overview

The G2156 has one channel,5.5V, 3A, synchronous step-down (buck) converter with integrated N/N-MOSFETs, three Channels 5.5V, 1A, synchronous step-down (buck) converter with integrated P/N-MOSFETs .

To improve performance during line and load transients the device implements a constant frequency, peak current mode control which reduces output capacitance and simplifies external frequency compensation design.

The switching frequency of the converters can operate 1 MHz.

The G2156 has a typical default start up voltage of 2.85V. The EN pin has an internal pull-up current source. In addition, the pull up current provides a default condition when the EN pin is floating for the device to operate. The total operating current for the G2156 is 200μA when not switching and under no load. When the device is disabled, the supply current is less than 2μA.

The G2156 reduces the external component count by integrating the boot recharge diode. The bias voltage for the integrated high side MOSFET is supplied by a capacitor on the BS1 to LX1 pin. This BOOT circuit allows the G2156 to operate approaching 100%. The output voltage can be stepped down to as low as the 0.8V reference.

The G2156 has a power good comparator (PG).

Fixed Frequency PWM Control

The G2156 uses a fixed frequency (1MHz), peak current mode control. The output voltage is compared through external resistors on the FB pin to an internal voltage reference by an error amplifier which drives the COMP pin. An internal oscillator initiates the turn on of the high side power switch. The error amplifier output is compared to the high side power switch current. When the power switch current reaches the COMP voltage level the high side power switch is turned off and the low side power switch is turned on.

The COMP pin voltage increases and decreases as the output current increases and decreases. The device implements a current limit by clamping the COMP pin voltage to a maximum level and also implements a minimum clamp for improved transient response performance.

Slope Compensation and Output Current

The G2156 adds a compensating ramp to the switch current signal. This slope compensation prevents sub-harmonic oscillations as duty cycle increases. The available peak inductor current remains constant over the full duty cycle range.

Bootstrap Voltage (BS1) and Low Dropout Operation

The G2156 has an integrated boot regulator and requires a small ceramic capacitor between the BS1 pin and LX1 pin to provide the gate drive voltage for the high side MOSFET. The value of the ceramic capacitor should be 0.1μF. A ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 10V or higher is recommended because of the stable characteristics over temperature and voltage.

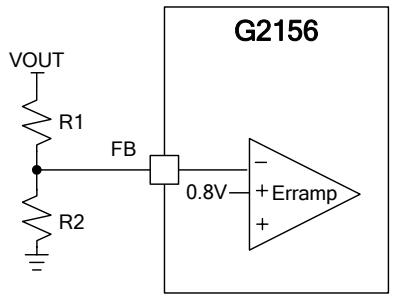
Voltage Reference

The voltage reference system produces a precise ±2% voltage reference over temperature by scaling the output of a temperature stable bandgap circuit. The bandgap and scaling circuits produce 0.8V at the non-inverting input of the error amplifier.

Adjusting the Output Voltage

The output voltage is set with a resistor divider from the output node to the FB pin. It is recommended to use divider resistors with 1% tolerance or better. Start with a 160kΩ for the R1 resistor and use the Equation 1 to calculate R2. To improve efficiency at very light loads consider using larger value resistors. If the values are too high the regulator is more susceptible to noise and voltage errors from the FB input current are noticeable.

$R2=R1*(0.8/(V_{OUT}-0.8))$ (Eq.1)



Voltage Divider Circuit

Over current Protection

The G2156 implements a cycle by cycle current limit. During each switching cycle the high side switch current is compared to the voltage on the COMP pin. When the instantaneous switch current intersects the COMP voltage, the high side switch is turned off. During over-current conditions that pull the output voltage low, the error amplifier responds by driving the COMP pin high, increasing the switch current. The error amplifier output is clamped internally. This clamp functions as a switch current limit.

Power Good (PGOOD Pin)

The PGOOD pin output is an open drain MOSFET. The output is pulled low when the FB voltage enters the fault condition by falling below 85% of the nominal internal reference voltage. There is a 10% hysteresis on the threshold voltage, so when the FB voltage rises to the good condition above 95% of the internal voltage reference the PGOOD output MOSFET is delayed 9.6mS before turned off. It is recommended to use a pull-up resistor between the values of 1kΩ and 100kΩ to a voltage source that is 6.0V or less. The PGOOD is in a valid state once the VIN input voltage is greater than 1.2V.

Over Load Protection (OLP)

The OLP comparator detects CH1 to CH4 output voltage while the power converters work at normal condition. At the same time, the voltage level of OLP is held at low level. If the output loads of these converters rapidly malfunction or short, causing the output voltage to drop, the OLP comparator detects that to enable dropout voltage protection. Dropout voltage detection time is internal takes 10mS.

Thermal Shutdown

The Thermal Protection comparator detects G2156 die temperature. If the die temperature exceeds 150°C, G2156 will be shutdown directly. Thermal shutdown circuit functions only when the G2156 is enabled.

Small Signal Model for Loop Response

Figure-3A shows an equivalent model for the G2156 control loop which can be modeled in a circuit simulation program to check frequency response and dynamic load response. The error amplifier is a trans-conductance amplifier with a gm of 130μA/V. The error amplifier can be modeled using an ideal voltage controlled current source. The resistor Ro and capacitor Co model the open loop gain and frequency response of the amplifier. The 1mV AC voltage source between the nodes a and b effectively breaks the control loop for the frequency response measurements. Plotting a/c shows the small signal response of the frequency compensation. Plotting a/b shows the small signal response of the overall loop. The dynamic loop response can be checked by replacing the RL with a current source with the appropriate load step amplitude and step rate in a time domain analysis.

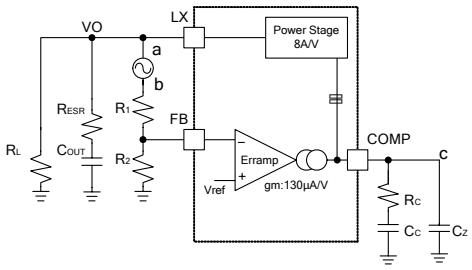


Figure-3A. Small Signal Model for Loop Response

Simple Small Signal Model for Peak Current Mode Control

Figure-3A of the above is a simple small signal model that can be used to understand how to design the frequency compensation. The G2156 power stage can be approximated to a voltage controlled current source (duty cycle modulator) supplying current to the output capacitor and load resistor. The control to output transfer function is shown in Equation 7 and consists of a dc gain, one dominant pole and one ESR zero. The quotient of the change in switch current and the change in COMP pin voltage (node c in figure 3A) is the power stage trans-conductance. The gm for the G2156 is 8.0 A/V. The low frequency gain of the power stage frequency response is the product of the trans-conductance and the load resistance as shown in Equation 8. As the load current increases and decreases, the low frequency gain decreases and increases, respectively. This variation with load may seem problematic at first glance, but the dominant pole moves with load current [see Equation 9]. The combined effect is highlighted by the dashed line in the right half of figure-3B. As the load current decreases, the gain increases and the pole frequency lowers, keeping the 0dB crossover frequency the same for the varying load conditions which makes it easier to design the frequency compensation.

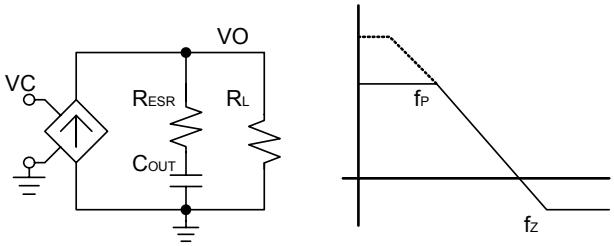


Figure 3B: Simple Small Signal Model and Frequency Response for Peak Current Mode Control

$$\frac{vo}{vc} = Adc \times \frac{\left(1+\frac{s}{2\pi \times fz}\right)}{\left(1+\frac{s}{2\pi \times fp}\right)} \quad \text{---- (Eq.7)}$$

$$Adc = gm_{ps} \times R_L \quad \text{---- (Eq.8)}$$

$$fp = \frac{1}{C_{OUT} \times R_L \times 2\pi} \quad \text{---- (Eq.9)}$$

$$fz = \frac{1}{C_{OUT} \times R_{ESR} \times 2\pi} \quad \text{---- (Eq.10)}$$

Small Signal Model for Frequency

The G2156 uses a trans-conductance amplifier for the error amplifier and readily supports two of the commonly used frequency compensation circuits. The compensation circuits are shown in Figure 3C. The Type 2 circuits are most likely implemented in high bandwidth power supply designs using low ESR output capacitors. In Type 2, one additional high frequency pole is added to attenuate high frequency noise.

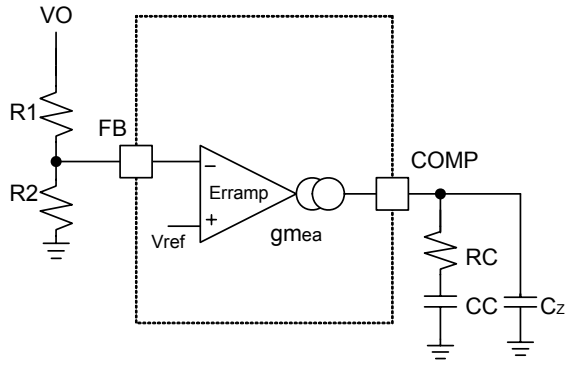


Figure 3C : Types of Frequency Compensation

The design guidelines for G2156 loop compensation are as follows:

1. The modulator pole (fpmod) and the esr zero(fzmod) must be calculated using Equation 11 and Equation 12. Derating the output capacitor (COUT) may be needed if the output voltage is a high percentage of the capacitor rating. Use the capacitor manufacturer information to derate the capacitor value. Use Equation 13 and Equation 14 to estimate a starting point for the crossover frequency, fc. Equation 13 is the geometric mean of the modulator pole and the esr zero and Equation 14 is the mean of modulator pole and the switching frequency. Use the lower value of Equation 13 or Equation 14 as the maximum crossover frequency (fc).

$$fp\,mod = \frac{I_{OUTMAX}}{2\pi \times V_{OUT} \times C_{OUT}} \quad \text{(Eq.11)}$$

$$fz\,mod = \frac{1}{2\pi \times Resr \times C_{OUT}} \quad \text{(Eq.12)}$$

$$fc = \sqrt{fp\,mod \times fz\,mod} \quad \text{(Eq.13)}$$

$$fc = \sqrt{fp\,mod \times \frac{fsw}{2}} \quad \text{(Eq.14)}$$

2. R_C can be determined by

$$R_C = \frac{2\pi \times fc \times Vo \times C_{OUT}}{gm_{ea} \times Vref \times gm_{ps}} \quad \text{(Eq.15)}$$

Where is the gm_{ea} amplifier gain (130 µA/V), gm_{ps} is the power stage gain (8.0A/V).

3. Place a compensation zero at the dominant pole:

$$fp = \frac{1}{C_{OUT} \times R_L \times 2\pi}$$

C_C can be determined by :

$$C_C = \frac{R_L \times C_{OUT}}{R_C} \quad \text{(Eq.16)}$$

3. Cz is optional. It can be used to cancel the zero from Cout's ESR.

$$C_Z = \frac{R_{ESR} \times C_{OUT}}{R_C} \quad \text{(Eq.17)}$$

Layout Guide

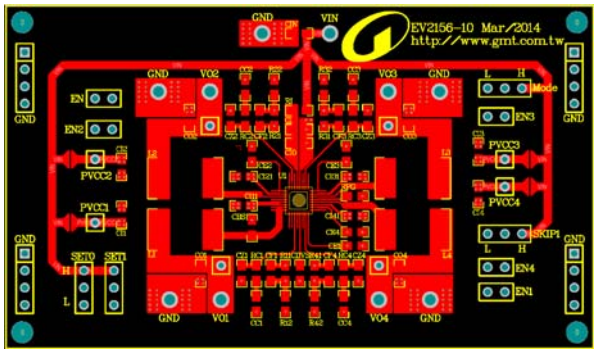
Layout is a critical portion of good power supply design. There are several signal paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance.

1. Care should be taken to minimize the loop area formed by the bypass capacitor connections and the VIN pins. The AGND pins and GND pin should be tied directly to the power pad under the IC. The power pad should be connected to any internal PCB ground planes using multiple vias directly under the IC. Additional vias can be used to connect the top side ground area to the internal planes near the input and output capacitors.
2. The top side ground area along with any additional internal ground planes must provide adequate heat dissipating area for operation at full rated load.
3. Locate the input bypass capacitor as close to the IC as possible. The LX pin should be routed to the output inductor. Since the LX connection is the switching node, the output inductor should be located very close to the LX pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling.
4. The boot capacitor must also be located close to the device. The sensitive analog ground connections for the feedback voltage divider, compensation components, slow start capacitor and frequency set resistor should be connected to a separate analog ground trace as shown.

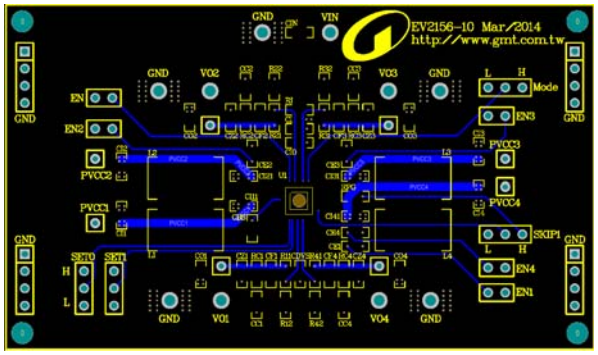
It may be possible to obtain acceptable performance with alternate PCB layouts, however this layout has been shown to produce good results and is meant as a guideline.

EV Board PCB Layout Section

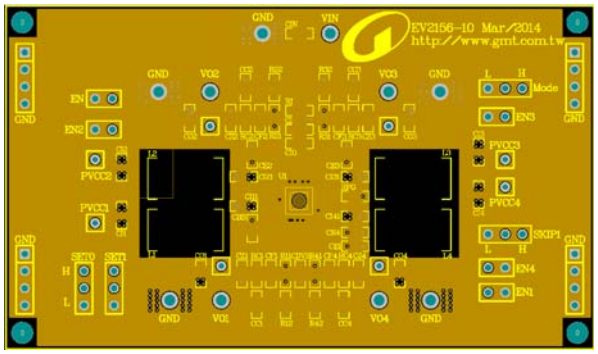
Top Layer



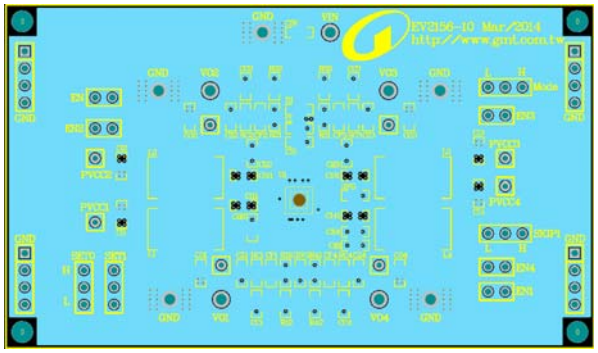
Bottom Layer



Internal Layer 1 (AGND)



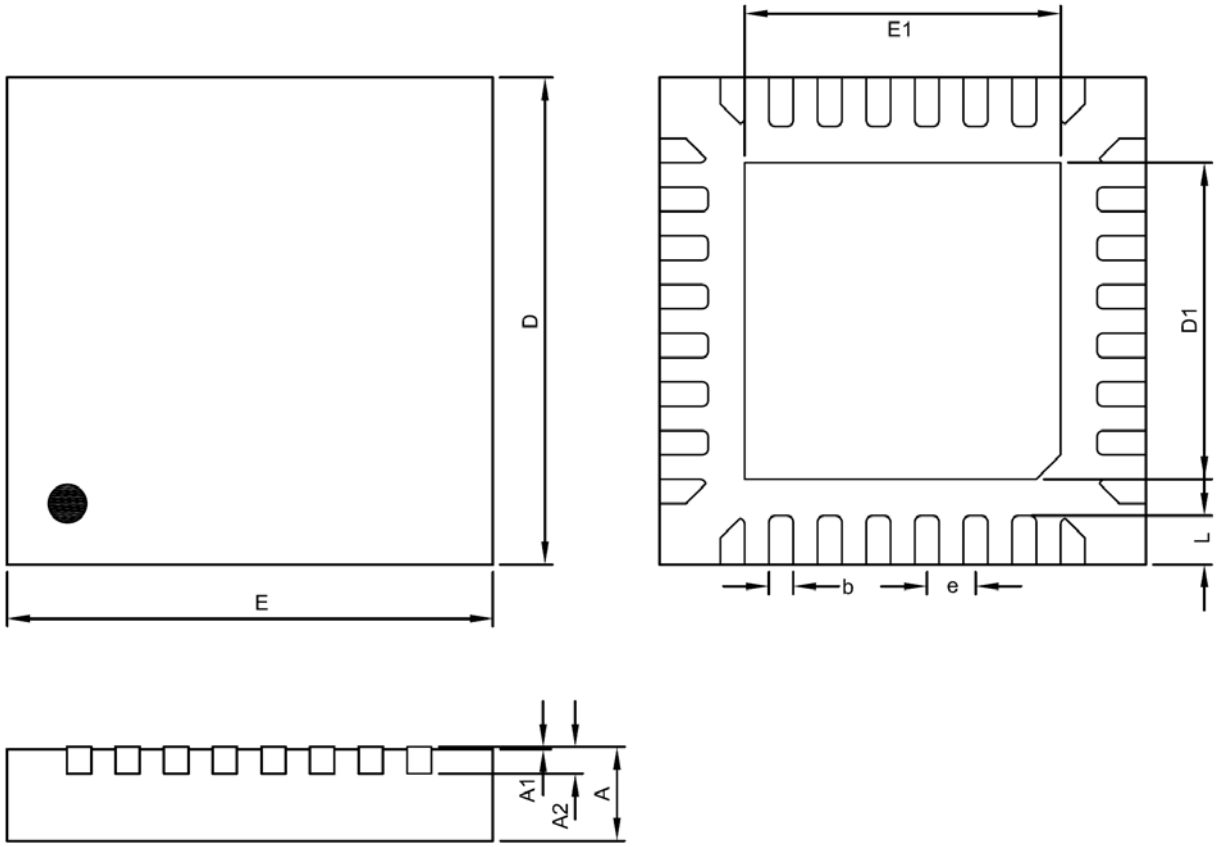
Internal Layer 2 (PGND)



Board Information

Board Material	FR4
Size	152.4mm*101.6mm
Board Thickness	1.6mm
Layers	4
Copper Thickness	1 oz.

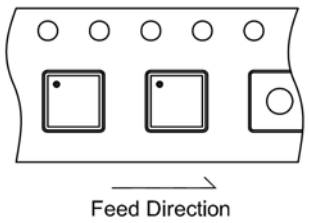
Package Information



TQFN4X4-32 Package

Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.0276	0.0295	0.0315
A1	0.00	- - -	0.05	0.0000	- - -	0.0020
A2	0.20 REF			0.0079 REF		
D	3.95	4.00	4.05	0.1555	0.1575	0.1594
E	3.95	4.00	4.05	0.1555	0.1575	0.1594
D1	2.65	2.70	2.85	0.1043	0.1063	0.1122
E1	2.65	2.70	2.85	0.1043	0.1063	0.1122
b	0.15	0.20	0.25	0.0059	0.0079	0.0098
e	0.40 BSC			0.0157 BSC		
L	0.33	0.40	0.45	0.0130	0.0157	0.0177

Taping Specification



PACKAGE	Q'TY/REEL
TQFN4X4-32	3,000 ea