G2195

Signage PMIC for Electronic Paper Display

Features

- **8.0V to 13.2V Input Voltage Range**
- **Auto Buck-Boost Controller VPOS1/VPOS2 /VPOS3 for Source Driver Supply of Positive Rails**
- **Inverting Buck-Boost Controller VNEG1/ VNEG2/VNEG3 for Source Driver Supply of Negative Rails**
  -VPOS1/VNEG1: ±2V to ±20V, 1.6A(max.)
  -VPOS2/VNEG2: ±2V to ±20V, 1.6A(max.)
  -VPOS3/VNEG3: ±2V to ±30V, 1.6A(max.)
  -Accurate Output Voltage Tracking
  VPOSx+VNEGx= ±500mV @ ±15V
- **Two Async-Boost Controller and One Async -Inverting Controller for Gate Driver Supply:**
  -VGH1/2: 12V to 50V, 200mA(max.)
  -VGL: -10V to -50V, 200mA(max.)
- **Adjustable Inverting Buck-Boost Converter DC VCOM, Boost Converter VCOMH and Inverting Buck-Boost Controller VCOML for Accurate Panel Backplane Biasing**
  - **DCVCOM: -5V to -0.1V, 2.5A(max.)**
  - **VCOMH: 4V to 20V, 2.5A(max.)**
  - **VCOML: -9V to -25V, 2.5A(max.)**
  - **±1.5% Accuracy**
  - **9-Bit DACs control**
- **Internal Active Discharge for VPOSx/VNEGx /VGHx, and external VCOM Discharge control**
- **Thermistor Monitoring**
  - **-25°C to +85°C Temperature Range**
  - **±1.0°C Accuracy from -20°C to 70°C**
- **I²C Slave Mode Interface (Address 0x48H)**
- **Protection: UVLO, OTP, OCP, SCP, UVP**
- **QFN12X12-100**

General Description

The G2195 is a single-chip power management IC (PMIC) for large-size electronic paper displays (EPD) that provides source- and gate-driver power supplies, a VCOM bias, and a temperature sensor. All rails are adjustable through the I2C interface to accommodate specific panel requirements.

The G2195 is available in 100-pin QFN (12X12) package and is specified over the -40°C to +85°C extended temperature range.

Applications

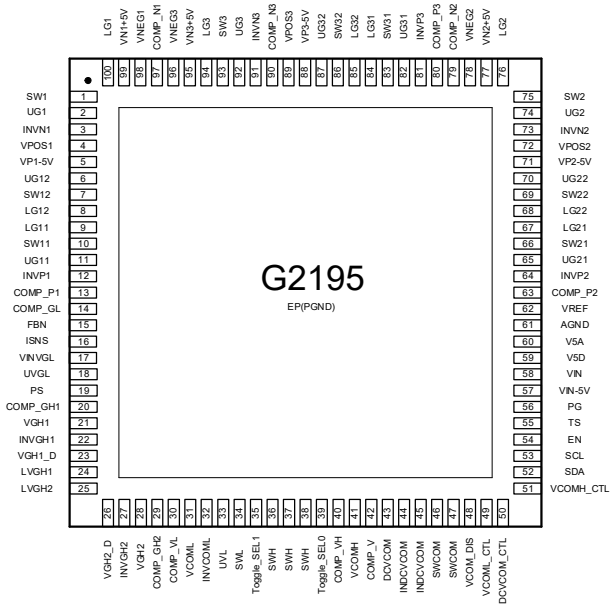
- **Large-size EPD Power Supplies**

Ordering Information

ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE (Green)
G2195HP1U	2195	-40°C to +85°C	QFN12X12-100

Note: HP:QFN12X12-100
1: Bonding code
U: Tape & Reel
Green: Lead Free / Halogen Free

Pin Configuration



Absolute Maximum Ratings*1

VIN, VIN-5V, INVPx, INVNx, INVGHx, VINVGL, INVCOML, INDVCOM, Input Voltage.... -0.3V to +14.5V
UG11/21/31, SW11/21/31, UGx, VGHx_D, ISNS, UVGL, UVL input Voltage . . . . . -0.3V to +14.5V
LG1x, LG2x, LG3x, LVGHx input Voltage. . -0.3V to +5.5V
VPOS1/2, VP1-5V, VP2-5V, SW12/22, UG12/22, input voltage . . . . . -0.3V to +23V
VPOS3, VP3-5V, SW32, UG32 input voltage -0.3V to 33V
VNEG1, VNEG2 input Voltage. . . . . -23V to +0.3V
VN1+5V,VN2+5V,LG1/2 input Voltage . . -23V to +5.5V
SW1, SW2 input Voltage . . . . . -23 to +14.5V
VNEG3 input Voltage. . . . . .-33V to +0.3V
VN3+5V, LG3, input Voltage. . . . . .-33V to 5.5V
SW3, input Voltage. . . . . .-33V to +14.5V
VGH1, VGH2 input Voltage . . . . . -0.3V to +53V
SWL, input Voltage. . . . . .-28V to +14.5V
VCOML input Voltage. . . . . .-28V to +0.3V
VCOMH, VCOMH_CTL input Voltage . . . . . .-0.3V to 23V
SWH input Voltage. . . . . -0.3V to +40V
DCVCOM_CTL,VCOML_CTL, input Voltage . . . . . -28V to +5.5V
SWCOM input Voltage. . . . . -7V to +14.5V
DCVCOM input Voltage. . . . . -7V to +0.3V
SDA, SCL, EN, TS, PG, FBN, COMP_x, VREF, PS, Toggle_SEL0, Toggle_SEL1, VCOM_DIS Input Voltage . . . . . .-0.3V to +5.5V
Thermal Resistance Junction to Ambient, (θ_{JA})
QFN12X12-100 . . . . . 23.3°C/W
Continuous Power Dissipation (T_A = +25°C)
QFN12X12-100 . . . . . .5360 mW
Operation Temperature . . . . . .-40°C to +85°C
Junction Temperature . . . . . .150°C
Storage Temperature Range . . . . . -65°C to 160°C
ESD Susceptibility (HBM) . . . . . .2kV(Note2)
Reflow Temperature (soldering, 10sec) . . . . . 260°C

Recommended Operation Conditions

VIN, INVPx, INVNx, INVGHx, INVCOM, INVGL . . . . . 8V to 13.2V
Operating Ambient Temperature (T_A) . . .-25°C to 85°C

1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Device are ESD sensitive. Handling precaution recommended. The Human Body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.

Electrical Characteristics

(V_{IN}=V_{INVPx}= V_{INVNx} = V_{INVGHx} = V_{INVGL} = V_{INVCOM} =12V±10%, T_A=25°C)

The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
GENERAL						
Supply Voltage	V_{IN}		8.0	---	13.2	V
VIN UVLO	V_{IN_UVLO}		---	7.5	---	V
VIN UVLO Hysteresis	V_{IN_HYS}		---	0.5	---	V
Quiescent Current in Normal Mode	I_{IN}	EN=High, ON/OFF bit=”0”	---	3.5	---	mA
Quiescent Current in Standby Mode	I_{STD}	EN=Low, ON/OFF bit=”X”	---	250	---	µA
Quiescent Current in Shutdown Mode	I_{SD}	PS=High	---	15	---	µA
Regulated Voltage for Pre-Drv Circuit	V_{VIN-5V}	Bypass Cap. Is10µF	---	VIN-5	---	V
Regulated Voltage for Analog Circuit	V_{5A}	Bypass Cap. Is10µF	---	5	---	V
Regulated Voltage for Digital Circuit	V_{5D}	Bypass Cap. Is10µF	---	5	---	V
VREF Voltage	V_{REF}	Bypass Cap. Is 10µF	---	2.5	---	V
Thermal Shutdown Trip Point	T_{SD}		---	150	---	°C
Thermal Shutdown Hysteresis	T_{HYS}		---	20	---	°C

Electrical Characteristics (Continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
VPOS1(Auto Buck-BOOST Controller)						
Switch Frequency	F_{SW_VPOS1}	FREQ_VPOS1[2]=0	---	500	---	KHz
Soft-Start period	T_{SS_VPOS1}	SS[7:6]="00"	---	6	---	ms
UGate Driver Source	R_{UG1x_SR}	UGate is high state	---	2	---	Ω
UGate Driver Sink	R_{UG1x_SK}	UGate is low state	---	2	---	Ω
LGate Driver Source	R_{LG1x_SR}	LGate is high state	---	5	---	Ω
LGate Driver Sink	R_{LG1x_SK}	LGate is low state	---	2	---	Ω
Gate Drive Output Voltage	V_{Gate}	$V_{Gate} = V_{INVP1} - V_{UG11}$	---	5	---	V
		$V_{Gate} = V_{VPOS1} - V_{UG12}$	---	5	---	V
		$V_{Gate} = V_{LG11} / V_{LG12}$	---	5	---	V
Switch Current Limit	I_{LIMIT}	V_{IN}=12V, MOS Ron=38 mΩ	---	4.5	---	A
Output Voltage Range	VPOS1	VPOS1[9:0] SET output voltage	2	---	20	V
Power Good Threshold		Fraction of nominal voltage	---	90	---	%
Output Accuracy		VPOS1[9:0]=10V, I_{Load}=200mA	-2	---	2	%
Discharge Impedance to Ground	R_{DIS}		---	750	---	Ω
Fault Protection		Fraction of nominal voltage, Falling	---	85	---	%
		Fault Timer	---	16	---	ms
VPOS2(Auto Buck-BOOST Controller)						
Switch Frequency	F_{SW_VPOS2}	FREQ_VPOS2[2]=0	---	500	---	KHz
Soft-Start period	T_{SS_VPOS2}	SS[7:6]="00"	---	6	---	ms
UGate Driver Source	R_{UG2x_SR}	UGate is high state	---	2	---	Ω
UGate Driver Sink	R_{UG2x_SK}	UGate is low state	---	2	---	Ω
LGate Driver Source	R_{LG2x_SR}	LGate is high state	---	5	---	Ω
LGate Driver Sink	R_{LG2x_SK}	LGate is low state	---	2	---	Ω
Gate Drive Output Voltage	V_{Gate}	$V_{Gate} = V_{INVP2} - V_{UG21}$	---	5	---	V
		$V_{Gate} = V_{VPOS2} - V_{UG22}$	---	5	---	V
		$V_{Gate} = V_{LG21} / V_{LG22}$	---	5	---	V
Switch Current Limit	I_{LIMIT}	V_{IN}=12V, MOS Ron=38 mΩ	---	4.5	---	A
Output Voltage Range	VPOS2	VPOS2[9:0] SET output voltage	2	---	20	V
Power Good Threshold		Fraction of nominal voltage	---	90	---	%
Output Accuracy		VPOS2[9:0]=15V, I_{Load}=200mA	-2	---	2	%
Discharge Impedance to Ground	R_{DIS}		---	750	---	Ω
Fault Protection		Fraction of nominal voltage, Falling	---	85	---	%
		Fault Timer	---	16	---	ms
VPOS3(Auto Buck-BOOST Controller)						
Switch Frequency	F_{SW_VPOS3}	FREQ_VPOS3[2]=0	---	500	---	KHz
Soft-Start period	T_{SS_VPOS3}	SS[7:6]="00"	---	6	---	ms
UGate Driver Source	R_{UG3x_SR}	UGate is high state	---	2	---	Ω
UGate Driver Sink	R_{UG3x_SK}	UGate is low state	---	2	---	Ω
LGate Driver Source	R_{LG3x_SR}	LGate is high state	---	5	---	Ω
LGate Driver Sink	R_{LG3x_SK}	LGate is low state	---	2	---	Ω
Gate Drive Output Voltage	V_{Gate}	$V_{Gate} = V_{INVP3} - V_{UG31}$	---	5	---	V
		$V_{Gate} = V_{VPOS3} - V_{UG32}$	---	5	---	V
		$V_{Gate} = V_{LG31} / V_{LG32}$	---	5	---	V
Switch Current Limit	I_{LIMIT}	V_{IN}=12V, MOS Ron=38 mΩ	---	6.8	---	A
Output Voltage Range	VPOS3	VPOS3[9:0] SET output voltage	2	---	30	V
Power Good Threshold		Fraction of nominal voltage	---	90	---	%
Output Accuracy		VPOS3[9:0]=24V, I_{Load}=200mA	-2	---	2	%
Discharge Impedance to Ground	R_{DIS}		---	750	---	Ω
Fault Protection		Fraction of nominal voltage, Falling	---	85	---	%
		Fault Timer	---	16	---	ms

Electrical Characteristics (Continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
VNEG1(INVERTING BUCK-BOOST REGULATOR)						
Switch Frequency	F_{SW_VNEG1}	FREQ_VNEG1[2]=0	---	500	---	KHz
Soft-Start period	T_{SS_VNEG1}	SS[7:6]="00"	---	6	---	ms
UGate Driver Source	R_{UG1_SR}	UGate is high state	---	2	---	Ω
UGate Driver Sink	R_{UG1_SK}	UGate is low state	---	2	---	Ω
LGate Driver Source	R_{LG1_SR}	LGate is high state	---	3	---	Ω
LGate Driver Sink	R_{LG1_SK}	LGate is low state	---	2	---	Ω
Gate Drive Output Voltage	V_{Gate}	$V_{Gate} = V_{INVN1} - V_{UG1}$	---	5	---	V
		$V_{Gate} = V_{LG1} - V_{VNEG1}$	---	5	---	V
Switch Current Limit	I_{LIMIT}	V_{IN}=12V, MOS Ron=38 mΩ	---	6	---	A
Output Voltage Range	VNEG1	VNEG1[9:0] SET output voltage	-20	---	-2	V
Power Good Threshold		Fraction of nominal voltage	---	90	---	%
Output Accuracy		VNEG1[9:0]=-10V, I_{Load}=200mA	-2	---	2	%
Discharge Impedance to Ground	R_{DIS}		---	500	---	Ω
Fault Protection		Fraction of nominal voltage, Falling	---	85	---	%
		Fault Timer	---	16	---	ms
VNEG2(INVERTING BUCK-BOOST REGULATOR)						
Switch Frequency	F_{SW_VNEG2}	FREQ_VNEG2[2]=0	---	500	---	KHz
Soft-Start period	T_{SS_VNEG2}	SS[7:6]="00"	---	6	---	ms
UGate Driver Source	R_{UG2_SR}	UGate is high state	---	2	---	Ω
UGate Driver Sink	R_{UG2_SK}	UGate is low state	---	2	---	Ω
LGate Driver Source	R_{LG2_SR}	LGate is high state	---	3	---	Ω
LGate Driver Sink	R_{LG2_SK}	LGate is low state	---	2	---	Ω
Gate Drive Output Voltage	V_{Gate}	$V_{Gate} = V_{INVN2} - V_{UG2}$	---	5	---	V
		$V_{Gate} = V_{LG2} - V_{VNEG2}$	---	5	---	V
Switch Current Limit	I_{LIMIT}	V_{IN}=12V, MOS Ron=38 mΩ	---	6	---	A
Output Voltage Range	VNEG2	VNEG2[9:0] SET output voltage	-20	---	-2	V
Power Good Threshold		Fraction of nominal voltage	---	90	---	%
Output Accuracy		VNEG2[9:0]=-15V, I_{Load}=200mA	-2	---	2	%
Discharge Impedance to Ground	R_{DIS}		---	500	---	Ω
Fault Protection		Fraction of nominal voltage, Falling	---	85	---	%
		Fault Timer	---	16	---	ms
VNEG3(INVERTING BUCK-BOOST REGULATOR)						
Switch Frequency	F_{SW_VNEG3}	FREQ_VNEG3[2]=0	---	500	---	KHz
Soft-Start period	T_{SS_VNEG3}	SS[7:6]="00"	---	6	---	ms
UGate Driver Source	R_{UG3_SR}	UGate is high state	---	2	---	Ω
UGate Driver Sink	R_{UG3_SK}	UGate is low state	---	2	---	Ω
LGate Driver Source	R_{LG3_SR}	LGate is high state	---	3	---	Ω
LGate Driver Sink	R_{LG3_SK}	LGate is low state	---	2	---	Ω
Gate Drive Output Voltage	V_{Gate}	$V_{Gate} = V_{INVN3} - V_{UG3}$	---	5	---	V
		$V_{Gate} = V_{LG3} - V_{VNEG3}$	---	5	---	V
Switch Current Limit	I_{LIMIT}	V_{IN}=12V, MOS Ron=48 mΩ	---	7	---	A
Output Voltage Range	VNEG3	VNEG3[9:0] SET output voltage	-30	---	-2	V
Power Good Threshold		Fraction of nominal voltage	---	90	---	%
Output Accuracy		VNEG3[9:0]=-24V, I_{Load}=200mA	-2	---	2	%
Discharge Impedance to Ground	R_{DIS}		---	800	---	Ω
Fault Protection		Fraction of nominal voltage, Falling	---	85	---	%
		Fault Timer	---	16	---	ms

Electrical Characteristics (Continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
VPOS1/2/3 and VNEG1/2/3 Tracking(Only for VPOS/VNEG are of opposite sign but same magnitude)						
Difference between VPOS1/2/3 and VNEG1/2/3	V_{DIFF}	(VPOS1/2/3,VNEG1/2/3)=(+15V ,-15V), I_{LOAD}=±20mA, -25°C to 80°C, TRACK1/2/3="1"	-500	---	500	mV
VGH1(ASYN-BOOST CONTROLLER)						
Switch Frequency	F_{SW_VGH1}	FREQ_VGH1[2]=0	---	500	---	KHz
Soft-Start period	T_{SS_VGH1}	SS[7:6]="00"	---	6	---	ms
Switch ON Resistance	R_{ON}	INVGH1 to VGH1_D	---	100	---	mΩ
LGate Driver Source	R_{VGH1_SR}	LGate is high state	---	3	---	Ω
LGate Driver Sink	R_{VGH1_SK}	LGate is low state	---	1	---	Ω
Switch Current Limit	I_{LIMIT}	V_{IN}=12V	---	3	---	A
Output Voltage Range	VGH1	VGH1[9:0] SET output voltage	12	---	50	V
Power Good Threshold		Fraction of nominal voltage	---	90	---	%
Output Accuracy		VGH1[9:0]=27V, I_{Load}=20mA	-1	---	1	%
Discharge Impedance to Ground	R_{DIS}	DIS_VGH1_CTL="0"	---	4000	---	Ω
Fault Protection		Fraction of nominal voltage, Falling	---	85	---	%
		Fault Timer	---	16	---	ms
VGH2(ASYN-BOOST CONTROLLER & POST DRIVE MODE)						
Switch Frequency	F_{SW_VGH2}	FREQ_VGH2[3]=0	---	500	---	KHz
Soft-Start period	T_{SS_VGH2}	SS[7:6]="00"	---	6	---	ms
Switch ON Resistance	R_{ON}	INVGH2 to VGH2_D	---	100	---	mΩ
LGate Driver Source	R_{VGH2_SR}	LGate is high state	---	3	---	Ω
LGate Driver Sink	R_{VGH2_SK}	LGate is low state	---	1	---	Ω
Switch Current Limit	I_{LIMIT}	V_{IN}=12V	---	3	---	A
Output Voltage Range	VGH2	VGH2[9:0] SET output voltage	12	---	50	V
Power Good Threshold		Fraction of nominal voltage	---	90	---	%
Output Accuracy		VGH2[9:0]=27V, I_{Load}=20mA	-1	---	1	%
Discharge Impedance to Ground	R_{DIS}	DIS_VGH2_CTL1	---	1500	---	Ω
VPDD Output Range	V_{VPDD}	VPDD[7:3] SET output voltage	2	---	10	V
Output Accuracy		VPDD[7:3]=3V, I_{Load}=20mA	-1	---	1	%
VPDD delay time	$T_{VPDD-LEN}$	VPDD_LEN[7:0] SET delay time	0	---	30	s
VDDH_EXT delay time	$T_{VDDH-EXT}$	VDDH_EXT[4:0] SET delay time	0	---	1	s
Discharge Impedance to Ground	R_{DIS}	DIS_VGH2_CTL2	---	2500	---	Ω
Fault Protection		Fraction of nominal voltage, Falling	---	85	---	%
		Fault Timer	---	16	---	ms
VGL(ASYN-INVERTING BUCK-BOOST CONTROLLER & POST DRIVE MODE)						
Switch Frequency	F_{SW_VGL}	FREQ_VGL[2]=0	---	500	---	KHz
Soft-Start period	T_{SS_VGL}	SS[7:6]="00"	---	6	---	ms
UGate Driver Source	R_{VGL_SR}	UGate is high state	---	1	---	Ω
UGate Driver Sink	R_{VGL_SK}	UGate is low state	---	3	---	Ω
Switch Current Limit	I_{LIMIT}	V_{IN}=12V, R_{SENSE}=10mΩ	---	2	---	A
Power Good Threshold		Fraction of nominal voltage	---	90	---	%
Output Voltage Range	VGL		-50	---	-10	V
FBN Regulation Voltage	V_{FBN}		---	0	---	V
FBN Accuracy	V_{FBN_REG}		-10	---	10	mV
VEE_EXT delay time	$T_{VDDH-EXT}$	VEE_EXT[7:1] SET delay time	0	---	6.3	s
Fault Protection		Falling	---	85	---	%
		Fault Timer	---	16	---	ms

Electrical Characteristics (Continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
DCVCOM(ASYN-INVERTING BUCK-BOOST CONVERTER)						
Switch Frequency	F_{SW_VCOM}	FREQ_VCOM[3]=0	---	500	---	KHz
Soft-Start period	T_{SS_VCOM}	SS[7:6]="00"	---	6	---	ms
Switch ON Resistance	R_{ON_P}	V_{IN}=12V	---	---	100	mΩ
Switch Current Limit	I_{LIMIT}	V_{IN}=12V	---	5	---	A
Output Voltage Range	DCVCOM	DCVCOM[8:0] SET output voltage	-5	---	0	V
Power Good Threshold		Fraction of nominal voltage	---	90	---	%
Output Accuracy		DCVCOM[8:0]=-2V, I_{Load}=20mA	-1.5	---	+1.5	%
Fault Protection		Fraction of nominal voltage, Falling	---	85	---	%
		Fault Timer	---	16	---	ms
VCOMH(ASYN- BOOST CONVERTER)						
Switch Frequency	F_{SW_VCOMH}	FREQ_VCOMH[2]=0	---	500	---	KHz
Soft-Start period	T_{SS_VCOMH}	SS[7:6]="00"	---	6	---	ms
Switch ON Resistance	R_{ON_N}	V_{IN}=12V	---	50	---	mΩ
Switch Current Limit	I_{LIMIT}	V_{IN}=12V	---	8	---	A
Output Voltage Range	VCOMH	VCOMH[8:0] SET output voltage	4	---	20	V
Power Good Threshold		Fraction of nominal voltage	---	90	---	%
Output Accuracy		VCOMH[8:0]=14V, I_{Load}=20mA	-1.5	---	+1.5	%
Fault Protection		Fraction of nominal voltage, Falling	---	85	---	%
		Fault Timer	---	16	---	ms
VCOML(ASYN- INVERTING BUCK-BOOST CONTROLLER)						
Switch Frequency	F_{SW_VCOML}	FREQ_VCOML[1]=0	---	500	---	KHz
Soft-Start period	T_{SS_VCOML}	SS[7:6]="00"	---	6	---	ms
UGate Driver Source	R_{VCOML_SR}	UGate is high state	---	1	---	Ω
UGate Driver Sink	R_{VCOML_SK}	UGate is low state	---	3	---	Ω
Switch Current Limit	I_{LIMIT}	V_{IN}=12V, MOS Ron=18 mΩ	---	12	---	A
Output Voltage Range	VCOML	VCOML[8:0] SET output voltage	-25	---	-9	V
Power Good Threshold		Fraction of nominal voltage	---	90	---	%
Output Accuracy		VCOML[8:0]=-14V, I_{Load}=20mA	-1.5	---	+1.5	%
Fault Protection		Fraction of nominal voltage, Falling	---	85	---	%
		Fault Timer	---	16	---	ms
VCOM CONTROL						
Input Low Threshold Level	V_{IL}	Toggle_SEL0/Toggle_SEL1	---	---	0.6	V
Input High Threshold Level	V_{IH}	Toggle_SEL0/Toggle_SEL1	1.5	---	---	V
Output Drive Source Current	I_{VCOM_DIS}	V_{VCOM_DIS}=3.5V	---	60	---	mA
VCOMH active-Output Low	V_{OL}	I_O=0.5mA,sink current(VCOMH_CTL)	---	1		V
VCOML active-Output High	V_{OH}		---	4.5	---	V
DCVCOM active-Output High	V_{OH}		---	4.5	---	V
Thermistor Monitor(Use 10KΩ Murata NCP15XH103F03RC)						
Offset	$Offset_{TMS}$	Temperature=0°C	---	1.22	---	V
Maximum Input Level	V_{TMS_MAX}	VREF	---	2.5	---	V
External Pull Up Resistor	R_{NTC_UP}		---	9.53	---	KΩ
External Linearization Resistor	R_{Linear}		---	13.7	---	KΩ
ADC Resolution	ADC_{RES}	Not Tested in production, 1-bit	---	10	---	mV
ADC Conversion Time	ADC_{DEL}	Not Tested in production	---	300	---	µs
Accuracy	TMS_{ACC}	Not Tested in production, 1-bit	-1	---	1	LSB
Logic Levels and Timing Characteristics (SCL, SDA, PG, EN, PS)						
Output Low Threshold Level	V_{OL}	I_O=3mA, sink current (SDA,PG)	---	---	0.4	V
Input Low Threshold Level	V_{IL}		---	---	0.6	V
Input High Threshold Level	V_{IH}		1.5	---	---	V
Deglitch Time, EN pin	$t_{Deglitch}$		---	100	---	µs
SCL Clock Frequency	F_{SCL}		---	---	400	KHz
I^2C Slave Address		7-bit slave address	---	0x48h	---	

Data Transmission Timing

(VIN=12V±10%, T_A=25°C, CL=100pF, unless otherwise specified**)**

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
I²C TIMING CHARCTERISTICS						
Serial-Clock Frequency	f_{SCL}		---	---	400	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}	F_{SCL}=100KHz	4.7	---	---	µs
		F_{SCL}=400KHz	1.3	---	---	
Hold Time (Repeated) START Condition	$t_{HD,STA}$	F_{SCL}=100KHz	4.0	---	---	µs
		F_{SCL}=400KHz	0.6	---	---	
SCL Pulse-Width Low	t_{LOW}	F_{SCL}=100KHz	4.7	---	---	µs
		F_{SCL}=400KHz	1.3	---	---	
SCL Pulse-Width High	t_{HIGH}	F_{SCL}=100KHz	4.0	---	---	µs
		F_{SCL}=400KHz	0.6	---	---	
Setup Time for a Repeated START Condition	$t_{SU,STA}$	F_{SCL}=100KHz	4.7	---	---	µs
		F_{SCL}=400KHz	0.6	---	---	
Data Hold Time	$t_{HD,DAT}$	F_{SCL}=100KHz	0	---	3.45	µs
		F_{SCL}=400KHz	0	---	0.9	
Data Setup Time	$t_{SU,DAT}$	F_{SCL}=100KHz	250	---	---	ns
		F_{SCL}=400KHz	100	---	---	
SDA and SCL Receiving Rise Time	t_R	F_{SCL}=100KHz	---	---	1000	ns
		F_{SCL}=400KHz	---	---	300	
SDA and SCL Receiving Fall Time	t_F	F_{SCL}=100KHz	---	---	300	ns
		F_{SCL}=400KHz	---	---	300	
Setup Time for STOP Condition	$t_{SU,STO}$	F_{SCL}=100KHz	4	---	---	µs
		F_{SCL}=400KHz	0.6	---	---	
Bus Capacitance	C_B		---	---	400	pF
Pulse Width of Suppressed Spike	t_{SP}		0	---	50	ns

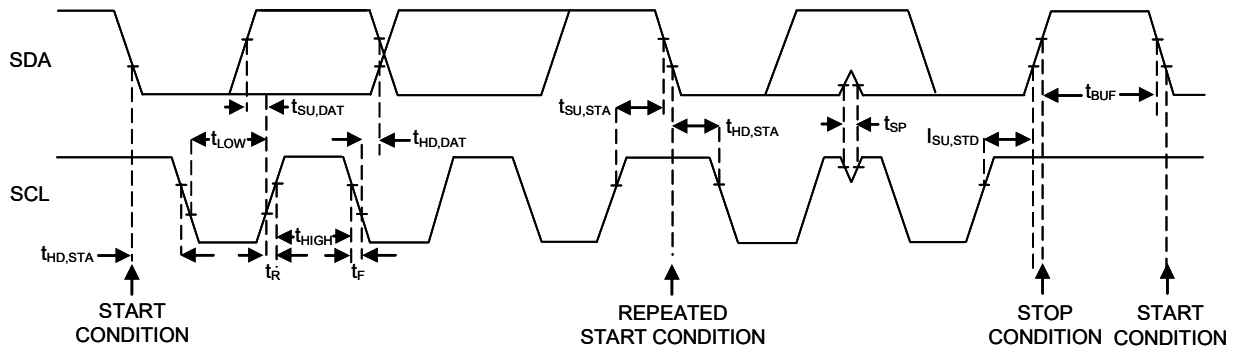
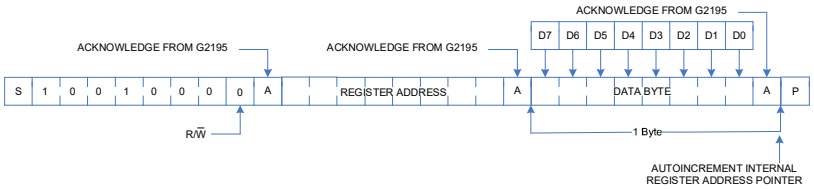


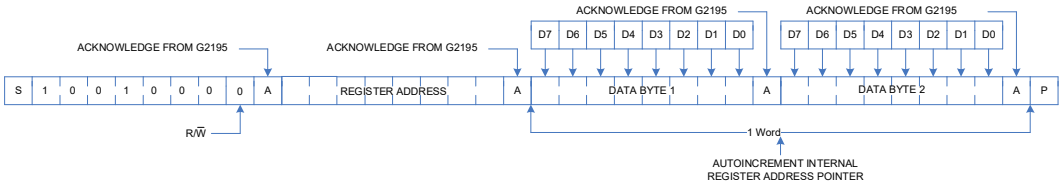
Figure 1. IC Serial-Interface Timing Diagram

I²C Protocol

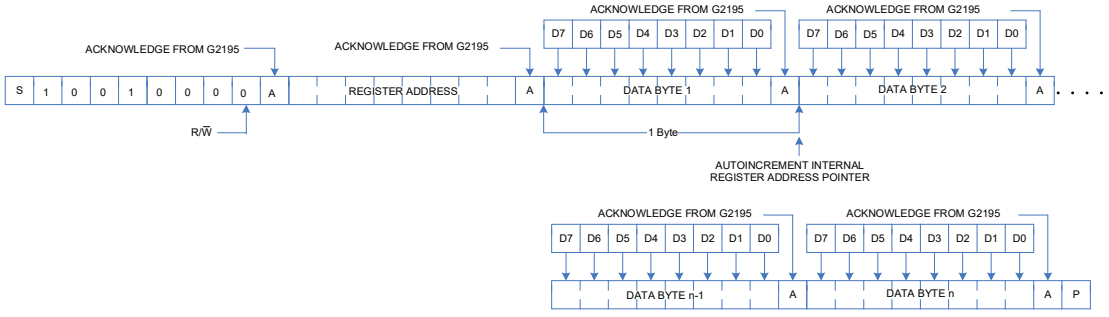
Write a Byte of Data to the G2195



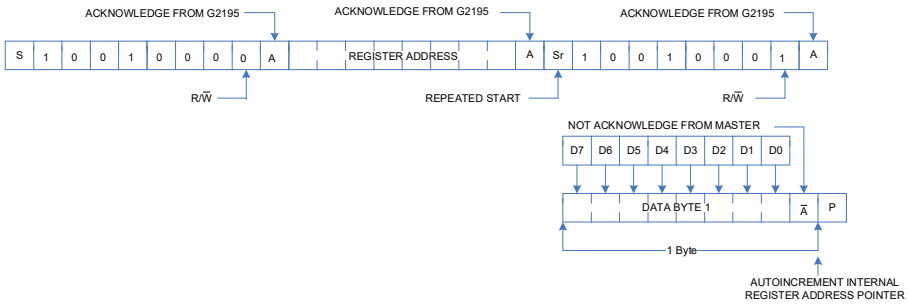
Write a Word of Data to the G2195



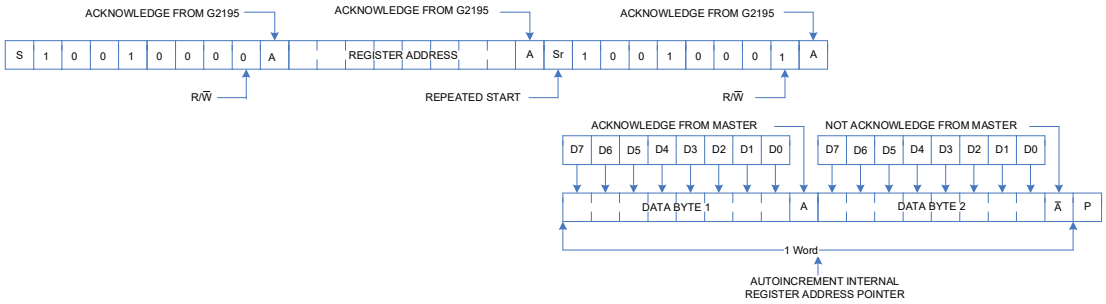
Write n Bytes of Data to the G2195



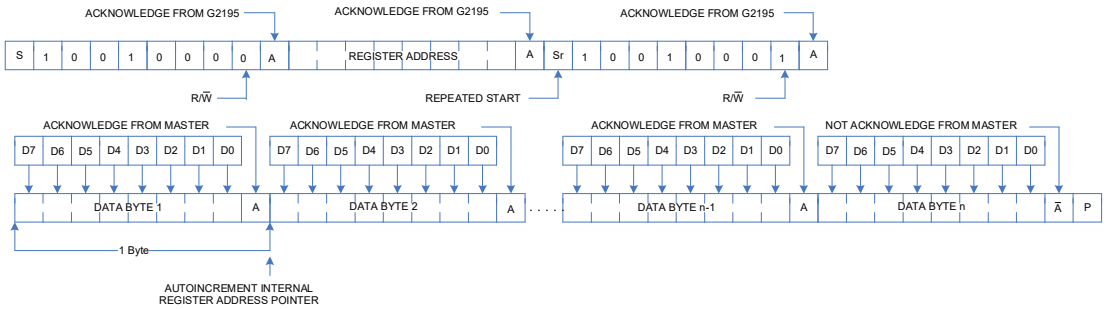
Read a Byte of Data to the G2195



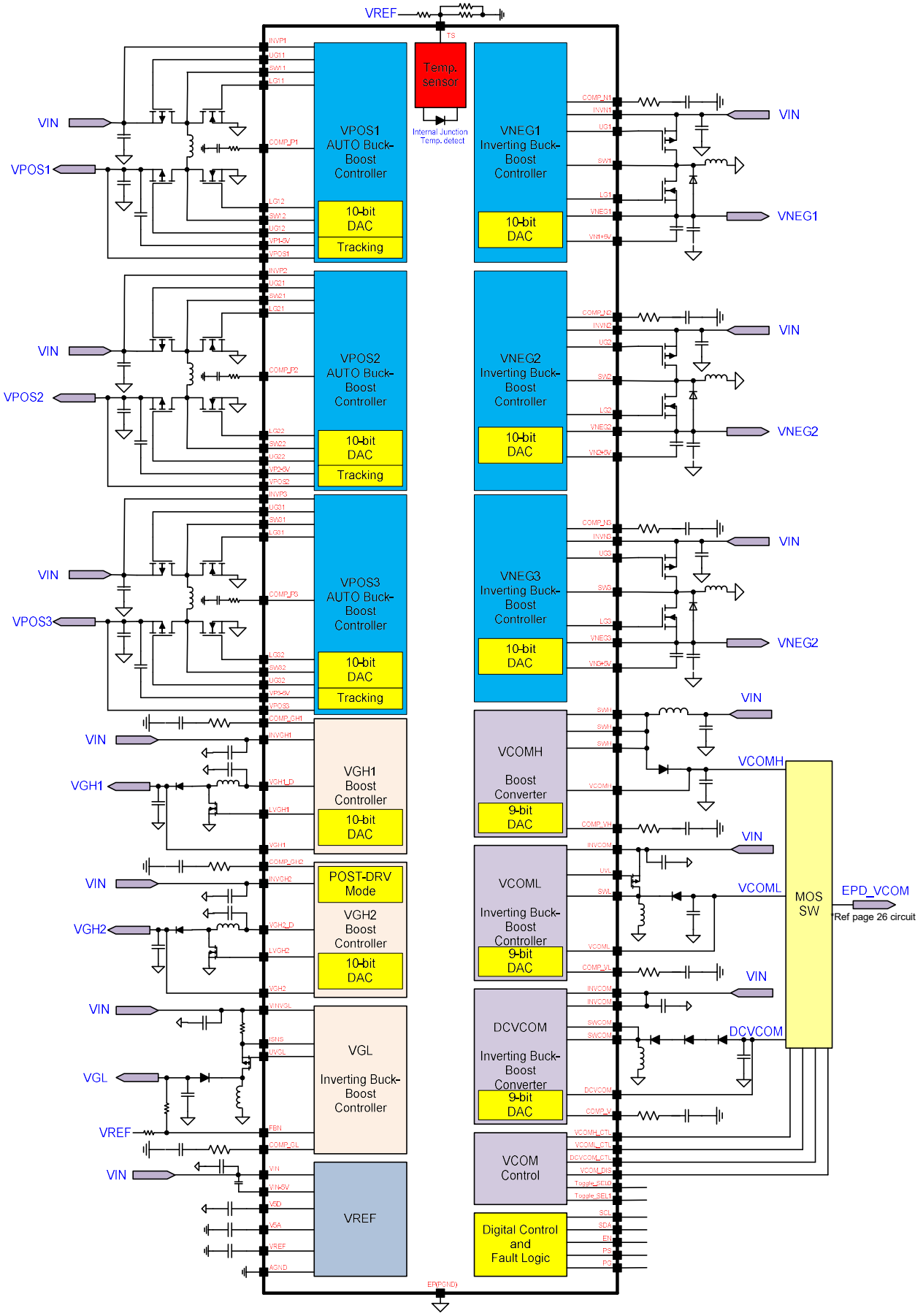
Read a Word of Data to the G2195



Read n Bytes of Data to the G2195



Typical Applications



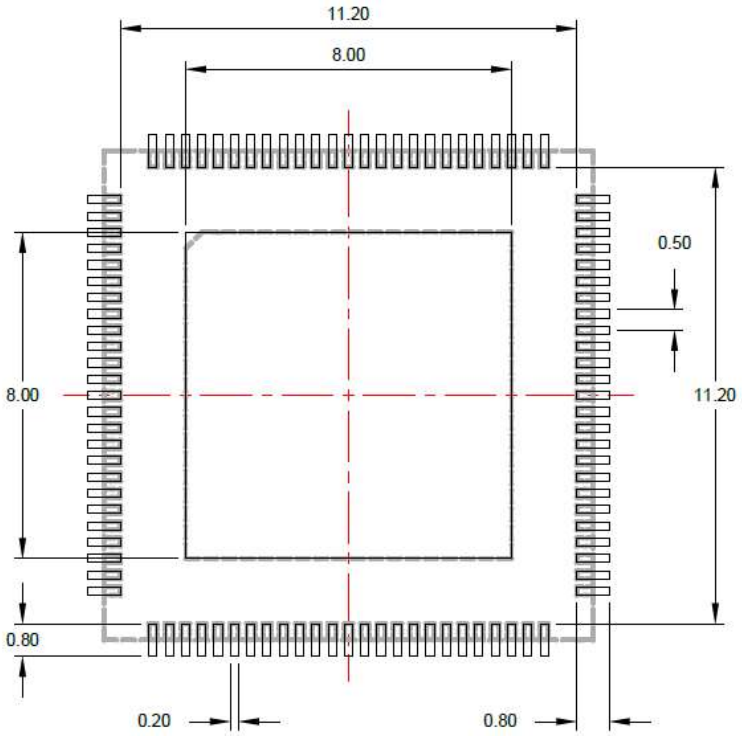
Pin Description

PIN	NAME	DESCRIPTION
1	SW1	The switching node
2	UG1	Output of the high-side gate driver
3	INVN1	Input Power Supply to VNEG1 rail
4	VPOS1	Positive supply output pin for panel source drivers. Discharge VPOS1 to Ground whenever the rail is disable.
5	VP1-5V	Bias to the high-side MOSFET gate driver.
6	UG12	Output of the high-side gate driver
7	SW12	The boost side switching node
8	LG12	Output of the low-side gate driver
9	LG11	Output of the low-side gate driver
10	SW11	The buck side switching node
11	UG11	Output of the high-side gate driver
12	INVP1	Input Power Supply to VPOS1 rail
13	COMP_P1	VPOS1 Compensation pin
14	COMP_GL	VGL Compensation pin
15	FBN	VGL Feedback pin
16	ISNS	VINVGL sense input. Connect to power stage input rail.
17	VINVGL	Input Power Supply to VGL rail
18	UVGL	Output of the high-side gate driver
19	PS	Pull this pin high to enter power save mode(IC shutdown)
20	COMP_GH1	VGH1 Compensation pin
21	VGH1	Positive supply output pin for panel gate drivers. Discharge VGH1 to Ground whenever the rail is disable.
22	INVGH1	Input Power Supply to VGH1 rail
23	VGH1_D	Base voltage output pin for VGH1
24	LVGH1	Output of the low-side gate driver
25	LVGH2	Output of the low-side gate driver
26	VGH2_D	Base voltage output pin for VGH2
27	INVGH2	Input Power Supply to VGH2 rail
28	VGH2	Positive supply output pin for panel gate drivers. Discharge VGH2 to Ground whenever the rail is disable.
29	COMP_GH2	VGH2 Compensation pin
30	COMP_VL	VCOML Compensation pin
31	VCOML	Negative supply output pin for VCOML
32	INVCOML	Input Power Supply to VCOML rail
33	UVL	Output of the high-side gate driver
34	SWL	VCOML Inductor switching node
35	Toggle_SEL1	VCOM AC+DC output control pin
36	SWH	VCOMH Inductor Switch Node
37	SWH	VCOMH Inductor Switch Node
38	SWH	VCOMH Inductor Switch Node
39	Toggle_SEL0	VCOM AC+DC output control pin/DCVCOM on/off control input@TOGGLE_VCOM[4]=0
40	COMP_VH	VCOMH Compensation pin
41	VCOMH	Positive supply output pin for VCOMH
42	COMP_V	DCVCOM Compensation pin
43	DCVCOM	Negative supply output pin for DCVCOM
44	INDCVCOM	Input Power Supply to DCVCOM rail
45	INDCVCOM	Input Power Supply to DCVCOM rail
46	SWCOM	DCVCOM Inductor Switch Node
47	SWCOM	DCVCOM Inductor Switch Node
48	VCOM_DIS	VCOM discharge control output pin
49	VCOML_CTL	ACVCOM control output pin
50	DCVCOM_CTL	ACVCOM control output pin

Pin Description (Continued)

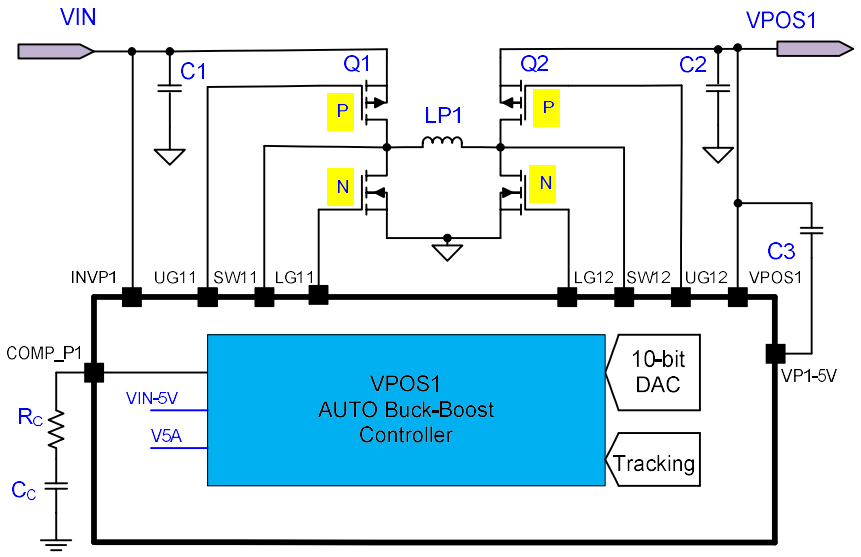
PIN	NAME	DESCRIPTION
51	VCOMH_CTL	ACVCOM control output pin
52	SDA	Serial interface(I^2C) data input/output
53	SCL	Serial interface(I^2C) clock input
54	EN	Pull this pin high to power up all output rails.
55	TS	Thermistor input pin.
56	PG	Open-drain power good output pin. Pin is pulled low when one or more rails are not in regulation.
57	VIN-5V	Bias to the high-side MOSFET gate driver.
58	VIN	Input power supply to general circuitry
59	V5D	5V filter pin for internal digital circuitry
60	V5A	5V filter pin for internal analog circuitry
61	AGND	Analog ground for general analog circuitry
62	VREF	Filter pin for 2.5V internal supply
63	COMP_P2	VPOS2 Compensation pin
64	INVP2	Input Power Supply to VPOS2 rail
65	UG21	Output of the high-side gate driver
66	SW21	The buck side switching node
67	LG21	Output of the low-side gate driver
68	LG22	Output of the low-side gate driver
69	SW22	The boost side switching node
70	UG22	Output of the high-side gate driver
71	VP2-5V	Bias to the high-side MOSFET gate driver.
72	VPOS2	Positive supply output pin for panel source drivers. Discharge VPOS2 to Ground whenever the rail is disable.
73	INVN2	Input Power Supply to VNEG2 rail
74	UG2	Output of the high-side gate driver
75	SW2	The switching node
76	LG2	Output of the low-side gate driver
77	VN2+5V	Bias to the low-side MOSFET gate driver.
78	VNEG2	Negative supply output pin for panel source drivers. Discharge VNEG2 to Ground whenever the rail is disable.
79	COMP_N2	VNEG2 Compensation pin
80	COMP_P3	VPOS3 Compensation pin
81	INVP3	Input Power Supply to VPOS3 rail
82	UG31	Output of the high-side gate driver
83	SW31	The buck side switching node
84	LG31	Output of the low-side gate driver
85	LG32	Output of the low-side gate driver
86	SW32	The boost side switching node
87	UG32	Output of the high-side gate driver
88	VP3-5V	Bias to the high-side MOSFET gate driver.
89	VPOS3	Positive supply output pin for panel source drivers. Discharge VPOS3 to Ground whenever the rail is disable.
90	COMP_N3	VNEG3 Compensation pin
91	INVN3	Input Power Supply to VNEG3 rail
92	UG3	Output of the high-side gate driver
93	SW3	The switching node
94	LG3	Output of the low-side gate driver
95	VN3+5V	Bias to the low-side MOSFET gate driver.
96	VNEG3	Negative supply output pin for panel source drivers. Discharge VNEG3 to Ground whenever the rail is disable.
97	COMP_N1	VNEG1 Compensation pin
98	VNEG1	Negative supply output pin for panel source drivers. Discharge VNEG1 to Ground whenever the rail is disable.
99	VN1+5V	Bias to the low-side MOSFET gate driver.
100	LG1	Output of the low-side gate driver
	EP(PGND)	Exposed Pad. Connect exposed pad to PGND(Power Ground of DC/DC Converter)

Minimum Footprint PCB Layout Section



Power Rails Topology

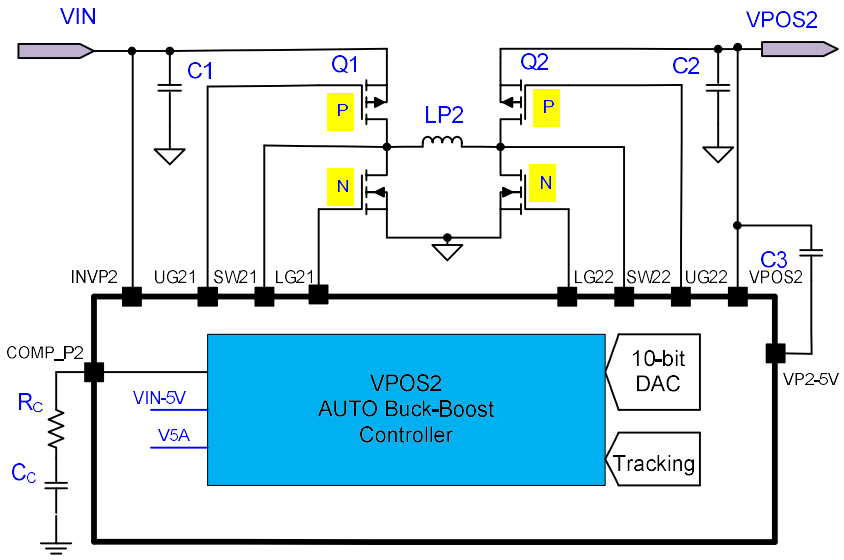
(1) VPOS1



Design Parameter	VPOS1=15V/1.6A, VIN=12V
C1	muRata, GRM31CR61E106K(10μF/25V/X5R, 1206)*1
C2	muRata, GRM31CR61E226KE15(22μF/25V/X5R, 1206)*3
C3	muRata, GRM31CR61E106K(10μF/25V/X5R, 1206)*1
LP1	ARLITECH, AMPI0630ED100MT(10μH/5.5A/68mΩ,6.6x7.1x3.0mm)
Q1	DIODES,DMC4040SSD(40V,P(45mΩ)+N(40mΩ))
Q2	DIODES,DMC4040SSD(40V,P(45mΩ)+N(40mΩ))
R_C*	130kΩ
C_C*	680pF

* The above design parameters are applicable to $T_A \geqq$-10°C. If working T_A <-10'C is required, it is strongly recommended to fine tune the compensation (R_C and C_C). Please contact GMT design service team for compensation adjustment for T_A <-10'C.

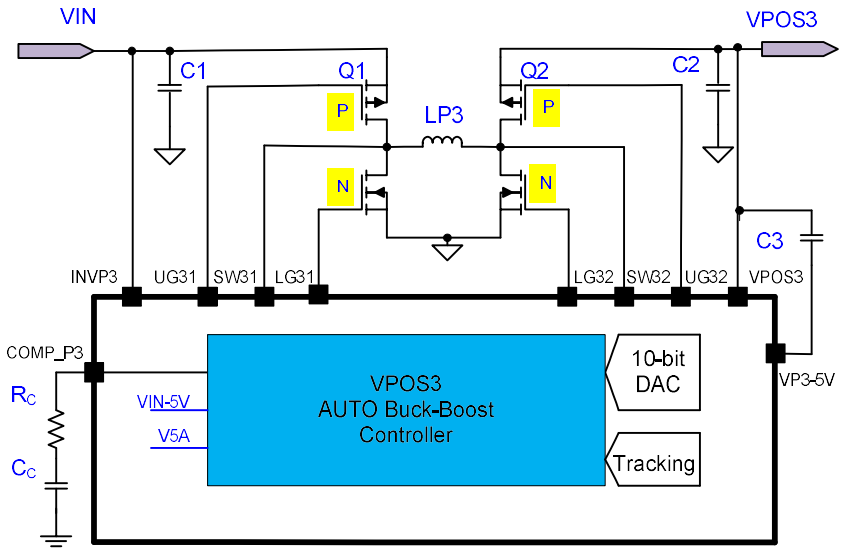
(2) VPOS2



Design Parameter	VPOS2=12V/1.6A, VIN=12V
C1	muRata, GRM31CR61E106K(10μF/25V/X5R, 1206)*1
C2	muRata, GRM31CR61E226KE15(22μF/25V/X5R, 1206)*3
C3	muRata, GRM31CR61E106K(10μF/25V/X5R, 1206)*1
LP2	ARLITECH, AMPI0630ED100MT(10μH/5.5A/68mΩ,6.6x7.1x3.0mm)
Q1	DIODES,DMC4040SSD(40V,P(45mΩ)+N(40mΩ))
Q2	DIODES,DMC4040SSD(40V,P(45mΩ)+N(40mΩ))
R_C^*	130kΩ
C_C^*	680pF

* The above design parameters are applicable to $T_A \geqq$-10°C. If working T_A <-10'C is required, it is strongly recommended to fine tune the compensation (R_C and C_C). Please contact GMT design service team for compensation adjustment for T_A <-10'C.

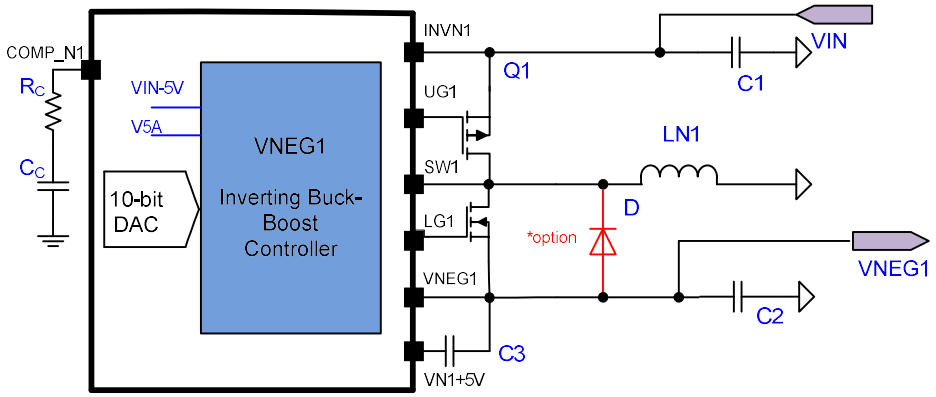
(3) VPOS3



Design Parameter	VPOS3=20V/1.6A, VIN=12V
C1	muRata, GRM31CR61E106K(10μF/25V/X5R, 1206)*1
C2	TDK, C3216X5R1V226M160AC(22μF/35V/X5R, 1206)*4
C3	muRata, GRM319R6YA106MA12(10μF/35V/X5R, 1206)*1
LP3	ARLITECH, AMPI1040ED150MT(15μH/7A/45mΩ,10x11.5x3.8mm)
Q1	DIODES,DMC4040SSD(40V,P(45mΩ)+N(40mΩ))
Q2	DIODES,DMC4040SSD(40V,P(45mΩ)+N(40mΩ))
R_C^*	130kΩ
C_C^*	680pF

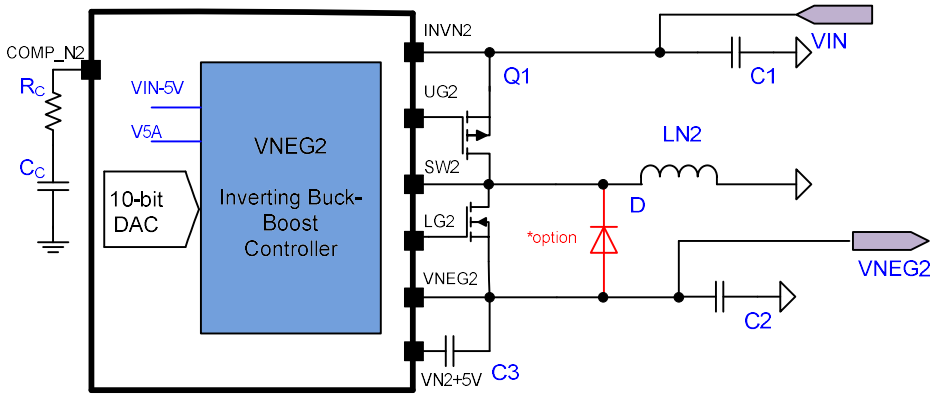
* The above design parameters are applicable to $T_A \geqq -10^{\circ}C$. If working T_A <-10'C is required, it is strongly recommended to fine tune the compensation (R_C and C_C). Please contact GMT design service team for compensation adjustment for T_A <-10'C.
*If the output is higher than 20V, the compensation parameters also need to be adjusted. Please contact GMT design service team for compensation adjustment.

(4) VNEG1



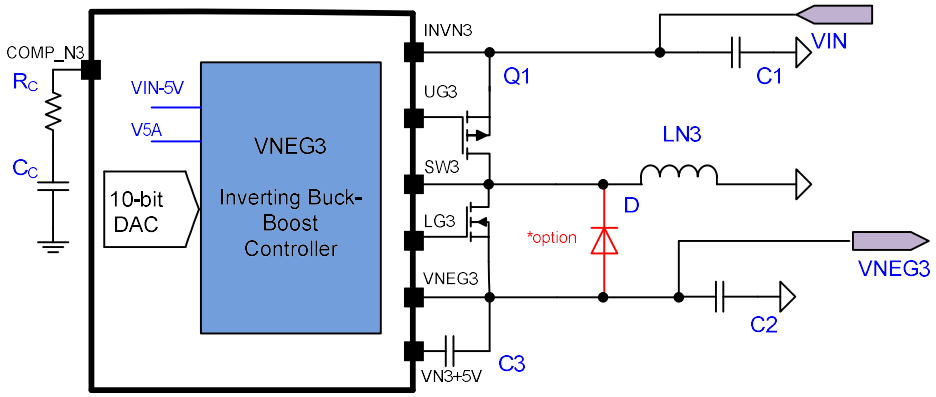
Design Parameter	VNEG1=-15V/1.6A, VIN=12V
C1	muRata, GRM31CR61E106K(10μF/25V/X5R, 1206)*1
C2	muRata, GRM31CR61E226KE15(22μF/25V/X5R, 1206)*4
C3	muRata, GRM188R6YA475KE15(4.7μF/35V/X5R, 0603)*1
LN1	ARLITECH, AMPI1040ED150MT(15μH/7A/45mΩ,10x11.5x3.8mm)
Q1	DIODES,DMC4040SSD(40V,P(45mΩ)+N(40mΩ))
D	DIODES,SBR3U60P1(3A/60V)
R_C	51kΩ
C_C	470pF

(5) VNEG2



Design Parameter	VNEG2=-12V/1.6A, VIN=12V
C1	muRata, GRM31CR61E106K(10μF/25V/X5R, 1206)*1
C2	muRata, GRM31CR61E226KE15(22μF/25V/X5R, 1206)*4
C3	muRata, GRM188R6YA475KE15(4.7μF/35V/X5R, 0603)*1
LN2	ARLITECH, AMPI1040ED150MT(15μH/7A/45mΩ,10x11.5x3.8mm)
Q1	DIODES,DMC4040SSD(40V,P(45mΩ)+N(40mΩ))
D	DIODES,SBR3U60P1(3A/60V)
R_C	51kΩ
C_C	470pF

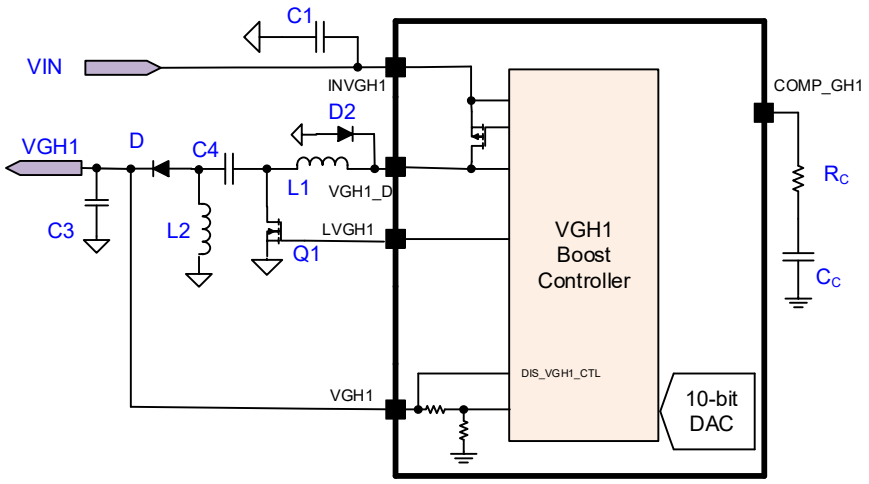
(6) VNEG3



Design Parameter	VNEG3=-20V/1.6A, VIN=12V
C1	muRata, GRM31CR61E106K(10μF/25V/X5R, 1206)*1
C2	TDK, C3216X5R1V226M160AC(22μF/35V/X5R, 1206)*5
C3	muRata, GRM188R6YA475KE15(4.7μF/35V/X5R, 0603)*1
LN3	ARLITECH, AMPI1040ED100MT(10μH/8.5A/30mΩ,10x11.5x3.8mm)
Q1	AOS, AO4611(60V, P(52mΩ)+N(30mΩ))
D	DIODES,SBR3U60P1(3A/60V)
R_C	51kΩ
C_C	470pF

*If the output is lower than -20V, the compensation parameters need to be adjusted. Please contact GMT design service team for compensation adjustment.

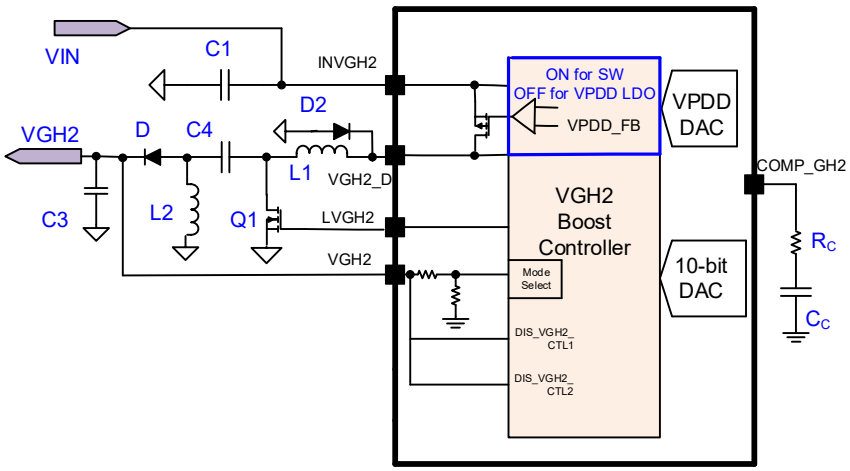
(7) VGH1



Design Parameter	VGH1=27V/200mA, VIN=12V
C1	muRata, GRM31CR61E106K(10μF/25V/X5R, 1206)*1
C3	muRata, GRT31CR61H106ME01(10UF/50V/X5R, 1206)*2
C4	0Ω
L1	ARLITECH, AMPI0603EL220MTA(22μH/3A/125mΩ,6.6x7.1x3.0mm)
L2	NC
D2*	Option, DIODES,SBR3U60P1(3A/60V)
D	DIODES,SBR3U60P1(3A/60V)
Q1	AOS, AON2260(60V, N(53mΩ))
R_C	200kΩ
C_C	470pF

*If the short-circuit limit test will be conducted, it is strongly recommended that D2 should be installed.

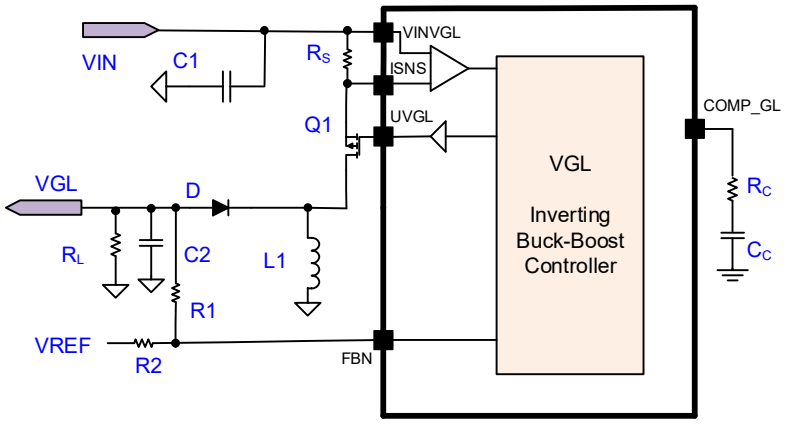
(8) VGH2



Design Parameter	VGH2=27V/200mA, VIN=12V
C1	muRata, GRM31CR61E106K(10μF/25V/X5R, 1206)*1
C3	muRata, GRT31CR61H106ME01(10μF/50V/X5R, 1206)*2
C4	0Ω
L1	ARLITECH, AMPI0603EL220MTA(22μH/3A/125mΩ,6.6x7.1x3.0mm)
L2	NC
D2*	Option, DIODES,SBR3U60P1(3A/60V)
D	DIODES,SBR3U60P1(3A/60V)
Q1	AOS, AON2260(60V, N(53mΩ))
R_C	200kΩ
C_C	470pF

* If the short-circuit limit test will be conducted, it is strongly recommended that D2 should be installed.

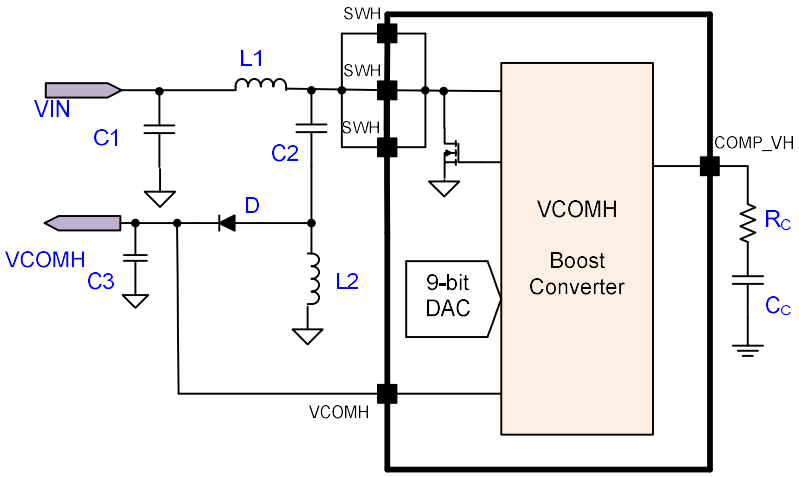
(9) VGL



Design Parameter	VGL=-20V/200mA, VIN=12V
C1	muRata, GRM31CR61E106K(10μF/25V/X5R, 1206)*1
C2	TDK, C3216X5R1V226M160AC(22μF/35V/X5R, 1206)*3
R_S	10mΩ
L1	ARLITECH, AMPI0603EL220MTA(22μH/3A/125mΩ,6.6x7.1x3.0mm)
D	DIODES, B170(1A/70V) or DIODES,SBR3U60P1(3A/60V)
Q1	DIODES, ZXMP7A17G(70V,P,250mΩ)
R1	82 kΩ
R2	10 kΩ
R_C	51kΩ
C_C	470pF
R_L	2KΩ

$$VGL = -\frac{R1}{R2} \times V_{REF}$$

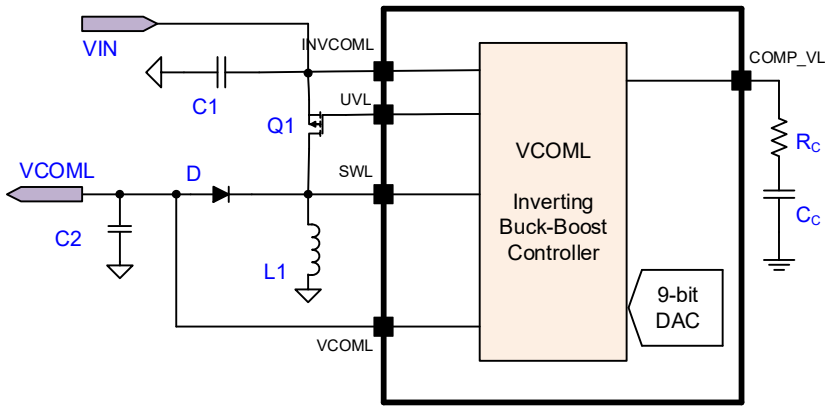
(10) VCOMH



Design Parameter	VCOMH=14V/2.5A, VIN=12V
C1	muRata, GRM31CR61E106K(10μF/25V/X5R, 1206)*1
C2	muRata, GRM31CR61E226KE15(22μF/25V/X5R, 1206)*1
C3	muRata, GRM31CR61E226KE15(22μF/25V/X5R, 1206)*2
L1	ARLITECH, AMPI1040ED100MT(10μH/8.5A/30mΩ,10x11.5x3.8mm)
L2	ARLITECH, AMPI1040ED100MT(10μH/8.5A/30mΩ,10x11.5x3.8mm)
D	DIODES,SBR3U60P1(3A/60V)
R_C*	110kΩ
C_C	680pF

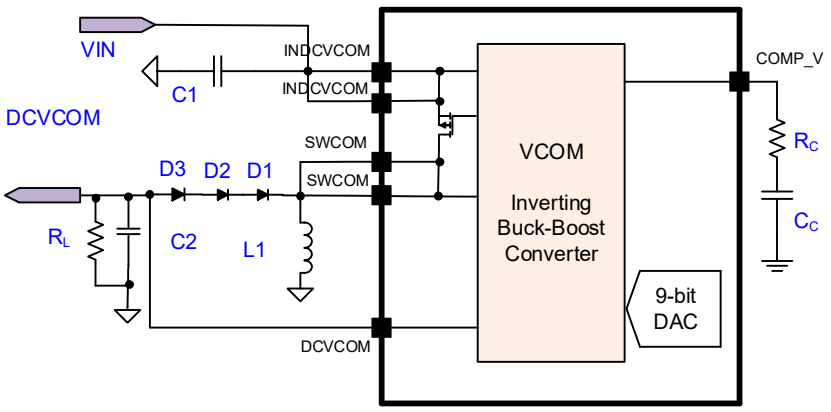
*If VCOMH is changed to Boost architecture instead of SEPIC, it is suggested to change R_C to 68K.

(11) VCOML



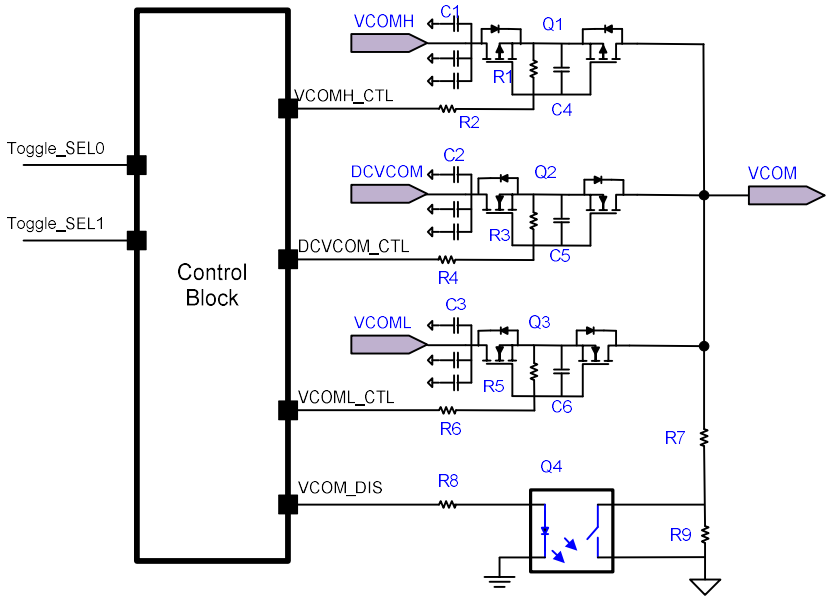
Design Parameter	VCOML=-14V/2.5A, VIN=12V
C1	muRata, GRM31CR61E106K(10μF/25V/X5R, 1206)*1
C2	TDK, C3216X5R1V226M160AC(22μF/35V/X5R, 1206)*3
L1	ARLITECH, AMPI1360ED100MT(10uH/12.5A/20.7mΩ,12.6x13.45x5.8mm)
Q1	AOS,AO4411(40V, P, 20mΩ)
D	DIODES,SBR3U60P1(3A/60V)
R_C	150kΩ
C_C	1.5nF

(12) DCVCOM



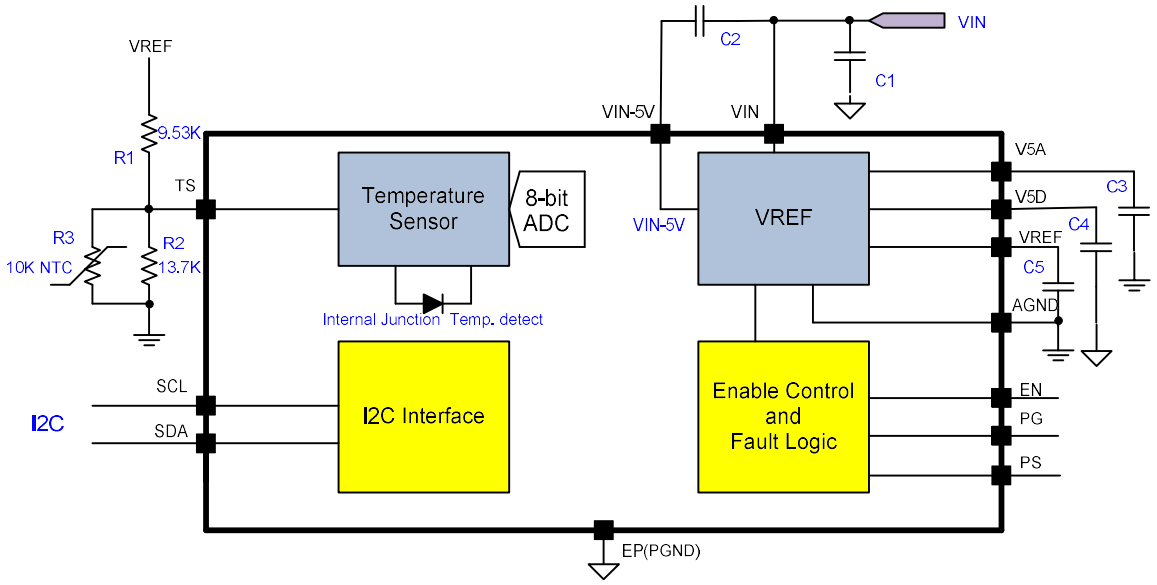
Design Parameter	DCVCOM=-1.5V/2.5A, VIN=12V
C1	muRata, GRM31CR61E106K(10μF/25V/X5R, 1206)*1
C2	muRata, GRM31CR61E226KE15(22μF/25V/X5R, 1206)*2
L1	ARLITECH, AMPI1040ED220MT(22μH/5.5A/66mΩ,10x11.5x3.8mm)
D1	0Ω
D2	0Ω
D3	DIODES,SBR3U60P1(3A/60V)
R_C	43kΩ
C_C	820pF
R_L	510Ω

(13) VCOM



Design Parameter	DCVCOM+ACVCOM
C1	TDK, C3216X5R1E336M160AC(33μF/25V/X5R, 1206)*3
C2	TDK, C3216X5R1E336M160AC(33μF/25V/X5R, 1206)*6
C3	TDK, C3216X5R1E336M160AC(33μF/25V/X5R, 1206)*3
C4	NC
C5	NC
C6	NC
Q1	DIODES,DMP4025LSD(Dual 40V P-MOS)
Q2	AOS, AO4882(Dual 40V N-MOS)
Q3	AOS, AO4882(Dual 40V N-MOS)
Q4	Panasonic, AQY210S(NC)
R1	2KΩ
R2	2KΩ
R3	10KΩ
R4	5.1KΩ
R5	3KΩ
R6	15KΩ
R7	510Ω
R8	330Ω(NC)
R9	0Ω

(14) Control & TS



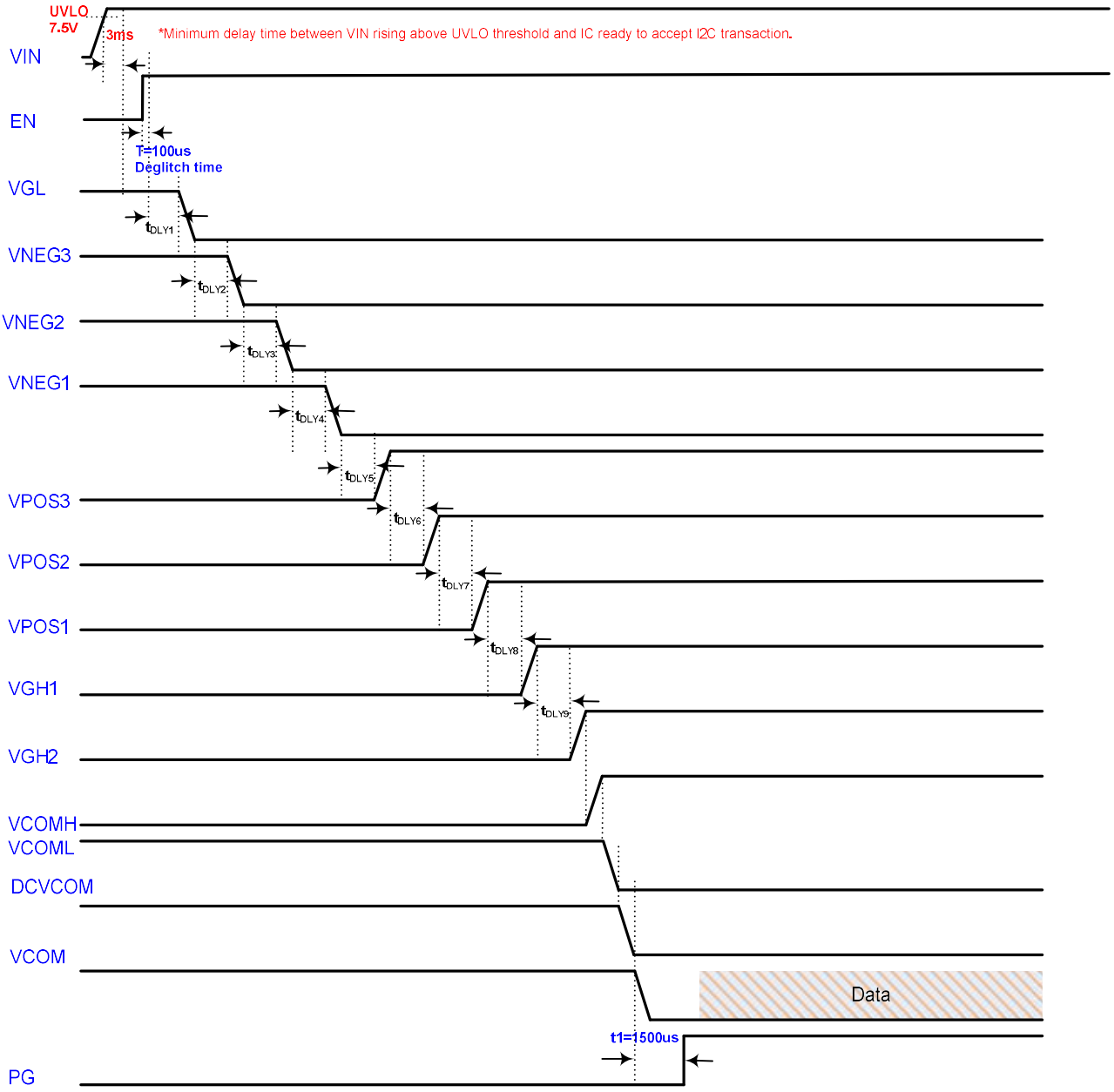
Design Parameter	VIN=12V
C1	muRata, GRM31CR61E106K(10μF/25V/X5R, 1206)*1
C2	muRata, GRM31CR61E106K(10μF/25V/X5R, 1206)*1
C3	muRata, GRM21BR61A106K (10μF/10V/X5R, 0805)*2
C4	muRata, GRM21BR61A106K (10μF/10V/X5R, 0805)*2
C5	muRata, GRM21BR61A106K (1μF/10V/X5R, 0805)*1
R1	9.53KΩ (1%)
R2	13.7KΩ (1%)
R3	muRata, NCP15XH103F03RC(NTC 10KΩ)

EN pin and 0x1Bh ON_OFF[7]

Hardware pin	ON_OFF[7]	Status
EN		
0	x	Standby Mode, Only I2C block enable
1	1	Normal Operation
1	0	Power Rails OFF (VPOSx,VNEGx,VGH1,VGH2,VGL,DCVCOM,VCOMH,VCOML);

Power-up and Power-down Sequence

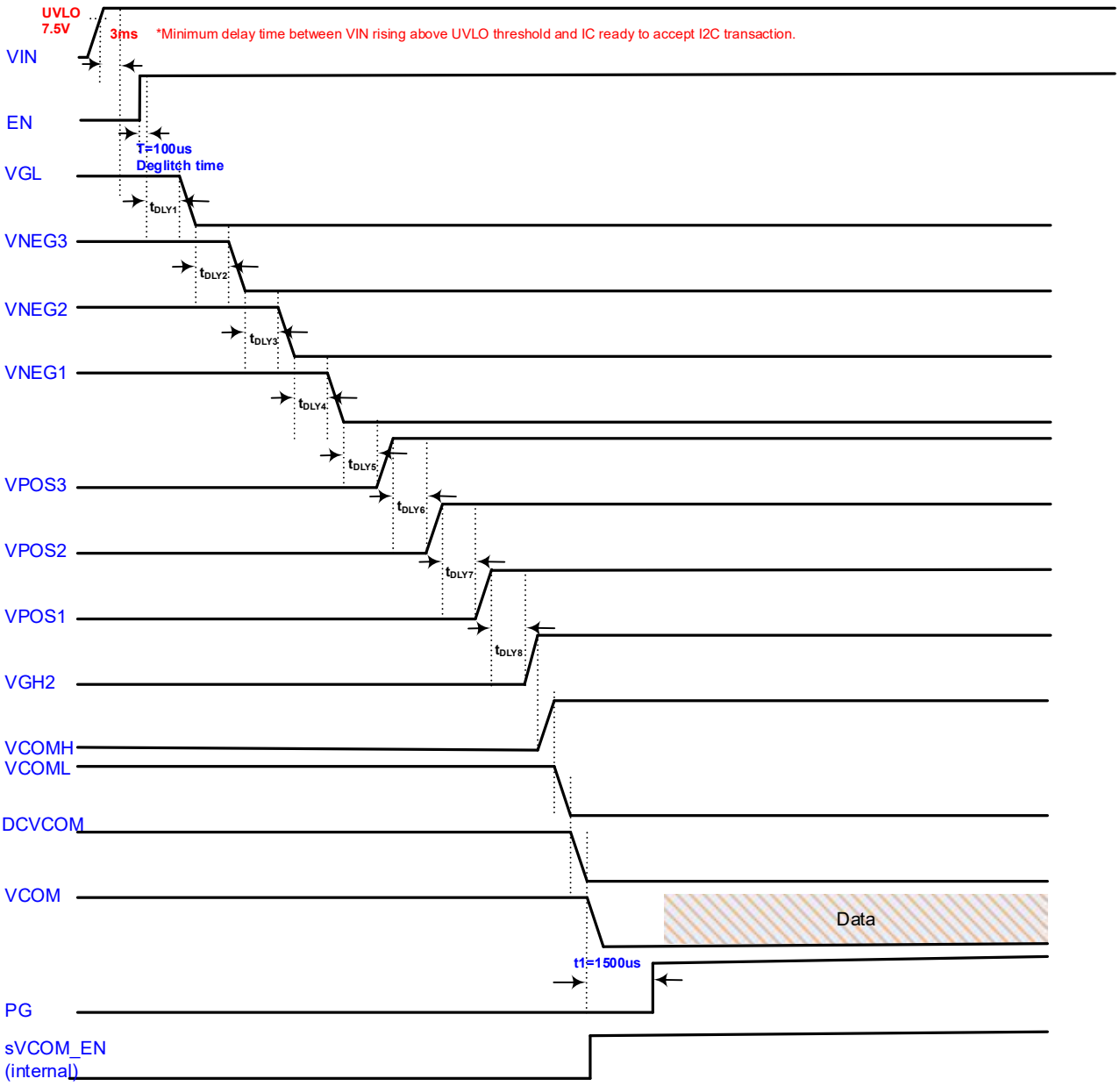
(A) Power-ON Sequence(7-Level Output, Normal, ACVCOM+DCVCOM)



1. t_{DLY1}~t_{DLY9} is programmable by register 0x13h,0x14h,0x15h(2-bit 0ms,1ms,**2ms**,4ms).
2. Soft-start time(VPOSx/VNEGx/VGHx/VGL/VCOMx) is setting by register 0x16h (**6ms**,8ms,10ms,12ms).
3. Discharge function only for VNEG3/2/1, VPOS3/2/1, VGH1/VGH2 & VCOM. VGL is no discharge function.
4. 3-Level or 7-Level output mode is setting by register 0x0Dh bit6 (3/7 LEVEL[6]).

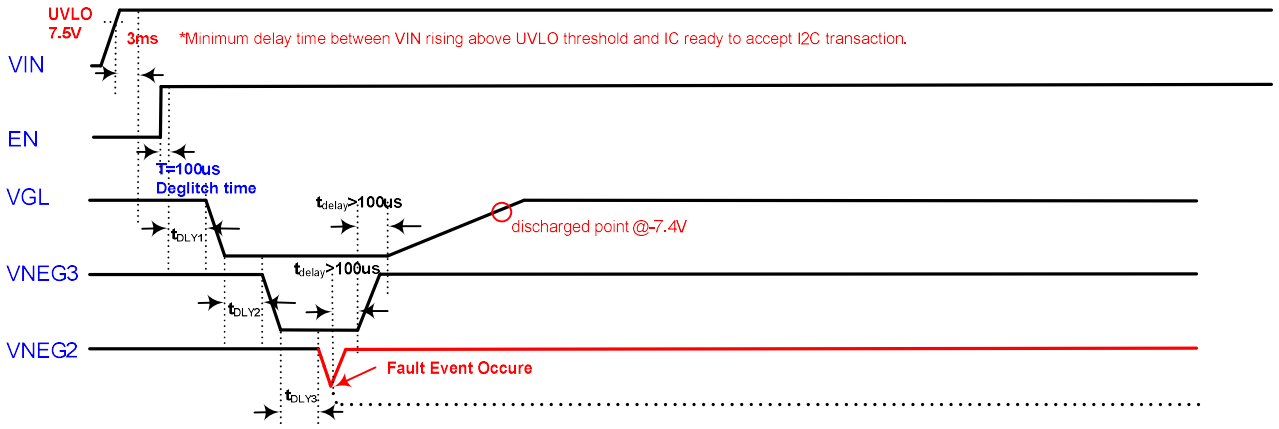
Item	Formula
t_{DLY1}(external)	t_{DLY1}[7:6] *1+SS[7:6]*0.2
t_{DLY2}(external)	t_{DLY2}[5:4] *1+SS[7:6]*0.2
t_{DLY3}(external)	t_{DLY3}[3:2] *1+SS[7:6]*0.2
t_{DLY4}(external)	t_{DLY4}[1:0] *1+SS[7:6]*0.2
t_{DLY5}(external)	t_{DLY5}[7:6] *1
t_{DLY6}(external)	t_{DLY6}[5:4] *1+SS[7:6]*0.2
t_{DLY7}(external)	t_{DLY7}[3:2] *1+SS[7:6]*0.2
t_{DLY8}(external)	t_{DLY8}[1:0] *1+SS[7:6]*0.2
t_{DLY9}(external)	t_{DLY9}[7:6] *1+SS[7:6]*0.2

(B) Power-ON Sequence(7-Level Output, Normal, Only VGH2/VGL output, ACVCOM + DCVCOM)

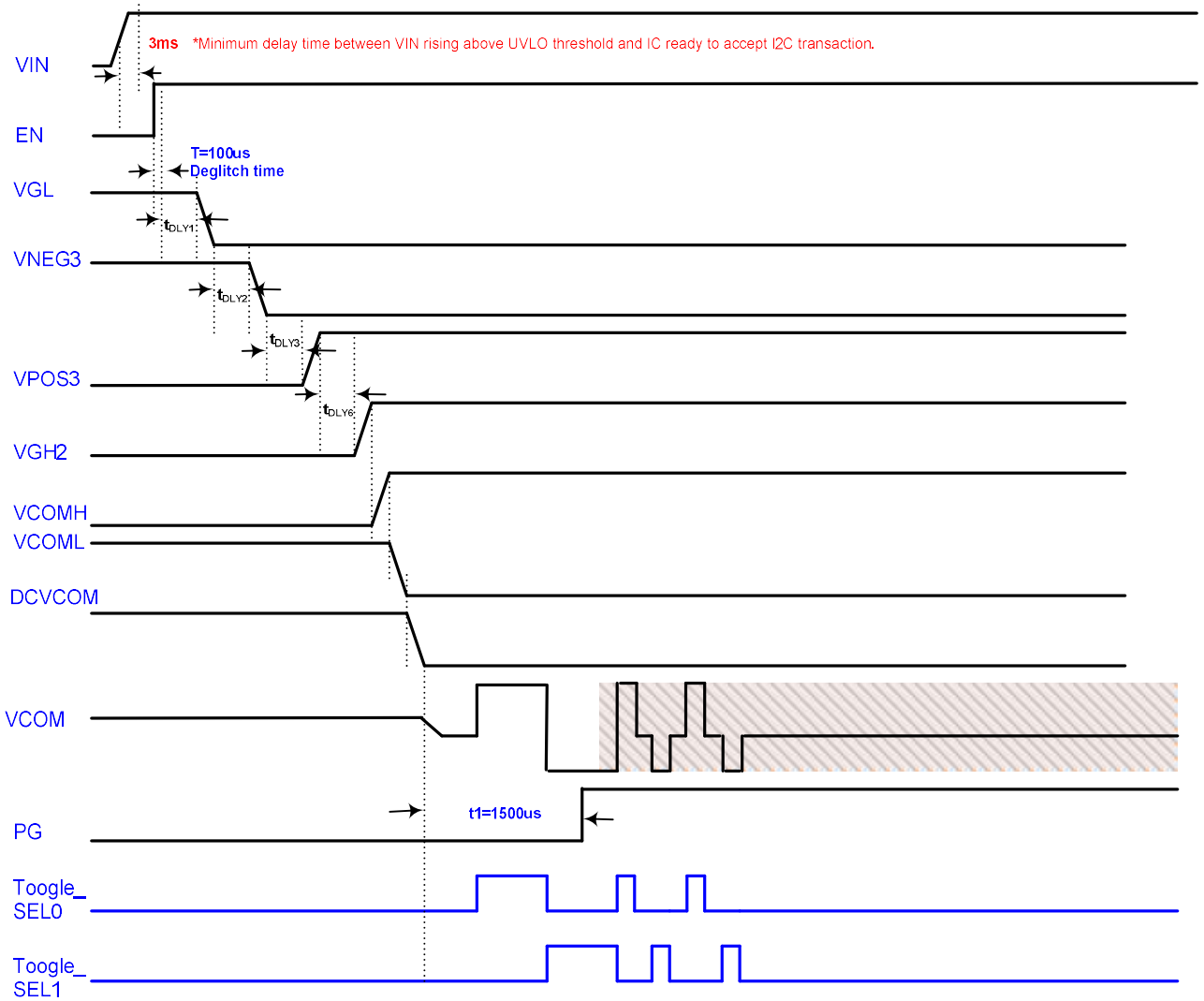


1. 3/7_LEVEL[6]=”0” & VGH_7_SEL[4]=”1” by register 0x16h, Gate driver supply are output VGH2/VGL.

(C) Power-ON Sequence with Fault Event(7-Level Output, Normal, FLT_VNEG2[1]=1)



(D) Power-ON Sequence(3-Level Output, Normal, ACVCOM+DCVCOM)



1.Register Setting

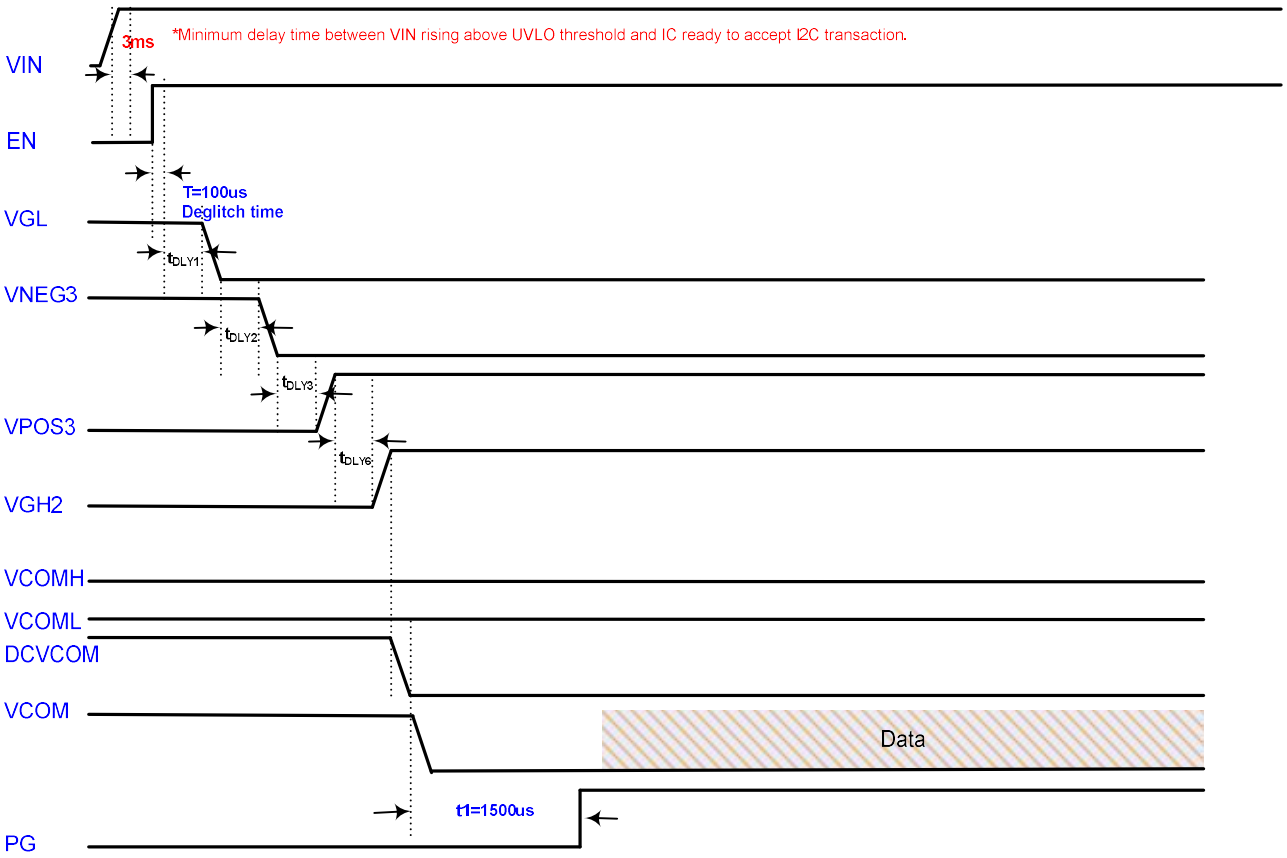
0x0DH	0x0DH	Function	Power Rail active	
3/7 LEVEL[6]	TOGGLE_VCOM[4]		Source Power	VCOM Power
0	0	7_LEVEL DCVCOM	VPOS1/VNEG1 VPOS2/VNEG2 VPOS3/VNEG3	DCVCOM:ON VCOMH:OFF VCOML:OFF
0	1	7_LEVEL ACVCOM+DCVCOM	VPOS1/VNEG1 VPOS2/VNEG2 VPOS3/VNEG3	DCVCOM:ON VCOMH:ON VCOML:ON
1	0	3_LEVEL DCVCOM	VPOS3/VNEG3	DCVCOM:ON VCOMH:OFF VCOML:OFF
1	**1**	**3_LEVEL ACVCOM+DCVCOM**	**VPOS3/VNEG3**	**DCVCOM:ON VCOMH:ON VCOML:ON**

2. Toggle VCOM output by hardware pin Toggle_SEL0 & Toggle_SEL1

sVCOM_EN	0x0DH	0x0DH	Toggle_SEL0	Toggle_SEL1	VCOMH_CTL	DCVCOM_CTL	VCOML_CTL	VCOM_DIS	VCOM Function	Note
	VCOM_DIS[5]	TOGGLE_VCOM[4]	(pin39)	(pin 35)	(pin 51)	(pin 50)	(pin 49)	(pin 48)		
0	0	x	x	x	OFF	OFF	OFF	ON	Discharge	G2195 disable
0	1	x	x	x	OFF	OFF	OFF	OFF	Disable	
1	0	0	0	x	OFF	ON	OFF	OFF	DCVCOM	DCVCOM
1	1	0	0	x	OFF	ON	OFF	OFF	DCVCOM	
1	0	0	1	x	OFF	OFF	OFF	ON	Discharge	
1	1	0	1	x	OFF	OFF	OFF	OFF	Disable	
1	0	1	0	0	OFF	ON	OFF	OFF	DCVCOM	ACVCOM
1	1	1	0	0	OFF	ON	OFF	OFF	DCVCOM	
1	0	1	0	1	OFF	OFF	ON	OFF	VCOML	
1	1	1	0	1	OFF	OFF	ON	OFF	VCOML	
1	0	1	1	0	ON	OFF	OFF	OFF	VCOMH	
1	1	1	1	0	ON	OFF	OFF	OFF	VCOMH	
1	0	1	1	1	OFF	OFF	OFF	ON	Discharge	
1	1	1	1	1	OFF	OFF	OFF	OFF	Disable	

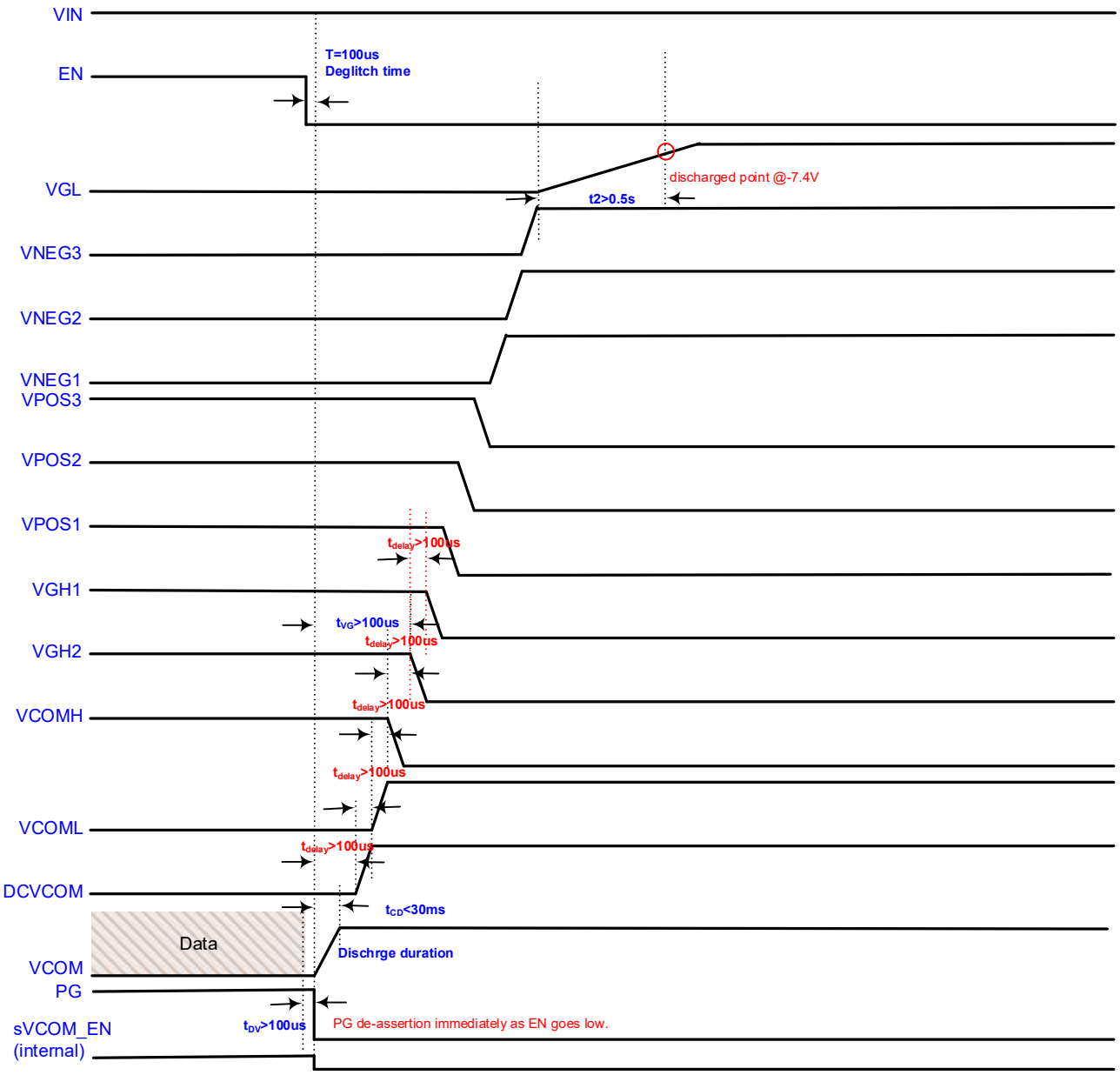
*sVCOM_EN is the internal VCOM enable signal. Please refer to page 29 and page 33 timing.

(E) Power-ON Sequence(3-Level Output, Normal, DCVCOM)



0x0DH	0x0DH	Function	Power Rail active	
3/7 LEVEL[6]	TOGGLE_VCOM[4]		Source Power	VCOM Power
0	0	7_LEVEL DCVCOM	VPOS1/VNEG1 VPOS2/VNEG2 VPOS3/VNEG3	DCVCOM:ON VCOMH:OFF VCOML:OFF
0	1	7_LEVEL ACVCOM+DCVCOM	VPOS1/VNEG1 VPOS2/VNEG2 VPOS3/VNEG3	DCVCOM:ON VCOMH:ON VCOML:ON
1	**0**	**3_LEVEL DCVCOM**	**VPOS3/VNEG3**	**DCVCOM:ON VCOMH:OFF VCOML:OFF**
1	1	3_LEVEL ACVCOM+DCVCOM	VPOS3/VNEG3	DCVCOM:ON VCOMH:ON VCOML:ON

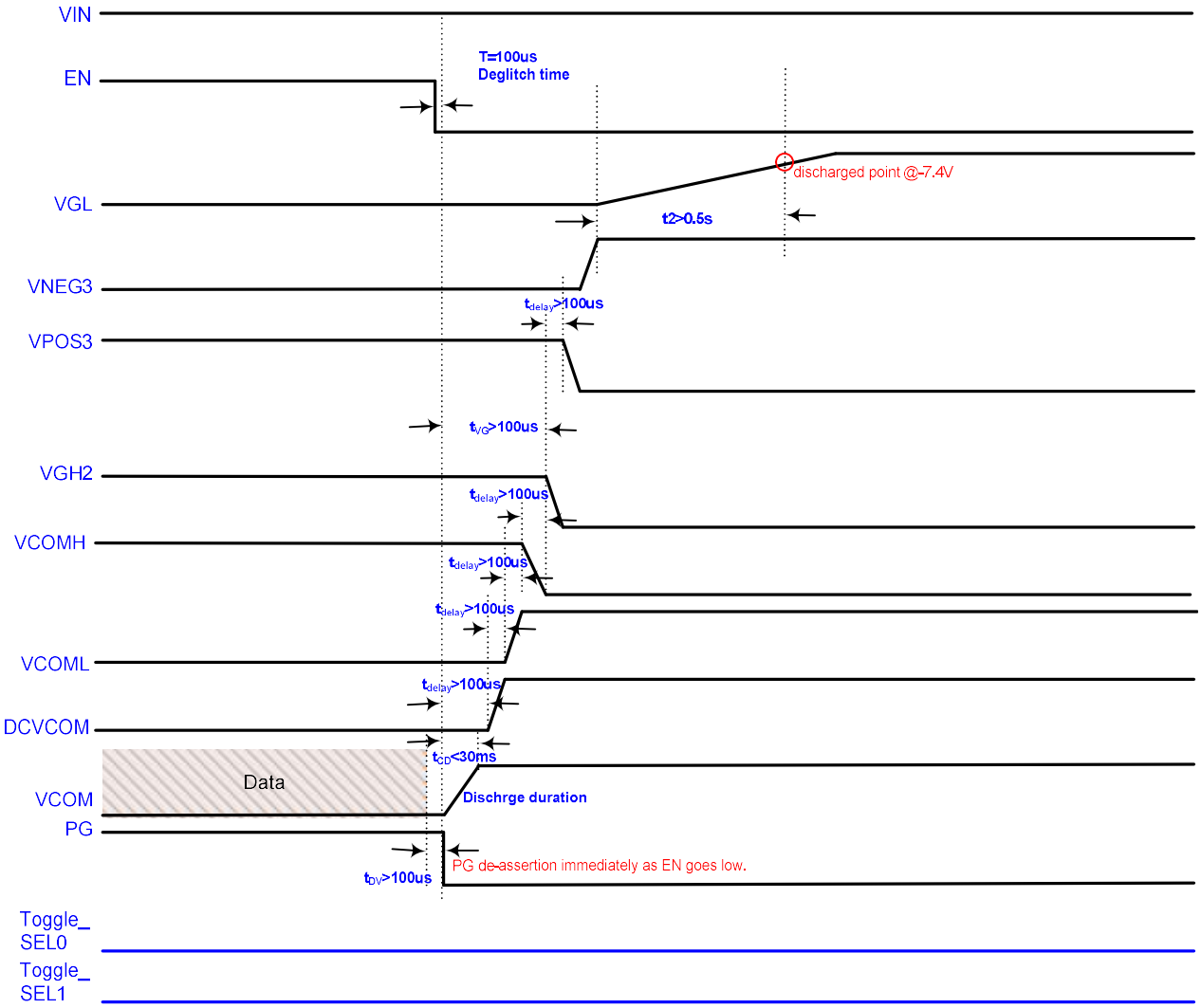
(F) Power-OFF Sequence (7-Level Output, Normal, ACVCOM+DCVCOM)



Normal Mode:

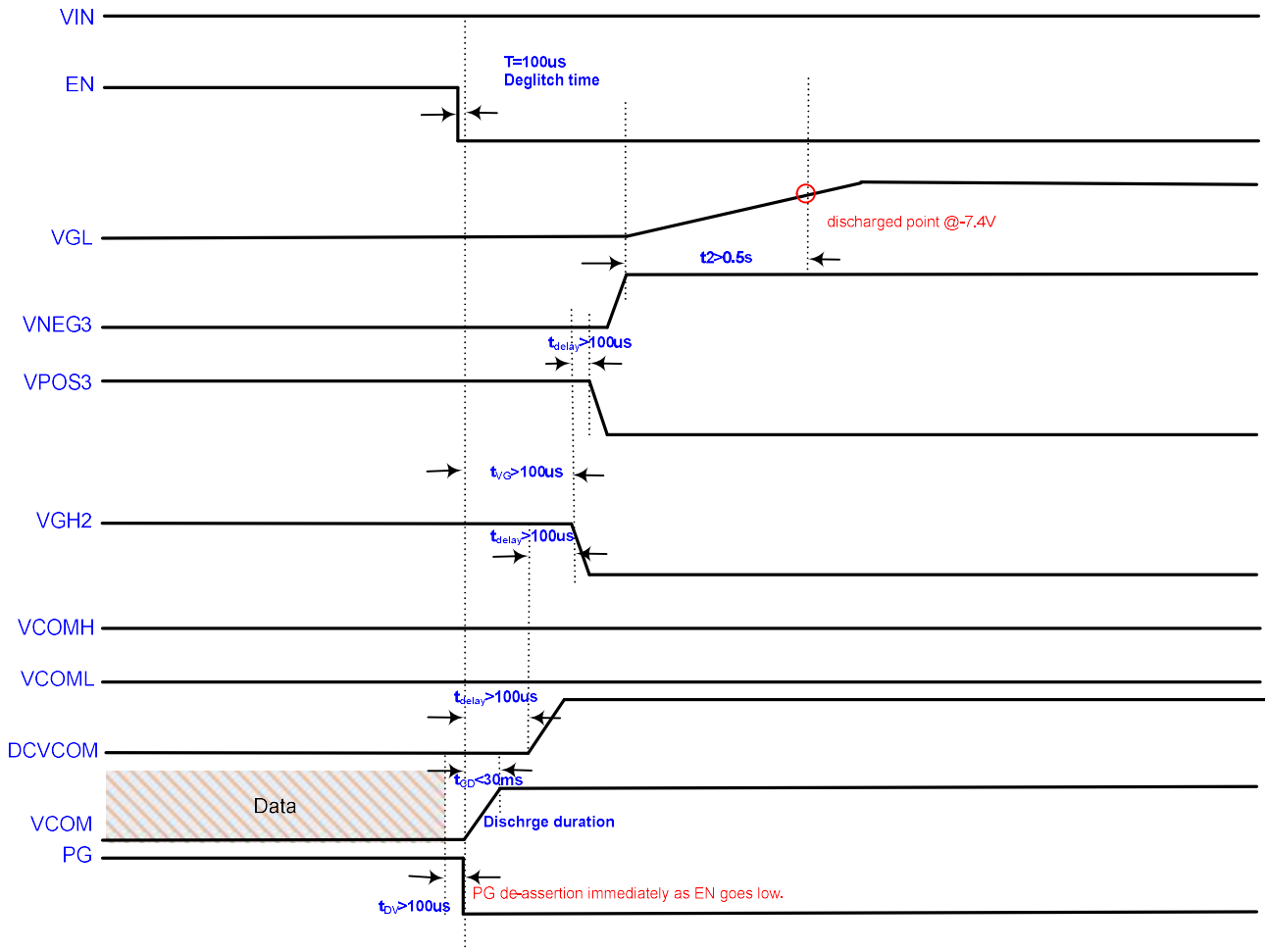
1. Supply voltage decay through pull-down resistors.
2. Normal mode off sequence is setting by 0x15h MODE[5] register.

(G) Power-OFF Sequence (3-Level Output Mode, Normal, AC-VCOM+DC-VCOM)



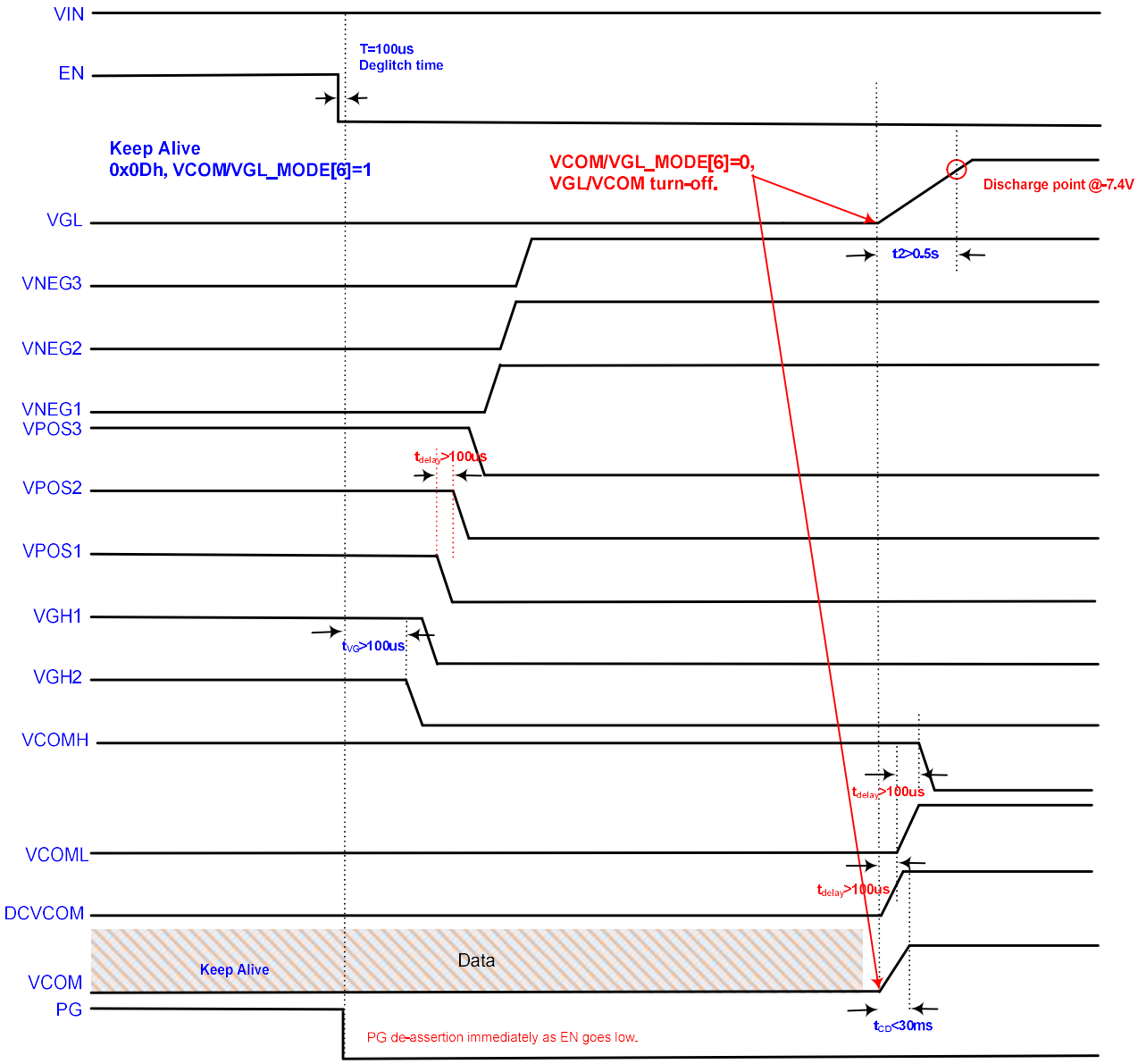
0x0DH	0x0DH	Function	Power Rail active	
3/7 LEVEL[6]	TOGGLE_VCOM[4]		Source Power	VCOM Power
0	0	7_LEVEL DCVCOM	VPOS1/VNEG1 VPOS2/VNEG2 VPOS3/VNEG3	DCVCOM:ON VCOMH:OFF VCOML:OFF
0	1	7_LEVEL ACVCOM+DCVCOM	VPOS1/VNEG1 VPOS2/VNEG2 VPOS3/VNEG3	DCVCOM:ON VCOMH:ON VCOML:ON
1	0	3_LEVEL DCVCOM	VPOS3/VNEG3	DCVCOM:ON VCOMH:OFF VCOML:OFF
1	**1**	**3_LEVEL ACVCOM+DCVCOM**	**VPOS3/VNEG3**	**DCVCOM:ON VCOMH:ON VCOML:ON**

(H) Power-OFF Sequence (3-Level Output Mode, Normal, DC-VCOM)



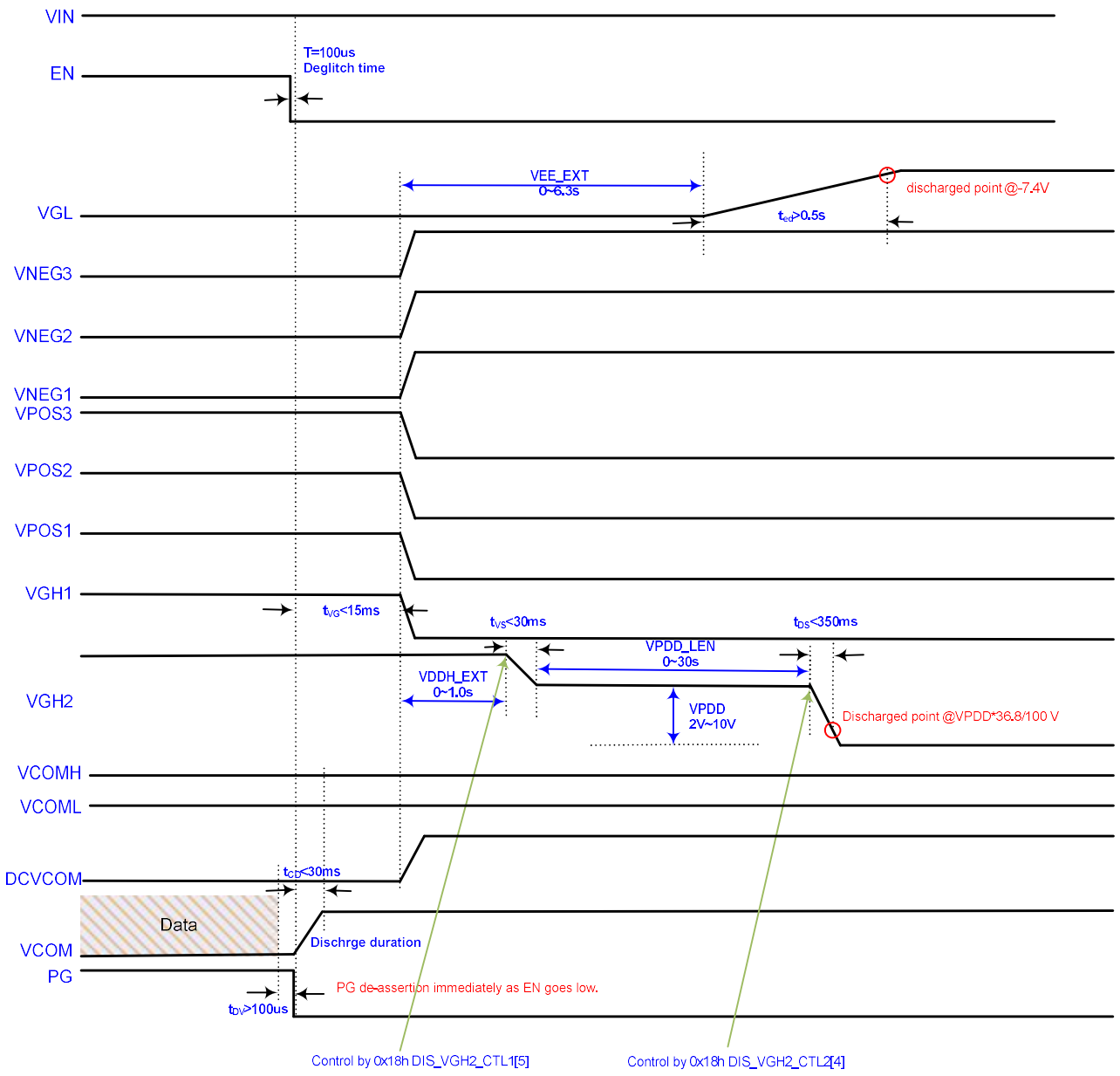
0x0DH	0x0DH	Function	Power Rail active	
3/7 LEVEL[6]	TOGGLE_VCOM[4]		Source Power	VCOM Power
0	0	7_LEVEL DCVCOM	VPOS1/VNEG1 VPOS2/VNEG2 VPOS3/VNEG3	DCVCOM:ON VCOMH:OFF VCOML:OFF
0	1	7_LEVEL ACVCOM+DCVCOM	VPOS1/VNEG1 VPOS2/VNEG2 VPOS3/VNEG3	DCVCOM:ON VCOMH:ON VCOML:ON
1	**0**	**3_LEVEL DCVCOM**	**VPOS3/VNEG3**	**DCVCOM:ON VCOMH:OFF VCOML:OFF**
1	1	3_LEVEL ACVCOM+DCVCOM	VPOS3/VNEG3	DCVCOM:ON VCOMH:ON VCOML:ON

(I) Power-OFF Sequence (7-Level Output Mode, ACVCOM+DCVCOM, VCOM/VGL Keep Alive)



1. For VCOM/VGL_MODE[7] =”1” set by I^2C (register 0x0Dh), VCOM and VGL continue power-on after EPD update.

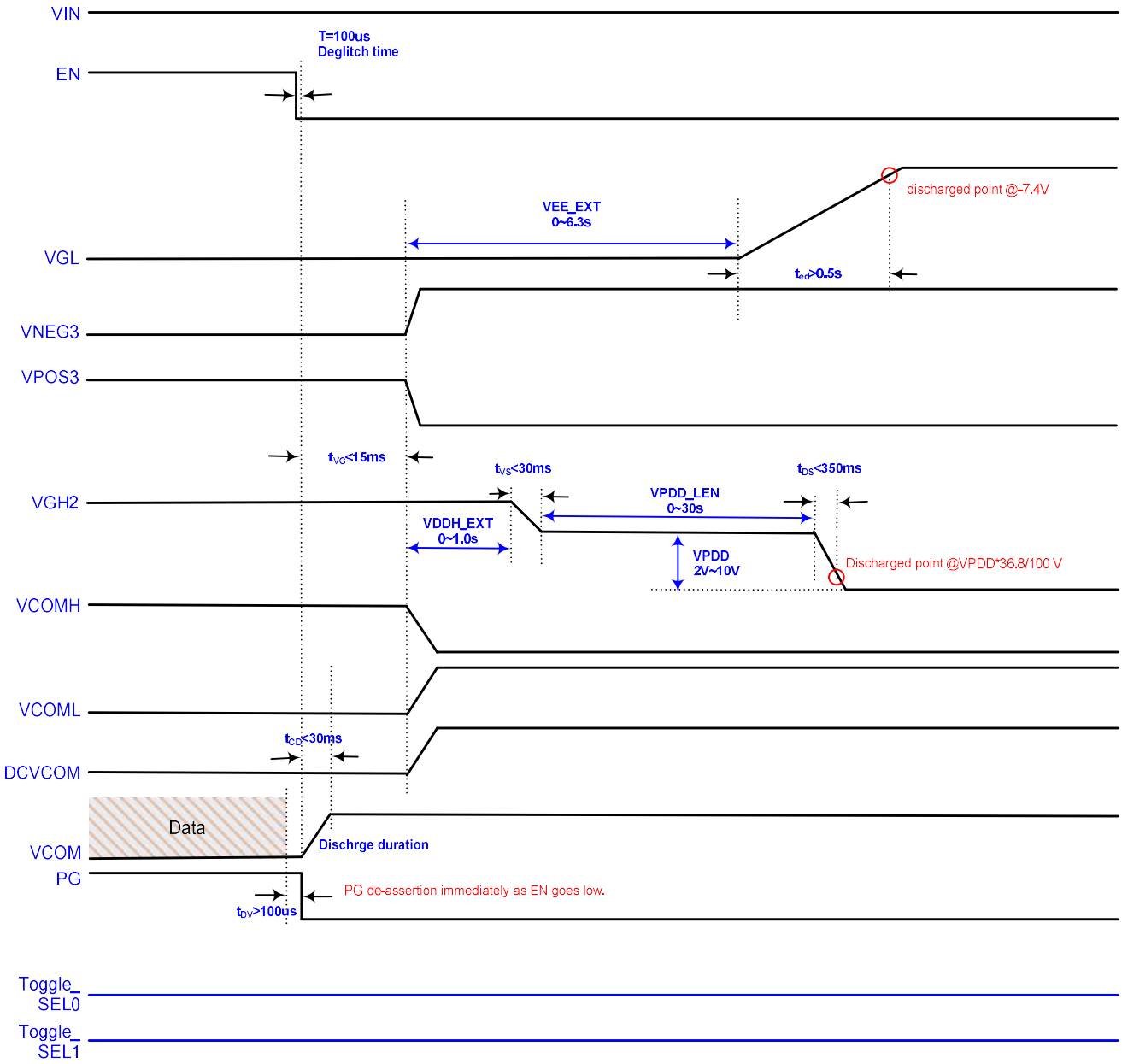
(J) Power-OFF Sequence (Post Drive Mode, 7-Level, DC-VCOM)



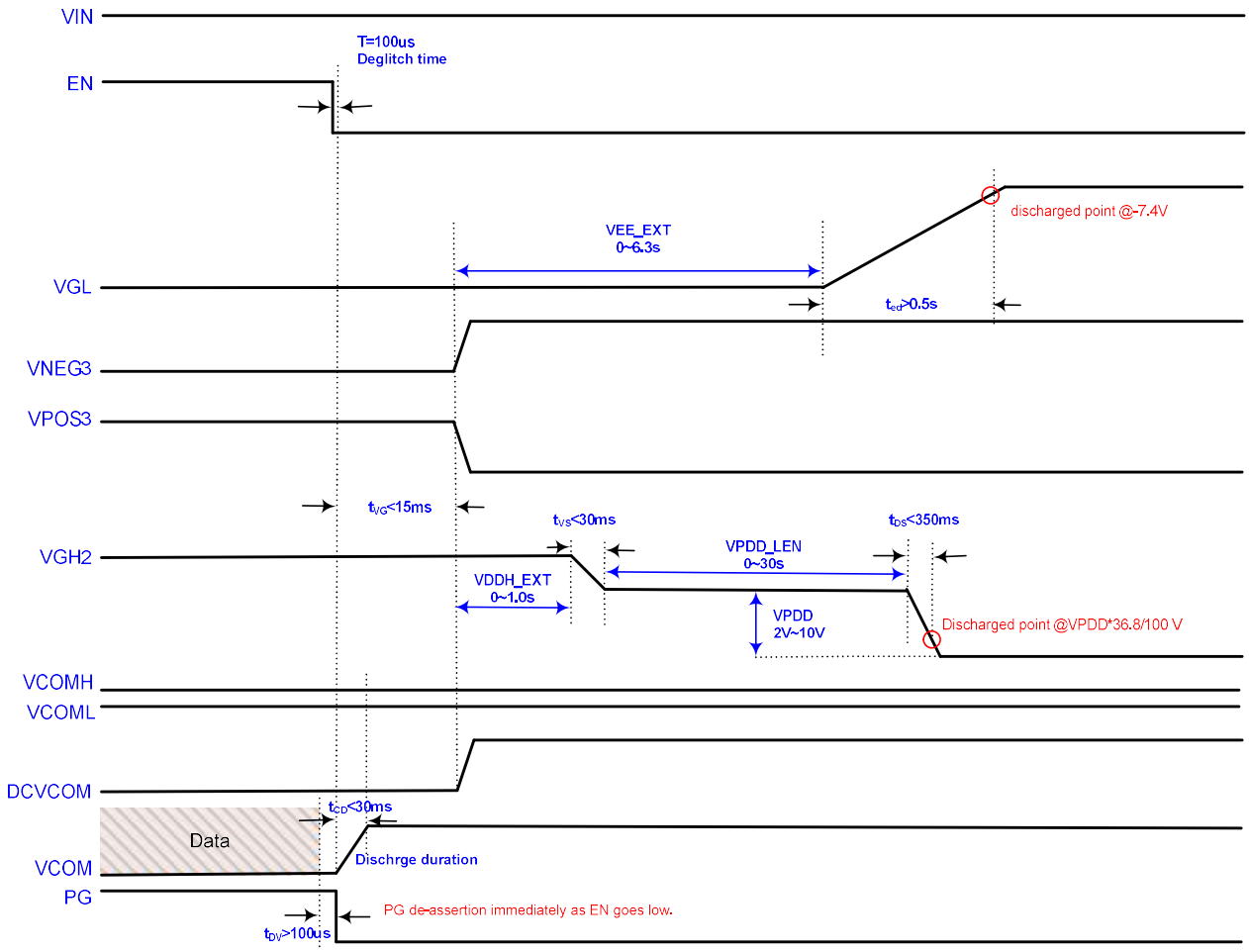
Post Drive Mode

1. Only VGH2 has post drive mode (Lightness Mode).
2. The gate high voltage (VGH2) can be extended beyond that required for the normal active update. The extension time is given by VDDH_EXT. VDDH_EXT starts after t_{VG} time where t_{VG} must be less than 15ms.
3. In addition, VGH2 is pulled to VPDD in less than 30ms(t_{VS}) when the PMIC powers down the standard VGH2 voltage. VPDD will be powered on for the time duration of VPDD_LEN. In addition, VGH2 powers down with RC decay of t_{DS} (<350ms).
4. The low gate voltage (VGL) can be extended beyond that which is required for the normal active update. The extension time is given by VEE_EXT.
5. VCOM will quickly be pulled to ground through a low resistance path (<30ms) after the active drive. A low resistance path of less than 1kΩ is desirable.

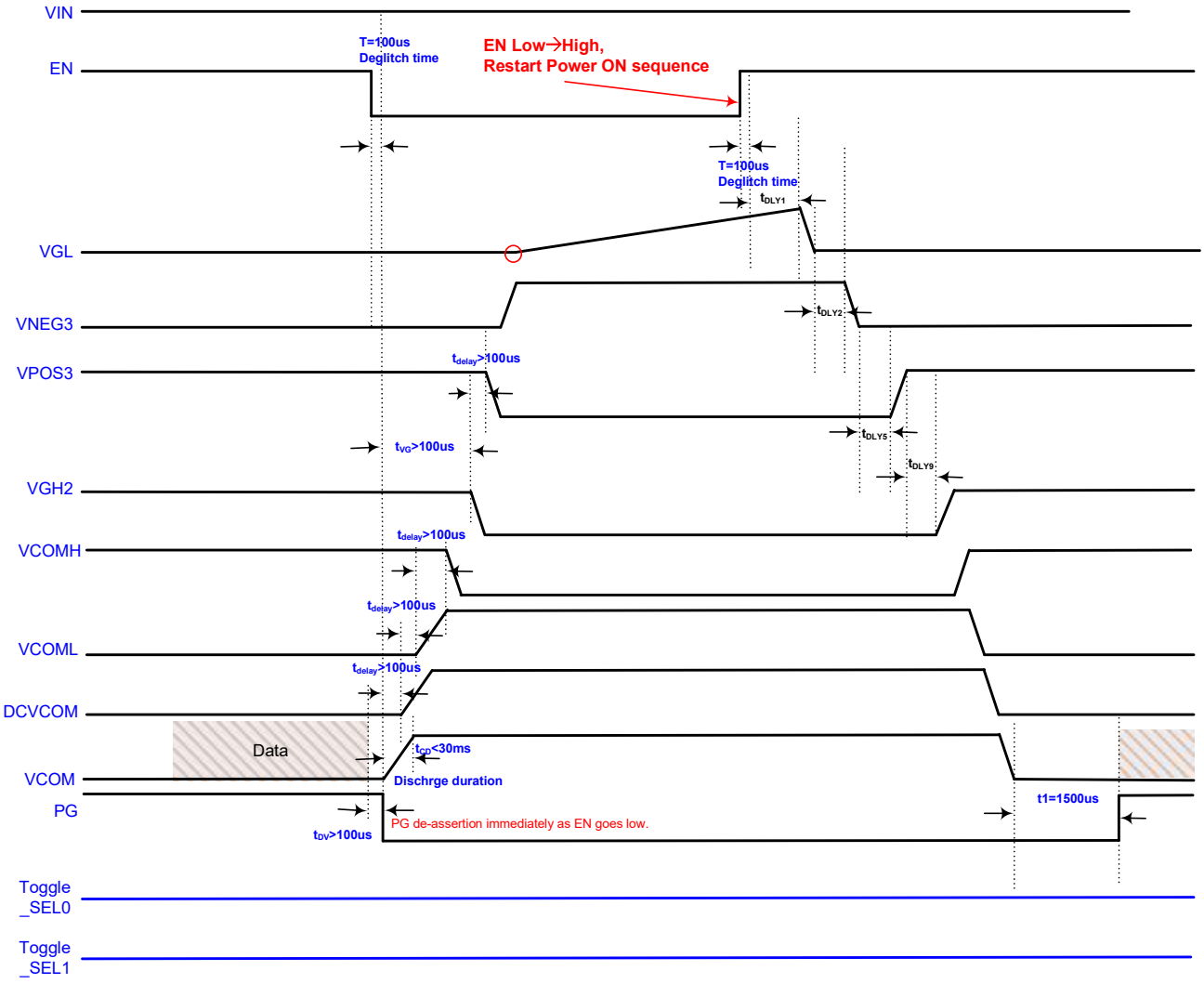
(K) Power-OFF Sequence (Post Drive Mode, 3-Level, AC-VCOM+DC-VCOM)



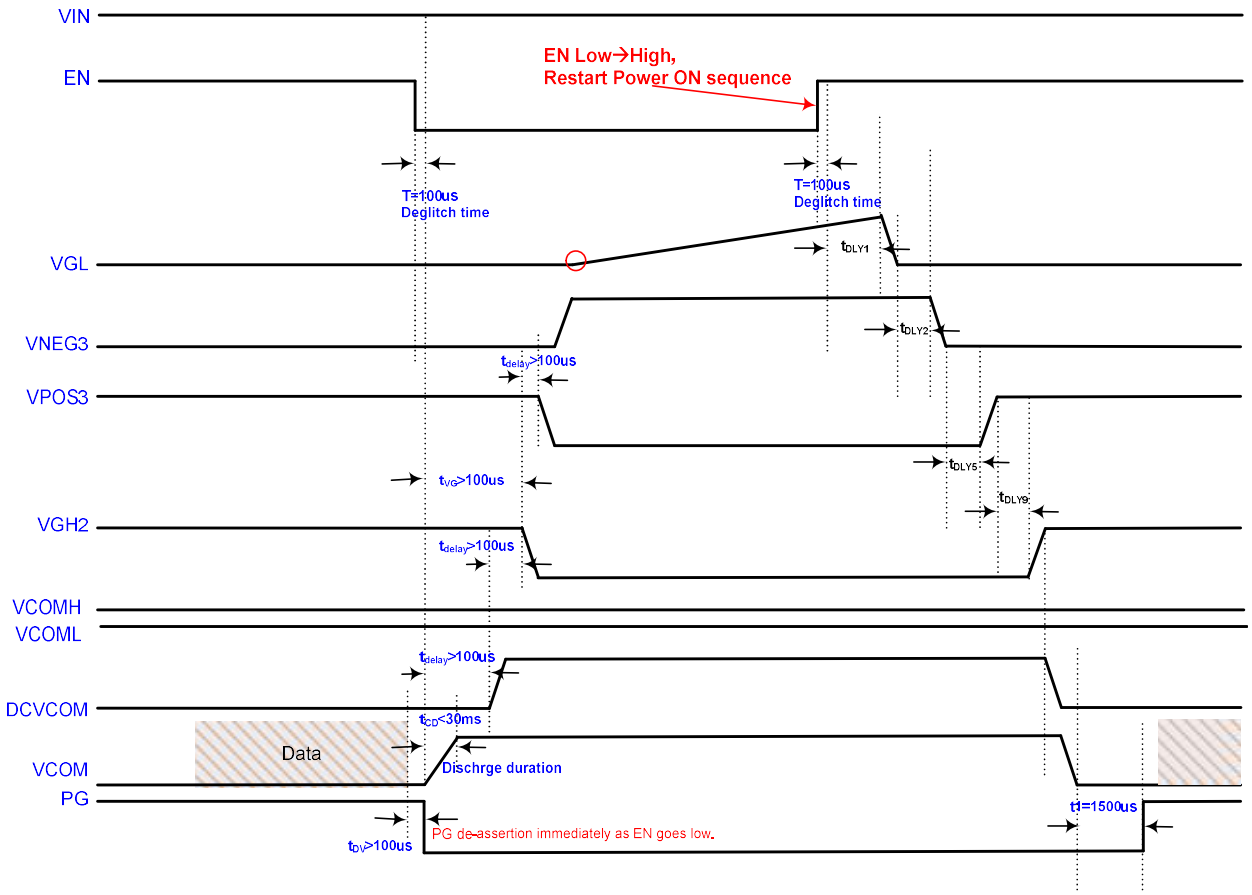
(L) Power-OFF Sequence (Post Drive Mode, 3-Level, DC-VCOM)



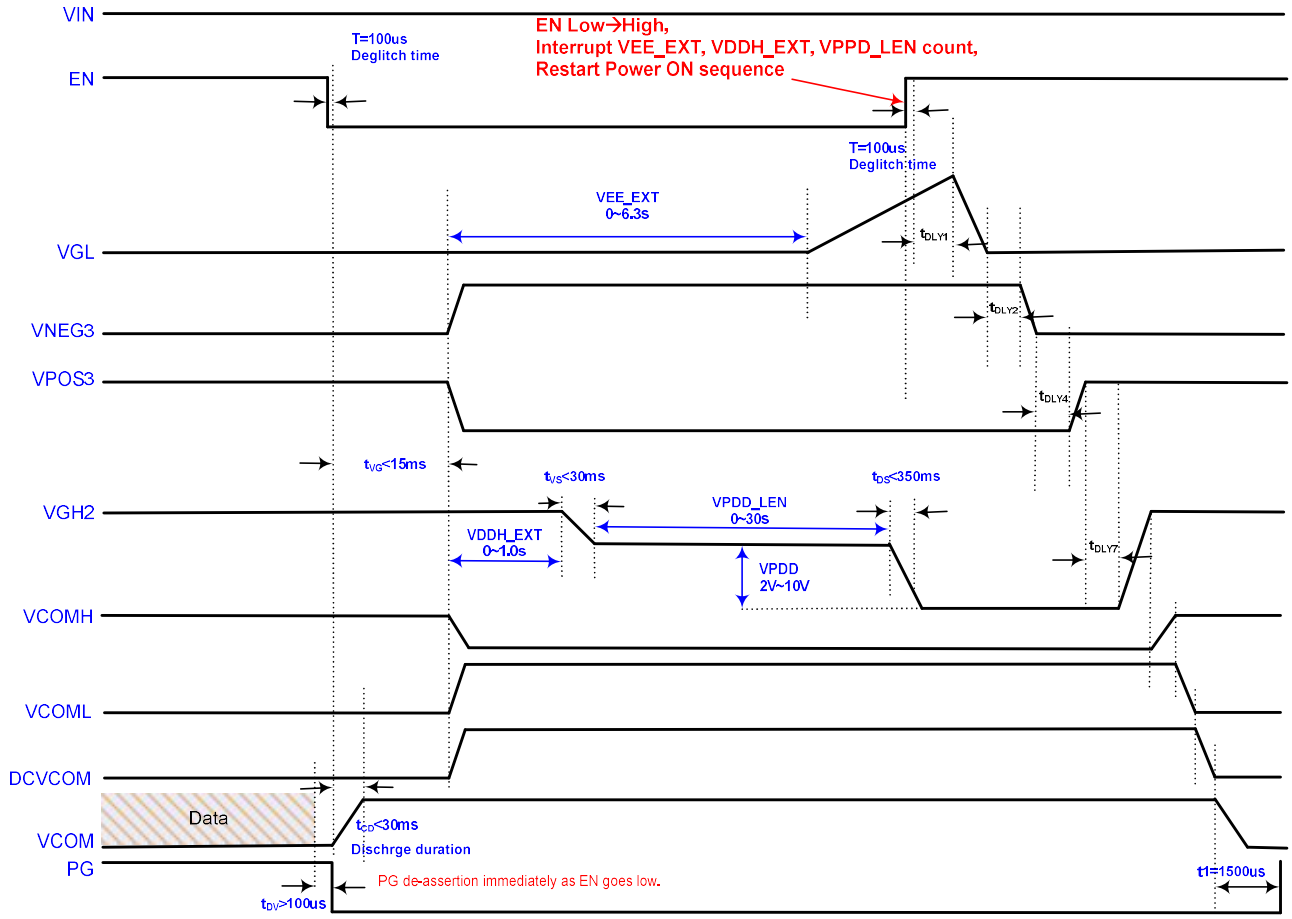
(M) Power-OFF to ON Sequence (3-Level Output, Normal, AC-VCOM+DC-VCOM)



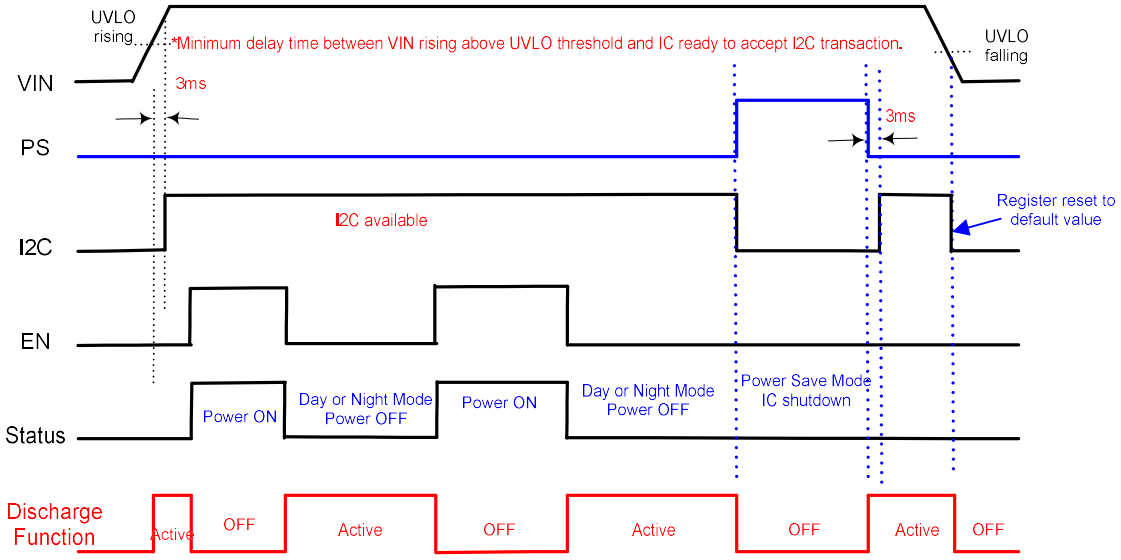
(N) Power-OFF to ON Sequence (3-Level Output, Normal, DC-VCOM)



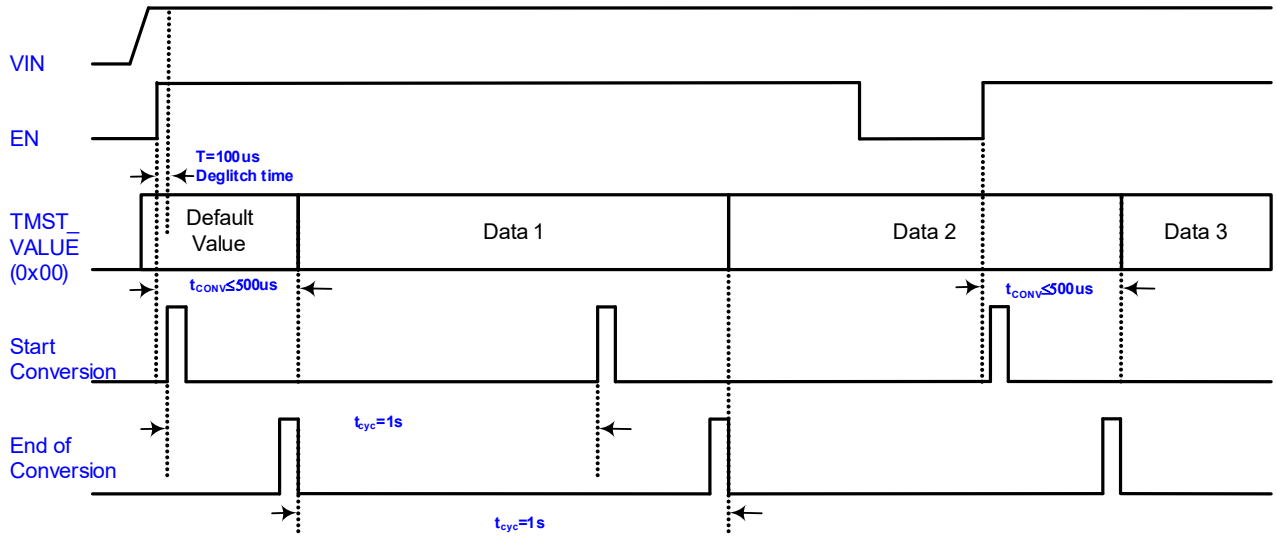
(O) Power-OFF to ON Sequence (Post Drive Mode, 3-Level, AC-VCOM+DC-VCOM)



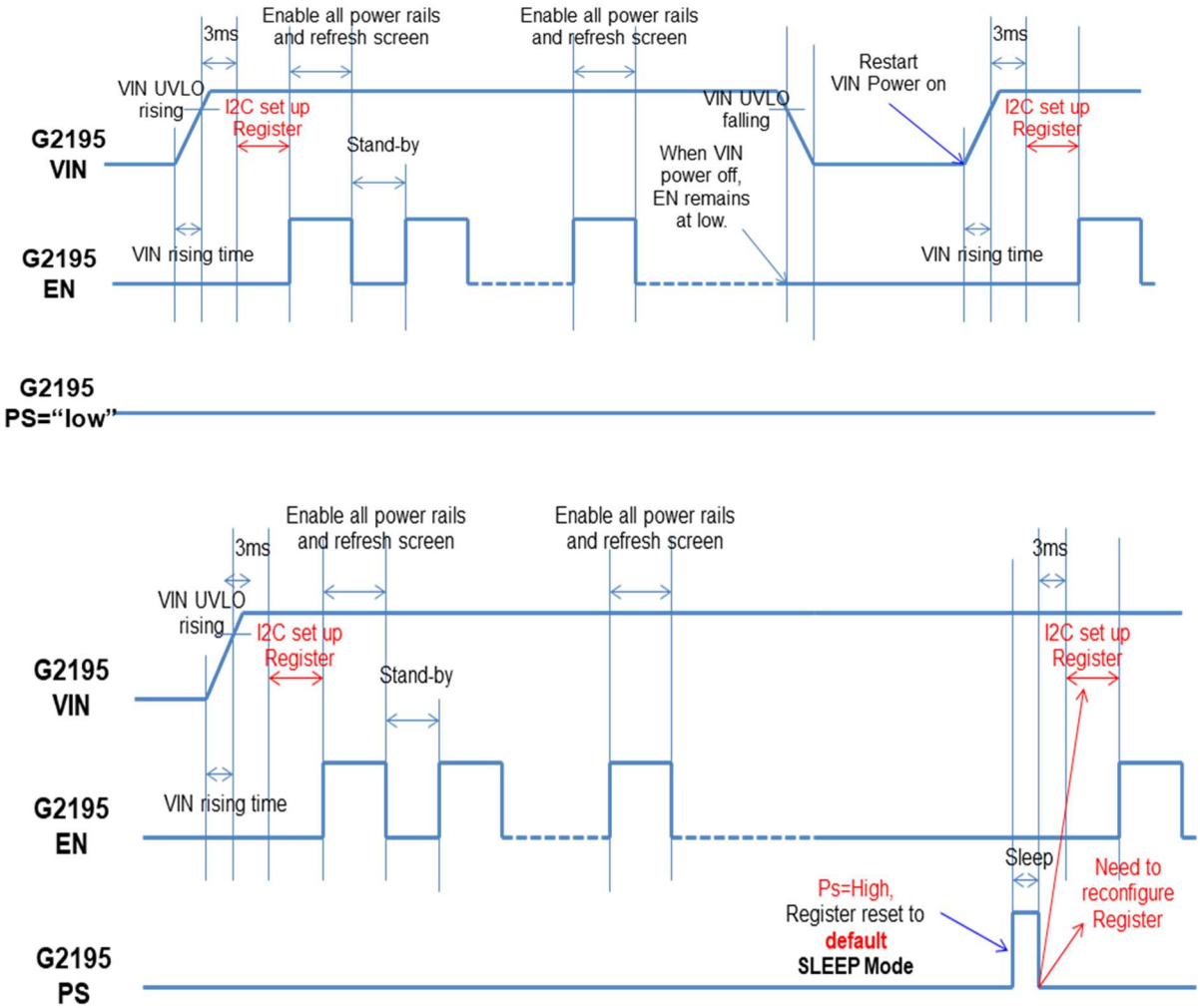
(P) EN vs. I²C



(Q) EN vs. Temperature Acquisition



(R) VIN vs. EN/PS Power On Timing



G2195 I²C Command Set up Example for 25.3" Signage EPD

	Normal Mode Sequence/All Power Rails operating frequence=500KHz			
G2195 GPIO setting	**PS=0 (Normal operating, Standby or Active)**			
	EN=0 (Standby Mode, disable all power rails, allow to accept I2C register settings)			
	The following I2C command settings follow the register definition in the datasheet.			
Step1. Set VOUT	**ID(No include R/W Bit)**	**Address**	**Data**	**Note**
VPOS1 Voltage	48	01	02E3	Set VPOS1= +15V, enable discharge
VNEG1 Voltage	48	03	02E3	Set VNEG1= -15V, enable discharge
VPOS2 Voltage	48	05	0238	Set VPOS2= +12V, enable discharge
VNEG2 Voltage	48	07	0238	Set VNEG2= -12V, enable discharge
VPOS3 Voltage	48	09	0292	Set VPOS3= +20V, enable discharge
VNEG3 Voltage	48	0B	0292	Set VNEG3= -20V, enable discharge
Step2. Set delay time	**ID(No include R/W Bit)**	**Address**	**Data**	**Note**
	48	13	FF	t_{DYL1}~t_{DYL4}=4ms
	48	14	FF	t_{DYL5}~t_{DYL8}=4ms
	48	15	C0	t_{DYL9}=4ms
Step3. Set VCOM	**ID(No include R/W Bit)**	**Address**	**Data**	**Note**
	48	0D	009A	Set DCVCOM=-1.5V disable Toggle VCOM, enable VCOM dis-charge function
Step4. Set VGH2 and Mode	**ID(No include R/W Bit)**	**Address**	**Data**	**Note**
	48	16	D194	7 level only VGH2/VGL,SS time=12ms enable VGH1 discharge function *no using VGH1(default +27V)
	48	18	1194	Set VGH2=+27V(default), enable VGH2 discharge function
	EN=1(Active Mode, enable all power rails)			

*** As long as the DAC settings in the Register need to be more than 8bits, such as VPOSx[9:0]/VNEGx[9:0]/ VCOM[8:0] /VCOMH[8:0]/ VCOML[8:0]/VGHx[9:0], I2C command should use word write for continuous writing.**
If the I2C command uses byte write mode on these registers, only the low byte of DAC will be written.

Register Address Map

Address(Hex)	Name	Default Value	Description
0x00	TMST_VALUE	0001 1001	Thermistor value read by ADC
0x01	VPOS1_SETTING & VPOS1_DIS, TRACK1, FREQ_VPOS1	0000 0001	Voltage settings for VPOS1(10-bit) & VPOS1 discharge function & Tracking
0x02		1100 0111	
0x03	VNEG1_SETTING & VNEG1_DIS, FREQ_VNEG1	0000 0001	Voltage settings for VNEG1(10-bit) & VNEG1 discharge function
0x04		1100 0111	
0x05	VPOS2_SETTING & VPOS2_DIS, TRACK2, FREQ_VPOS2	0000 0010	Voltage settings for VPOS2(10-bit) & VPOS2 discharge function & Tracking
0x06		1110 0011	
0x07	VNEG2_SETTING & VNEG2_DIS, FREQ_VNEG2	0000 0010	Voltage settings for VNEG2(10-bit) & VNEG2 discharge function
0x08		1110 0011	
0x09	VPOS3_SETTING VPOS3_DIS, TRACK3, FREQ_VPOS3	0000 0011	Voltage settings for VPOS3(10-bit) & VPOS3 discharge function & Tracking
0x0A		0010 0100	
0x0B	VNEG3_SETTING & VNEG3_DIS, FREQ_VNEG3	0000 0011	Voltage settings for VNEG3(10-bit) & VNEG3 discharge function
0x0C		0010 0100	
0x0D	DC VCOM_SETTING, VCOM/VGL_CTL, VCOM_DIS &VCOM toggle, FREQ_VCOM,FREQ_VCOMH,FREQ_VCOML	0010 0000	Voltage settings for DCVCOM(9-bit) & VCOM/VGL power off sequence, VCOM discharge function , DC/Toggle VCOM switch(1-bit) & 3 level and 7-level output switch(1-bit)
0x0E		1100 1101	
0x0F	VCOMH_SETTING & VPDD	0001 0001	Voltage settings for VCOMH(9-bit) & VPDD voltage setting for post drive discharge function(5-bit)
0x10		0011 1111	
0x11	VCOML_SETTING & VEE_EXT SETTING	0000 0000	Voltage settings for VCOML(9-bit) & VEE_EXT delay setting for post drive discharge function(7-bit)
0x12		1001 1111	
0x13	PWRON_DELAY1	1010 1010	Power on delay time set for VGL & VNEGx
0x14	PWRON_DELAY2	1010 1010	Power on delay time set for VPOSx & VGH1 or VGH2
0x15	PWRON_DELAY3 , MODE & VDDH_EXT SETTING	1000 0000	Power on delay time set for VGH2, Normal Mode or Post Drive Mode and VDDH_EXT delay setting for post drive discharge function
0x16	VGH1_SETTING & PMIC SS, VGH1 Freq & Discharge Function	0001 1001	Soft-Start time setting(2-bit) 7-Level VGH2/VGH1 or VGH2 select VGH1 Discharge function, FREQ_VGH1 Voltage settings for VGH1(10-bit)
0x17		1001 0100	
0x18	VGH2_SETTING & VGH2/VGL Freq & Discharge Function	0011 0001	VGH2 Discharge function, FREQ_VGH2, FREQ_VGL Voltage settings for VGH1(10-bit)
0x19		1001 0100	
0x1A	VPDD_LEN	0000 0000	VPDD_LEN delay setting for post drive discharge function(8-bit)
0x1B	ON_OFF & Bypass Control	1000 0000	Power On/Off Control(1-bit) Power on sequence Bypass
0x1C	Bypass Control	0000 0000	Power on sequence Bypass
0x1D	Fault Flag1	0000 0000	Show error code and Power-Good signal
0x1E	Fault Flag2	0000 0000	Show error code

0x00h

Address-0x00h								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	TMST_VALUE[7:0]							
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	1	1	0	0	1

Field Name	BIT Definition
TMST_VALUE[7:0]	Temperature read-out
	1111 0000 : <-25°C
	1111 0001 : -25°C
	……..
	1111 0110 : -10°C
	1111 0111 : -9°C
	……..
	1111 1110 : -2°C
	1111 1111 : -1°C
	0000 0000 : 0°C
	0000 0001 : 1°C
	0000 0010 : 2°C
	……..
	0001 1001 : 25°C
	……..
	0101 0101 : 85°C
	0101 0101 : > 85°C

0x01h & 0x02h

Address-0x01h								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VPOS1_DIS	TRACK1	Reserved			FREQ_VPOS1	VPOS1[9:8]	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	1
Address-0x02h								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VPOS1[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	0	0	0	1	1	1

Field Name	BIT Definition
VPOS1_DIS[7]	**0: enable VPOS1 discharge function**
	1: disable VPOS1 discharge function
TRACK1[6]	**VPOS1/VNEG1 Tracking function**
	0: disable
	1: enable(Only for VPOS/VNEG are of opposite sign but same magnitude)
Reserved[5:3]	Reserved bit
FREQ_VPOS1[2]	VPOS1 Switching Frequency
	0: 500KHz
	1: 1MHz
VPOS1[9:0]	VPOS1 voltage adjustment
	VPOS1=20V-(1023-VPOS1[9:0])*17.6mV

0x03h & 0x04h

Address-0x03h								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VNEG1_DIS	Reserved				FREQ_VNEG1	VNEG1[9:8]	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	1
Address-0x04h								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VNEG1[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	0	0	0	1	1	1

Field Name	BIT Definition
VNEG1_DIS[7]	**0: enable VNEG1 discharge function**
	1: disable VNEG1 discharge function
Reserved[6:3]	Reserved bit
FREQ_VNEG1[2]	VNEG1 Switching Frequency
	0: 500KHz
	1: 1MHz
VNEG1[9:0]	VNEG1 voltage adjustment
	VNEG1=-20V+(1023-VNEG1[9:0])*17.6mV

0x05h & 0x06h

Address-0x05h								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VPOS2_DIS	TRACK2	Reserved			FREQ_VPOS2	VPOS2[9:8]	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	1	0
Address-0x06h								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VPOS2[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	1	0	0	0	1	1

Field Name	BIT Definition
VPOS2_DIS[7]	**0: enable VPOS2 discharge function**
	1: disable VPOS2 discharge function
TRACK2[6]	VPOS2/VNEG2 Tracking function
	0: disable
	1: enable(Only for VPOS/VNEG are of opposite sign but same magnitude)
Reserved[5:3]	Reserved bit
FREQ_VPOS2[2]	VPOS2 Switching Frequency
	0: 500KHz
	1: 1MHz
VPOS2[9:0]	VPOS2 voltage adjustment
	VPOS2=20V-(1023-VPOS2[9:0])*17.6mV

0x07h & 0x08h

Address-0x07h								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VNEG2_DIS	Reserved				FREQ_VNEG2	VNEG2[9:8]	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	1	0
Address-0x08h								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VNEG2[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	1	0	0	0	1	1

Field Name	BIT Definition
VNEG2_DIS[7]	**0: enable VNEG2 discharge function**
	1: disable VNEG2 discharge function
Reserved[6:3]	Reserved bit
FREQ_VNEG2[2]	VNEG2 Switching Frequency
	0: 500KHz
	1: 1MHz
VNEG2[9:0]	VNEG2 voltage adjustment
	VNEG2=-20V+(1023-VNEG2[9:0])*17.6mV

0x09h & 0x0Ah

Address-0x09h								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VPOS3_DIS	TRACK3	Reserved			FREQ_VPOS3	VPOS3[9:8]	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	1	1
Address-0x0Ah								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VPOS3[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	1	0	0	1	0	0

Field Name	BIT Definition
VPOS3_DIS[7]	**0: enable VPOS3 discharge function**
	1: disable VPOS3 discharge function
TRACK3[6]	VPOS3/VNEG3 Tracking function
	0: disable
	1: enable(Only for VPOS/VNEG are of opposite sign but same magnitude)
Reserved[5:3]	Reserved bit
FREQ_VPOS3[2]	VPOS3 Switching Frequency
	0: 500KHz
	1: 1MHz
VPOS3[9:0]	VPOS3 voltage adjustment
	VPOS3=30V-(1023-VPOS3[9:0])*27.4mV

0x0Bh & 0x0Ch

Address-0x0Bh								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VNEG3_DIS	Reserved				FREQ_VNEG3	VNEG3[9:8]	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	1	1
Address-0x0Ch								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VNEG3[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	1	0	0	1	0	0

Field Name	BIT Definition
VNEG3_DIS[7]	**0: enable VNEG3 discharge function**
	1: disable VNEG3 discharge function
Reserved[6:2]	Reserved bit
FREQ_VNEG3[2]	VNEG3 Switching Frequency
	0: 500KHz
	1: 1MHz
VNEG3[9:0]	VNEG3 voltage adjustment
	VNEG3=-30V+(1023-VNEG3[9:0])*27.4mV

0x0Dh & 0x0Eh

Address-0x0Dh								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VCOM/VGL_MODE	3/7_LEVEL	VCOM_DIS	TOGGLE_VCOM	FREQ_ VCOM	FREQ_ VCOMH	FREQ_ VCOML	DCVCOM[8]
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	1	0	0	0	0	0
Address-0x0Eh								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	DCVCOM[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	0	0	1	1	0	1

Field Name	BIT Definition
VCOM/VGL_MODE[7]	**0: normal power off sequence for VCOM/VGL**
	1: VCOM/VGL keep alive when power off after EPD update
3/7 LEVEL[6]	**0: 7-Level output**
	1: 3-Level output
VCOM_DIS[5]	0: enable VCOM discharge function
	1: disable VCOM discharge function
TOGGLE VCOM[4]	**0: DC VCOM output**
	1: Toggle VCOM output
FREQ_VCOM[3]	DCVCOM Switching Frequency
	0: 250KHz
	1: 500KHz
FREQ_VCOMH[2]	VCOMH Switching Frequency
	0: 500KHz
	1: 1MHz
FREQ_VCOML[1]	VCOML Switching Frequency
	0: 500KHz
	1: 1MHz
DCVCOM[8:0]	DCVCOM voltage adjustment
	DCVCOM=-5V+(1022-DCVCOM[8:0]*2)*4.9mV

***It is recommended to set DCVCOM between -0.1V and -5V. The setting of 0V~-0.1V will cause G2195 DCVCOM inverting converter to fail to operate normally and protect it.**

0x0Fh & 0x10h

Address-0x0Fh								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VPDD[7:3]					Reserved		VCOMH[8]
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	1	0	0	0	1
Address-0x10h								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VCOMH[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	1	1	1	1	1	1

Field Name	BIT Definition
VPDD[7:3]	VPDD voltage setting for post drive discharge function
	VPDD=VPDD[7:3]*500mV+2.0V
Reserved[2:1]	Reserved bit
VCOMH[8:0]	VCOMH voltage adjustment
	VCOMH=20V-(1022-VCOMH[8:0]*2)*15.6mV

0x11h & 0x12h

Address-0x11h								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VEE_EXT[7:1]							VCOML[8]
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Address-0x12h								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VCOML[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	0	0	1	1	1	1	1

Field Name	BIT Definition
VEE_EXT[7:1]	VEE_EXT delay setting for post drive discharge function(0~6.3s)
	VEE_EXT=VEE_EXT[7:1]*50ms
VCOML[8:0]	VCOML voltage adjustment
	VCOML=-25V+(1022-VCOML[8:0]*2)*15.6mV

0x13h

Address-0x13h								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	t_{DYL1}		t_{DYL2}		t_{DYL3}		t_{DYL4}	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	0	1	0	1	0	1	0

Field Name	BIT Definition
t_{DYL1}[7:6]	Delay time set from EN to VGL
	00: 0ms
	01: 1ms
	10: 2ms
	11: 4ms
t_{DYL2}[5:4]	Delay time set from VGL to VNEG3
	00: 0ms
	01: 1ms
	10: 2ms
	11: 4ms
t_{DYL3}[3:2]	Delay time set from VNEG3 to VNEG2
	00: 0ms
	01: 1ms
	10: 2ms
	11: 4ms
t_{DYL4}[1:0]	Delay time set from VNEG2 to VNEG1
	00: 0ms
	01: 1ms
	10: 2ms
	11: 4ms

0x14h

Address-0x14h								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	t_{DYL5}		t_{DYL6}		t_{DYL7}		t_{DYL8}	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	0	1	0	1	0	1	0

Field Name	BIT Definition
t_{DYL5}[7:6]	Delay time set from VNEG1 to VPOS3
	00: 0ms
	01: 1ms
	10: 2ms
	11: 4ms
t_{DYL6}[5:4]	Delay time set from VPOS3 to VPOS2
	00: 0ms
	01: 1ms
	10: 2ms
	11: 4ms
t_{DYL7}[3:2]	Delay time set from VPOS2 to VPOS1
	00: 0ms
	01: 1ms
	10: 2ms
	11: 4ms
t_{DYL8}[1:0]	Delay time set from VPOS1 to VGH1 or VGH2(VGH_7_SEL=1)
	00: 0ms
	01: 1ms
	10: 2ms
	11: 4ms

0x15h

Address-0x15h								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	t_{DYL9}		MODE	VDDH_EXT[4:0]				
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	0	0	0	0	0	0	0

Field Name	BIT Definition
t_{DYL9}[7:6]	Delay time set from VGH1 to VGH2
	00: 0ms
	01: 1ms
	10: 2ms
	11: 4ms
MODE[5]	**0: normal mode power off sequence**
	1: post drive discharge mode power off sequence
VDDH_EXT[4:0]	VDDH_EXT delay setting for post drive discharge function(0~1s)
	VDDH_EXT=VDDH_EXT[4:0]*50ms

0x16h & 0x17h

Address-0x16h								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	SS		Reserved	VGH_7_SEL	DIS_VGH1_CTL	FREQ_VGH1	VGH1[9:8]	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	1	1	0	0	1
Address-0x17h								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VGH1[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	0	0	1	0	1	0	0

Field Name	BIT Definition
SS[7:6]	PMIC soft-start time (VPOS1/VPOS2/VPOS3/VNEG1/VNEG2/VNEG3/ VGH1/VGH2/VGL/VCOMDC/VCOMH/VCOML)
	00: 6ms
	01: 8ms
	10: 10ms
	11: 12ms
Reserved[5]	Reserved bit
VGH_7_SEL[4]	0: 7-Level output VGH2/VGH1/VGL
	1: 7-Level output only VGH2/VGL(VGH1 disable)
DIS_VGH1_CTL[3]	0: enable VGH1 discharge function
	1: disable VGH1 discharge function
FREQ_VGH1[2]	VGH1 Switching Frequency
	0: 500KHz
	1: 250KHz
VGH1[9:0]	VGH1 voltage adjustment
	VGH1=50V-(1023-VGH1[9:0])*37.1mV

0x18h & 0x19h

Address-0x18h								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	Reserved		DIS_VGH2_CTL1	DIS_VGH2_CTL2	FREQ_VGH2	FREQ_VGL	VGH2[9:8]	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	1	1	0	0	0	1
Address-0x19h								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VGH2[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	0	0	1	0	1	0	0

Field Name	BIT Definition
Reserved[7:6]	Reserved bit
DIS_VGH2_ CTL1[5]	0: enable VGH2 discharge function
	1: disable VGH2 discharge function
DIS_VGH2_ CTL2[4]	0: enable VGH2 discharge function(only for Post Drive)
	1: disable VGH2 discharge function(only for Post Drive)
FREQ_VGH2[3]	VGH2 Switching Frequency
	0: 500KHz
	1: 250KHz
FREQ_VGL[2]	VGL Switching Frequency
	0: 500KHz
	1: 250KHz
VGH2[9:0]	VGH2 voltage adjustment
	VGH2=50V-(1023-VGH2[9:0])*37.1mV

0x1Ah

Address-0x1Ah								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VPDD_LEN[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Field Name	BIT Definition
VPDD_LEN[7:0]	VPDD_LEN delay setting(0~30s)
	VPDD_LEN follow RFQ reguest as below

Index	Time(ms)	Index	Time(ms)	Index	Time(ms)	Index	Time(ms)
0	0	64	3820	128	8850	192	16230
1	50	65	3890	129	8950	193	16380
2	110	66	3960	130	9040	194	16530
3	160	67	4030	131	9130	195	16680
4	210	68	4090	132	9230	196	16830
5	270	69	4160	133	9320	197	16980
6	320	70	4230	134	9420	198	17140
7	380	71	4300	135	9510	199	17290
8	430	72	4370	136	9610	200	17450
9	490	73	4440	137	9710	201	17610
10	540	74	4510	138	9810	202	17770
11	600	75	4580	139	9900	203	17930
12	650	76	4650	140	10000	204	18100
13	710	77	4720	141	10100	205	18260
14	760	78	4800	142	10200	206	18430
15	820	79	4870	143	10300	207	18600
16	870	80	4940	144	10400	208	18770
17	930	81	5010	145	10510	209	18940
18	990	82	5080	146	10610	210	19120
19	1040	83	5160	147	10710	211	19290
20	1100	84	5230	148	10820	212	19470
21	1160	85	5310	149	10920	213	19650
22	1210	86	5380	150	11030	214	19830
23	1270	87	5450	151	11130	215	20020
24	1330	88	5530	152	11240	216	20210
25	1390	89	5600	153	11350	217	20390
26	1440	90	5680	154	11460	218	20590
27	1500	91	5760	155	11570	219	20780
28	1560	92	5830	156	11680	220	20980
29	1620	93	5910	157	11790	221	21170
30	1680	94	5990	158	11900	222	21370

Index	Time(ms)	Index	Time(ms)	Index	Time(ms)	Index	Time(ms)
31	1740	95	6060	159	12010	223	21580
32	1800	96	6140	160	12120	224	21780
33	1860	97	6220	161	12240	225	21990
34	1920	98	6300	162	12350	226	22200
35	1980	99	6380	163	12470	227	22420
36	2040	100	6460	164	12580	228	22640
37	2100	101	6540	165	12700	229	22860
38	2160	102	6620	166	12820	230	23080
39	2220	103	6700	167	12940	231	23300
40	2280	104	6780	168	13060	232	23530
41	2340	105	6860	169	13180	233	23770
42	2400	106	6940	170	13300	234	24000
43	2460	107	7020	171	13420	235	24240
44	2530	108	7110	172	13540	236	24490
45	2590	109	7190	173	13670	237	24730
46	2650	110	7270	174	13790	238	24990
47	2710	111	7360	175	13920	239	25240
48	2780	112	7440	176	14050	240	25500
49	2840	113	7520	177	14170	241	25760
50	2900	114	7610	178	14300	242	26030
51	2970	115	7700	179	14430	243	26300
52	3030	116	7780	180	14570	244	26580
53	3100	117	7870	181	14700	245	26860
54	3160	118	7960	182	14830	246	27150
55	3230	119	8040	183	14970	247	27440
56	3290	120	8130	184	15100	248	27740
57	3360	121	8220	185	15240	249	28050
58	3420	122	8310	186	15380	250	28360
59	3490	123	8400	187	15520	251	28670
60	3550	124	8490	188	15660	252	28990
61	3620	125	8580	189	15800	253	29320
62	3690	126	8670	190	15940	254	29660
63	3750	127	8760	191	16090	255	30000

0x1Bh

Address-0x1Bh								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	ON_OFF	VGL_PASS	VNEG3_PASS	VNEG2_PASS	VNEG1_PASS	VPOS3_PASS	VPOS2_PASS	VPOS1_PASS
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	0	0	0	0	0	0	0

Field Name	BIT Definition
ON_OFF[7]	0: turn off all power rails(VPOSx,VNEGx,VGH1,VGH2,VGL,VCOMx)
	1: turn on all power rails(VPOSx,VNEGx,VGH1,VGH2,VGL,VCOMx)
VGL_PASS[6]	power rail bypass sequence @ power on
	0: Normal
	1: Bypass
VNEG3_PASS[5]	power rail bypass sequence @ power on
	0: Normal
	1: Bypass
VNEG2_PASS[4]	power rail bypass sequence @ power on
	0: Normal
	1: Bypass
VNEG1_PASS[3]	power rail bypass sequence @ power on
	0: Normal
	1: Bypass
VPOS3_PASS[2]	power rail bypass sequence @ power on
	0: Normal
	1: Bypass
VPOS2_PASS[1]	power rail bypass sequence @ power on
	0: Normal
	1: Bypass
VPOS1_PASS[0]	power rail bypass sequence @ power on
	0: Normal
	1: Bypass

0x1Ch

Address-0x1Ch								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VGH1_PASS	VGH2_PASS	VCOMH_PASS	DCVCOM_PASS	VCOML_PASS	Reserved		
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Field Name	BIT Definition
VGH1_PASS[7]	power rail bypass sequence @ power on
	0: Normal
	1: Bypass
VGH2_PASS[6]	power rail bypass sequence @ power on
	0: Normal
	1: Bypass
VCOMH_PASS[5]	power rail bypass sequence @ power on
	0: Normal
	1: Bypass
DCVCOM_PASS[4]	power rail bypass sequence @ power on
	0: Normal
	1: Bypass
VCOML_PASS[3]	power rail bypass sequence @ power on
	0: Normal
	1: Bypass
Reserved[2:0]	Reserved bit

0x1Dh

Address-0x1Dh								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	PG	TSD	FLT_VPOS1	FLT_VPOS2	FLT_VPOS3	FLT_VNEG1	FLT_VNEG2	FLT_VNEG3
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0

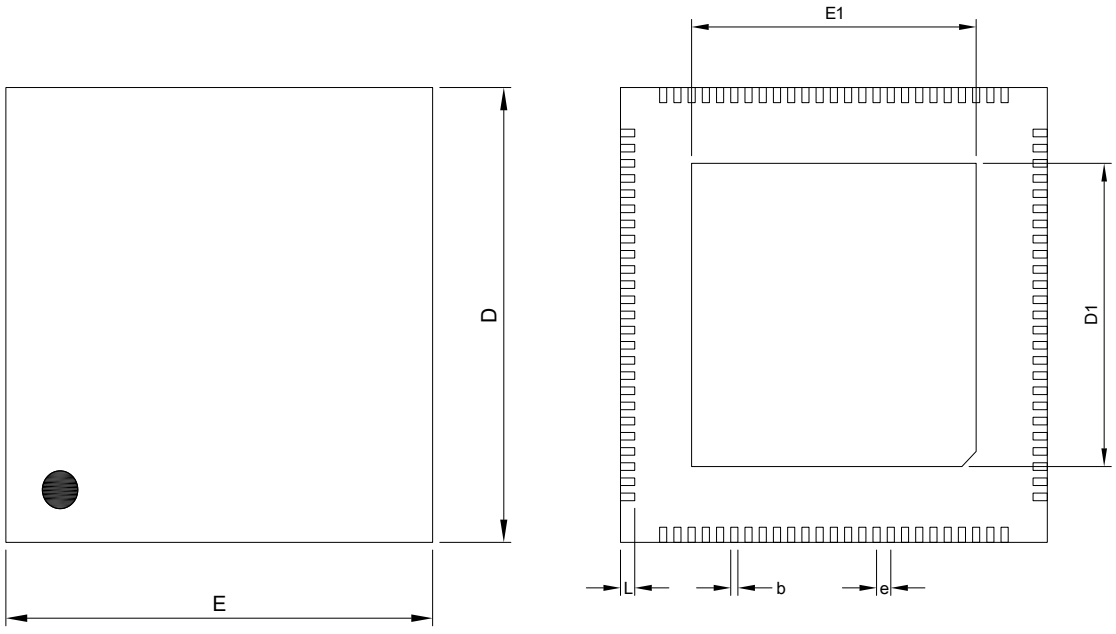
Field Name	BIT Definition
PG[7]	**0: VPOS1/2/3, VNEG1/2/3, VGH1/2, VGL ,VCOMx are not in regulation or turn off**
	1: VPOS1/2/3, VNEG1/2/3, VGH1/2, VGL , VCOMx are in regulation
TSD[6]	**0: no fault event**
	1: Thermal shutdown
FLT_VPOS1[5]	**0: no fault event**
	1: UVP or SCP
FLT_VPOS2[4]	**0: no fault event**
	1: UVP or SCP
FLT_VPOS3[3]	**0: no fault event**
	1: UVP or SCP
FLT_VNEG1[2]	**0: no fault event**
	1: UVP or SCP
FLT_VNEG2[1]	**0: no fault event**
	1: UVP or SCP
FLT_VNEG3[0]	**0: no fault event**
	1: UVP or SCP

0x1Eh

Address-0x1Eh								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	FLT_VGH1	FLT_VGH2	FLT_VGL	FLT_VCOMDC	FLT_VCOMH	FLT_VCOML	Re-served	ID
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	1

Field Name	BIT Definition
FLT_VGH1[7]	**0: no fault event**
	1: UVP or SCP
FLT_VGH2[6]	**0: no fault event**
	1: UVP or SCP
FLT_VGL[5]	**0: no fault event**
	1: UVP or SCP
FLT_VCOMDC[4]	**0: no fault event**
	1: UVP or SCP
FLT_VCOMH[3]	**0: no fault event**
	1: UVP or SCP
FLT_VCOML[2]	**0: no fault event**
	1: UVP or SCP
Reserved[1]	Reserved bit
ID[0]	0: V3 Toggle_SEL0/Toggle_SEL1 control table
	1: V4 Toggle_SEL0/Toggle_SEL1 control table

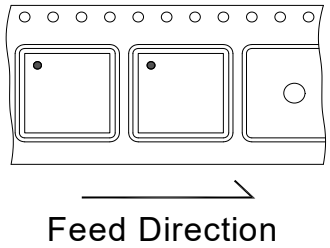
Package Information



QFN12X12-100 Package

Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.85	0.90	0.0315	0.0335	0.0354
A1	0.00	- - -	0.05	0.0000	- - -	0.0020
A2		0.20 REF			0.0079 REF	
D	11.95	12.00	12.05	0.4705	0.4724	0.4744
E	11.95	12.00	12.05	0.4705	0.4724	0.4744
D1	7.95	8.00	8.05	0.3130	0.3150	0.3170
E1	7.95	8.00	8.05	0.3130	0.3150	0.3170
b	0.15	0.20	0.25	0.0059	0.0079	0.0098
e		0.40 BSC			0.0157 BSC	
L	0.35	0.40	0.45	0.0138	0.0157	0.0177

Taping Specification



PACKAGE	Q'TY/REEL
QFN12X12-100	2,000ea