5+1 channels PMIC

Features

- **3.0V ~ 5.5V Input Voltage Operation**
- **95% Efficient DC/DC Converter**
- **Built-in 5-ch synchronous buck converter, 1-ch LDO**
- **Bucks and LDO can be set to lower IQ at low load**
- **Buck2 and Buck3 Support DVS Function, 12.5mV/step**
- **Built-In Power ON/OFF Sequence for PMU**
- **Built-In Short Circuit Protection (SCP), Under Voltage Protection (UVP), and cycle-by cycle current limit for DC/DC Converters**
- **LDO is Programmable to Voltage Options by I^2C**
- **Built-In Thermal Shutdown Function**
- **Built-In VCC OVP Function**
- **TQFN4X4-32 Package**

General Description

The G2237 provide a complete power supply solution for handsets or data card. It contains 5 dc/dc converters and 1 LDO to power each critical blocks of mobile phone, and is optimized for maximum battery life, featuring a low ground current when in standby mode operation. All channels DC/DC converters operate at one fixed frequency of 3.0MHz to optimize size, cost, and efficiency. All Synchronous converters operate at pulse skipping mode at light load. The G2237 features a I^2C compatible interface.

The G2237 is available in TQFN4X4-32 package.

Applications

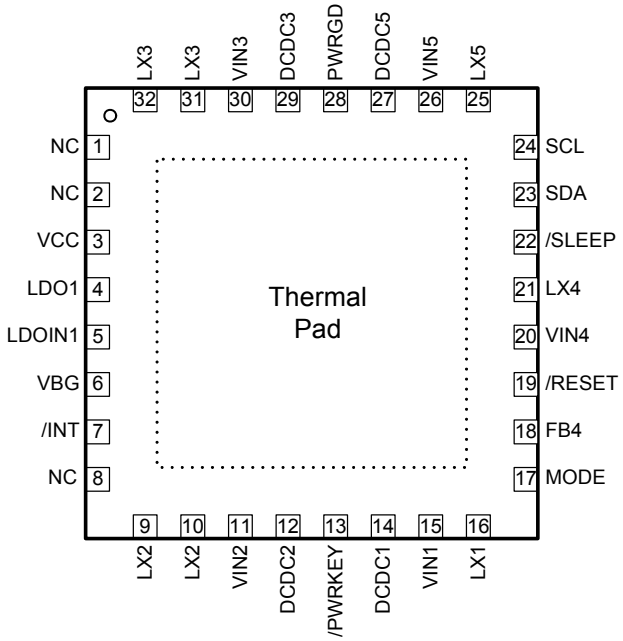
- **Mobile Handsets**
- **TV Dongle**
- **Smart Phone**
- **Set Top Box**

Ordering Information

ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE (Green)
G2237K11U	2237	-40°C~+85°C	TQFN4X4-32

Note: K1:TQFN4X4-32
1: Bonding code
U: Tape & Reel
Green : Lead Free / Halogen Free

Pin Configuration



G2237 TQFN4X4-32

Note: Recommend connecting the Thermal Pad to the Ground for excellent power dissipation.

Absolute Maximum Ratings

VCC, VIN1, VIN2, VIN3, VIN4, VIN5, LDOIN1 . . . . . -0.3V to +6.3V
DCDC1, DCDC2, DCDC3, FB4, DCDC5, LDO1 . . . . . -0.3V to +6.3V
LX1, LX2, LX3, LX4, LX5 . . . . . -0.3V to +6.3V
Other Pins . . . . . -0.3V to +6.3V
Thermal Resistance Junction to Ambient, (θ_{JA})
TQFN4X4-32 . . . . . .52°C/W

Continuous Power Dissipation (T_A=25°C)
TQFN4X4-32. . . . . .1.923W
Thermal Resistance Junction to Case, (θ_{JC})
TQFN4X4-32 . . . . . .7°C/W
Operating Ambient Temperature .-35°C to 85°C
Storage Temperature Range. . . . . -55°C to +150°C
Reflow Temperature (soldering, 10 sec) . . . . . 260°C
ESD (HBM). 2KV
ESD (MM) 200V

1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Device are ESD sensitive. Handling precaution recommended. The Human Body model is a 100pF capacitor discharged through a 1.5KΩ resistor into each pin.

Electrical characteristics

(**VCC=VINx=LDOINx=5V, T_A=25°C, unless otherwise specified)**

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
GENERAL						
VCC Operating Voltage for PMU	V_{VCC_PMU}		3.0	---	5.5	V
VCC Over Voltage threshold	V_{VCC_OVLO}	VCC rising	5.75	6.0	6.25	V
VCC Under Voltage threshold	V_{VCC_UVLO}	VCC falling	---	3.0	---	V
VCC Under Voltage Hysteresis	$V_{VCC\_UVLOHYS}$		---	500	---	mV
PMU Stand-by Supply Current	I_{VCC}	ALL converters enter ECO mode, and without loading current.	---	---	180	uA
OSCILLATOR						
Frequency	F_{OSC}		2.4	3.0	3.6	MHz
DCDC1 Buck Converter						
Soft-Start Internal	SS_CH1		---	2	---	mS
VO1 regulation voltage accuracy	%VO1		-1.5	---	1.5	%
Load Regulation	$\Delta V_{O1,LOAD}$	FPWM	---	0.5	---	%
Maximum Duty Cycle	D_{max1}		---	100	---	%
VIN1 Leakage Current	I_{VIN1_LK}	V_{LX1}=0V, VIN1=5.0V	---	1	5	µA
LX1 Leakage Current	I_{LX1_LK}	V_{LX1}=5.0V	---	1	5	µA
Switch ON Resistance	Ron1-P		---	150	---	mΩ
	Ron1-N		---	120	---	
Peak Current Limit	I_{LIM_CH1}		2.5	2.8	---	A
Under Voltage Protection Threshold	$\%V_{UVP\_CH1}$	Ratio=V_{UVP}/V_{OUT}	---	75	---	%
DCDC2, DCDC3 Buck Converter						
Soft-Start Internal	SS_CHx		---	2	---	mS
VOx regulation voltage accuracy	%VOx		-1.5	---	1.5	%
Load Regulation	$\Delta V_{Ox,LOAD}$	FPWM	---	0.5	---	%
Maximum Duty Cycle	D_{max}		---	100	---	%
VINx Leakage Current	I_{VINx_LK}	V_{LXx}=0V, VINx=5.0V	---	1	5	µA
LXx Leakage Current	I_{LXx_LK}	V_{LXx}=5.0V	---	1	5	µA
Switch ON Resistance	Ron2-P		---	80	---	mΩ
	Ron2-N		---	35	---	
Peak Current Limit	I_{LIM_CHx}		3.6	4.0	---	A
Under Voltage Protection Threshold	ΔV_{UVP_CHx}	$\Delta V_{UVP\_CHx}=VOUT_{SET}-VOUT_{UVP}$	---	100	---	mV

Electrical characteristics (continued)

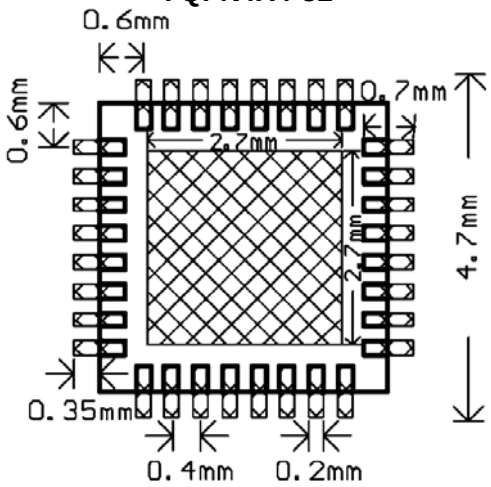
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
DCDC4 Buck Converter						
Soft-Start Internal	SS_CH4		---	2	---	mS
FB4 pin regulation voltage	V_{FB4}		0.788	0.80	0.812	V
Load Regulation	$\Delta V_{FB4,LOAD}$	FPWM	---	0.5	---	%
Maximum Duty Cycle	D_{max4}		---	100	---	%
VIN4 Leakage Current	I_{VIN4_LK}	V_{LX4}=0V, VIN4=5.0V	---	1	5	µA
LX4 Leakage Current	I_{LX4_LK}	V_{LX4}=5.0V	---	1	5	µA
Switch ON Resistance	Ron4-P		---	150	---	mΩ
	Ron4-N		---	90	---	
Peak Current Limit	I_{LIM_CH4}		2.5	2.8	---	A
Under Voltage Protection Threshold	$\%V_{UVP\_CH4}$	Ratio=V_{UVP}/V_{OUT}	---	87.5	---	%
DCDC5 Buck Converter						
Soft-Start Internal	SS_CH5		---	2	---	mS
VO5 regulation voltage accuracy	%VO5		-1.5	---	1.5	%
Load Regulation	$\Delta V_{O5,LOAD}$	FPWM	---	0.5	---	%
Maximum Duty Cycle	D_{max5}		---	100	---	%
VIN5 Leakage Current	I_{VIN5_LK}	V_{LX5}=0V, VIN5=5.0V	---	1	5	µA
LX5 Leakage Current	I_{LX5_LK}	V_{LX5}=5.0V	---	1	5	µA
Switch ON Resistance	Ron5-P		---	150	---	mΩ
	Ron5-N		---	120	---	
Peak Current Limit	I_{LIM_CH1}		2.5	2.8	---	A
Under Voltage Protection Threshold	$\%V_{UVP\_CH1}$	Ratio=V_{UVP}/V_{OUT}	---	83	---	%
LDO1						
Input voltage range	V_{LDOIN1}	LDOIN1	2.8	---	5.5	V
Soft-Start Internal	SS_{LDO1}		---	2	---	mS
Output Voltage accuracy	$\%V_{LDO1}$	Io=100mA	-1.5	---	1.5	%
Continuous output current at ECO mode	I_{O1_ECO}		---	---	5	mA
LDO Input Current	I_{LDOIN1}	Io=0mA, Normal mode	---	---	32	µA
	I_{LDOIN1_ECO}	Io=0mA, ECO mode	---	---	10	µA
Dropout Voltage	V_{DOLDO1}	Io=300mA, Normal mode	---	200	400	mV
	$V_{DOLLDO1}$	Io=50mA, Normal mode		35	70	mV
Output current limit	$I_{LIMLDO1}$	LDOIN1>LDO1+1.0V, Normal mode	500	600	---	mA
LDO Load Regulation	%LD1	LDOIN1>LDO1+1.0V, Normal mode Io=1mA~200mA	---	---	1	%
Short Circuit Protection threshold	$\%V_{SCPLDO1}$	Ratio=V_{SCP}/V_{OUT}	---	8.5	---	%
Ripple Rejection	PSRR1	f=10Hz~3kHz, Io=100mA, Normal mode	---	65	---	dB
Output Noise Voltage		f=10Hz~100kHz, Normal mode	---	45	---	uVrms
ECO exit time	t_{d1_ECO}	Minimum wait time to draw full current after leaving ECO mode	---	---	50	uS
Protection						
UVP Protection Fault Delay	t_{D_Fault}	DCDC1~DCDC5	128	---	---	mS
Thermal Shutdown Detect	T_{SD}		---	150	---	°C
Thermal Shutdown Hysteresis	ΔT_{SD}		---	20	---	°C

Electrical characteristics (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Control Signal						
Logic-Input Threshold	V_{TH}	High threshold	1.4	---	---	V
(/PWRKEY, /SLEEP, /RESET, MODE)	V_{TL}	Low threshold	---	---	0.5	V
Pull High Resistance (/PWRKEY, /SLEEP, /RESET)	R_{PH}		---	100	---	KΩ
Pull High Resistance (MODE)	R_{PH2}		---	250	---	KΩ
Open-Drain Output Low Voltage (PWRGD,/INT,)	V_{ODLOW}	I_{SINK}=5mA, V_{VCC}=3.7V	---	---	100	mV
Open-Drain Output Leakage Current (PWRGD./INT)	I_{LK_OD}	V_{OD}=5V	---	---	1	µA
PWRGD Delay Time	t_{RDLY_PWRGD}		---	12	---	mS
Re-start up Delay Time	$t_{DLY\_REBOOST}$		---	1	---	Sec
SMBus Interface						
Logic Input High Voltage	V_{IH}	SCL, SDA	1.4	---	---	V
Logic Input Low Voltage	V_{IL}	SCL, SDA	---	---	0.5	V
Logic Input Current		Logic inputs forced to VCC or GND	-2	---	2	µA
SMBus Input Capacitance		SCL, SDA	---	5	---	pF
SMBus Clock Frequency	f_{SCL}	Fast mode	---	---	400	kHz
		High-speed mode, load 400pF max	---	---	1.7	MHz
		High-speed mode, load 100pF max	---	---	3.4	MHz
SCL Clock Low Time	t_{LOW}	Fast mode	1.3	---	---	µS
SCL Clock High Time	t_{HIGH}	Fast mode	0.6	---	---	µS
SDA Setup Time	$t_{SU:DAT}$	Fast mode	100	---	---	nS
SDA Hold Time	$t_{HD:DAT}$	Fast mode	0	---	0.9	uS
Bus-Free Time from START and STOP	t_{BUF}	Fast mode	1.3	---	---	µS
Hold Time Repeated START Condition	$t_{HD:STA}$	Fast mode	0.6	---	---	µS
Setup Time Repeated START Condition	$t_{SU:STA}$	Fast mode	0.6	---	---	µS
Setup Time for STOP Condition	$t_{SU;STO}$	Fast mode	0.6	---	---	µS
Rise Time of SCL/SDA signals	t_r	10% to 90% points	20	---	300	nS
Fall Time of SCL/SDA signals	t_f	90% to 10% points	20	---	300	nS

Minimum Footprint PCB Layout Section

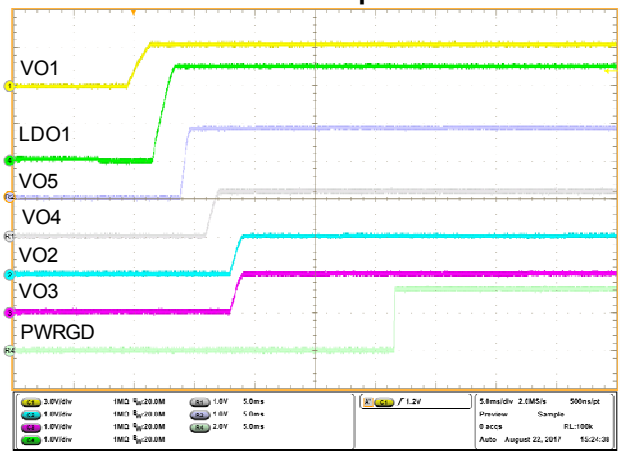
TQFN4X4-32



Typical Performance Characteristics

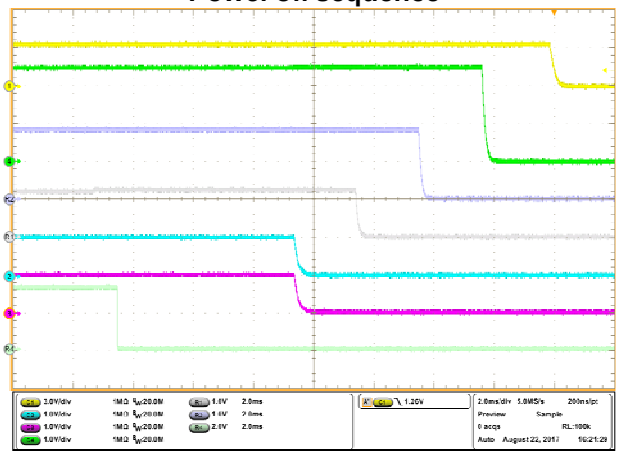
(VCC=VINx=5.5V, T_A=25°C, unless otherwise specified)

Power on sequence



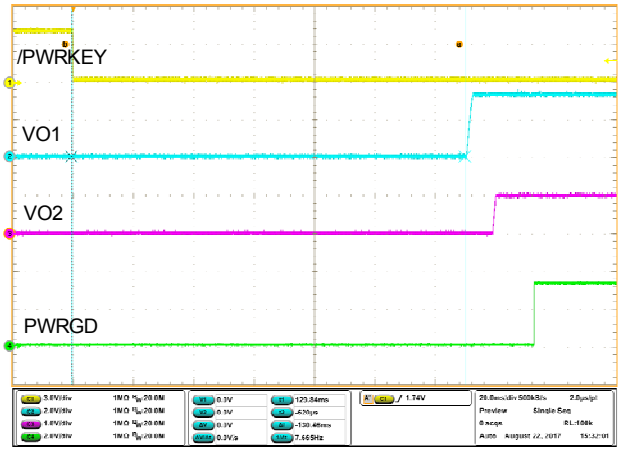
Scope time scale =5ms

Power off sequence



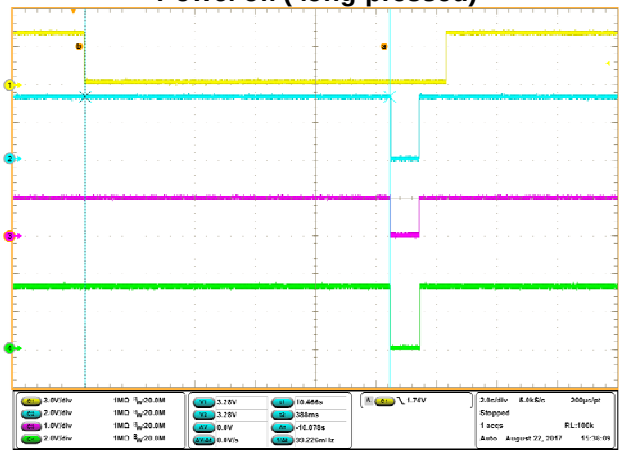
Scope time scale =2ms

Power on (MODE=FLOATING)



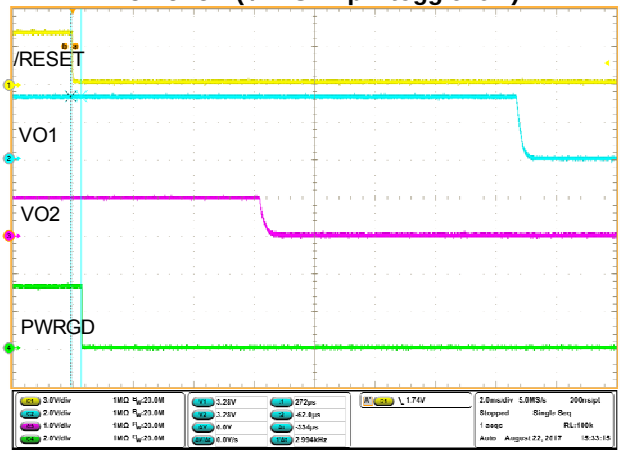
Scope time scale =20ms

Power off (long-pressed)



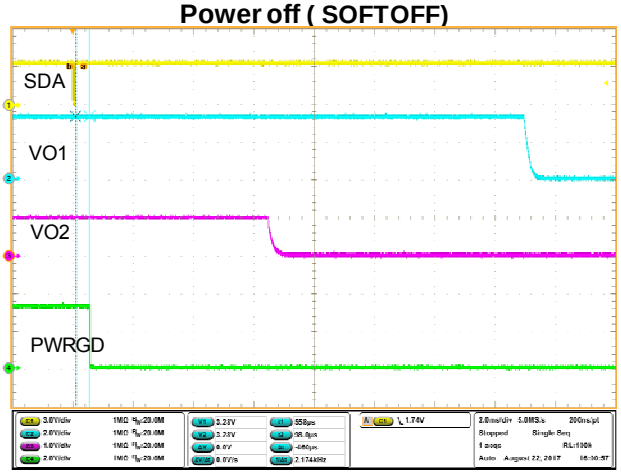
Scope time scale =2s

Power off (/RESET pin toggle low)



Scope time scale =2ms

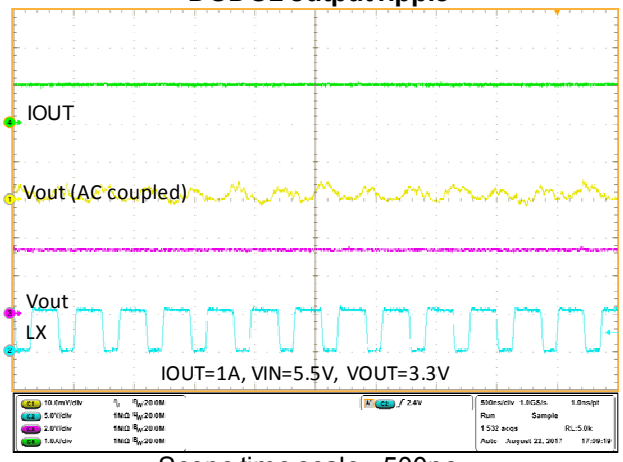
Power off (SOFTOFF)



Scope time scale =2ms

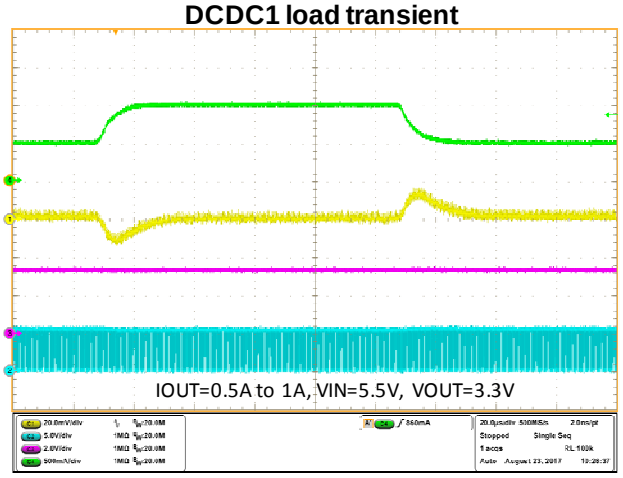
Typical Performance Characteristics (Continued)

DCDC1 output ripple



Scope time scale =500ns

DCDC1 load transient

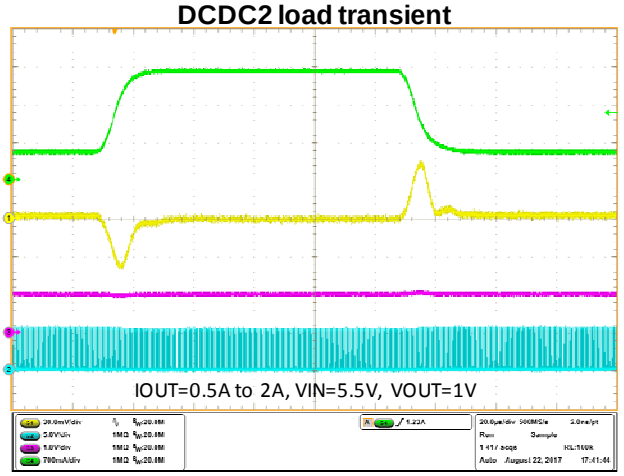


Scope time scale =20us

DCDC2 output ripple

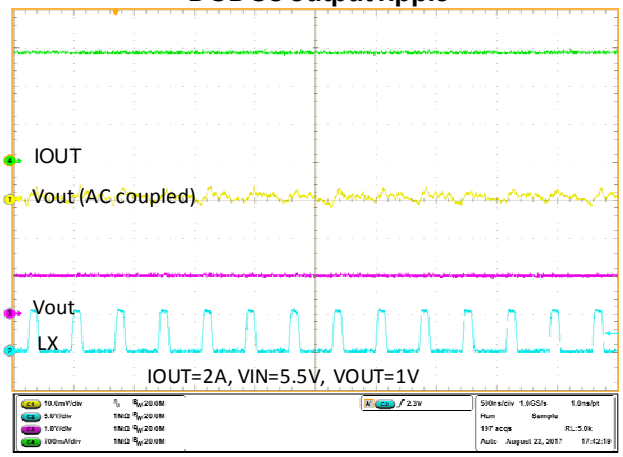
Scope time scale =500ns

DCDC2 load transient



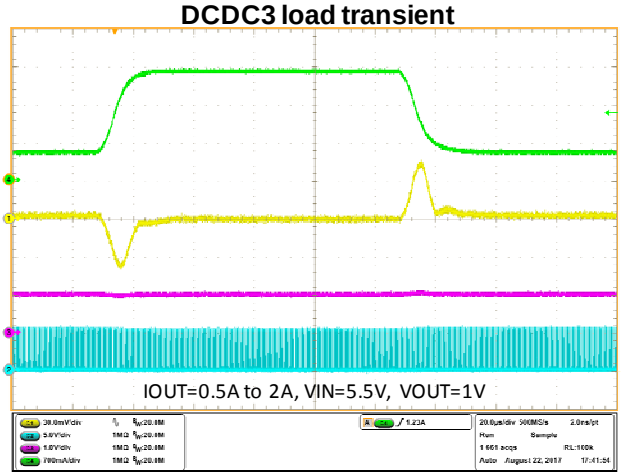
Scope time scale =20us

DCDC3 output ripple



Scope time scale =500ns

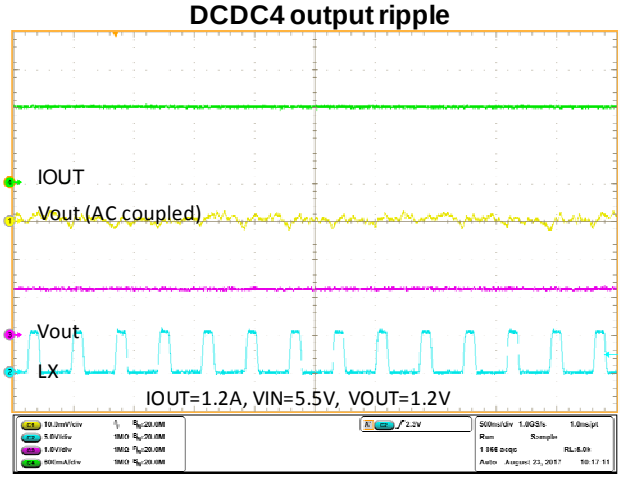
DCDC3 load transient



Scope time scale =20us

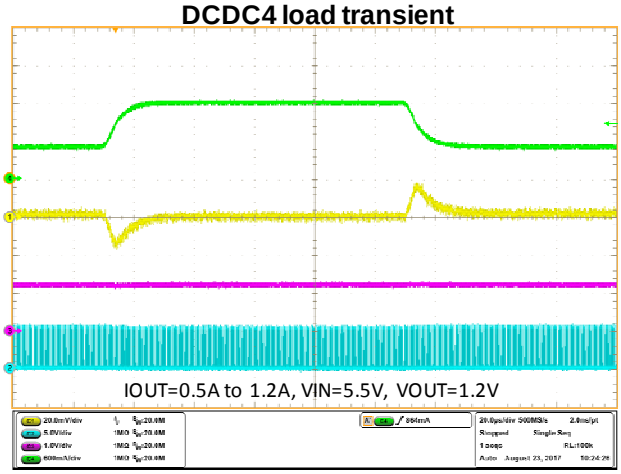
Typical Performance Characteristics (Continued)

DCDC4 output ripple



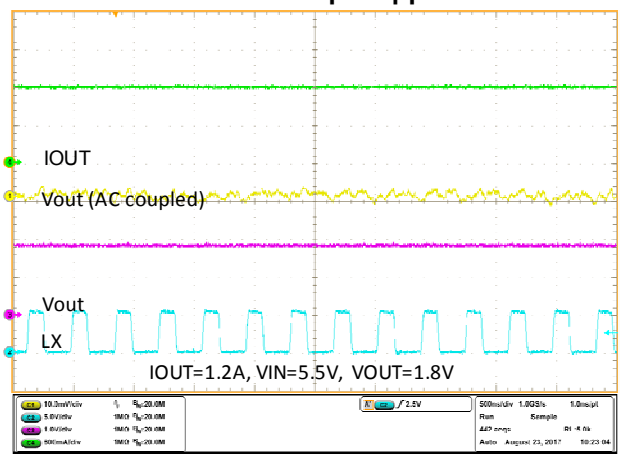
Scope time scale =500ns

DCDC4 load transient



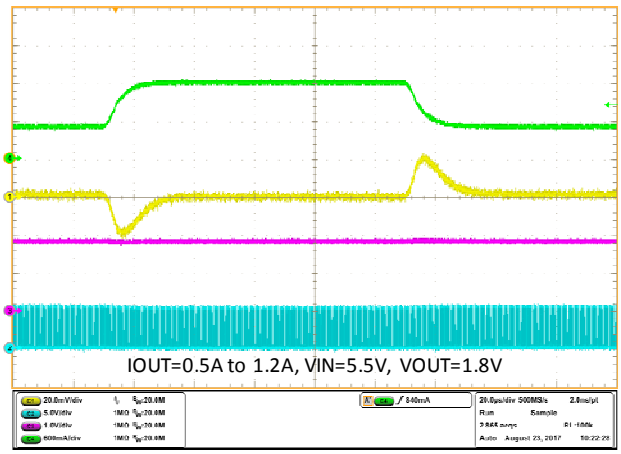
Scope time scale =20us

DCDC5 output ripple



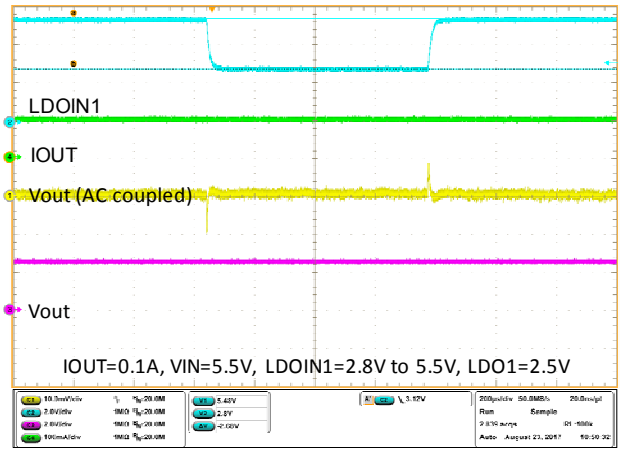
Scope time scale =500ns

DCDC5 load transient



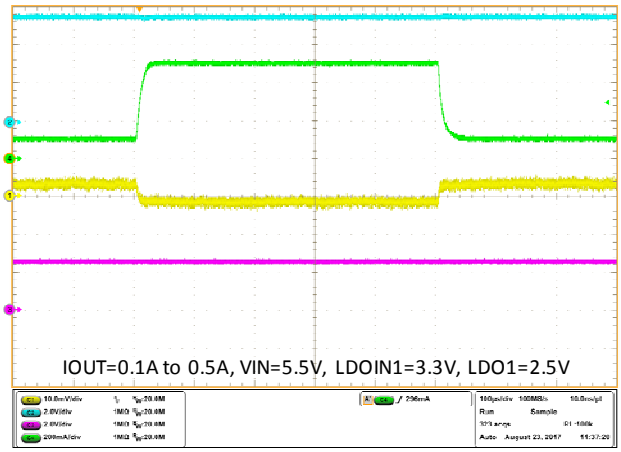
Scope time scale =20us

LDO1 line transient



Scope time scale =200us

LDO1 load transient

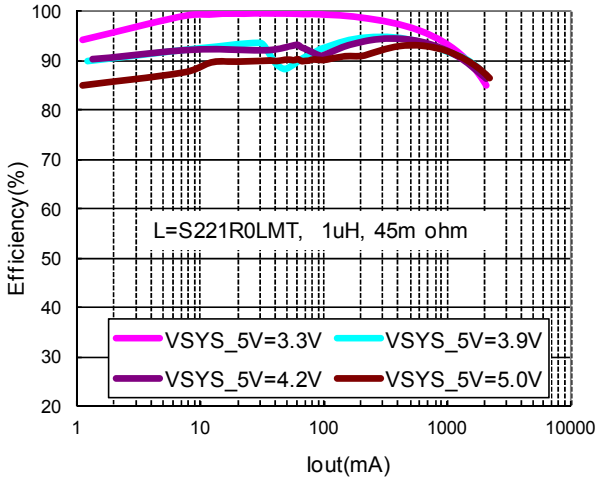


Scope time scale =100us

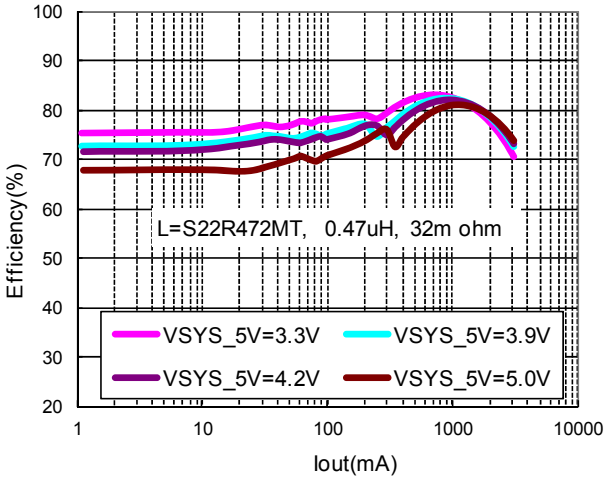
Typical Performance Characteristics (Continued)

DC curves

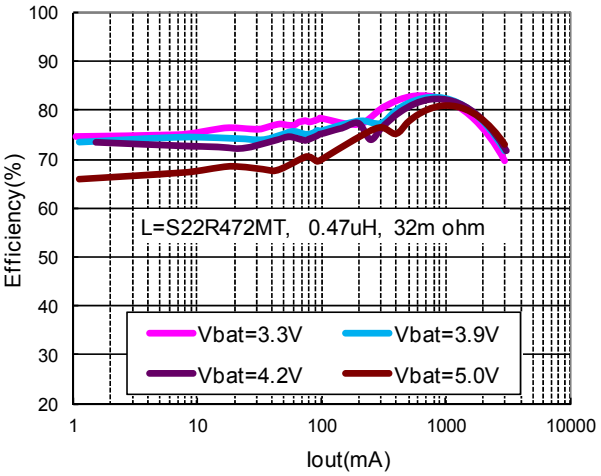
DCDC1, Auto PSM



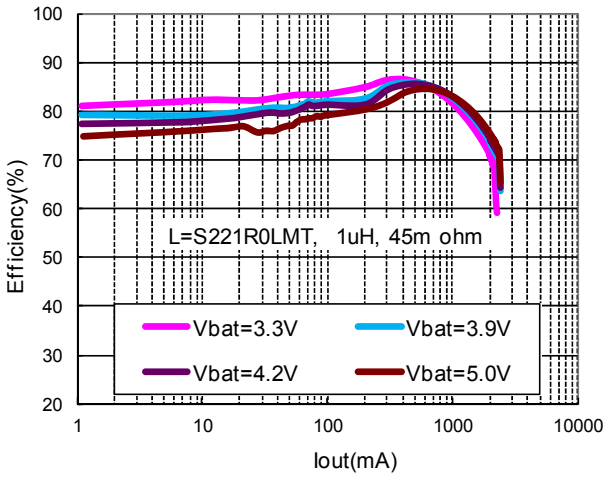
DCDC2, Auto PSM



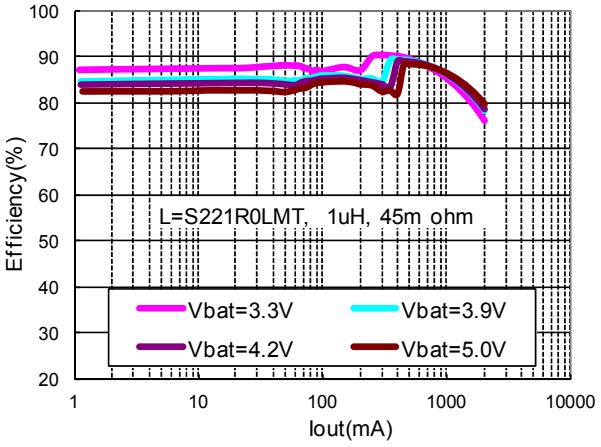
DCDC3, Auto PSM



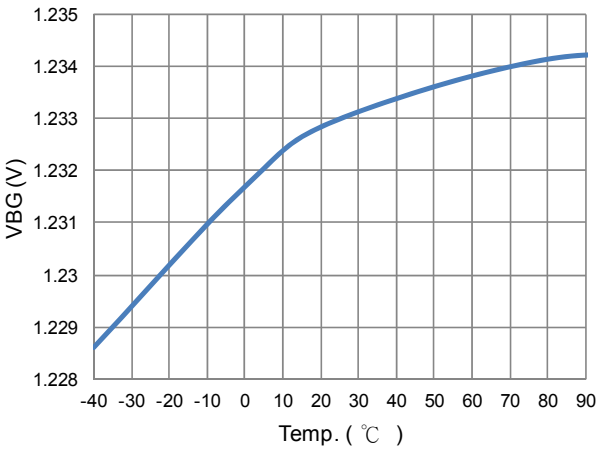
DCDC4, Auto PSM



DCDC5, Auto PSM

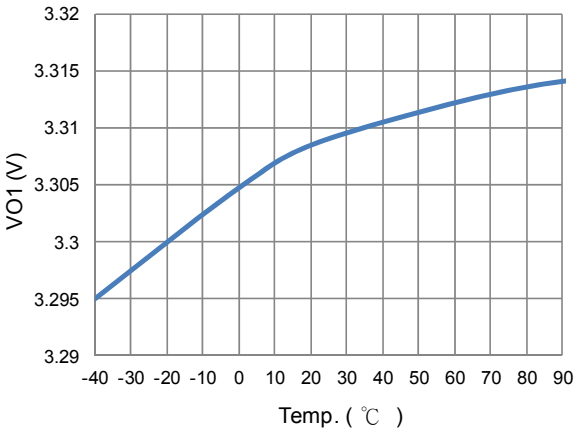


VBG vs Temp.

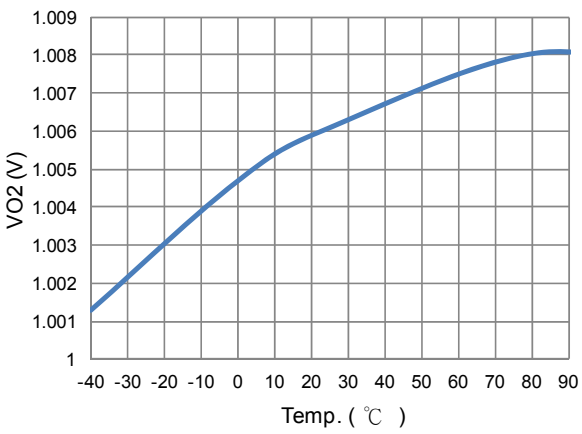


Typical Performance Characteristics (Continued)

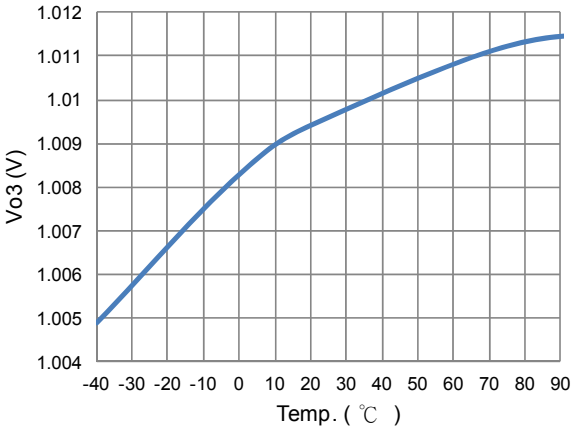
VO1 vs Temp.



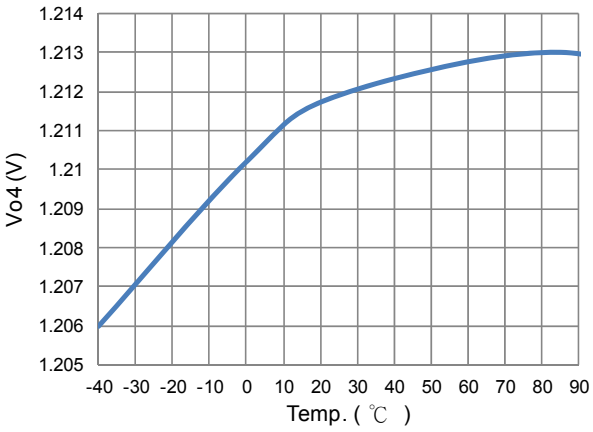
VO2 vs Temp.



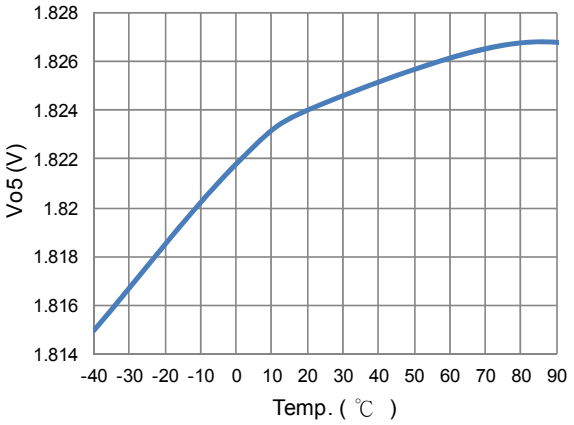
VO3 vs Temp.



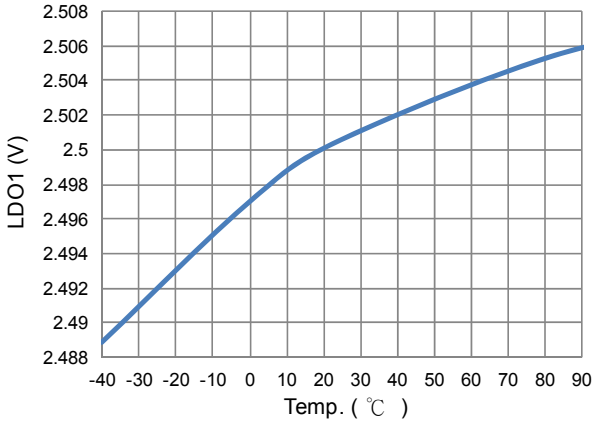
VO4 vs Temp.



VO4 vs Temp.



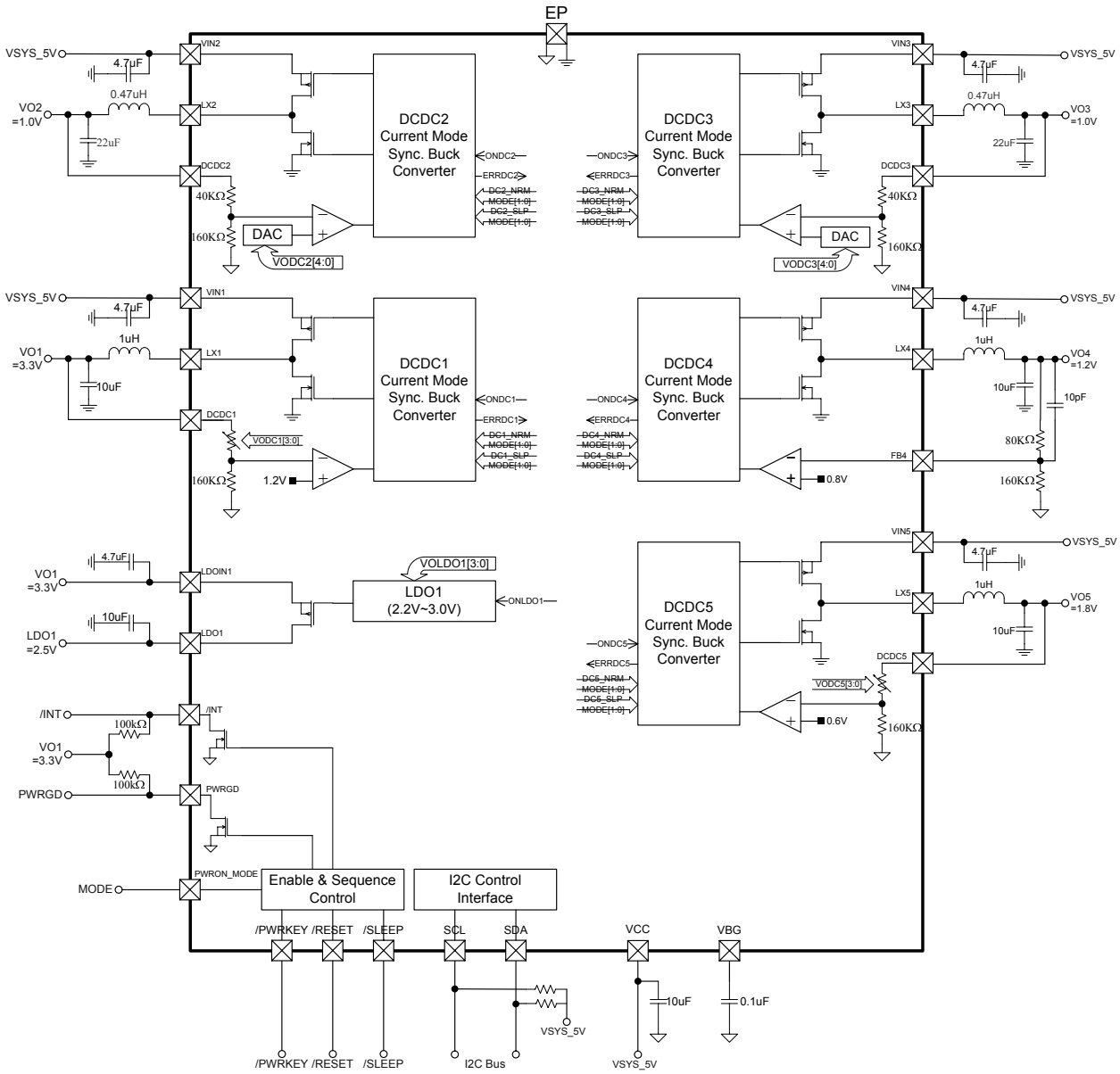
LDO1 vs Temp.



Pin Description

Pin No	Pin Name	Function
1	NC	No Connection
2	NC	No Connection
3	VCC	IC Power Supply Input pin. Bypass with a 10uF or greater ceramic capacitor.
4	LDO1	LDO Output of LDO1.
5	LDOIN1	Power Input of LDO1.
6	VBG	1.23v Reference Voltage Output. Bypass this pin to ground with a 0.1μF ceramic capacitor.
7	/INT	Interrupt Indicator with open drain output.
8	NC	No Connection
9	LX2	Inductor switch node of DCDC2 Buck Converter.
10	LX2	Inductor switch node of DCDC2 Buck Converter.
11	VIN2	Power Input of DCDC2 Buck Converter.
12	DCDC2	Sensing Input of DCDC2 Buck Converter's output voltage.
13	/PWRKEY	Power on/off key. Internal pull high to VCC.
14	DCDC1	Sensing Input of DCDC1 Buck Converter's output voltage.
15	VIN1	Power Input of DCDC1 Buck Converter.
16	LX1	Inductor switch node of DCDC1 Buck Converter.
17	MODE	Power ON/OFF Mode Select Pin.
18	FB4	Feedback Input of DCDC4 Buck Converter.
19	/RESET	RESET PIN of G2237. Internal pull high to VCC.
20	VIN4	Power Input of DCDC4 Buck Converter.
21	LX4	Inductor switch node of DCDC4 Buck Converter.
22	/SLEEP	SLEEP mode control pin. Internal pull high to VCC.
23	SDA	Data Input PIN of I^2C interface.
24	SCL	Clock Input PIN of I^2C interface.
25	LX5	Inductor switch node of DCDC5 Buck Converter.
26	VIN5	Power Input of DCDC5 Buck Converter.
27	DCDC5	Sensing Input of DCDC5 Buck Converter's output voltage.
28	PWRGD	Indicator of PMU power on/off with open drain output.
29	DCDC3	Sensing Input of DCDC3 Buck Converter's output voltage.
30	VIN3	Power Input of DCDC3 Buck Converter.
31	LX3	Inductor switch node of DCDC3 Buck Converter.
32	LX3	Inductor switch node of DCDC3 Buck Converter.
EP	VSSA, VSSD, PGNDX	All converters' power ground and chip analog ground. For good thermal dissipation, connect EP to the power and analog ground plane.

Block Diagram & Application Circuit



I2C Interface

G2237 I2C slave address=7'b0010010. The write or read bit stream (N≥1) is shown below:

Driven by Master

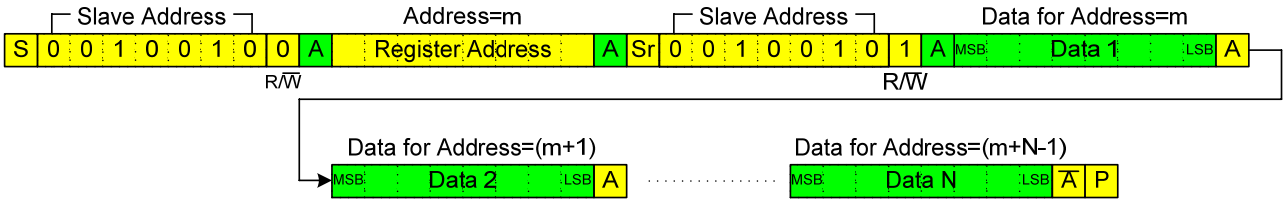
Driven by G2237

S Start

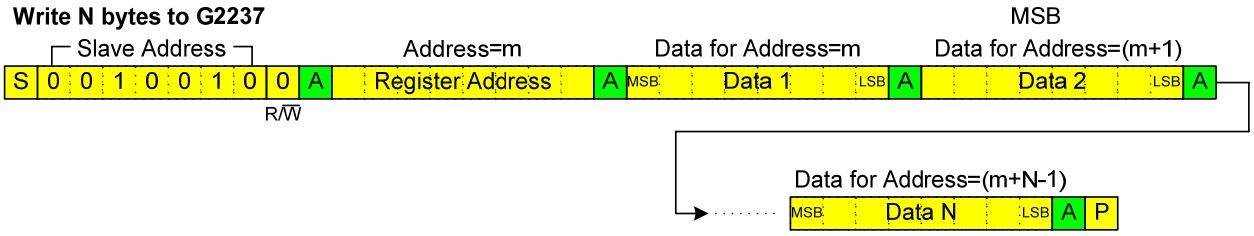
P Stop

Sr Repeat Start

Read N bytes from G2237



Write N bytes to G2237



I2C Register Map

ADDR	Byte Name		Data							
			b7	b6	b5	b4	b3	b2	b1	b0
0x00	INTR	Meaning	INT		PWRKEY	PWRKEY_LP	PWRKEY_IT			
		Default	0		0	0	0			
		Read/Write	R/W		R	R	R			
0x01	INTR _MASK	Meaning			MASK _PWRKEY	MASK_LP	MASK_IT			
		Default			0	0	0			
		Read/Write			R/W	R/W	R/W			
0x02	PWRKEY CONTROL	Meaning	LPOFF_TO_ DO	ENLPOFF	TIME_IT[1:0]		TIME_LP[1:0]		TIME_LPOFF[1:0]	
		Default	1	1	0	0	0	1	1	1
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0x03	DCDC Fault Status	Meaning	ERRDC1	ERRDC2	ERRDC3	ERRDC4	ERRDC5			ERRLDO1
		Default	0	0	0	0	0			0
		Read/Write	R	R	R	R	R			R
0x04	SYS _Control	Meaning	SOFTOFF		RST_ERR					
		Default	0		0					
		Read/Write	R/W		R/W					
0x05	DCDC _ONOFF CONTROL	Meaning	ONDC1	ONDC2	ONDC3	ONDC4	ONDC5			ONLDO1
		Default	1	1	1	1	1			1
		Read/Write	R/W	R/W	R/W	R/W	R/W			R/W
0x06	DCDC _DISCHG CONTROL	Meaning	ENDIS_DC1	ENDIS_DC2	ENDIS_DC3	ENDIS_DC4	ENDIS_DC5			ENDIS_L1
		Default	1	1	1	1	1			1
		Read/Write	R/W	R/W	R/W	R/W	R/W			R/W
0x07	DC1DC2 _MODE CONTROL	Meaning	DC1_NRMMODE[1:0]		DC1_SLPMODE[1:0]		DC2_NRMMODE[1:0]		DC2_SLPMODE[1:0]	
		Default	0	0	1	0	0	0	1	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0x08	DC3DC4 _MODE CONTROL	Meaning	DC3_NRMMODE[1:0]		DC3_SLPMODE[1:0]		DC4_NRMMODE[1:0]		DC4_SLPMODE[1:0]	
		Default	0	0	1	0	0	0	1	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0x09	DC5LDO1 _MODE CONTROL	Meaning	DC5_NRMMODE[1:0]		DC5_SLPMODE[1:0]		LDO1_NRMMODE[1:0]		LDO1_SLPMODE[1:0]	
		Default	0	0	1	0	0	0	1	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0x0A	DCDC1 _NRMVOLT	Meaning					VODC1_NRM[3:0]			
		Default					1	0	1	1
		Read/Write					R/W	R/W	R/W	R/W
0x0B	DCDC2 _NRMVOLT	Meaning				VODC2_NRM[4:0]				
		Default				1	0	0	0	0
		Read/Write				R/W	R/W	R/W	R/W	R/W
0x0C	DCDC3 _NRMVOLT	Meaning				VODC3_NRM[4:0]				
		Default				1	0	0	0	0
		Read/Write				R/W	R/W	R/W	R/W	R/W
0x0D	DCDC5 _NRMVOLT	Meaning					VODC5_NRM[3:0]			
		Default					1	1	0	0
		Read/Write					R/W	R/W	R/W	R/W
0x0E	LDO1 _NRMVOLT	Meaning					VOLDO1_NRM[3:0]			
		Default					0	0	1	1
		Read/Write					R/W	R/W	R/W	R/W
0x0F	DCDC1 _SLPVOLT	Meaning					VODC1_SLP[3:0]			
		Default					1	0	1	1
		Read/Write					R/W	R/W	R/W	R/W
0x10	DCDC2 _SLPVOLT	Meaning				VODC2_SLP[4:0]				
		Default				1	0	0	0	0
		Read/Write				R/W	R/W	R/W	R/W	R/W
0x11	DCDC3 _SLPVOLT	Meaning				VODC3_SLP[4:0]				
		Default				1	0	0	0	0
		Read/Write				R/W	R/W	R/W	R/W	R/W
0x12	DCDC5 _SLPVOLT	Meaning					VODC5_SLP[3:0]			
		Default					1	1	0	0
		Read/Write					R/W	R/W	R/W	R/W
0x13	LDO1 _SLPVOLT	Meaning					VOLDO1_SLP[3:0]			
		Default					0	0	1	1
		Read/Write					R/W	R/W	R/W	R/W
0x14	CHIP_ID	Meaning			CHIP_ID[5:0]					
		Default			1	0	0	1	0	1
		Read/Write			R	R	R	R	R	R
0x15	VERSION	Meaning					VERSION[3:0]			
		Default					0	0	0	0
		Read/Write					R	R	R	R
0xF1	GMT Testing	Meaning				TM[5:1]				
		Default				0	0	0	0	0
		Read/Write				R/W	R/W	R/W	R/W	R/W

I2C Register Reset Conditions

ADDR.	Register Function	Rest Condition
0x00	Interrupt Registers	VCC<3.0V, or the power-off reset pulse. Also reset by reading them
0x02	Power-key IT/LP/LPOFF Registers	VCC<3.0V, or the power-on leading pulse
0x03, 0x04[5]	DCDC&LDO Fault Status	VCC<3.0V or 0x04[5] is written to 1
0x04[7]	SOFTOFF	VCC<3.0V, or the power-on leading pulse
0x06	DCDC and LDO enable discharge Registers	VCC<3.0V, or the power-on leading pulse
Other Registers		VCC<3.0V, or the power-off reset pulse.

I2C Register Function Table

Interrupt and Status

ADDR	Data Bit	Data Name	Function Description
0x00	b7	INT	INT is used to control the output status of /INT pin. When interrupt events happen, /INT pin goes low and this bit is set to 1'b1. After Micro-processor write the bit to be 1'b0, /INT pin goes to high-Z state. INT: 0 = Hi-Z; 1 = Low
0x00	b5	PWRKEY	PWRKEY is used to record the /PWRKEY pin status has changed since last read.
0x00	b4	PWRKEY_LP	PWRKEY_LP is used to record the /PWRKEY pin long press status. PWRKEY_LP is reset to 0 when this byte is read each time. This bit is also reset to 0 at each /PWRKEY pin falling edge or VCC plug-in/out. PWRKEY_LP: 0 = NO; 1 = YES ($T>T_{dPWRKEYLP}$)
0x00	b3	PWRKEY_IT	PWRKEY_IT is used to record the /PWRKEY pin falling status. PWRKEY_IT is reset to 0 when this byte is read each time. This bit is reset to 0 at each /PWRKEY pin falling edge or VCC plug-in/out. PWRKEY_IT: 0 = NO; 1 = YES ($T>T_{dbPWRKEYF}$)
0x01	b5	MASK _PWRKEY	By writing 1'b1 to MASK_PWRKEY to disable asserting /INT low when the event of /PWRKEY pin is toggled low occurs.
0x01	b4	MASK_LP	By writing 1'b1 to MASK_LP to disable asserting /INT low when the event of /PWRKEY pin is toggled low with duration longer than TdPWRKEYLP occurs.
0x01	b3	MASK_IT	By writing 1'b1 to MASK_IT to disable asserting /INT low when the event of /PWRKEY pin is toggled low duration longer than TdbPWRKEYF occurs.

Software PMIC ON/OFF Control

ADDR	Data Bit	Data Name	Function Description
0x04	b7	SOFTOFF	Write 1 to SOFTOFF to perform power-off sequence when PMIC is in operation mode.

Power-Key Function and Timing Control

ADDR	Data Bit	Data Name	Function Description
0x02	b7	LPOFF_TO_DO	Setting PMIC operating mode after it finishes power-off sequence caused by /PWRKEY pin long pressed with duration longer than $T_{dPWRKEYLPOFF}$. Default=1'b1 LPOFF_TO_DO: 0 = Remain in shutdown mode; ***1*** = ***Re-startup by sequence***
0x02	b6	ENLPOFF	Enable PMIC shutdown when /PWRKEY pin long pressed with duration longer than $T_{dPWRKEYLPOFF}$ defined by register TIME_LPOFF[1:0]. Default=1'b1 $T>T_{dPWRKEYLPOFF}$: 0 = NO; ***1*** = ***YES***
0x02	b5,b4	TIME_IT [1:0]	TIME_IT[1:0] is used to defined the /PWRKEY pin falling-edge de-bouncing delay time $T_{dbPWRKEYF}$. When /PWRKEY pin is toggled low with duration longer than $T_{dbPWRKEYF}$, PMIC enters power-on process and the register PWRKEY_IT is 1'b1. Default=2'b00 TIME_IT[1:0]: ***00*** = $T_{dbPWRKEYF}$ ***128mS***; 01 = 0.5S; 10 = 1.0S; 11 = 1.5S
0x02	b3,b2	TIME_LP [1:0]	TIME_LP[1:0] is used to defined the /PWRKEY pin long-press delay time $T_{dPWRKEYLP}$. When /PWRKEY pin is toggled low with duration longer than $T_{dPWRKEYLP}$, the register PWRKEY_LP is 1'b1. Default=2'b01 TIME_LP[1:0]: 00 = 1.0S; ***01*** = ***2.0S***; 10 = 3.0S; 11 = 4.0S
0x02	b1,b0	TIME_LPOFF [1:0]	TIME_LPOFF[1:0] is used to defined the /PWRKEY pin long-press delay time $T_{dPWRKEYLPOFF}$. When /PWRKEY pin is toggled low with duration longer than $T_{dPWRKEYLPOFF}$, PMIC enters power-off process, and the register PWRKEY_LPOFF is 1'b1. The function of /PWRKEY pin long-press delay to turn off PMIC can be inactive by writing 0 to the register ENLPOFF. Default=2'b11 TIME_LPOFF[1:0]: 00 = 6.0S; 01 = 7.0S; 10 = 8.0S; ***11*** = ***10.0S***

Fault Status of DCDC Converters and LDOs

ADDR	Data Bit	Data Name	Function Description
0x03	b7~b3	ERRDCX	Record whether the UVP protection of DCDC1~DCDC5 ever occurs respectively. ERRDCx: 0 = NO; 1 = YES
0x03	b0	ERRLDO1	Record whether the UVP protection of LDO1 ever occurs respectively. ERRLDOx: 0 = NO; 1 = YES
0x04	b5	RST_ERR	Write 1 to this bit to reset 0x03 to 0.

ON/OFF Control of DCDC Converters and LDOs

ADDR	Data Bit	Data Name	Function Description
0x05	b7~ b3	ONDCx	DCDC1~DCDC5 Enable Signal. ONDCx: 0 = Shutdown; ***1*** = ***Operation***
0x05	b0	ONLDO1	LDO1 Enable Signal. ONLDOx: 0 = Shutdown; ***1*** = ***Operation***

Discharge Function of DCDC Converters and LDOs

ADDR	Data Bit	Data Name	Function Description
0x06	b7~ b3	ENDIS_DCx	Enable DCDC output discharge function during PMIC in shutdown mode. Default=1'b1 DCDC converter still has discharge function during power-off procedure even this bit is written to 0 ENDIS_DCx: 0 = Disable; ***1*** = ***Enable***
0x06	b0	ENDIS_L1	Enable LDO output discharge function. Default=1'b1 ENDIS_L1: 0 = Disable; ***1*** = ***Enable***

Mode Control of DCDC1~DCDC5

ADDR	Data Bit	Data Name	Function Description
0x07 0x08 0x09	b7,b6 b3,b2	DCx _NRMMODE [1:0]	Setting the operating mode of DCDC1~DCDC5 when /SLEEP pin is toggled high. Default=2'b00 DCx_NRMMODE[1:0]: ***00*** = ***Auto PWM/PSM with ECO***; 01 = ***Auto PWM/PSM with ECO***; 10 = Force PWM; 11 = Auto PWM/PSM w/o ECO
0x07 0x08 0x09	b5,b4 b1,b0	DC1~3, DC5 _SLPMODE [1:0]	Setting the DCDC1, DCDC2, DCDC3, and DCDC5s' operating mode, and output voltage configuration when /SLEEP pin is toggled low. Default=2'b10 DCx_SLPMODE[1:0]: 00 = Auto PWM/PSM w/o ECO, VODCx_NRM[x:0]; 01 = ***Auto PWM/PSM with ECO***, VODCx_NRM[x:0]; ***10*** = ***Auto PWM/PSM with ECO***, ***VODCx_SLP[x:0]***; 11 = shutdown, X
0x08	b1,b0	DC4 _SLPMODE [1:0]	Setting the operating mode of DCDC4 when /SLEEP pin is toggled low. Default=2'b10 DC4_SLPMODE[1:0]: 00 = Auto PWM/PSM w/o ECO; 01 = ***Auto PWM/PSM with ECO***; ***10*** = ***Auto PWM/PSM with ECO***; 11 = shutdown

Mode Control of LDO1

<table>
<tr><th>ADDR</th><th>Data Bit</th><th>Data Name</th><th>Function Description</th></tr>
<tr><td>0x09</td><td>b3,b2</td><td>LDO1
_NRMMODE
[1:0]</td><td>Setting the LDO1 operating mode and output voltage when /SLEEP pin is toggled high.
Default=2’b00
<table>
<tr><th>LDOx_NRMMODE[1:0]</th><th>MODE</th><th>Output Voltage</th></tr>
<tr><td>00</td><td rowspan="2">Normal</td><td rowspan="2">VOLDOx_NRM [3:0]</td></tr>
<tr><td>01</td></tr>
<tr><td>10</td><td>ECO</td><td>VOLDOx_NRM[3:0]</td></tr>
<tr><td>11</td><td>Normal</td><td>VOLDOx_NRM [3:0]</td></tr>
</table></td></tr>
<tr><td>0x09</td><td>b1,b0</td><td>LDO1
_SLPMODE
[1:0]</td><td>Setting the LDO1 operating mode and output voltage when /SLEEP pin is toggled low,
Default=2’b10
<table>
<tr><th>LDOx_SLPMODE[1:0]</th><th>MODE</th><th>Output Voltage</th></tr>
<tr><td>00</td><td>Normal</td><td>VOLDOx_NRM [3:0]</td></tr>
<tr><td>01</td><td>Normal</td><td>VOLDOx_SLP [3:0]</td></tr>
<tr><td>10</td><td>ECO</td><td>VOLDOx_SLP[3:0]</td></tr>
<tr><td>11</td><td>Shutdown</td><td>X</td></tr>
</table></td></tr>
</table>

Voltage Control of LDO1

<table>
<tr><th>ADDR</th><th>Data Bit</th><th>Data Name</th><th>Function Description</th></tr>
<tr><td>0x0E
0x13</td><td>b3~b0</td><td>VOLDO1
_NRM[3:0]
/VOLDO1
_SLP[3:0]</td><td>Setting the output voltage of LDO1,
VOLDO1_NRM/VOLDO1_SLP Default=4’b0011
<table>
<tr><th>VOLDO2_
[3:0]</th><th>LDO2</th><th>VOLDO2_
[3:0]</th><th>LDO2</th><th>VOLDO2_
[3:0]</th><th>LDO2</th><th>VOLDO2_
[3:0]</th><th>LDO2</th></tr>
<tr><td>1111</td><td>3.0V</td><td>1011</td><td>3.0V</td><td>0111</td><td>2.9V</td><td>0011</td><td>2.5V</td></tr>
<tr><td>1110</td><td>3.0V</td><td>1010</td><td>3.0V</td><td>0110</td><td>2.8V</td><td>0010</td><td>2.4V</td></tr>
<tr><td>1101</td><td>3.0V</td><td>1001</td><td>3.0V</td><td>0101</td><td>2.7V</td><td>0001</td><td>2.3V</td></tr>
<tr><td>1100</td><td>3.0V</td><td>1000</td><td>3.0V</td><td>0100</td><td>2.6V</td><td>0000</td><td>2.2V</td></tr>
</table></td></tr>
</table>

Voltage Control of DCDC1~DCDC5

<table>
<tr><th>ADDR</th><th>Data Bit</th><th>Data Name</th><th>Function Description</th></tr>
<tr><td>0x0A
0x0F</td><td>b3~b0</td><td>VODC1
_NRM[3:0]
/VODC1
_SLP[3:0]</td><td>Setting the output voltage of DCDC1 in Normal/Sleep mode, Default=4’b1011
<table>
<tr><th>VODC1 [3:0]</th><th>VO1</th><th>VODC1 [3:0]</th><th>VO1</th><th>VODC1 [3:0]</th><th>VO1</th><th>VODC1 [3:0]</th><th>VO1</th></tr>
<tr><td>1111</td><td>3.7V</td><td>1011</td><td>3.3V</td><td>0111</td><td>2.9V</td><td>0011</td><td>2.5V</td></tr>
<tr><td>1110</td><td>3.6V</td><td>1010</td><td>3.2V</td><td>0110</td><td>2.8V</td><td>0010</td><td>2.4V</td></tr>
<tr><td>1101</td><td>3.5V</td><td>1001</td><td>3.1V</td><td>0101</td><td>2.7V</td><td>0001</td><td>2.3V</td></tr>
<tr><td>1100</td><td>3.4V</td><td>1000</td><td>3.0V</td><td>0100</td><td>2.6V</td><td>0000</td><td>2.2V</td></tr>
</table></td></tr>
<tr><td>0x0B
0x0C
0x10
0x11</td><td>b4~b0</td><td>VODCx
_NRM[4:0]
/VODCx
_SLP[4:0]</td><td>Setting the feedback reference voltage of DCDC2, and DCDC3 in Normal/Sleep mode.
VOx=VFBx/0.8, Default=5’b10000
VFBx=0.64V + 10mV x Value, VOx=0.8V + 12.5mV x Value, where Value is 5-bit binary code
<table>
<tr><th>FBDCX[4:0]</th><th>VFBX</th><th>VOX</th><th>FBDCX[4:0]</th><th>VFBX</th><th>VOX</th></tr>
<tr><td>11111</td><td>0.95V</td><td>1.1875V</td><td>01111</td><td>0.79V</td><td>0.9875V</td></tr>
<tr><td>11110</td><td>0.94V</td><td>1.1750V</td><td>01110</td><td>0.78V</td><td>0.9750V</td></tr>
<tr><td>11101</td><td>0.93V</td><td>1.1625V</td><td>01101</td><td>0.77V</td><td>0.9625V</td></tr>
<tr><td>11100</td><td>0.92V</td><td>1.1500V</td><td>01100</td><td>0.76V</td><td>0.9500V</td></tr>
<tr><td>11011</td><td>0.91V</td><td>1.1375V</td><td>01011</td><td>0.75V</td><td>0.9375V</td></tr>
<tr><td>11010</td><td>0.90V</td><td>1.1250V</td><td>01010</td><td>0.74V</td><td>0.9250V</td></tr>
<tr><td>11001</td><td>0.89V</td><td>1.1125V</td><td>01001</td><td>0.73V</td><td>0.9125V</td></tr>
<tr><td>11000</td><td>0.88V</td><td>1.1000V</td><td>01000</td><td>0.72V</td><td>0.9000V</td></tr>
<tr><td>10111</td><td>0.87V</td><td>1.0875V</td><td>00111</td><td>0.71V</td><td>0.8875V</td></tr>
<tr><td>10110</td><td>0.86V</td><td>1.0750V</td><td>00110</td><td>0.70V</td><td>0.8750V</td></tr>
<tr><td>10101</td><td>0.85V</td><td>1.0625V</td><td>00101</td><td>0.69V</td><td>0.8625V</td></tr>
<tr><td>10100</td><td>0.84V</td><td>1.0500V</td><td>00100</td><td>0.68V</td><td>0.8500V</td></tr>
<tr><td>10011</td><td>0.83V</td><td>1.0375V</td><td>00011</td><td>0.67V</td><td>0.8375V</td></tr>
<tr><td>10010</td><td>0.82V</td><td>1.0250V</td><td>00010</td><td>0.66V</td><td>0.8250V</td></tr>
<tr><td>10001</td><td>0.81V</td><td>1.0125V</td><td>00001</td><td>0.65V</td><td>0.8125V</td></tr>
<tr><td>10000</td><td>0.80V</td><td>1.0000V</td><td>00000</td><td>0.64V</td><td>0.8000V</td></tr>
</table></td></tr>
<tr><td>0x0D
0x12</td><td>b3~b0</td><td>VODC5
_NRM[3:0]
/VODC5
_SLP[3:0]</td><td>Setting the output voltage of DCDC5 in Normal/Sleep mode, Default=4’b1100
<table>
<tr><th>VODC7 [3:0]</th><th>VO7</th><th>VODC7 [3:0]</th><th>VO7</th><th>VODC7 [3:0]</th><th>VO7</th><th>VODC7 [3:0]</th><th>VO7</th></tr>
<tr><td>1111</td><td>2.5V</td><td>1011</td><td>1.7V</td><td>0111</td><td>1.2V</td><td>0011</td><td>0.95V</td></tr>
<tr><td>1110</td><td>2.0V</td><td>1010</td><td>1.6V</td><td>0110</td><td>1.1V</td><td>0010</td><td>0.90V</td></tr>
<tr><td>1101</td><td>1.9V</td><td>1001</td><td>1.5V</td><td>0101</td><td>1.05V</td><td>0001</td><td>0.85V</td></tr>
<tr><td>1100</td><td>1.8V</td><td>1000</td><td>1.3V</td><td>0100</td><td>1.0V</td><td>0000</td><td>0.80V</td></tr>
</table></td></tr>
</table>

Version Code of G2237

ADDR	Data Bit	Data Name	Function Description
0x14	b5~b0	CHIP_ID [5:0]	CHIP_ID[5:0] is the identification code of G2237, code=6’b100101
0x15	b3~b0	VERSION [3:0]	VERSION[3:0] is the version code of G2237

FUNCTION DESCRIPTION

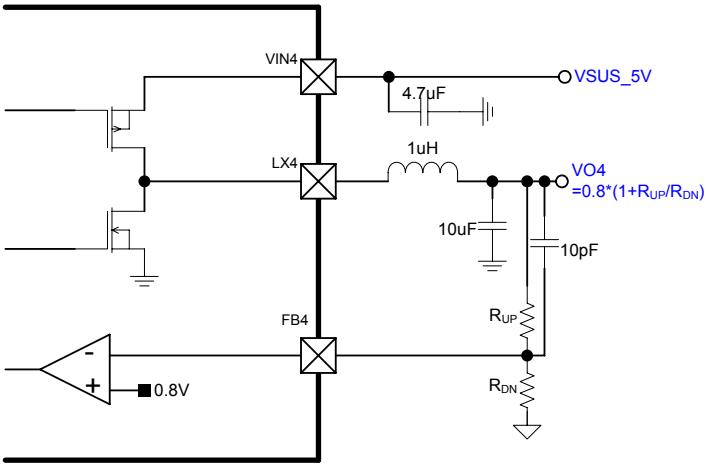
PMU

The G2237 includes 5 DC/DC Converters, and 1 LDO regulator to generate a multiple-output power-supply system.

	Topology	Default V_{OUT}	V_{OUT} range	Current rating	ON/OFF Control
DCDC1	3MHz Sync. Buck Converter	3.3V	16-steps voltages from 2.2v to 3.7v configured by I^2C	2.0A	Controlled by register bit ONDC1
DCDC2	3MHz Sync. Buck Converter	1.0V	32-steps DVS from 0.8v to 1.1875v configured by I^2C	3.0A	Controlled by register bit ONDC2
DCDC3	3MHz Sync. Buck Converter	1.0V	32-steps DVS from 0.8v to 1.1875v configured by I^2C	3.0A	Controlled by register bit ONDC3
DCDC4	3MHz Sync. Buck Converter	1.2V	Configured by FB4 pin resistors.	2.0A	Controlled by register bit ONDC4
DCDC5	3MHz Sync. Buck Converter	1.8V	16-steps voltages from 0.8v to 2.5v configured by I^2C	2.0A	Controlled by register bit ONDC5
LDO1	PMOS LDO	2.5V	16-steps voltages from 2.2v to 3.0v configured by I^2C	600mA	Controlled by register bit ONLDO1

DCDC4 Output Voltage Setting

The output voltage of DCDC4 is decided according to the resistor R_{UP} connecting between FB4 to converter's output voltage, and the resistor R_{DN} connecting between FB4 to ground. The suggesting resistance of R_{DN} is 160kΩ.



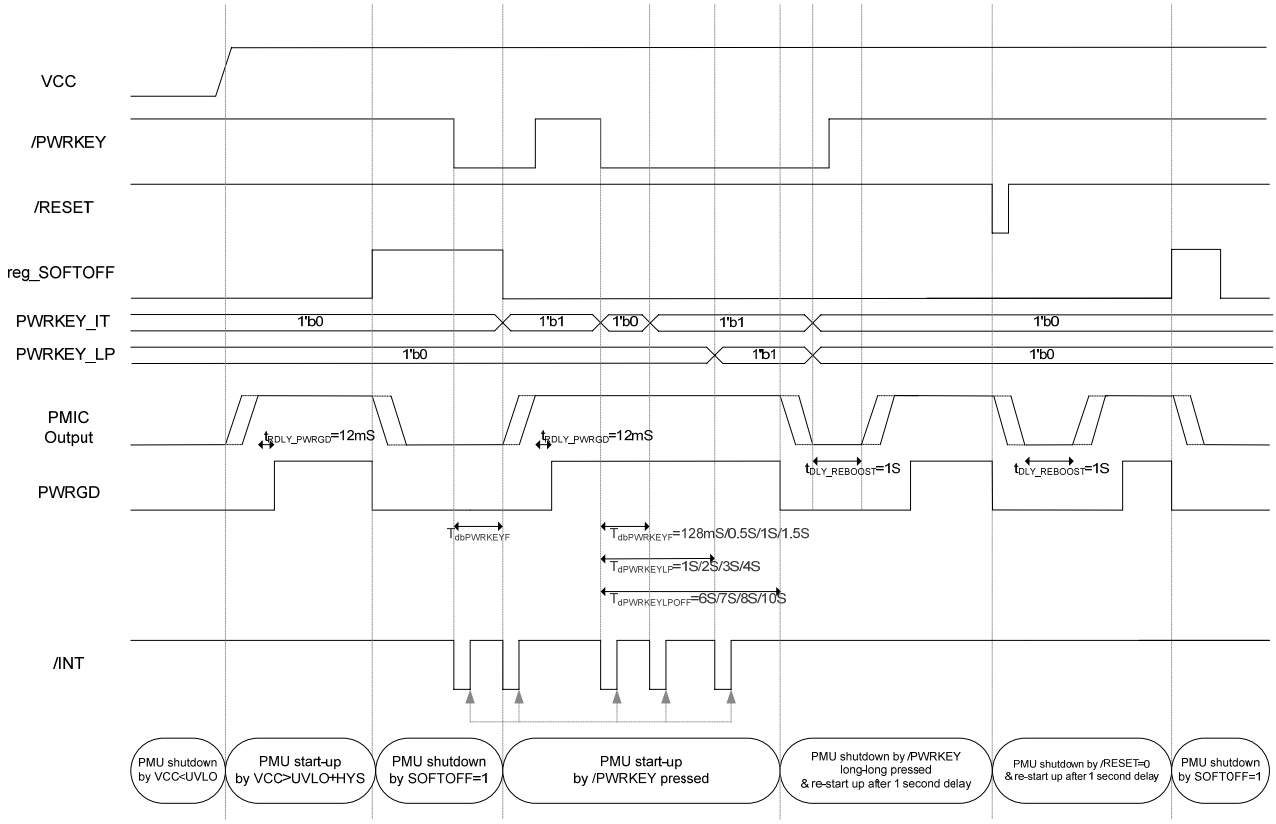
PMU Power ON/OFF Initiation (MODE=0)

The following conditions are available to turn on the PMU of G2237:

- /PWRKEY pin is low-level pressed with duration longer than $T_{dbPWRKEYF}$
- After 1 second delay from shutdown of G2237 caused by /PWRKEY pin is long-long pressed with duration longer than $T_{dPWRKEYLPOFF,}$ and register ENLPOFF=1'b1, LPOFF_TO_DO=1'b1.
- After 1 second delay from shutdown of G2237 caused by toggling /RESET pin low.
- The voltage applied in VCC pin is higher than $V_{VCC\_UVLO}+V_{VCC\_UVLOHYS}$ (3.5V typ.)

The following conditions are available to turn off the PMU of G2237:

- /PWRKEY pin is low-level pressed with duration longer than $T_{dPWRKEYLPOFF}$ (if ENLPOFF=1'b1)
- Write 1 to register SOFTOFF after PWRGD is turned high.
- /RESET pin is toggle low.
- Output voltage UVP of DCDC converters occurs with duration longer than 128mS
- G2237 thermal shutdown occurs.



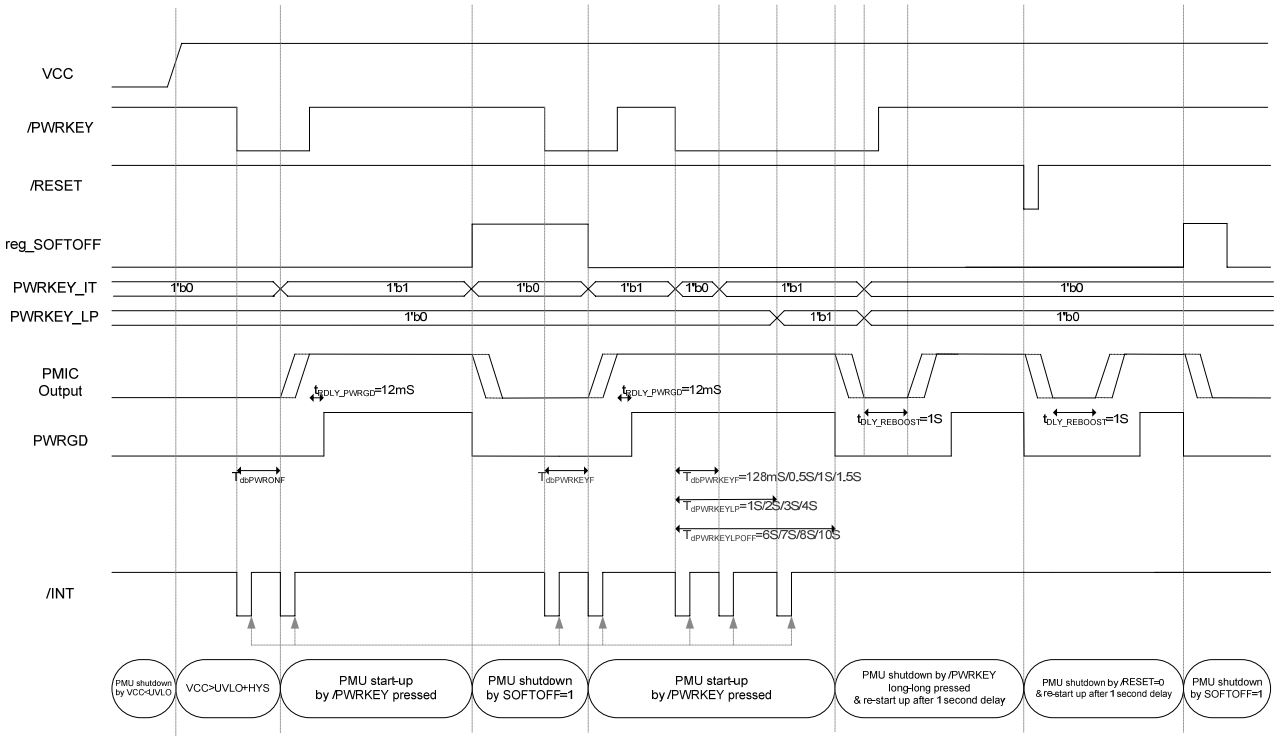
PMU Power ON/OFF Initiation (MODE=FLOATING)

The following conditions are available to turn on the PMU of G2237:

- /PWRKEY pin is low-level pressed with duration longer than $T_{dbPWRKEYF}$
- After 1 second delay from shutdown of G2237 caused by /PWRKEY pin is long-long pressed with duration longer than $T_{dPWRKEYLPOFF,}$ and register ENLPOFF=1'b1, LPOFF_TO_DO=1'b1.
- After 1 second delay from shutdown of G2237 caused by toggling /RESET pin low.

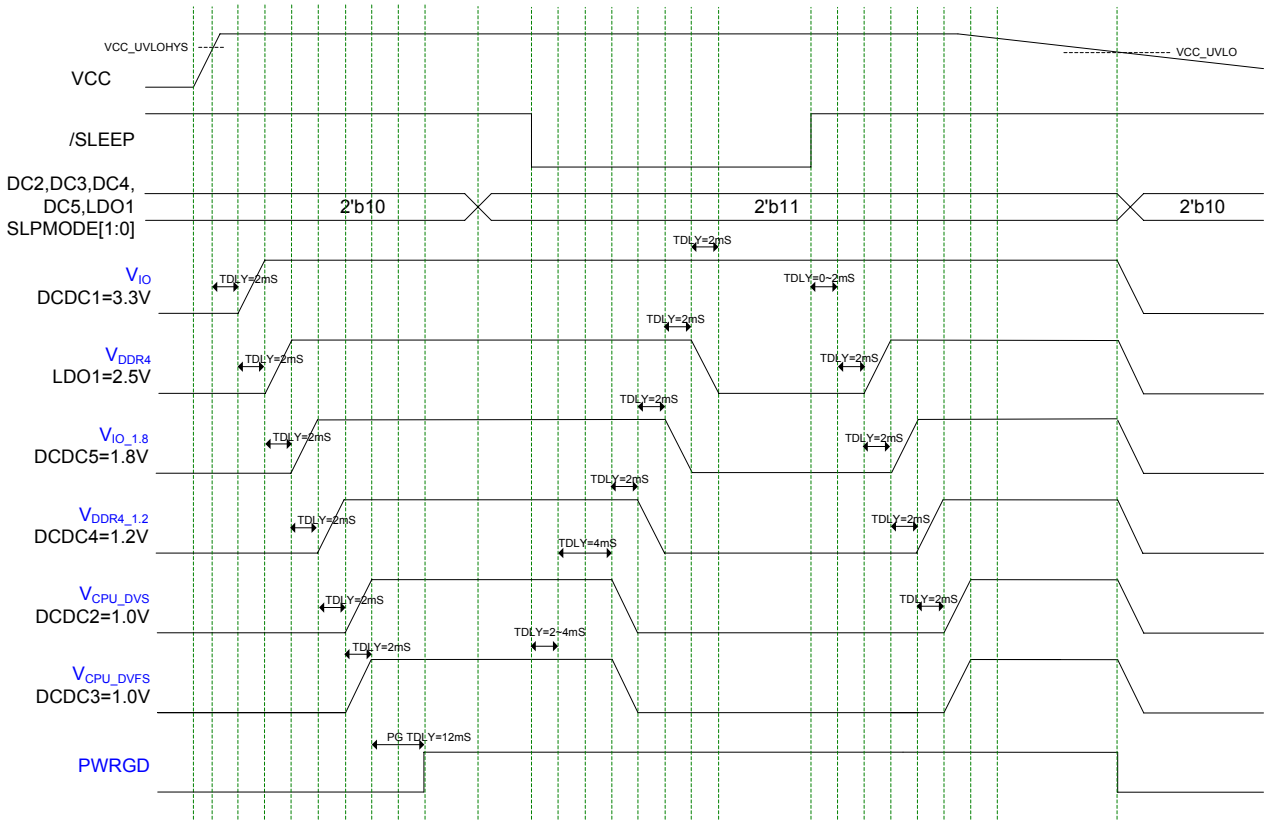
The following conditions are available to turn off the PMU of G2237:

- /PWRKEY pin is low-level pressed with duration longer than $T_{dPWRKEYLPOFF}$ (if ENLPOFF=1'b1)
- Write 1 to register SOFTOFF after PWRGD is turned high.
- /RESET pin is toggle low.
- Output voltage UVP of DCDC converters occurs with duration longer than 128mS
- G2237 thermal shutdown occurs.



PMU Power ON/OFF Sequence

When the power on condition is met, these five DC/DC converters, and LDO1 start up in sequence. After these converters finish power on sequence, the open-drain output PWRGD is high with 12ms time delay from DCDC3 is power ready. When G2237 enter sleep mode controlled by toggling /SLEEP pin low, PWRGD pin keeps high, and all converters' on/off mode is according to the setting of SLPMODE[1:0].



PMU Fault Protection

G2237 PMU provides VCC over voltage protection, over-current protection, under-voltage protection, short-circuit protection, and thermal shutdown protection to achieve complete protection.

	Protection type	Threshold	Protection methods	Reset Method
VCC	OVP	VCC>6.0V	IC shutdown	Reset by the power- on/off initiation conditions
DCDC1 Buck	Current Limit	pMOS current>2.8A	pMOS Off, nMOS on	Automatic Reset at next cycle
	UVP	VOUT1<75%*$VOUT_{SET}$	IC shutdown if period above 128ms	Reset by the power- on/off initiation conditions
DCDC2 Buck	Current Limit	pMOS current>4.0A	pMOS Off, nMOS on	Automatic Reset at next cycle
	UVP	VOUT2< $VOUT_{SET}$-100mV	IC shutdown if period above 128ms	Reset by the power- on/off initiation conditions
DCDC3 Buck	Current Limit	pMOS current>4.0A	pMOS Off, nMOS on	Automatic Reset at next cycle
	UVP	VOUT3< $VOUT_{SET}$-100mV	IC shutdown if period above 128ms	Reset by the power- on/off initiation conditions
DCDC4 Buck	Current Limit	pMOS current>2.8A	pMOS Off, nMOS on	Automatic Reset at next cycle
	UVP	VOUT4<87.5%*$VOUT_{SET}$	IC shutdown if period above 128ms	Reset by the power- on/off initiation conditions
DCDC5 Buck	Current Limit	pMOS current>2.8A	pMOS Off, nMOS on	Automatic Reset at next cycle
	UVP	VOUT5<83%*$VOUT_{SET}$	IC shutdown if period above 128ms	Reset by the power- on/off initiation conditions
LDO1 LDO	Current Limit	pMOS current>600mA		pMOS current<450mA
	UVP	LDOO1<8.5%*$LDOO1_{SET}$	pMOS Off	Reset by the power- on/off initiation conditions, or I^2C ONLDO1 control
Thermal	TSD	Junction Temp. >150°C	IC shutdown	Reset by the power- on/off initiation conditions

Application Information

Inductor Selection

The inductor value is chosen based on the desired ripple current. Large value inductors lower ripple current. The ΔIL is inductor peak-to-peak ripple current:

$$\Delta I_L = \frac{V_{OUT}}{F_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

,where Fsw is switching frequency.

A good rule between physical size and efficiency is to allow the peak-to-peak ripple current equal to 30% of the maximum load current. The reasonable inductor current ripple is usually set as 20% to 50% of maximum output current. The DC current rating of the inductor should be at least equal to the maximum load current plus half the ripple current to prevent core saturation.

$$I_{L,MAX} = I_{LOAD,MAX} + \frac{\Delta I_L}{2}$$

Input Capacitor Selection

Because the input current to the step-down converter is discontinuous, a capacitor is required to supply the AC current to the converter to maintain the DC input voltage. To prevent large voltage transients, a low ESR capacitor sized for maximum RMS current must be used. The input capacitor is given by:

$$C_{IN,MIN} = \frac{I_{LOAD}}{F_{SW} \times \Delta V_{IN\_RIPPLE,MAX}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Output Capacitor Selection

The selection of COUT is driven by the required effective series resistance (ESR). Typically, once the ESR requirement for COUT has been met, the RMS current rating generally far exceeds the COUT requirement. The output ripple ΔVOUT is determined by:

$$\Delta V_{OUT} \cong \Delta I_L \times \left(R_{ESR} + \frac{1}{8 \times F_{SW} \times C_{OUT}}\right)$$

For a fixed output voltage, the output ripple is highest at maximum input voltage since ΔIL increase with input voltage.

Load Step Regulation

The max positive and negative steps in output load current, ∆Iout, cause maximum output capacitor voltage undershoots, ∆Vsag, and overshoots, ∆Vsoar, repsectively. They are limited by rate at which the output inductor can supply or remove the new load current after the step. The change in current due to the step is initially removed from or supplied to the output capacitor, until the inductor can fully supply the new load current. This is expressed in the equations below:

$$V_{SAG} = \frac{L \times \left(\Delta I_{LOAD}\right)^2}{2 \times C_{OUT} \times \left(V_{IN,MIN} \times D_{MAX} - V_{OUT}\right)}$$

$$V_{SOAR} = \frac{L \times \left(\Delta I_{LOAD}\right)^2}{2 \times C_{OUT} \times V_{OUT}}$$

Setting the DCDC4 Output Voltage

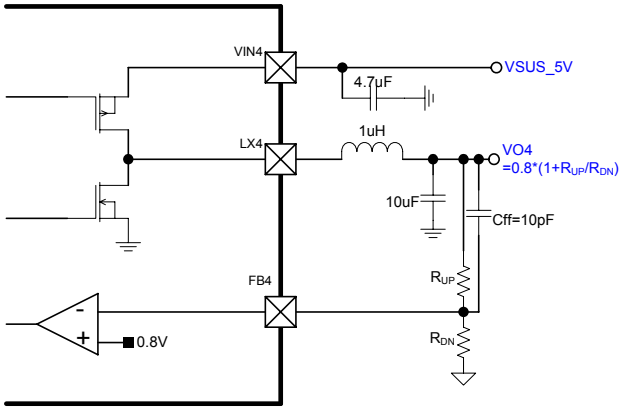
The output voltage of DCDC4 is set by a resistive divider according to the following formula:

$$V_{O4} = 0.8 \times \left(1 + \frac{R_{UP}}{R_{DN}}\right)$$

To optimize transient response, a Cff value is chosen such that the gain and phase boost of the feedback increases the bandwidth of the converter, while still maintaining an acceptable phase margin. Calculate the appropriate capacitor in parallel with the high-side feedback resistor (Rup) to achieve this:

$$C_{FF} = \frac{1}{2 \times \pi \times F_{Z,FF} \times R_{UP}}$$

The feedforward capacitor Cff provides an ac coupling path between VOUT and the FB pin which reduces the output ripple. It is highly recommended to keep the Cff value in the range of 10pF.



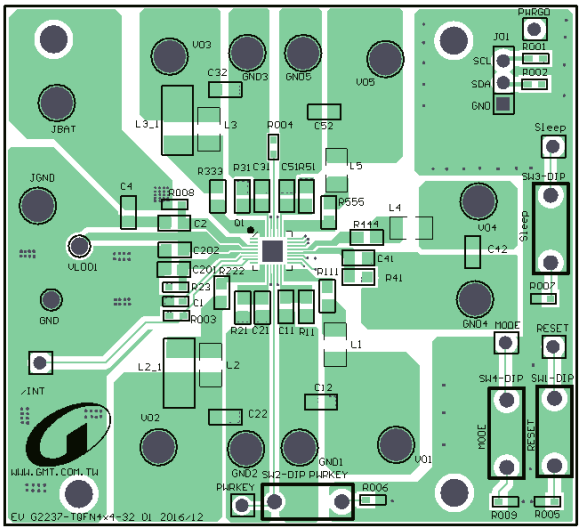
Layout guidelines

Careful printed circuit layout is extremely important to avoid causing parasitical capacitance and line inductance. The following layout guidelines are recommended to achieve optimum performance.

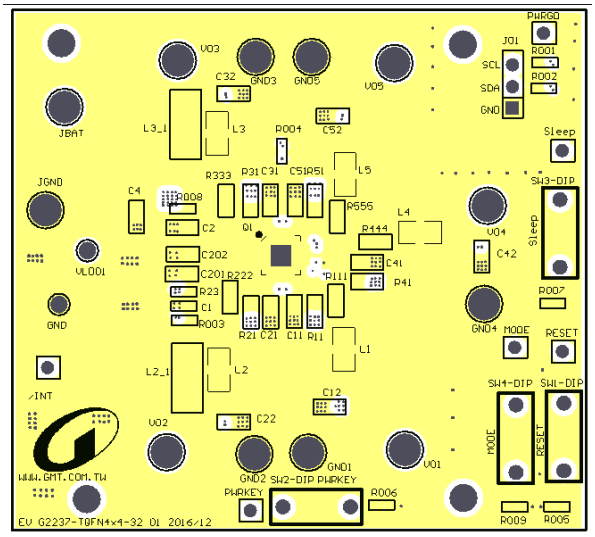
- Please the buck converter inductor close to the LX pin. Keep traces short, direct, and wide.
- Please ceramic bypass capacitors near the input/output pin.
- All feedback signal must first go through the regulator capacitors. Place feedback connection points near the output capacitors and minimize the control feedback loop as much as possible to achieve the best regulation performance.

EV Board PCB Layout Section

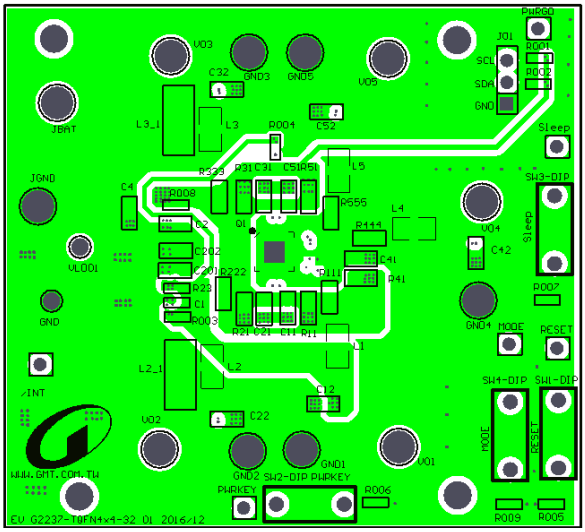
TOP view + TOP overlay



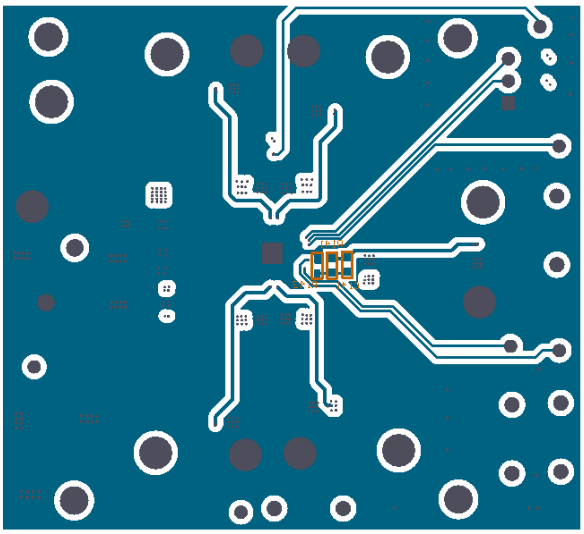
MidLayer1 view+ TOP overlay



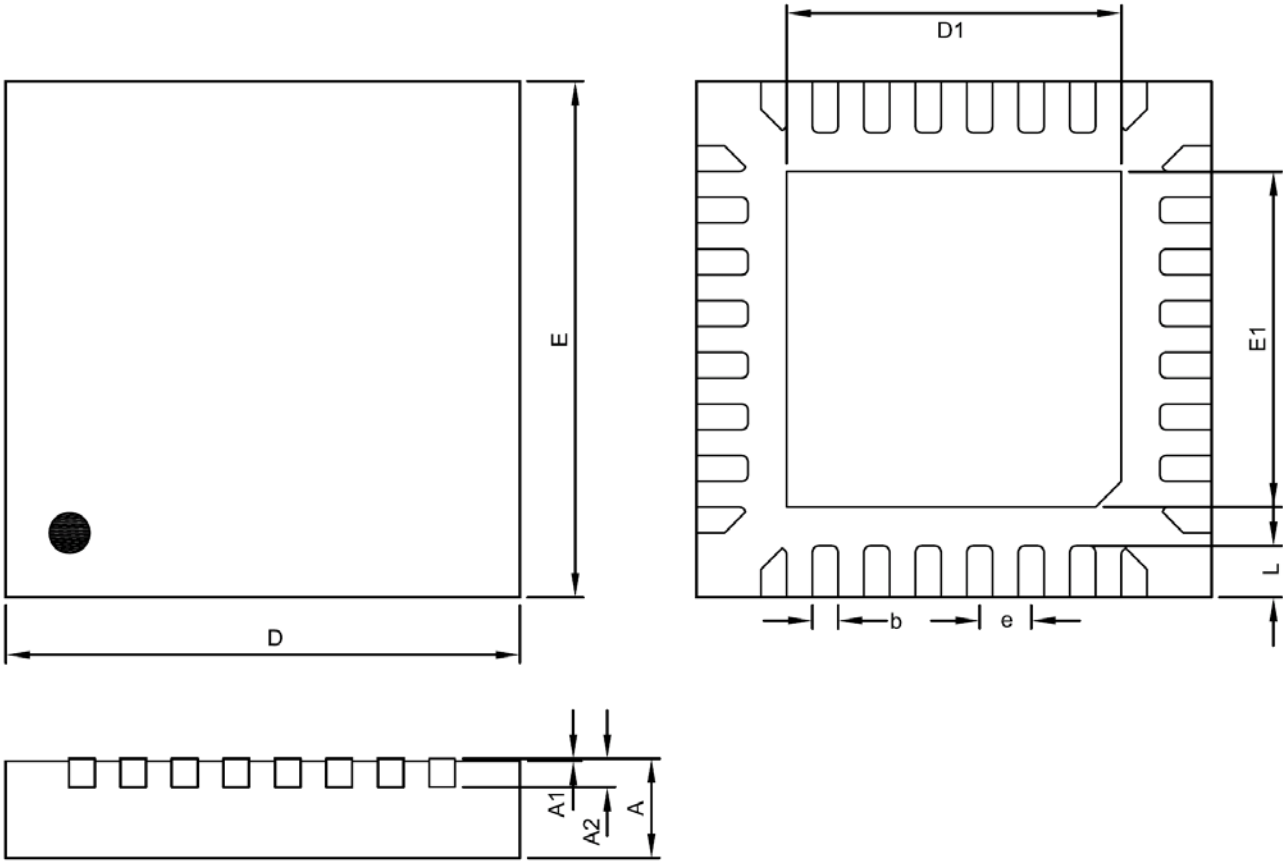
MidLayer2 view + TOP overlay



Bottom view + Bottom overlay



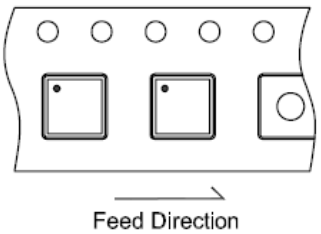
Package Information



TQFN4X4-32 Package

Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.0276	0.0295	0.0315
A1	0.00	- - -	0.05	0.0000	- - -	0.0020
A2	0.20 REF			0.0079 REF		
D	3.95	4.00	4.05	0.1555	0.1575	0.1594
E	3.95	4.00	4.05	0.1555	0.1575	0.1594
D1	2.65	2.70	2.75	0.1043	0.1063	0.1082
E1	2.65	2.70	2.75	0.1043	0.1063	0.1082
b	0.15	0.20	0.25	0.0059	0.0079	0.0098
e	0.40 BSC			0.0157 BSC		
L	0.25	0.30	0.35	0.0098	0.0118	0.0138

Taping Specification



PACKAGE	Q'TY/REEL
TQFN4X4-32	3,000 ea