

4A, 2.4MHz, COT Synchronous Step-Down Converter

Features

- Efficiency Up to 95%
- 31mΩ and 25mΩ Internal Power MOSFET
- V_{IN} Range 2.6V to 6V
- Adjustable Output Voltage from 0.8V to V_{IN}
- Power Save Mode for Light Load Efficiency
- Constant-On-Time Control Scheme Design for Fast Transient Response, Stability with MLCC Output Capacitor
- 100% Duty Cycle for Lowest Dropout
- 17uA Operating Quiescent Current
- Fixed Soft-Start 0.8ms
- Output Discharge
- Power Good Output
- Cycle-by-Cycle Over Current Protection
- Input Under Voltage Lockout
- Output Under Voltage Protection (Hiccup)
- Thermal Shutdown Protection

Applications

- Portable and Mobile Devices
- Wireless and Networking Devices
- LCD TV Power Supply
- Solid State Drive

Ordering Information

ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE (Green)	
G2275AM51U	2275	-40°C to +85°C	ADFN2X2-7	1: 0.85mm
G2275AM51D	2275	-40°C to +85°C	ADFN2X2-7	1: 0.85mm
G2275AM52U	275A	-40°C to +85°C	ADFN2X2-7	2: 0.35mm
G2275AM52D	275A	-40°C to +85°C	ADFN2X2-7	2: 0.35mm

Note: M5: ADFN2X2-7

1 & 2: Bonding Code

U & D: Tape & Reel

Green: Lead Free / Halogen Free

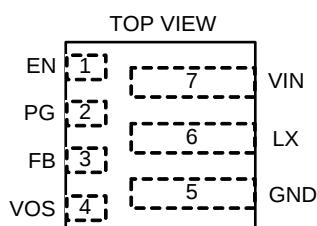
General Description

The G2275A is a monolithic, step-down, switch mode converter with built-in internal power MOSFETs. It achieves 4A continuous output current from a 2.6V to 6.0V input voltage with excellent load and line regulation. The Output voltage can be regulated to as low as 0.8V. At medium to heavy loads, the switching frequency is 2.4MHz. At light load, the device automatically enters PSM to maintain high efficiency.

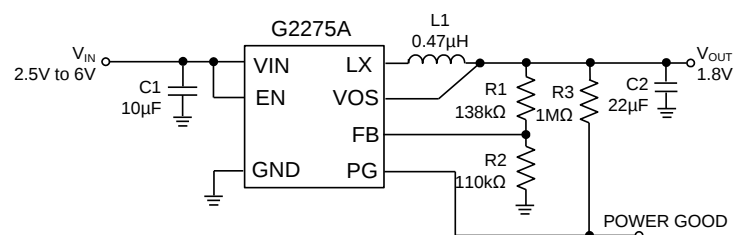
The Constant-On-Time control scheme in G2275A provides fast transient response to be optimized over a wide range of loads and output capacitors. Thermal shutdown and cycle-by-cycle current limiting are used for protection.

The G2275A is available in 0.35mm and 0.85mm thick ADFN2X2-7 packages.

Pin Configuration



Typical Application Circuit



Absolute Maximum Ratings

VIN, LX, FB -0.3V to 6V
 EN -0.3V to (VIN+0.3V)
 LX (AC, less than 10nS) -3V to 10V
 VIN-LX (AC, less than 10nS) -4V to 9V
 Thermal Resistance of Junction to Ambient, (θ_{JA})
 ADFN2X2-7. 65°C/W
 Continuous Power Dissipation ($T_A = +25^\circ\text{C}$)
 ADFN2X2-7. 2.1W
 Thermal Resistance of Junction to Ambient, (θ_{JC})
 ADFN2X2-7. 21°C/W

Junction Temperature -40°C to 150°C
 Storage Temperature -65°C to 150°C
 Reflow Temperature (soldering, 10sec) 260°C
 ESD (HBM) 2KV

Recommended Operating Conditions

Supply Input Voltage. 2.6V to 5.5V
 Ambient Temperature Range. -40°C to 85°C
 Junction Temperature Range. -40°C to 125°C

* : Please refer to EV Board PCB Layout Section

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(VIN=5V, TA=25°C)

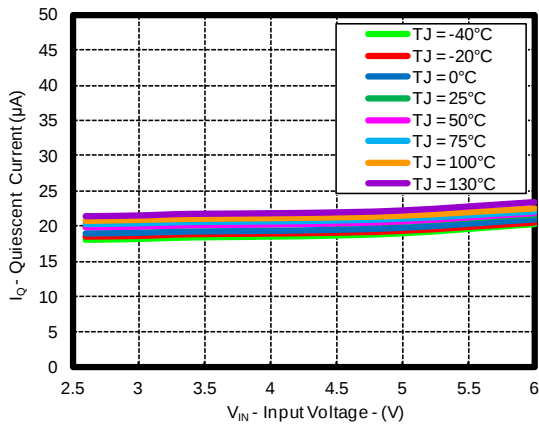
The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage	VIN		2.6	---	6	V
VIN Quiescent Current	IQ	No load, device not switching	12	17	27	μA
VIN Shutdown Current	ISD	VEN=0V, shutdown	0	---	1	μA
VIN Under Voltage Lock Out Threshold	VUVLO	VIN falling	2.3	2.4	2.45	V
VIN Under Voltage Lock Out Hysteresis	VUVLO_HYS		40	100	150	mV
Thermal Shutdown Threshold	TJSD	TJ rising	---	150	---	°C
Thermal Shutdown Hysteresis	TJSD_HYS		---	30	---	°C
EN Input Logic High Voltage	VIH	2.6V ≤ VIN ≤ 5.5V	1	---	---	V
EN Input Logic Low Voltage	VIL	2.6V ≤ VIN ≤ 5.5V	---	---	0.4	V
EN Input Current	IEN	VEN= High	---	---	0.1	μA
EN Pull Low Resistance	RPL_EN	VEN= Low	---	400	---	kΩ
Soft-Start Time	TSS	Time from EN high to 95% of VOUT nominal	0.55	0.8	1	mS
Power Good Threshold	VPGR	VOUT rising, referenced to VOUT nominal	90	95	99	%
	VPGHYST	VOUT falling hysteresis, referenced to VOUT nominal	3	5	10	%
PG Low-Level Output Voltage	VPGL	ISINK=1mA	---	---	0.4	V
PG Input Leakage Current	IPGLK	VPGL=5V	---	---	0.1	μA
Power Good Delay	tPG_DLY	VFB falling	20	40	80	μS
Feedback Reference Voltage	VREF	2.6V ≤ VIN ≤ 5.5V	0.792	0.8	0.808	V
Feedback Leakage Current	IFBLK	VFB = 1V	---	---	0.1	μA
Output discharge FET On-Resistance	RDIS	VEN=0V, VOUT=1.8V	---	260	---	Ω
PWM Switching Frequency	fSW	IOUT=1A	---	2.4	---	MHz
Minimum Off Time	tOFF(MIN)	High side PFET	---	80	---	nS
PFET Switch On Resistance	RDSON(P)	VIN=3.6V, ISW=500mA	---	31	47	mΩ
NFET Switch On Resistance	RDSON(N)	VIN=3.6V, ISW=500mA	---	25	40	mΩ
PFET Switch Current Limit	ILIM(P)		4.8	6.5	---	A
NFET Switch Current Limit	ILIM(N)		4	4.5	---	A

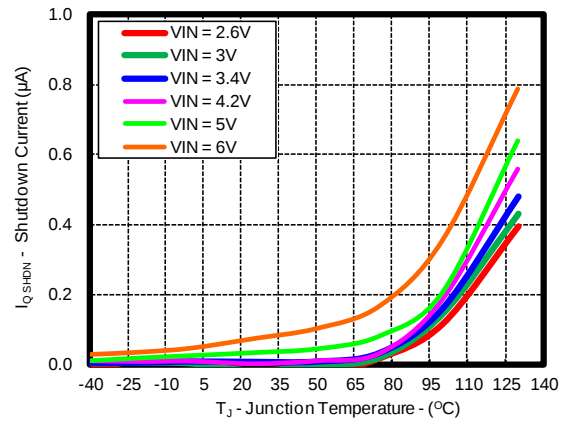
Typical Performance Characteristics

($V_{IN} = 5V$, $V_{OUT} = 1.8V$, $T_A = 25^\circ C$, unless otherwise noted.)

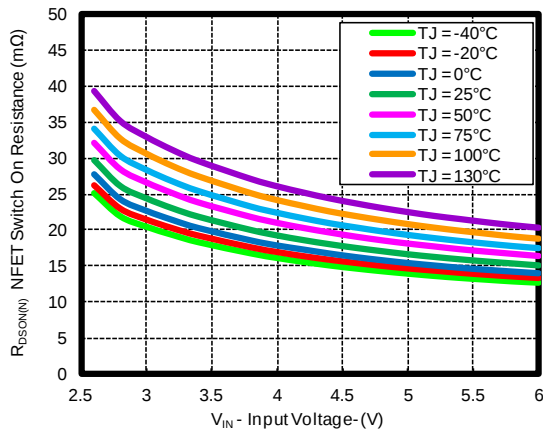
Quiescent Current vs Input Voltage



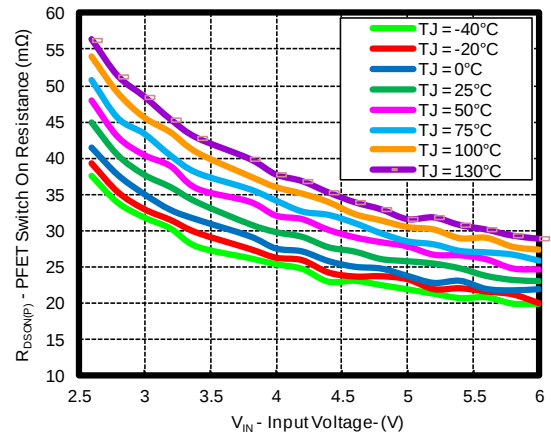
Shutdown Current vs Junction Temperature



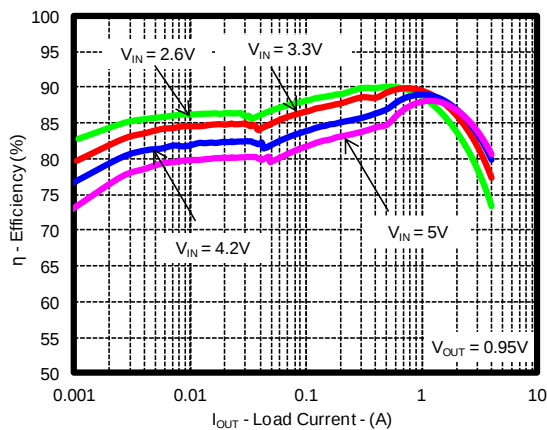
NFET Switch On Resistance vs Input Voltage



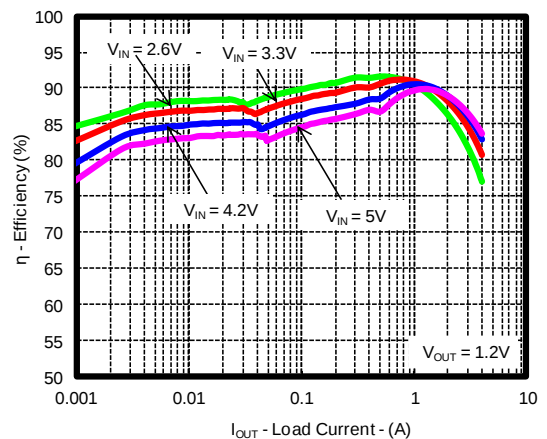
PFET Switch On Resistance vs Input Voltage



Efficiency

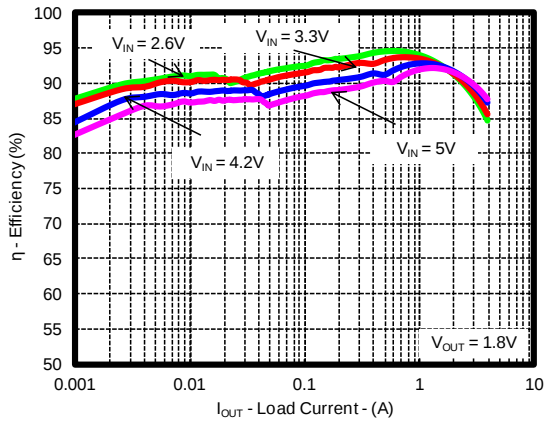


Efficiency

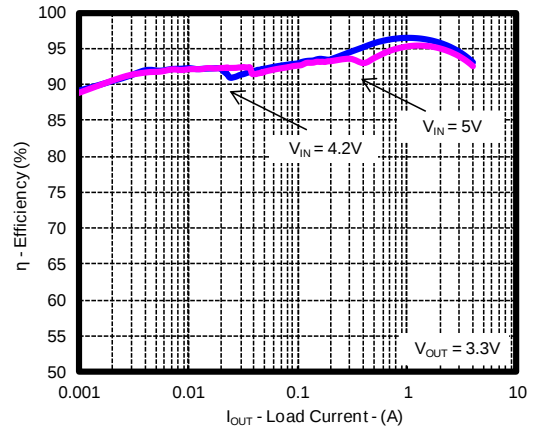


Typical Performance Characteristics (continued)

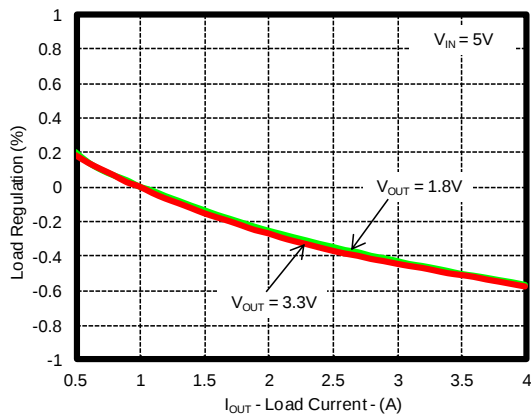
Efficiency



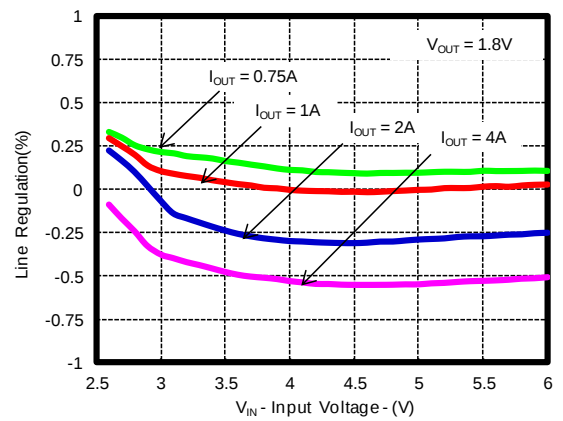
Efficiency



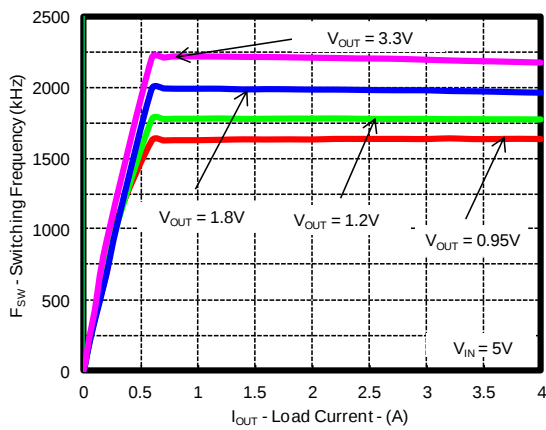
Load Regulation



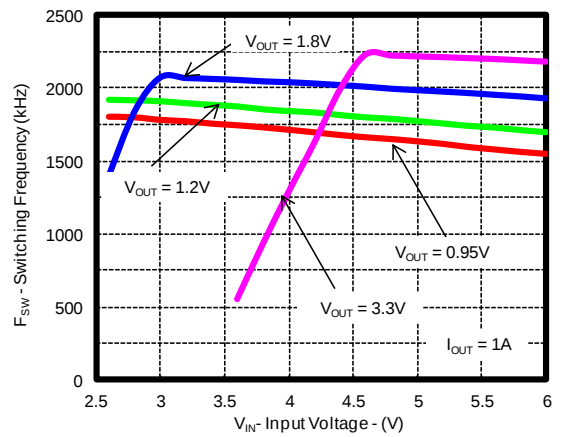
Line Regulation



Switching Frequency

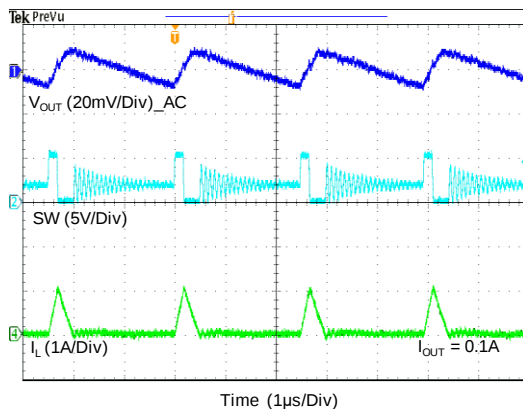


Switching Frequency

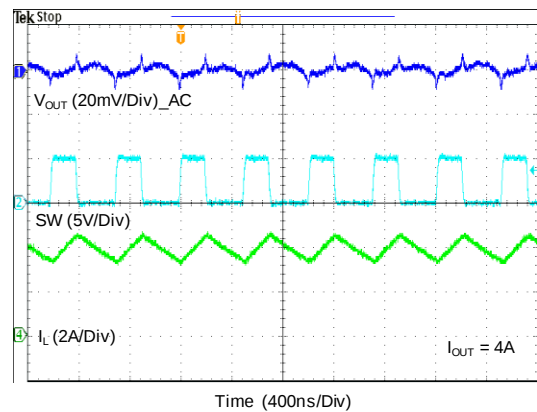


Typical Performance Characteristics (continued)

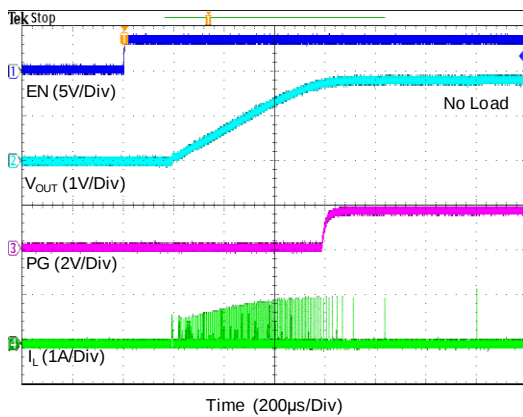
PSM Operation



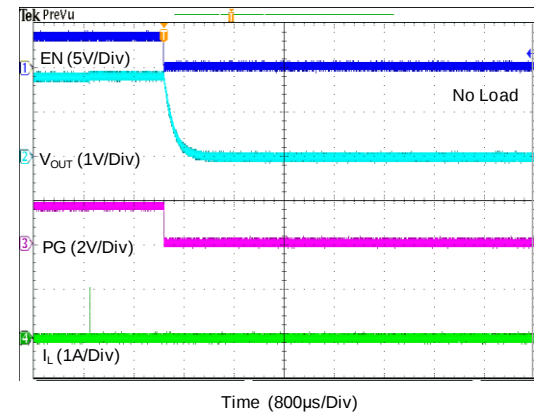
PWM Operation



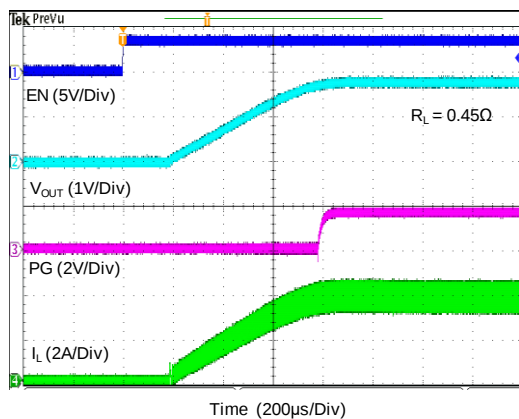
Start-Up without Load



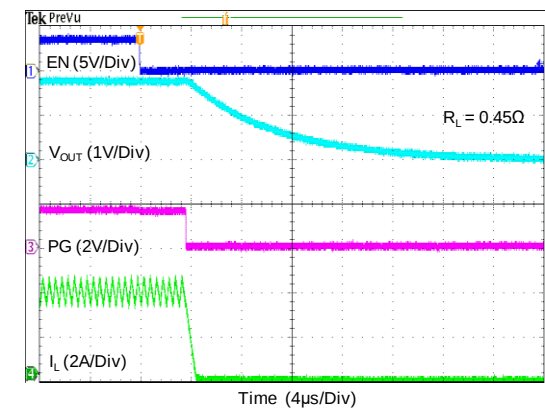
Shutdown without Load



Start-Up with Load

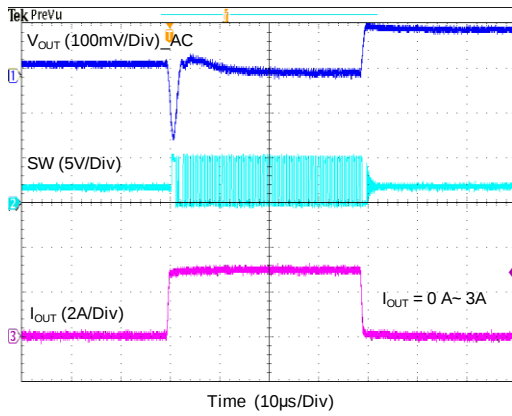


Shutdown with Load

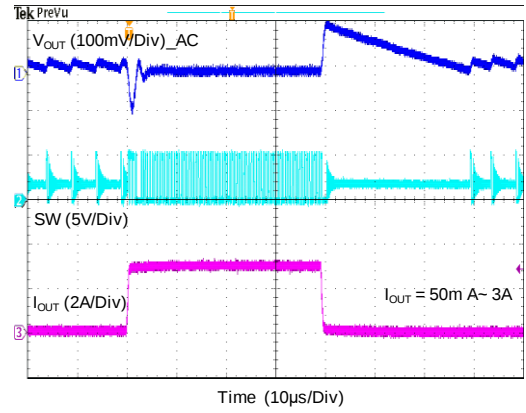


Typical Performance Characteristics (continued)

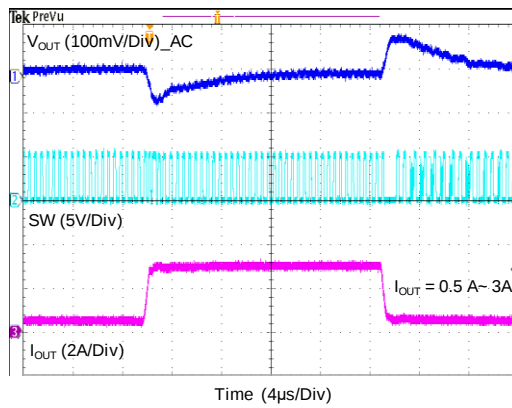
Load Transient Response



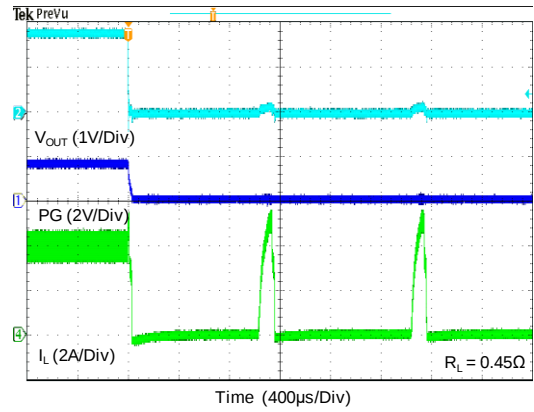
Load Transient Response



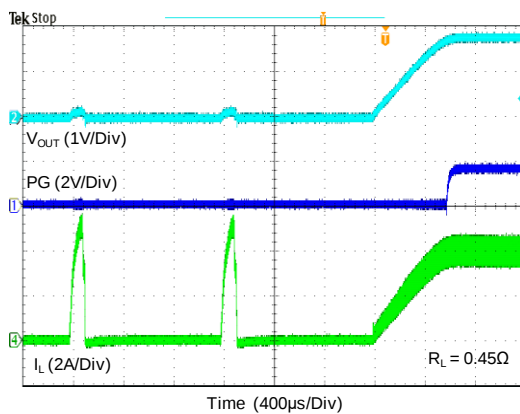
Load Transient Response



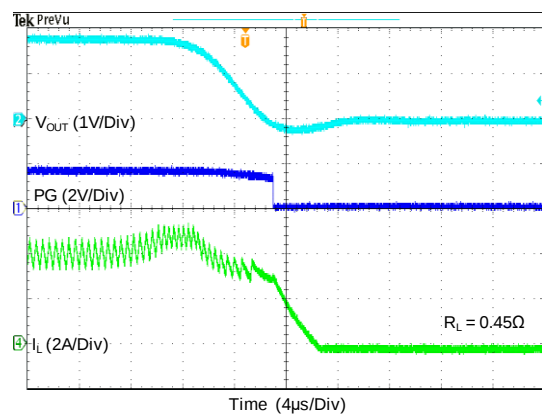
Output Short Circuit Protection, Entry (Hiccup)



Output Short Circuit Protection, Recovery (Hiccup)



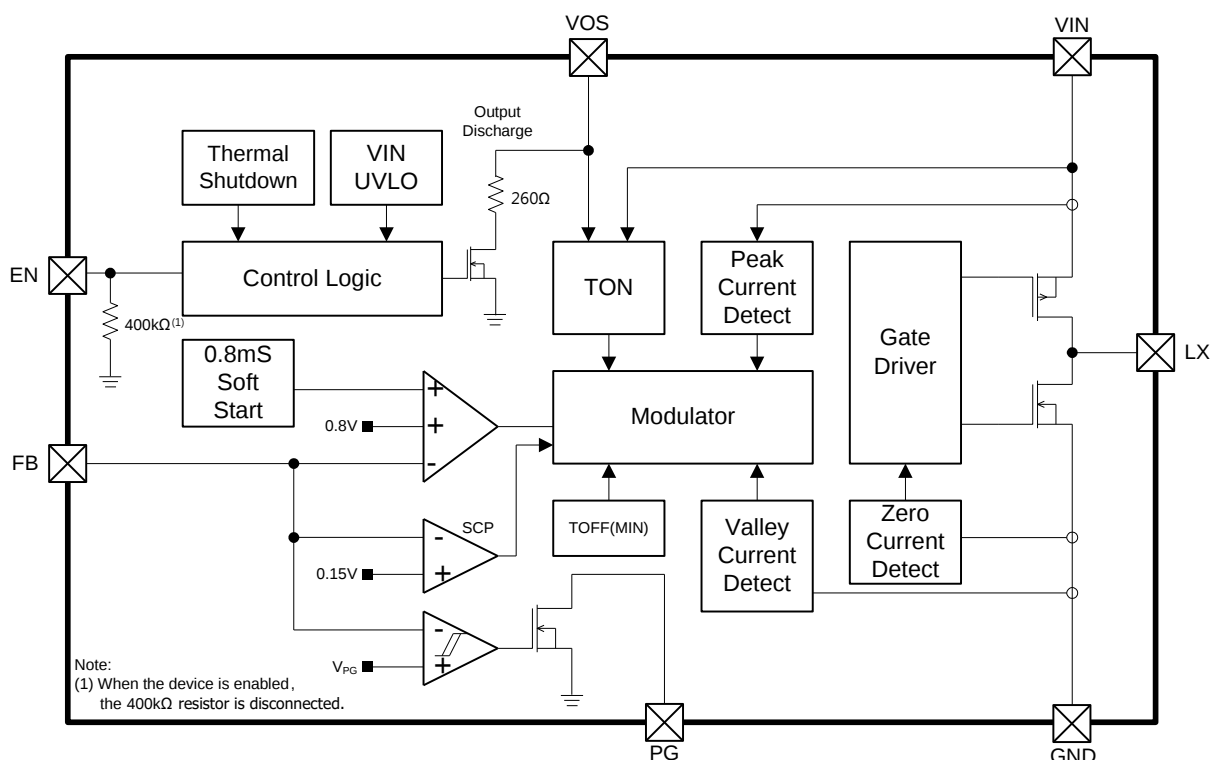
Output Short Circuit Protection (Hiccup) - Zoom in



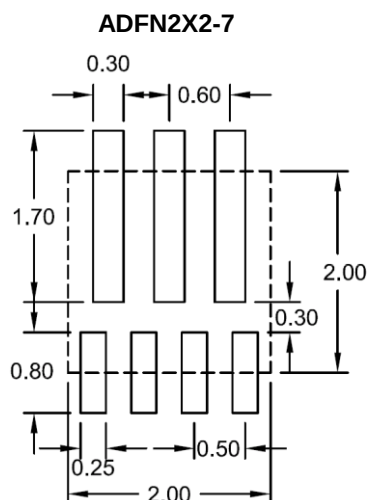
Pin Description

Pin	NAME	FUNCTION
1	EN	Enable control input. A pull low resistance 400kΩ exists in this pin when disabled.
2	PG	Power good open drain output pin. The pull-up resistor cannot be connected to any voltage higher than 6V. If unused, leave it floating.
3	FB	An external resistor divider from the output to GND, tapped to the FB pin, sets the output voltage.
4	VOS	Output voltage sense pin, directly connected to the output capacitor
5	GND	Ground.
6	LX	Switch node.
7	VIN	Supply voltage input.

Block Diagram



Minimum Footprint PCB Layout Section



Operation

The G2275A is a high efficiency synchronous step-down DC/DC converter. G2275A provides an adjustable regulated output voltage from 0.8V to V_{IN} while delivering up to 4A of output current with input voltage from 2.6V to 5.5V.

The G2275A uses the constant on-time control scheme. In normal operation, the high side P-MOSFET is turned on when the switch controller is set by the comparator and is turned off when the Ton comparator resets the switch controller.

Low side MOSFET current is measured. The error amplifier adjusts COMP voltage by comparing the feedback signal (VFB) from the output voltage with the internal 0.8V reference. When the load current increases, it causes a drop in the feedback voltage relative to the reference, then the COMP voltage rises to allow higher inductor current to match the load current.

Enable

When the input voltage is greater than the under voltage lockout threshold, a logic-high (>1V) enables the converter; a logic-low (<0.4V) or floating forces the IC into shutdown mode. There is an internal 400k Ohm resistor from EN pin to GND when EN is low. This pull low resistance is disconnected when EN is high.

When the device is disabled, there is a resistive discharge path (260 Ohm) from VOS pin.

Soft-Start (SS)

There is an internal built-in soft-start to ramp the output voltage at a fixed slew rate to avoid in-rush current. The typical soft-start time is 0.8ms.

Over Current Protection (OCP)

The G2275A provides the over current protection by detecting the high side MOSFET peak inductor current (6.5A typ.) and the low-side MOSFET valley inductor current (4.5A typ.). If the inductor current is over the peak current limit threshold, the high-side MOSFET is turned off and the low-side MOSFET is turned on. Once the inductor current is larger than the valley current limit, the next switching cycle is not allowed. This avoids increasing the inductor current and protects the components.

HICCUP Protection

When the inductor current limit is triggered 8 times, the inductor current limit is reduced to half for the next 8 cycles, and then the device stops switching to protect the components. After a delay of 1ms, G2275A automatically starts a new start-up procedure. Therefore, Hiccup protection is achieved and repeated until the high load condition is removed.

Thermal Shutdown (OTP)

The device implements an internal thermal shutdown function when the junction temperature exceeds 150°C. The thermal shutdown forces the device to stop switching when the junction temperature exceeds the thermal shutdown threshold. Once the die temperature decreases below the hysteresis of 30°C, the device reinstates the power up sequence.

Power Good (PG)

G2275A has an open drain and needs an external pull up resistor for the power good indicator. When V_{FB} is high than 95% of regulated voltage, PG is pulled high by the external pull up resistor. If V_{FB} drops lower than 90% of regulated voltage, PG is pulled low by the internal NMOS. Please keep PG pull up voltage is lower than V_{IN} . Leave the PG pin unconnected when not used. Table 1 shows the PG logic status.

Table 1. PG logic status

	Conditions	PG
Enable	EN=High , $V_{FB} \geq V_{PG_R}$	High Z
	EN=High , $V_{FB} < V_{PG_F}$	Low
	EN=Low	Low
OTP	$T_J > 150^\circ\text{C}$	Low
UVLO	$0.5V < V_{IN} < V_{UVLO}$	Low
VIN Removal	$V_{IN} \leq 0.5V$	High Z

Application Information

The G2275A is a single-phase step-down converter. It provides single feedback loop, constant on-time control with fast transient response. An internal 0.8V reference allows the output voltage to be precisely regulated for low output voltage applications and internal compensation are integrated to minimize external component count. Protection features include over current protection, under voltage protection and over temperature protection.

Output Voltage Setting

Connect a resistive voltage divider at the FB between V_{OUT} and GND to adjust the output voltage. The output voltage is set according to the following equation :

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right)$$

where V_{REF} is the feedback reference voltage 0.8V (typ.).

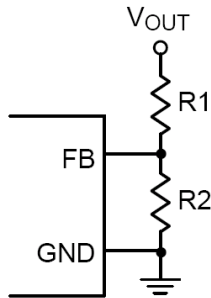


Figure 1. Setting V_{OUT} with a Voltage Divider

Chip Enable and Disable

The EN pin allows for power sequencing between the controller bias voltage and another voltage rail. The G2275A remains in shutdown if the EN pin is lower than 400mV. When the EN pin rises above the VEN trip point, the G2275A begins a new initialization and soft-start cycle.

Internal Soft-Start

The G2275A provides an internal soft-start function to prevent large inrush current and output voltage overshoot when the converter starts up. The soft-start (SS) automatically begins once the chip is enabled. During soft-start, the internal soft-start capacitor becomes charged and generates a linear ramping up voltage across the capacitor. This voltage clamps the voltage at the FB pin, causing PWM pulse width to increase slowly and in turn reduce the input surge current. The internal 0.8V reference takes over the loop control once the internal ramping-up voltage becomes higher than 0.8V.

UVLO Protection

The G2275A has input Under Voltage Lockout protection (UVLO). If the input voltage exceeds the UVLO rising threshold voltage (2.5V typ.), the converter resets and prepares the PWM for operation. If the input voltage falls below the UVLO falling threshold voltage during normal operation, the device will stop switching. The UVLO rising and falling threshold voltage has a hysteresis to prevent noise-caused reset.

Inductor Selection The switching frequency (on-time) and operating point (% ripple or LIR) determine the inductor value as shown below :

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{f_{SW} \times LIR \times I_{LOAD(MAX)} \times V_{IN}}$$

where LIR is the ratio of the peak-to-peak ripple current to the average inductor current. Find a low loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. The core must be large enough not to saturate at the peak inductor current (I_{PEAK}) :

$$I_{PEAK} = I_{LOAD(MAX)} + \left(\frac{LIR}{2} \times I_{LOAD(MAX)}\right)$$

The calculation above serves as a general reference. To further improve transient response, the output inductor can be further reduced. This relation should be considered along with the selection of the output capacitor. Inductor saturation current should be chosen over IC's current limit.

Input Capacitor Selection

High quality ceramic input decoupling capacitor, such as X5R or X7R, with values greater than 10uF are recommended for the input capacitor. The X5R and X7R ceramic capacitors are usually selected for power regulator capacitors because the dielectric material has less capacitance variation and more temperature stability.

Voltage rating and current rating are the key parameters when selecting an input capacitor. Generally, selecting an input capacitor with voltage rating 1.5 times greater than the maximum input voltage is a conservatively safe design.

The input capacitor is used to supply the input RMS current, which can be approximately calculated using the following equation :

$$I_{IN_RMS} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The next step is selecting a proper capacitor for RMS current rating. One good design uses more than one capacitor with low equivalent series resistance (ESR) in parallel to form a capacitor bank.

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be approximately calculated using the following equation :

$$\Delta V_{IN} = \frac{I_{OUT(MAX)}}{C_{IN} \times f_{SW}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Output Capacitor Selection

The output capacitor and the inductor form a low pass filter in the Buck topology. In steady state condition, the ripple current flowing into/out of the capacitor results in ripple voltage. The output voltage ripple (VP-P) can be calculated by the following equation :

$$V_{P_P} = LIR \times I_{LOAD(MAX)} \times \left(ESR + \frac{1}{8 \times C_{OUT} \times f_{SW}}\right)$$

When load transient occurs, the output capacitor supplies the load current before the controller can respond. Therefore, the ESR will dominate the output voltage sag during load transient. The output voltage undershoot (VSAG) can be calculated by the following equation :

$$V_{SAG} = \Delta I_{LOAD} \times ESR$$

For a given output voltage sag specification, the ESR value can be determined.

Another parameter that has influence on the output voltage sag is the equivalent series inductance (ESL). The rapid change in load current results in di/dt during transient. Therefore, the ESL contributes to part of the voltage sag. Using a capacitor with low ESL can obtain better transient performance. Generally, using several capacitors connected in parallel can have better transient performance than using a single capacitor for the same total ESR.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding air-flow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA} , is layout dependent. The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA} .

PCB layout guidelines

1. Component Placement :

Place input capacitors as close as possible to VIN.

Place the feedback resistors and compensation components as close as possible to the IC.

2. Layout Recommendation :

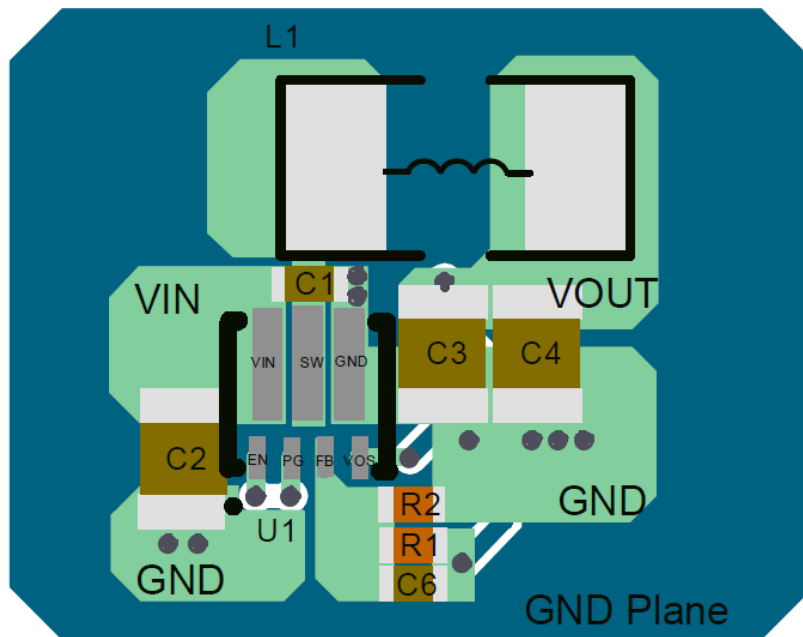
To prevent electromagnetic interference (EMI) problems and reduce voltage ripple of the device, any high current copper trace which see high frequency switching should be optimized.

Therefore, use short and wide traces for power current paths and for power ground tracks, power plane and ground plane are recommended if possible.

It is important to minimize the area of the switching nodes and use the ground plane under them to minimize crosstalk to sensitive signals and ICs.

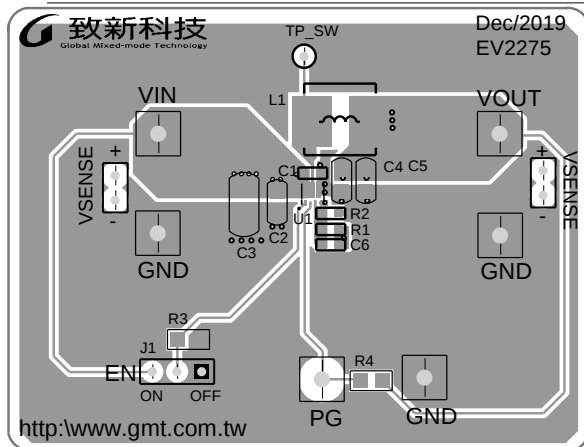
It's suggested to keep as complete of a ground plane under G2275 if possible.

It is always good practice to keep the sensitive tracks such as feedback connection (FB) away from switching signal connections (SW)

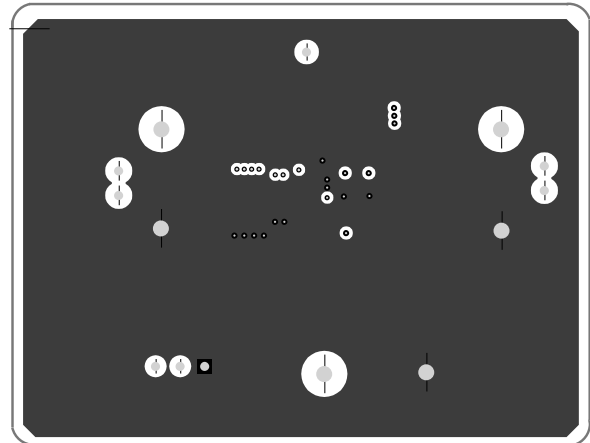


EV Board PCB Layout Section

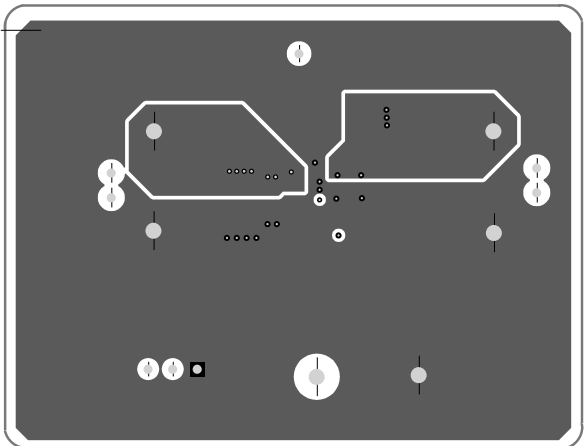
Top Layer



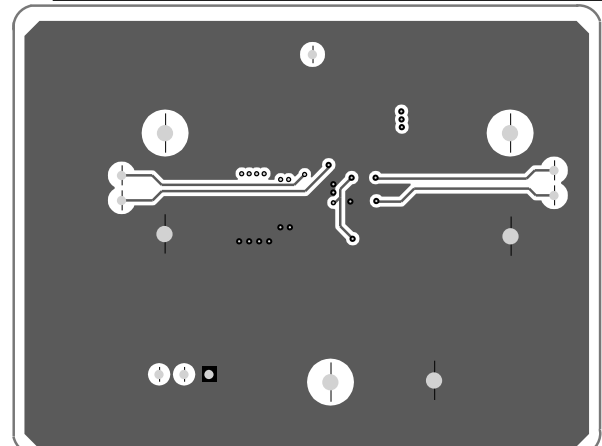
Mid Layer 1



Mid Layer 2



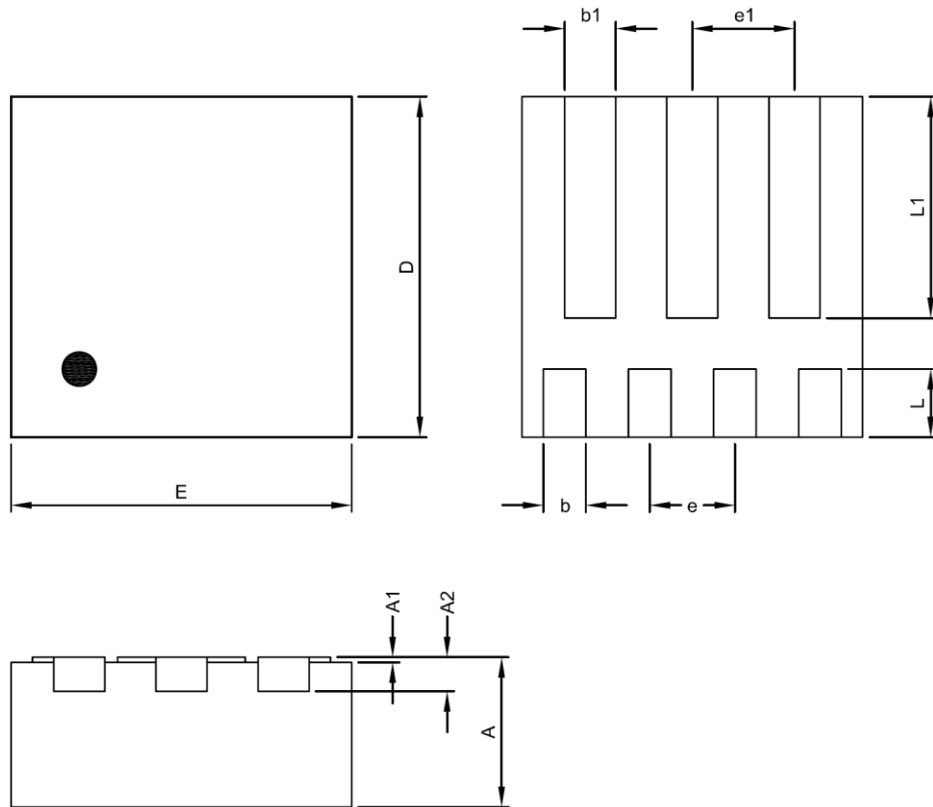
Bottom Layer



EV2275 PCB	Information
Board Material	FR4
Size	60mm×45mm
Board Thickness	1.6mm
Layers	4
Copper Thickness	2 oz.

Package Information

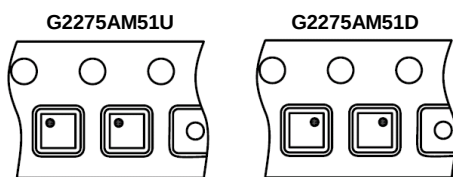
G2275AM51U & G2275AM51D



ADFN2X2-7 Package

Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.85	0.90	0.0315	0.0335	0.0354
A1	0.00	---	0.05	0.0000	---	0.0020
A2	0.203 REF			0.0080 REF		
D	1.95	2.00	2.05	0.0768	0.0787	0.0807
E	1.95	2.00	2.05	0.0768	0.0787	0.0807
b	0.20	0.25	0.30	0.0079	0.0098	0.0118
b1	0.25	0.30	0.35	0.0098	0.0118	0.0138
e	0.50 BSC			0.0197 BSC		
e1	0.60 BSC			0.0236 BSC		
L	0.35	0.40	0.45	0.0138	0.0157	0.0177
L1	1.25	1.30	1.35	0.0492	0.0512	0.0531

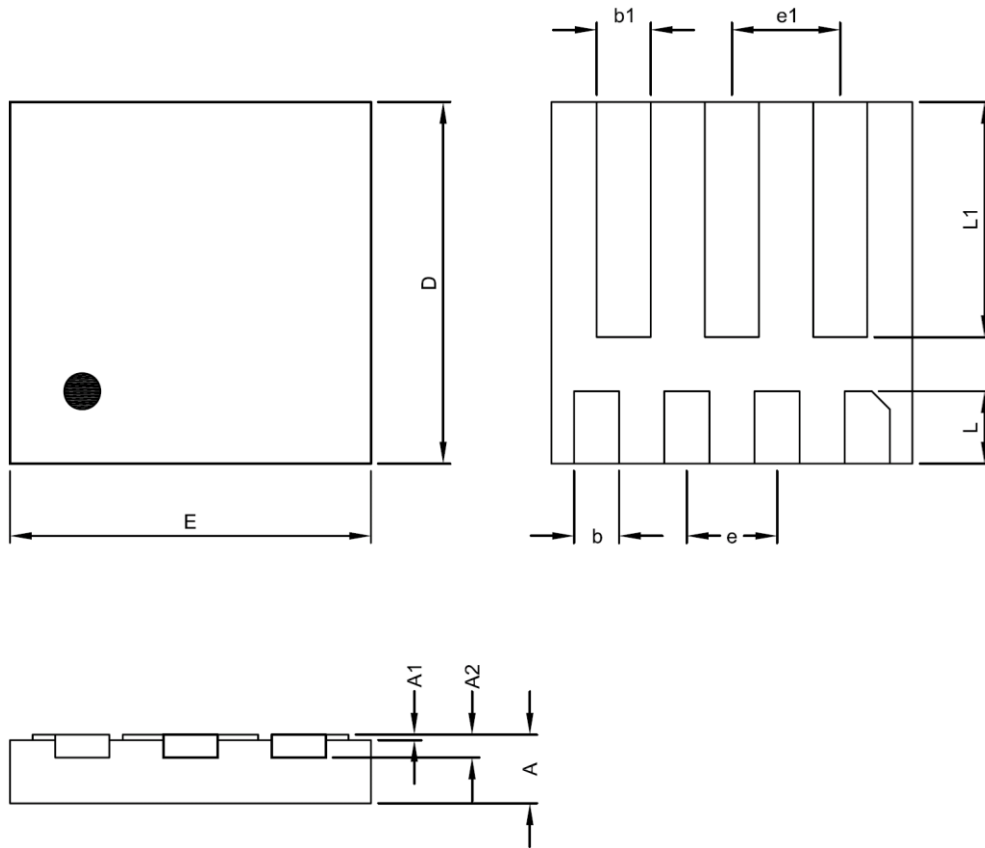
Taping Specification



Feed Direction

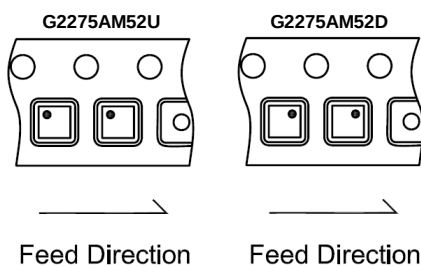
Feed Direction

PACKAGE	Q'TY/REEL
ADFN2X2-7	3,000 ea


ADFN2X2-7 Package

Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.30	0.35	0.40	0.0118	0.0138	0.0157
A1	0.00	---	0.05	0.0000	---	0.0020
A2	0.127 REF			0.0050 REF		
D	1.95	2.00	2.05	0.0768	0.0787	0.0807
E	1.95	2.00	2.05	0.0768	0.0787	0.0807
b	0.20	0.25	0.30	0.0079	0.0098	0.0118
b1	0.25	0.30	0.35	0.0098	0.0118	0.0138
e	0.50 BSC			0.0197 BSC		
e1	0.60 BSC			0.0236 BSC		
L	0.35	0.40	0.45	0.0138	0.0157	0.0177
L1	1.25	1.30	1.35	0.0492	0.0512	0.0531

Taping Specification



PACKAGE	Q'TY/REEL
ADFN2X2-7	3,000 ea

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