G2517A

Integrated Power Supply for TFT-LCD

Features

- **Input Supply Range: 2.5V ~ 5.5V**
- **I^2C Interface**
- **Current Mode Sync. Boost Converter for AVDD**
  - **Programmable Switching Frequency**
  - **7V to 13.5V Programmable Output**
  - **Fast Transient Response to Pulsed Load**
  - **High-Accuracy Output Voltage (±1%)**
- **Sync. Buck Converter for V_{buck}**
  - **Programmable Switching Frequency**
  - **0.8V to 2.8V Programmable Output for V_{buck}**
  - **Fast Transient Response to Pulsed Load**
  - **High-Accuracy Output Voltage (±1.5%)**
- **Charge Pump for V_{GH}**
  - **Programmable Delay Time**
  - **Programmable VGH Output Voltage**
- **Low Dropout Regulator**
  - **1.0V to 2.8V Programmable Output**
- **Programmable 7-bit VCOM Calibrator**
- **Programmable OP for HAVDD**
- **2-ch Rail to Rail Programmable Gamma Buffers**
- **Programmable 2-ch Voltage Detector**
  - **1.8V to 2.7V Programmable Output**
- **Protection Function**
  - **Over-Current Protection (OCP)**
  - **Over-Temperature Protection (OTP)**
  - **Over-Voltage Protection (OVP)**
  - **Output Under Voltage Protection (UVP)**
  - **Short Circuit Protection (SCP)**
- **Available in TQFN 3.5X3.5-24 Pin Package**

General Description

The G2517A is a multi-channel power solution for TFT-LCD, tablet and notebook display panels. The G2517A includes I^2C interface, one synchronous boost converters for AVDD, one buck converters for Vbuck, one VGH can be programmable timing and output voltage, one LDO regulator, two voltage detectors, one programmable V_{COM} generator with a high-speed amplifier for VCOM, one high-speed operation amplifier for HAVDD, two rail to rail operation amplifiers for GMA1 and GMA2. This device is suitable for TFT-LCD panel.

The G2517A is available in a TQFN3.5X3.5-24 pin package.

Applications

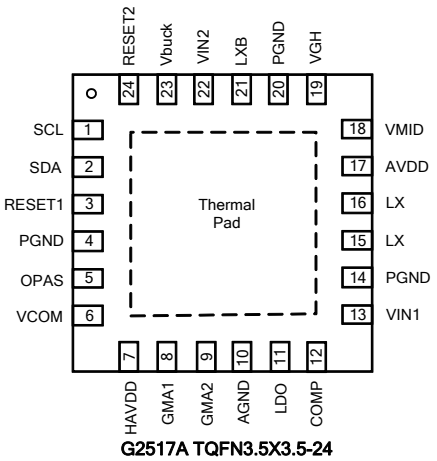
- **NB PCs**
- **Tablet PCs**

Ordering Information

ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE (Green)
G2517AKM1U	2517A	-40°C to 85°C	TQFN3.5X3.5-24

Note: KM: TQFN3.5X3.5-24
1: Bonding Code
U: Tape & Reel
Green: Lead Free / Halogen Free

Pin Configuration



G2517A TQFN3.5X3.5-24

Note: Recommend connecting the Thermal Pad to the Ground for excellent power dissipation.

Absolute Maximum Rating

VIN1~2 to PGND . . . . . 0.3V to 6V
SDA, SCL to AGND . . . . . -0.3V to 6V
VIN1~2 to PGND (100ms pulse). . . . . 0.3V to 12V
PGND, AGND to GND. . . . . ±0.3V
COMP, RESET1~2 to AGND . . . . . -0.3V to 6V
AVDD, LX to PGND . . . . . -0.3V to 14.5V
OPAS to PGND . . . . . -0.3V to 14.5V
VMID to PGND . . . . . -0.3V to (V_{AVDD}+0.3V)
LXB to PGND . . . . . -0.3V to 6V
Vbuck to PGND . . . . . -0.3V to 6V
VGH to PGND . . . . . -0.3V to 35V
Vbuck, LDO to PGND . . . . . -0.3V to 6V
VCOM, HAVDD to PGND . . . . . -0.3V to (OPAS+0.3V)
GMA1, GMA2 to PGND . . . . . -0.3V to (OPAS+0.3V)

Thermal Resistance Junction to Ambient, (θ_{JA})
TQFN 3.5X3.5-24 . . . . . TBD
Continuous Power Dissipation (T_A = +25°C)
TQFN 3.5X3.5-24 . . . . . TBD
Thermal Resistance Junction to Case, (θ_{JC})
TQFN 3.5X3.5-24. . . . . TBD
Operating Temperature Range . . . . . .-40°C to 85°C
Storage Temperature Range. . . . . -65°C to 150°C
Junction Temperature . . . . . 160°C
Reflow Temperature (soldering, 10sec) . . . . . 250°C
Electrostatic Discharge, VESD (Note1)
Human Body Mode (HBM) 2kV
Machine Mode (MM) 200V

Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
VIN1~2 Supply Range	V_{IN}		2.5	3.3	6	V
AVDD Output Range	AVDD	Step:100mV	7	9.0	13.5	V
Vbuck Output Range	V_{CORE}	Step:50mV	0.8	1.2	2.8	V
VGH Output Voltage	VGH	Step:1V	10	22	34	V
LDO Output Range	V_{LDO}	Step:100mV	1.8	2.5	2.8	V
VCOM Output Range	D-V_{com}	Step:20mV	2.5	---	7.0	V
	D-V_{com_P}	Step:10mV	VCOM-10mVx64	---	VCOM+10mVx63	
HAVDD Range	HAVDD	Step:50mV	2.5	---	7.0	V
GMA1 Output Range	GMA1	Step:20mV	AVDD-1	---	AVDD-0.1	V
GMA2 Output Range	GMA2	Step:20mV	0.1	---	1	V
RESET1~2 setting range			2.0	2.5	2.7	V
Operating ambient temperature	T_A		-40	---	85	°C
Operating junction temperature	T_J		-40	---	125	°C

Electrical Characteristics

($V_{IN1&2}$=3.3V, V_{AVDD}=9V, Vbuck=1.2V, VLDO=2.5V, T_A = 25°C)

The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL					
Input Voltage Range		2.5	3.3	6	V
VIN Quiescent Current	All converter no switching	---	2.5	---	mA
	All converter switching	---	5.5	---	
Under-voltage Lockout Threshold	V_{IN} rising	---	2.3	---	V
	V_{IN} falling hysteresis	---	0.3	---	
Duration to Trigger Fault Condition		---	60	---	ms
Thermal Shutdown Protection	Temperature rising	---	150	---	°C
AVDD Boost Converter					
Output Voltage Range	Programmable	7	--	13.5	V
Output Voltage Bit		---	7	---	Bits
Output Voltage Resolution		---	0.1	---	V
Output Voltage Accuracy	AVDD = 9V	-1	--	+1	%
Switching Frequency	Programmable (Accuracy ±10%)	600	715	1225	kHz
Switching Frequency Bit		---	3	---	Bits
Maximum Duty Cycle		86	90	94	%
Line Regulation	V_{IN} = 2.5V to 5V	-0.3	--	+0.3	%/V
LX On-Resistance	Low Side $R_{DS(ON)}$	---	150	---	mΩ
	High Side $R_{DS(ON)}$	---	300	---	mΩ
LX Leakage Current	V_{LX} = 13.5V	---	1	5	μA
LX Current Limit	Programmable	0.5	---	2	A
LX Current Limit Bit		---	2	---	Bits
LX Current Limit Resolution		---	0.5	---	A
Output Current Ability		250	---	---	mA
Soft-start time	Programmable	5	---	20	ms
Soft-start time Bit		---	2	---	Bits
Soft-start time Resolution		---	5	---	ms
Delay time		0	---	35	ms
Delay time Bit		---	3	---	Bits
Delay time Resolution		---	5	---	ms
Under Voltage Fault Trip Level	V_{AVDD} falling edge	---	NOMx80%	---	V
VGH Output					
Voltage Range		10	---	34	V
Voltage Bit		---	5	---	Bits
Voltage Resolution		---	1	---	V
Delay time		0	---	55	ms
Delay time Bit		---	4	---	Bits
Delay time Resolution		---	5	---	ms
Vbuck Buck Converter					
Output Voltage Range	Programmable	0.8	1.2	2.8	V
Output Voltage Bit		---	6	---	Bits
Output Voltage Resolution		---	0.05	---	V
Output Voltage Accuracy	VIO=1.8V	-1	---	+1	%
Switching Frequency	Programmable (Accuracy ±10%)	600	715	1225	kHz
Switching Frequency Bit		---	3	---	Bits

Electrical Characteristics

($V_{IN1\&2}$=3.3V, V_{AVDD}=9V, Vbuck=1.2V, VLDO=2.5V, T_A = 25°C)

The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LXB to VIN Switch $R_{DS(ON)}$		---	500	---	mΩ
LXB to PGND Switch $R_{DS(ON)}$		---	200	---	mΩ
LXB Current Limit	Programmable	---	1.0	---	A
LXB Current Limit Bit		---	2	---	Bits
LXB Current Limit Resolution		---	0.5	---	A
Output Current Ability		300	---	---	mA
LXB Leakage Current	V_{LXB} = 3.3V and 0V	---	1	5	μA
Soft-start time		---	3	---	ms
Delay time		0	---	9	ms
Delay time Bit		---	2	---	Bits
Delay time Resolution		---	3	---	ms
Under Voltage Fault Trip Level	V_{GH} falling edge	---	NOMx80%	---	V
Low Dropout Linear Regulator					
Output Voltage Range		1.0	---	2.8	V
Output Voltage Bit		---	5	---	Bits
Output Voltage Resolution		---	0.1	---	V
Output Voltage Accuracy	V_{LDO} = 2.5V	-1	---	+1	%
Dropout Voltage	V_{IN} = 3.3V, I_{OUT} = 200mA	---	0.2	--	V
Current Limit		---	200	--	mA
Output Current Ability		100	---	---	mA
Delay time		0	---	9	ms
Delay time Bit		---	2	---	Bits
Delay time Resolution		---	3	---	ms
Under Voltage Fault Trip Level	V_{LDO} falling edge	---	NOMx80%	---	V
HAVDD Output					
OPAS Quiescent Current		---	1.0	--	mA
OPAS Voltage Range		7	---	13.5	V
Output Voltage Range		2.5	---	7.0	V
Output Voltage Bit		---	6	---	Bits
Output Voltage Resolution		---	0.05	---	V
Output Current Ability		---	±75	---	mA
Short-Circuit Current	Source	---	250	---	mA
	Sink	---	-250	---	mA
-3dB Bandwidth	R_L=10kΩ, C_L=10pF	---	10	---	MHz
Gain-Bandwidth Product	R_L=10kΩ, C_L=10pF	---	5	---	MHz
Integral Nonlinearity Error	HAVDD=2.5V to 8.0V	---	1	---	LSB
Differential Nonlinearity Error	HAVDD=2.5V to 8.0V	---	1	---	LSB

Electrical Characteristics

($V_{IN1\&2}$=3.3V, V_{AVDD}=9V, Vbuck=1.2V, VLDO=2.5V, T_A = 25°C)

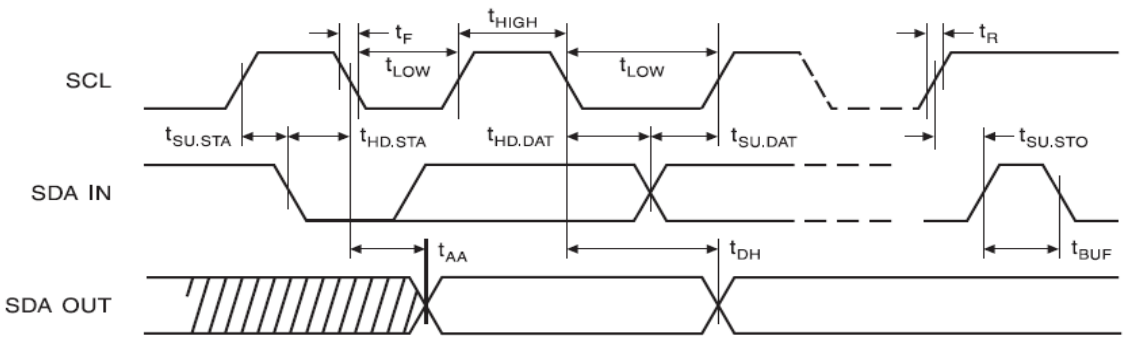
The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
D-VCOM Amplifier					
Output Voltage Range	20mV/step	2.5	---	7	V
Input Offset Voltage	VCOM=3.7V	-15	---	+15	mV
Input Bias Current		-100	---	+100	nA
Output Voltage Swing High	IOUT = 100μA	AVDD-0.03	VSUP-0.05	--	V
	IOUT = 75mA	AVDD-1.9	AVDD-1.5	---	V
Output Voltage Swing Low	IOUT = -100μA	---	GND+5	GND+3	mV
	IOUT = -75mA	---	GND+1.5	GND+1.9	V
Short-Circuit Current	Source	---	+150	---	mA
	Sink	---	-150	---	mA
Slew Rate		---	12	---	V/μs
-3dB Bandwidth	R_L=10kΩ, C_L=10pF	---	10	---	V/μs
Gain-Bandwidth Product	R_L=10kΩ, C_L=10pF	---	5	---	MHz
Soft-start time	0V to 3.7V	---	3	---	ms
Delay time		0	---	155	ms
Delay time Bit		---	5	---	Bits
Delay time Resolution		---	5	---	ms
Programmable VCOM Calibrator					
Resolution		---	7	---	Bits
Integral Nonlinearity Error		---	1	---	LSB
Differential Nonlinearity Error		---	1	---	LSB
GMAx Output					
GMA1 Output Voltage Range	20mV/step	AVDD-1	---	AVDD-0.1	V
GMA2 Output Voltage Range	20mV/step	0.1	---	1	V
Output Current Ability		1	---	---	mA
GMA1 Output Voltage Swing High	IOUT = 1mA	AVDD-0.2	---	---	V
GMA2 Output Voltage Swing Low	IOUT = 1mA	---	--	GND+0.2	V
Resolution		---	5	---	Bits
Integral Nonlinearity Error		---	1	---	LSB
Differential Nonlinearity Error		---	1	---	LSB
RESET1 & 2 (Voltage Detector)					
Output Voltage Range	Programmable	2.0	2.2	2.7	V
Output Voltage Bit		---	3	---	Bits
Output Voltage Resolution		---	0.1	---	V
Output Voltage Accuracy		-2	---	+2	%
Delay time		0	---	75	ms
Delay time Bit		---	4	---	Bits
Delay time Resolution		---	5	---	ms

I²C Timing Characteristics

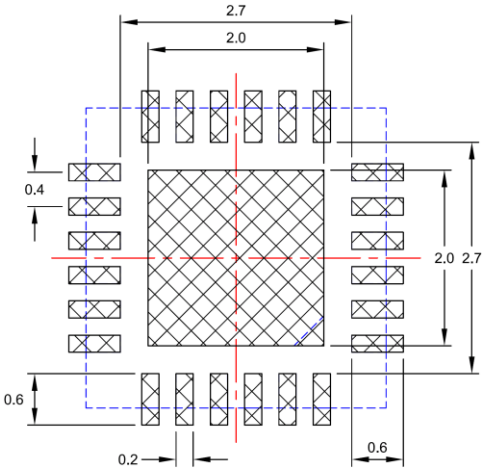
PARAMETER	Symbol	CONDITIONS	MIN	TYP	MAX	UNITS
Logic Input High Voltage Threshold	VIH	SDC, SCL	1.2	---	---	V
Logic Input Low Voltage Threshold	VIL	SDC, SCL	---	---	0.4	V
SDA Output Sink Current	$I_{SINK-SDA}$	V_{SDA}=0.4V	---	6	---	mA
Serial-Clock Frequency	F_{SCL}		0.2	400	1000	kHz
Data Setup Time	$t_{SU,DAT}$		100	---	---	ns
Data Hold Time	$t_{HD,DAT}$		---	---	300	ns
SDA and SCL Rise Time	t_R		20+0.1CB	---	200	ns
SDA and SCL Fall Time	t_F		20+0.1CB	---	200	ns
SDA and SCL Input Capacitance			---	5	---	pF
START Condition of Setup Time	$T_{SU.STA}$		0.25	---	---	μs
START Condition of Hold Time	$T_{HD.STA}$	10% of SDA to 90% of SCL	0.25	---	---	μs
Bus Free Time Between STOP and START Conditions	t_{BUF}		0.5	---	---	μs
SDA_ACK on Voltage			---	---	0.4	V
Pulse Width of Suppressed Spike	T_{SP}		---	---	50	ns
Clock Pulse Width Low	t_{LOW}		1.3	---	---	μs
Clock Pulse Width Low	t_{LHIGH}		0.6	---	---	μs
Bus Free Time Between Stop	$t_{SU.STO}$		0.6	---	---	μs
Clock Low to Data Out Valid	t_{AA}		0.1	---	0.9	μs
Data Out Hold Time	t_{DH}		50	---	---	μs

I²C Bus Timing:



Minimum Footprint PCB Layout Section (Unit: mm)

TQFN3.5X3.5-24

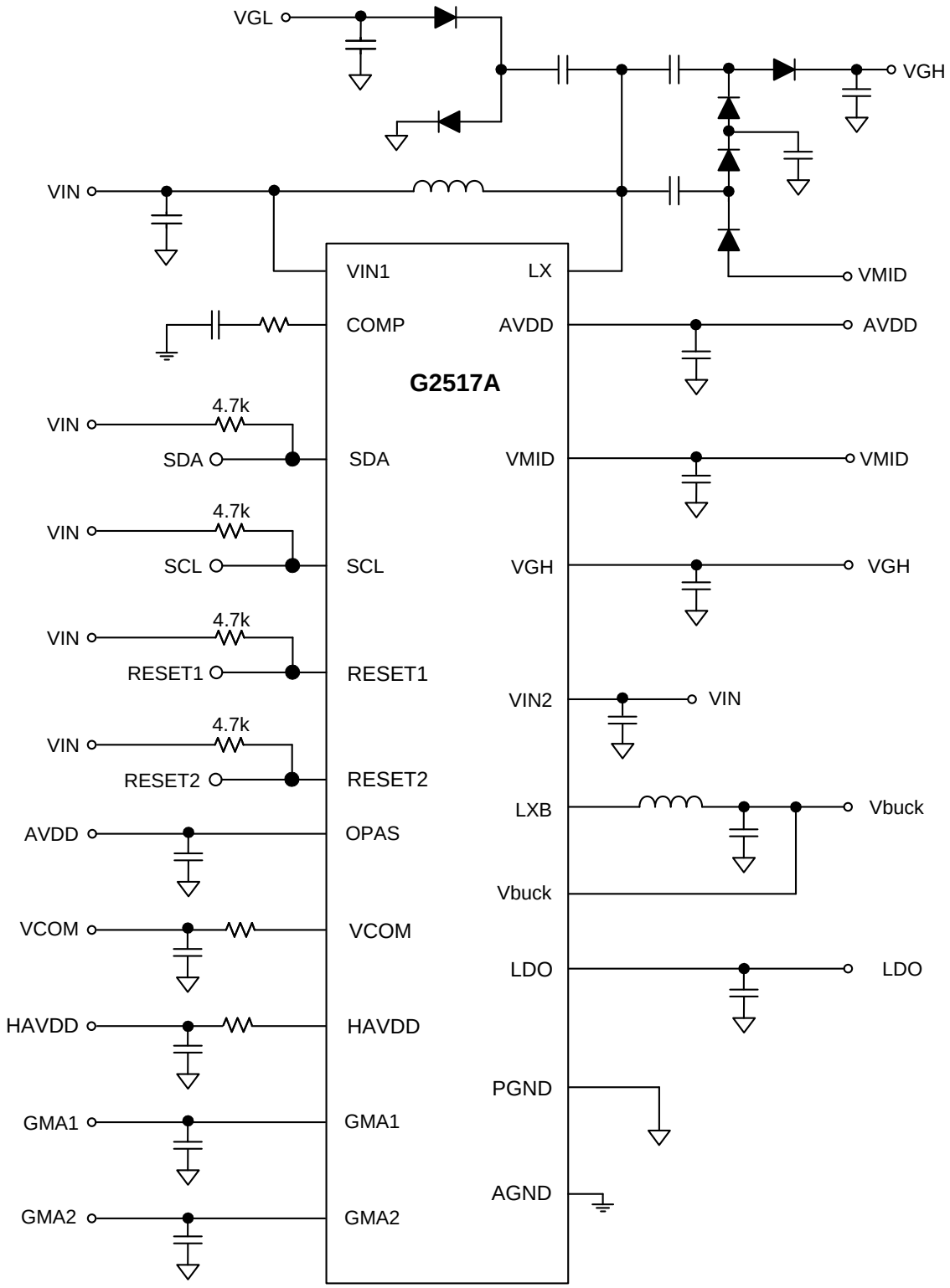


Pin Description

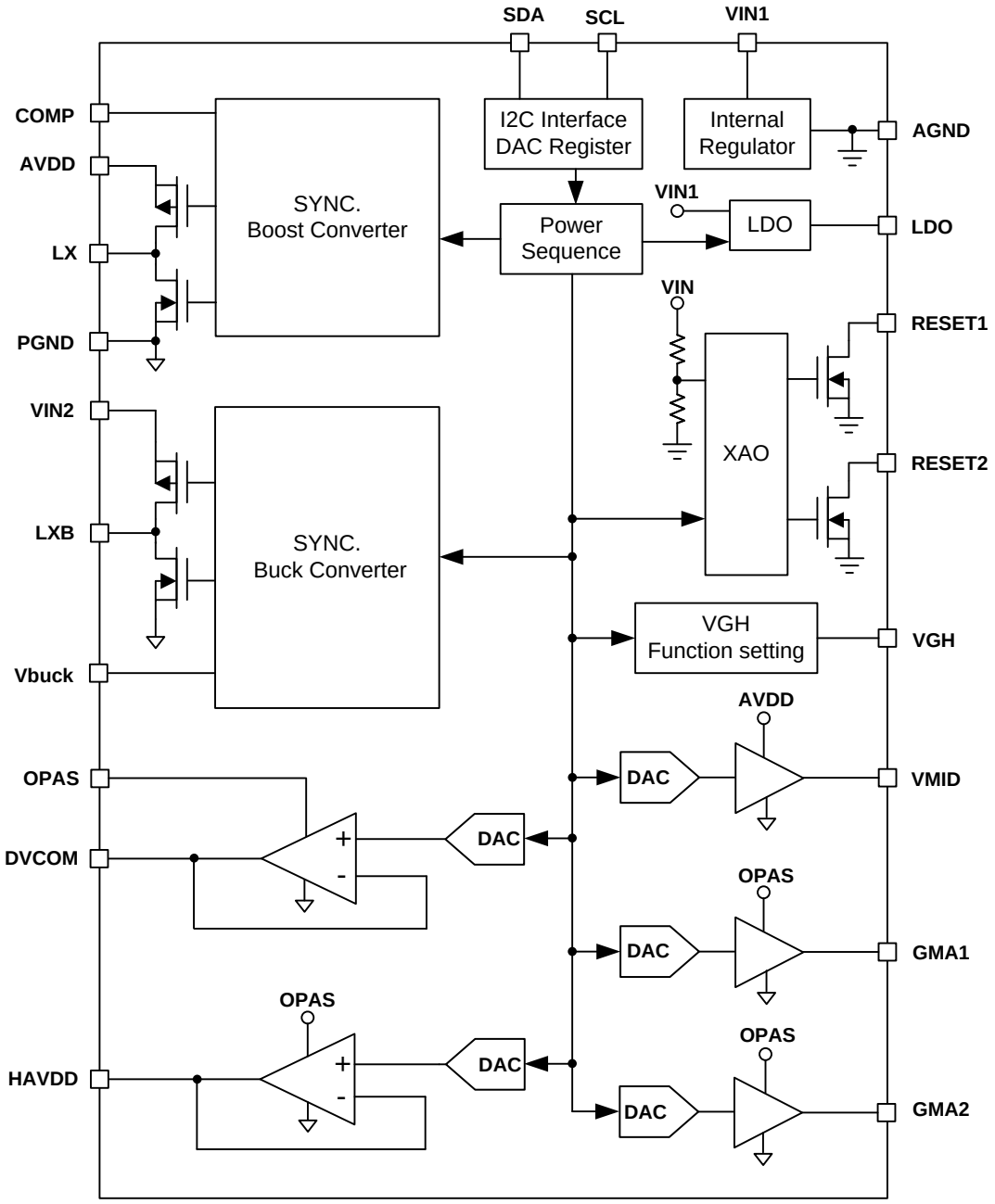
PIN	NAME	I/O/P	FUNCTION
1	SCL	I	Clock Input for I2C interface.
2	SDA	I/O	Serial data input/output for I2C Interface.
3	RESET1	O	Output of voltage detector function.
4	PGND	G	Power ground.
5	OPAS	I	Operation amplifier positive power supply.
6	VCOM	O	VCOM OP-amp output.
7	HAVDD	O	HVADD output.
8	GMA1	O	Gamma1 output pin.
9	GMA2	O	Gamma2 output pin.
10	AGND	P	Analog Ground.
11	LDO	O	LDO Output
12	COMP	O	AVDD Boost converter compensation input.
13	VIN1	P	IC supply voltage input1.
14	PGND	G	Power ground.
15	LX	P	Switching Pin of AVDD Boost Converter
16	LX	P	Switching Pin of AVDD Boost Converter
17	AVDD	O	Output of AVDD Boost Converter
18	VMID	O	VDC output.
19	VGH	O	Output of VGH.
20	PGND	G	Power ground.
21	LXB	P	Vbuck buck switching node.
22	VIN2	P	IC supply voltage input2.
23	Vbuck	I	Vbuck output feedback.
24	RESET2	O	Output of voltage detector function.
	PGND (Exposed Pad)	P	GND. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Note: P: power/ground; I: Input; O: Output; I/O: Bi-direction

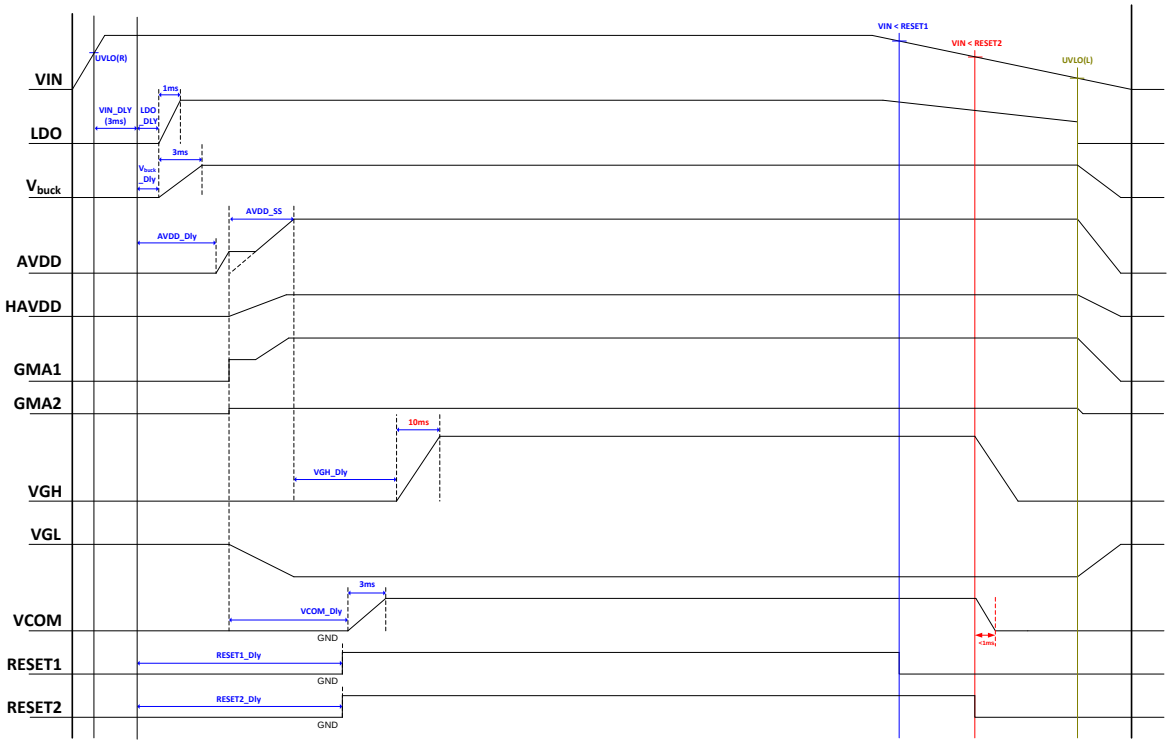
Application Circuit :



Block Diagram



Timing Diagram :



Note :

1. HAVDD/GAM1/GAM2 can power on with AVDD, but the voltage level can't be higher than AVDD
2. AVDD power on sequence : imbedded MOS for AVDD isolation.
3. VCOM power on delay time range: ~155ms, Power off VCOM to GND ⩽ 1ms.

Device Address Setting

PMIC Device Address 7'b1110100

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PMIC Slave Address 7'b1110100							Read:1 Write:0

Configuration Parameter VCOM Device Address 7'b1001111

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Configuration Parameter VCOM Slave Address 7'b1001111							Read:1 Write:0

PMIC I^{2}C Command

Write Operation

(a) Write Single Byte to DAC Register

Example : Writing 29h to DAC Address 07h

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		
Start	1	1	1	0	1	0	0	0	Slave ACK	0	0	0	0	0	1	1	1	Slave ACK	0	0	1	0	1	0	0	1	Slave ACK	Stop

(b) Write Multi Byte to DAC Register

Example : Writing 29h, 2Ah, 2Bh to DAC Address 06h, 07h, 08h

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
Start	1	1	1	0	1	0	0	0	Slave ACK	0	0	0	0	0	1	1	0	Slave ACK	0	0	1	0	1	0	0	1	Slave ACK

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		
0	0	1	0	1	0	1	0	Slave ACK	0	0	1	0	1	0	1	1	Slave ACK	Stop

(C) Write All DAC Register into EEPROM

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		
1	1	1	0	1	0	0	0	Slave ACK	1	1	1	1	1	1	1	1	Slave ACK	1	0	0	0	0	0	0	0	Slave ACK	Stop

Read Operation

(a) Read data form DAC register

Example : Reading Data form DAC Register Address 08h, 09h, 0Ah, 0Bh

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		
Start	1	1	1	0	1	0	0	0	Slave ACK	1	1	1	1	1	1	1	1	Slave ACK	0	0	0	0	0	0	0	0	Slave ACK	Stop

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
Start	1	1	1	0	1	0	0	0	Slave ACK	0	0	0	0	1	0	0	0	Slave ACK

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
Repeat Start	1	1	1	0	1	0	0	1	Slave ACK	D	D	D	D	D	D	D	D	Master ACK	D	D	D	D	D	D	D	D	Master ACK

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		
D	D	D	D	D	D	D	D	Master ACK	D	D	D	D	D	D	D	D	Master N-ACK	Stop

(b) Read data form EEPROM

Example : Reading Data form EEPROM Address 03h, 04h, 05h, 06h

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		
Start	1	1	1	0	1	0	0	0	Slave ACK	1	1	1	1	1	1	1	1	Slave ACK	0	0	0	0	0	0	0	1	Slave ACK	Stop

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
Start	1	1	1	0	1	0	0	0	Slave ACK	0	0	0	0	0	0	1	1	Slave ACK

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
Repeat Start	1	1	1	0	1	0	0	1	Slave ACK	D	D	D	D	D	D	D	D	Master ACK	D	D	D	D	D	D	D	D	Master ACK

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		
D	D	D	D	D	D	D	D	Master ACK	D	D	D	D	D	D	D	D	Master N-ACK	Stop

Configuration Parameter VCOM I²C Command

Write Operation

(a) Write Single Byte to DAC Register

Example : Writing 77h (7bit data) to DAC

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		
Start	1	0	0	1	1	1	1	0	Slave ACK	1	1	1	0	1	1	1	1	Slave ACK	Stop

(b) Write Single Byte to DAC Register and EEPROM

Example : Writing 77h (7bit data) to DAC and EEPROM

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		
Start	1	0	0	1	1	1	1	0	Slave ACK	1	1	1	0	1	1	1	0	Slave ACK	Stop

Read Operation

(a) Read Single data from DAC when DAC data same as EEPROM

Example : Read Data from DAC

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		
Start	1	0	0	1	1	1	1	1	Slave ACK	D	D	D	D	D	D	D	0	Slave ACK	Stop

(b) Read Single data from DAC when DAC data different to EEPROM

Example : Read Data from DAC

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		
Start	1	0	0	1	1	1	1	1	Slave ACK	D	D	D	D	D	D	D	1	Slave ACK	Stop

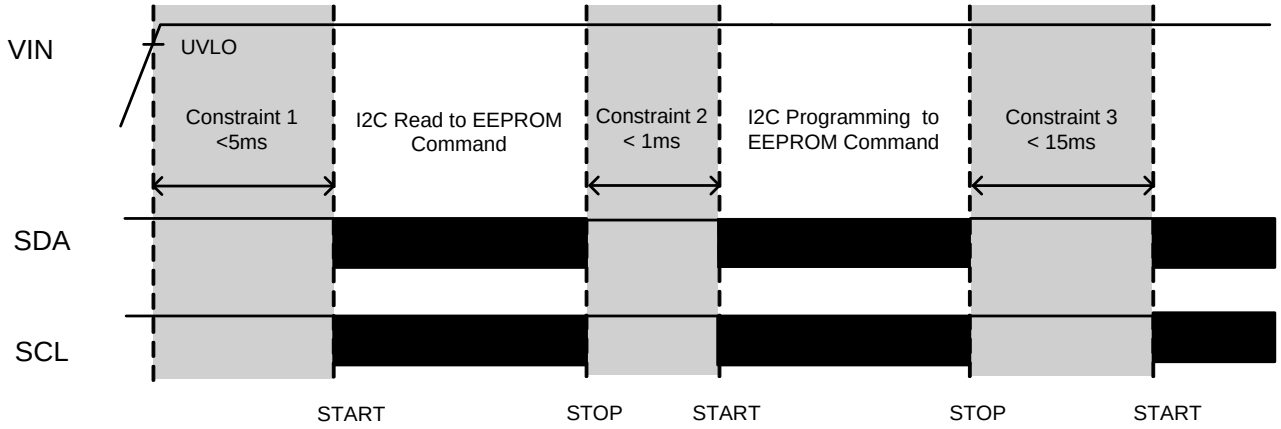
PMIC Register Map :

PMIC Device Address : 0xE8h

DVCOM Device Address : 0x9Eh

Note	Inst/Prar	7	6	5	4	3	2	1	0	register default	description
	0x00h	RESET1_Enable	GMA1/GMA2 _Enable	VCOM_Enable	HAVDD_Enable	VLDO_Enable	VGH_Enable	Vbuck_Enable	AVDD_Enable	0xFFh	Channel setting [7:0] : 0h=Disable 1h=Enable
	0x01					VCOM off follow RESET2	VGH off follow RESET2	Vbuck off follow RESET2	RESET2_Enable	0x09h	RESET2 setting [0] : 0h=Disable 1h=Enable
	0x02h					VGH_discharge	AVDD_discharge	Vbuck_discharge	VCOM_discharge	0x01h	Channel discharge setting [3:0] : 0h=Disable 1h=Enable
	0x03h		AVDD Voltage							0x14h	AVDD Voltage [6:0] : adjust AVDD output range 7V~13.5V, Resolution : 0.1V/step default : 9V
	0x04h			Vbuck Voltage						0x08h	Vbuck Voltage [5:0] : adjust Vbuck output range 0.8V~2.8V, Resolution : 0.05V/step default : 1.2V
	0x05h				VGH Voltage					0x0Ch	VGH Voltage [4:0] adjust VMID output range 10~34V, Resolution : 1V/step default : 22V
	0x06h				VLDO Voltage					0x0Fh	VLDO Voltage [4:0] : adjust VLDO output range 1.0V~2.8V, Resolution : 0.1V/step default : 2.5V
	0x07h		HAVDD Voltage							0x28h	HAVDD Voltage [6:0] : adjust VCOM output range 2.5V~7.0V, Resolution : 0.05V/step default : 4.5V
	0x08h	VCOM Voltage								0x3Ch	VCOM Voltage [7:0] : adjust VCOM output range 2.5V~7.0V, Resolution : 0.02V/step default : 3.7V
	0x09h			GMA1 Voltage						0x05h	GMA1 Voltage [5:0] : adjust GMA1 output range AVDD-0.1V~AVDD-1V, Resolution : 0.02V/step default : AVDD-(10*0.02)V
	0x0Ah			GMA2 Voltage						0x0Fh	GMA2 Voltage [5:0] : adjust GMA2 output range 0.1V~1.0V, Resolution : 0.02V/step default :0.4V
	0x0Bh			RESET2 Voltage			RESET1 Voltage			0x1Ch	RESET1 Voltage [3:0] : adjust RESET1 output range 2.0V~2.7V, Resolution : 0.1V/step default : 2.3V RESET2 Voltage [3:0] : adjust RESET2 output range 2.0V~2.7V, Resolution : 0.1V/step default : 2.2V
	0x0Ch		AVDD LX Slew Rate_Fall		AVDD LX Slew Rate_Rise		AVDD FREQ.			0x29h	AVDD FREQ. [2:0] : adjust AVDD FREQ. Range 600kHz~1225kHz default : 715kHz AVDD Slew Rate_Rise [4:3] : adjust AVDD Slew Rate_Rise range default : Normal (0x01) AVDD Slew Rate_Fall [6:5] : adjust AVDD Slew Rate_Fall range default : Normal (0x01)
	0x0Dh		AVDD Current Limit		AVDD Soft Start Time		AVDD Delay Time			0x22h	AVDD Delay Time [2:0] : adjust AVDD Delay Time Range 0ms~35ms Resolution :5ms default : 10ms AVDD Soft Start Time [4:3] : adjust AVDD Soft Start Time range 5ms~20ms Resolution :5ms default : 5ms AVDD Current Limit [6:5] : adjust AVDD Current Limit range 0.5A~2.0A Resolution : 0.5A default : 1A
	0x0Eh				VGH delay off	VGH Delay Time				0x03h	VGH Delay Time [3:0] : adjust VGH Delay Time Range 0ms~35ms Resolution :5ms default : 20ms VGH delay off [4] : 0h=Disable 1h=Enable
	0x0Fh		Vbuck Current Limit		LXB Slew Rate		LXB FREQ.			0x29h	LXB FREQ. [2:0] : adjust Vbuck FREQ. Range 600kHz~1225kHz default : 715kHz LXB Slew Rate [4:3] : adjust Vbuck Slew Rate range default : Normal (0x01h) Vbuck Current Limit [6:5] : adjust Vbuck Current Limit range 0.5A~2.0A Resolution : 0.5A default : 1A
	0x10h					VLDO Delay Time		Vbuck Delay Time		0x05h	Vbuck Delay Time [1:0] : adjust VCORE Delay Time Range 0ms~9ms Resolution :3ms default : 3ms VLDO Delay Time [1:0] : adjust VLDO Delay Time Range 0ms~9ms Resolution :3ms default : 3ms
	0x11h	RESET2 Delay Time				RESET1 Delay Time				0x88h	RESET1 Delay Time [3:0] : adjust RESET1 Delay Time Range 0ms~75ms Resolution :5ms default : 35ms RESET2 Delay Time [7:4] : adjust RESET2 Delay Time Range 0ms~75ms Resolution :5ms default : 35ms
	0x12h				VCOM Delay Time					0x05h	VCOM Delay Time [4:0] : adjust VCOM Delay Time Range 0ms~155ms Resolution :5ms default : 25ms
		Configuration Parameter VCOM									
	0xFF	Control Register									00 : Read data form DAC register 01 : Read data from EEPROM 80 : Write all DAC into EEPROM

I²C Communication Timing Chart



Constraint 1: EEPROM start up blanking time.
It is the time from VIN powered up (after UVLO threshold) to the end of loading EEPROM data to DAC. Any attempt from the I²C master talking to G2517A is not acknowledged.

Constraint 2: Read to EEPROM blanking time
It is the time from a valid stop condition of a EEPROM read command to the end of the internal operation cycle. Any attempt from the I²C master talking to G2517A is not acknowledged.

Constraint 3: Programming EEPROM blanking time.
It is the time from a valid stop condition of a EEPROM write command to the end of internal EEPROM programming operation. Any attempt from the I²C master talking to G2517A is not acknowledged.

Registers and DAC Settings

AVDD Voltage Register – Address 0x03h [6:0]

DAC Value	AVDD Voltage (V)	DAC Value	AVDD Voltage (V)	DAC Value	AVDD Voltage (V)	DAC Value	AVDD Voltage (V)
00h	7.0	11h	8.7	22h	10.4	33h	12.1
01h	7.1	12h	8.8	23h	10.5	34h	12.2
02h	7.2	13h	8.9	24h	10.6	35h	12.3
03h	7.3	14h	9.0	25h	10.7	36h	12.4
04h	7.4	15h	9.1	26h	10.8	37h	12.5
05h	7.5	16h	9.2	27h	10.9	38h	12.6
06h	7.6	17h	9.3	28h	11.0	39h	12.7
07h	7.7	18h	9.4	29h	11.1	3Ah	12.8
08h	7.8	19h	9.5	2Ah	11.2	3Bh	12.9
09h	7.9	1Ah	9.6	2Bh	11.3	3Ch	13.0
0Ah	8.0	1Bh	9.7	2Ch	11.4	3Dh	13.1
0Bh	8.1	1Ch	9.8	2Dh	11.5	3Eh	13.2
0Ch	8.2	1Dh	9.9	2Eh	11.6	3Fh	13.3
0Dh	8.3	1Eh	10.0	2Fh	11.7	40h	13.4
0Eh	8.4	1Fh	10.1	30h	11.8	41h	13.5
0Fh	8.5	20h	10.2	31h	11.9		
10h	8.6	21h	10.3	32h	12.0		

AVDD LX Frequency Register – Address 0x0Ch [2:0]

DAC Value	LX FREQ (KHz)	DAC Value	LX FREQ (KHz)	DAC Value	LX FREQ (KHz)	DAC Value	LX FREQ (KHz)
00h	600	02h	800	04h	1000	05h	1225
01h	715	03h	933				

AVDD LX Slew Rate_Rise – Address 0x0Ch [4:3]

DAC Value	S.R. Time (ms)	DAC Value	S.R. Time (ms)	DAC Value	S.R. Time (ms)	DAC Value	S.R. Time (ms)
00h	Fast	01h	Normal	02h	Slow	03h	Slowest

AVDD LX Slew Rate_Fall – Address 0x0Ch [6:5]

DAC Value	S.R. Time (ms)	DAC Value	S.R. Time (ms)	DAC Value	S.R. Time (ms)	DAC Value	S.R. Time (ms)
00h	Fast	01h	Normal	02h	Slow	03h	Slowest

AVDD Current Limit Register – Address 0x0Dh [6:5]

DAC Value	Current Limit (A)	DAC Value	Current Limit (A)	DAC Value	Current Limit (A)	DAC Value	Current Limit (A)
00h	0.5	01h	1.0	02h	1.5	03h	2.0

AVDD Delay Time Register – Address 0x0Dh [2:0]

DAC Value	Delay Time (ms)	DAC Value	Delay Time (ms)	DAC Value	Delay Time (ms)	DAC Value	Delay Time (ms)
00h	0	02h	10	04h	20	06h	30
01h	5	03h	15	05h	26	07h	35

AVDD Soft-Start Time Register – Address 0x0Dh [4:3]

DAC Value	SS Time (ms)	DAC Value	SS Time (ms)	DAC Value	SS Time (ms)	DAC Value	SS Time (ms)
00h	5	01h	10	02h	15	03h	20

Vbuck Voltage Register – Address 0x04h [4:0]

DAC Value	Vbuck Voltage (V)	DAC Value	Vbuck Voltage (V)	DAC Value	Vbuck Voltage (V)	DAC Value	Vbuck Voltage (V)
00h	0.8	0Bh	1.35	16h	1.9	21h	2.45
01h	0.85	0Ch	1.4	17h	1.95	22h	2.5
02h	0.9	0Dh	1.45	18h	2	23h	2.55
03h	0.95	0Eh	1.5	19h	2.05	24h	2.6
04h	1	0Fh	1.55	1Ah	2.1	25h	2.65
05h	1.05	10h	1.6	1Bh	2.15	26h	2.7
06h	1.1	11h	1.65	1Ch	2.2	27h	2.75
07h	1.15	12h	1.7	1Dh	2.25	28h	2.8
08h	1.2	13h	1.75	1Eh	2.3		
09h	1.25	14h	1.8	1Fh	2.35		
0Ah	1.3	15h	1.85	20h	2.4		

LXB Frequency Register – Address 0x0Fh [2:0]

DAC Value	LXB FREQ (KHz)	DAC Value	LXB FREQ (KHz)	DAC Value	LXB FREQ (KHz)	DAC Value	LXB FREQ (KHz)
00h	600	02h	800	04h	1000	05h	1225
01h	715	03h	933				

LXB Slew Rate – Address 0x0Fh [4:3]

DAC Value	S.R. Time (ms)	DAC Value	S.R. Time (ms)	DAC Value	S.R. Time (ms)	DAC Value	S.R. Time (ms)
00h	Fast	01h	Normal	02h	Slow	03h	Slowest

Vbuck Current Limit Register – Address 0x0Fh [6:5]

DAC Value	Current Limit (A)	DAC Value	Current Limit (A)	DAC Value	Current Limit (A)	DAC Value	Current Limit (A)
00h	0.5	01h	1.0	02h	1.5	03h	2.0

Vbuck Delay Time Register – Address 0x10h [1:0]

DAC Value	Delay Time (ms)	DAC Value	Delay Time (ms)	DAC Value	Delay Time (ms)	DAC Value	Delay Time (ms)
00h	0	01h	3	02h	6	03h	9

LDO Voltage Register – Address 0x06h [3:0]

DAC Value	LDO Voltage (V)	DAC Value	LDO Voltage (V)	DAC Value	LDO Voltage (V)	DAC Value	LDO Voltage (V)
00h	1.0	05h	1.5	0Ah	2.0	0Fh	2.5
01h	1.1	06h	1.6	0Bh	2.1	10h	2.6
02h	1.2	07h	1.7	0Ch	2.2	11h	2.7
03h	1.3	08h	1.8	0Dh	2.3	12h	2.8
04h	1.4	09h	1.9	0Eh	2.4		

VLDO Delay Time Register – Address 0x11h [1:0]

DAC Value	Delay Time (ms)	DAC Value	Delay Time (ms)	DAC Value	Delay Time (ms)	DAC Value	Delay Time (ms)
00h	0	01h	3	02h	6	03h	9

VGH Voltage Register – Address 0x05h [4:0]

DAC Value	VGH Voltage (V)	DAC Value	VGH Voltage (V)	DAC Value	VGH Voltage (V)	DAC Value	VGH Voltage (V)
00h	10	07h	17	0Eh	24	15h	31
01h	11	08h	18	0Fh	25	16h	32
02h	12	09h	19	10h	26	17h	33
03h	13	0Ah	20	11h	27	18h	34
04h	14	0Bh	21	12h	28		
05h	15	0Ch	22	13h	29		
06h	16	0Dh	23	14h	30		

VGH Delay Time Register – Address 0x0Eh [3:0]

DAC Value	Delay Time (ms)	DAC Value	Delay Time (ms)	DAC Value	Delay Time (ms)	DAC Value	Delay Time (ms)
00h	0	03h	15	06h	30	09h	45
01h	5	04h	20	07h	35	0Ah	50
02h	10	05h	25	08h	40	0Bh	55

HAVDD Voltage Register – Address 0x07h [6:0]

DAC Value	HAVDD Voltage (V)	DAC Value	HAVDD Voltage (V)	DAC Value	HAVDD Voltage (V)	DAC Value	HAVDD Voltage (V)
00h	2.5	17h	3.65	2Eh	4.8	45h	5.95
01h	2.55	18h	3.7	2Fh	4.85	46h	6
02h	2.6	19h	3.75	30h	4.9	47h	6.05
03h	2.65	1Ah	3.8	31h	4.95	48h	6.1
04h	2.7	1Bh	3.85	32h	5	49h	6.15
05h	2.75	1Ch	3.9	33h	5.05	4Ah	6.2
06h	2.8	1Dh	3.95	34h	5.1	4Bh	6.25
07h	2.85	1Eh	4	35h	5.15	4Ch	6.3
08h	2.9	1Fh	4.05	36h	5.2	4Dh	6.35
09h	2.95	20h	4.1	37h	5.25	4Eh	6.4
0Ah	3	21h	4.15	38h	5.3	4Fh	6.45
0Bh	3.05	22h	4.2	39h	5.35	50h	6.5
0Ch	3.1	23h	4.25	3Ah	5.4	51h	6.55
0Dh	3.15	24h	4.3	3Bh	5.45	52h	6.6
0Eh	3.2	25h	4.35	3Ch	5.5	53h	6.65
0Fh	3.25	26h	4.4	3Dh	5.55	54h	6.7
10h	3.3	27h	4.45	3Eh	5.6	55h	6.75
11h	3.35	28h	4.5	3Fh	5.65	56h	6.8
12h	3.4	29h	4.55	40h	5.7	57h	6.85
13h	3.45	2Ah	4.6	41h	5.75	58h	6.9
14h	3.5	2Bh	4.65	42h	5.8	59h	6.95
15h	3.55	2Ch	4.7	43h	5.85	5Ah	7
16h	3.6	2Dh	4.75	44h	5.9		

RESET1 Voltage Register – Address 0x0Bh [2:0]

DAC Value	RESET1 Voltage (V)	DAC Value	RESET1 Voltage (V)	DAC Value	RESET1 Voltage (V)	DAC Value	RESET1 Voltage (V)
00h	2.0	02h	2.2	04h	2.4	06h	2.6
01h	2.1	03h	2.3	05h	2.5	07h	2.7

RESET1 Delay Time Register – Address 0x12h [3:0]

DAC Value	Delay Time (ms)	DAC Value	Delay Time (ms)	DAC Value	Delay Time (ms)	DAC Value	Delay Time (ms)
00h	0	04h	20	08h	40	0Ch	60
01h	5	05h	25	09h	45	0Dh	65
02h	10	06h	30	0Ah	50	0Eh	70
03h	15	07h	35	0Bh	55	0Fh	75

RESET2 Voltage Register – Address 0x0Bh [5:3]

DAC Value	RESET2 Voltage (V)	DAC Value	RESET2 Voltage (V)	DAC Value	RESET2 Voltage (V)	DAC Value	RESET2 Voltage (V)
00h	2.0	02h	2.2	04h	2.4	06h	2.6
01h	2.1	03h	2.3	05h	2.5	07h	2.7

RESET2 Delay Time Register – Address 0x12h [7:4]

DAC Value	Delay Time (ms)	DAC Value	Delay Time (ms)	DAC Value	Delay Time (ms)	DAC Value	Delay Time (ms)
00h	0	04h	20	08h	40	0Ch	60
01h	5	05h	25	09h	45	0Dh	65
02h	10	06h	30	0Ah	50	0Eh	70
03h	15	07h	35	0Bh	55	0Fh	75

GMA1 Voltage Register – Address 0x09h [4:0]

DAC Value	GMA1 Voltage (V)	DAC Value	GMA1 Voltage (V)	DAC Value	GMA1 Voltage (V)	DAC Value	GMA1 Voltage (V)
00h	(AVDD-20mVx5)	0Bh	(AVDD-20mVx16)	16h	(AVDD-20mVx27)	22h	(AVDD-20mVx39)
01h	(AVDD-20mVx6)	0Ch	(AVDD-20mVx17)	17h	(AVDD-20mVx28)	23h	(AVDD-20mVx40)
02h	(AVDD-20mVx7)	0Dh	(AVDD-20mVx18)	18h	(AVDD-20mVx29)	24h	(AVDD-20mVx41)
03h	(AVDD-20mVx8)	0Eh	(AVDD-20mVx19)	19h	(AVDD-20mVx30)	25h	(AVDD-20mVx42)
04h	(AVDD-20mVx9)	0Fh	(AVDD-20mVx20)	1Ah	(AVDD-20mVx31)	26h	(AVDD-20mVx43)
05h	(AVDD-20mVx10)	10h	(AVDD-20mVx21)	1Bh	(AVDD-20mVx32)	27h	(AVDD-20mVx44)
06h	(AVDD-20mVx11)	11h	(AVDD-20mVx22)	1Ch	(AVDD-20mVx33)	28h	(AVDD-20mVx45)
07h	(AVDD-20mVx12)	12h	(AVDD-20mVx23)	1Dh	(AVDD-20mVx34)	29h	(AVDD-20mVx46)
08h	(AVDD-20mVx13)	13h	(AVDD-20mVx24)	1Eh	(AVDD-20mVx35)	2Ah	(AVDD-20mVx47)
09h	(AVDD-20mVx14)	14h	(AVDD-20mVx25)	1Fh	(AVDD-20mVx36)	2Bh	(AVDD-20mVx48)
0Ah	(AVDD-20mVx15)	15h	(AVDD-20mVx26)	20h	(AVDD-20mVx37)	2Ch	(AVDD-20mVx49)
				21h	(AVDD-20mVx38)	2Dh	(AVDD-20mVx50)

GMA2 Voltage Register – Address 0x0Ah [4:0]

DAC Value	GMA2 Voltage (V)	DAC Value	GMA2 Voltage (V)	DAC Value	GMA2 Voltage (V)	DAC Value	GMA2 Voltage (V)
00h	20mVx5	0Bh	20mVx16	16h	20mVx27	22h	20mVx39
01h	20mVx6	0Ch	20mVx17	17h	20mVx28	23h	20mVx40
02h	20mVx7	0Dh	20mVx18	18h	20mVx29	24h	20mVx41
03h	20mVx8	0Eh	20mVx19	19h	20mVx30	25h	20mVx42
04h	20mVx9	0Fh	20mVx20	1Ah	20mVx31	26h	20mVx43
05h	20mVx10	10h	20mVx21	1Bh	20mVx32	27h	20mVx44
06h	20mVx11	11h	20mVx22	1Ch	20mVx33	28h	20mVx45
07h	20mVx12	12h	20mVx23	1Dh	20mVx34	29h	20mVx46
08h	20mVx13	13h	20mVx24	1Eh	20mVx35	2Ah	20mVx47
09h	20mVx14	14h	20mVx25	1Fh	20mVx36	2Bh	20mVx48
0Ah	20mVx15	15h	20mVx26	20h	20mVx37	2Ch	20mVx49
				21h	20mVx38	2Dh	20mVx50

VCOM Voltage Register – Address 0x08h [7:0]

DAC Value	VCOM(V)	DAC Value	VCOM(V)	DAC Value	VCOM(V)	DAC Value	VCOM(V)	DAC Value	VCOM(V)
00h	2.5	2Dh	3.4	5Ah	4.3	87h	5.2	B4h	6.1
01h	2.52	2Eh	3.42	5Bh	4.32	88h	5.22	B5h	6.12
02h	2.54	2Fh	3.44	5Ch	4.34	89h	5.24	B6h	6.14
03h	2.56	30h	3.46	5Dh	4.36	8Ah	5.26	B7h	6.16
04h	2.58	31h	3.48	5Eh	4.38	8Bh	5.28	B8h	6.18
05h	2.6	32h	3.5	5Fh	4.4	8Ch	5.3	B9h	6.2
06h	2.62	33h	3.52	60h	4.42	8Dh	5.32	BAh	6.22
07h	2.64	34h	3.54	61h	4.44	8Eh	5.34	BBh	6.24
08h	2.66	35h	3.56	62h	4.46	8Eh	5.36	BCh	6.26
09h	2.68	36h	3.58	63h	4.48	90h	5.38	BDh	6.28
0Ah	2.7	37h	3.6	64h	4.5	91h	5.4	BEh	6.3
0Bh	2.72	38h	3.62	65h	4.52	92h	5.42	BFh	6.32
0Ch	2.74	39h	3.64	66h	4.54	93h	5.44	C0h	6.34
0Dh	2.76	3Ah	3.66	67h	4.56	94h	5.46	C1h	6.36
0Eh	2.78	3Bh	3.68	68h	4.58	95h	5.48	C2h	6.38
0Fh	2.8	3Ch	3.7	69h	4.6	96h	5.5	C3h	6.4
10h	2.82	3Dh	3.72	6Ah	4.62	97h	5.52	C4h	6.42
11h	2.84	3Eh	3.74	6Bh	4.64	98h	5.54	C5h	6.44
12h	2.86	3Fh	3.76	6Ch	4.66	99h	5.56	C6h	6.46
13h	2.88	40h	3.78	6Dh	4.68	9Ah	5.58	C7h	6.48
14h	2.9	41h	3.8	6Eh	4.7	9Bh	5.6	C8h	6.5
15h	2.92	42h	3.82	6Fh	4.72	9Ch	5.62	C9h	6.52
16h	2.94	43h	3.84	70h	4.74	9Dh	5.64	CAh	6.54
17h	2.96	44h	3.86	71h	4.76	9Eh	5.66	CBh	6.56
18h	2.98	45h	3.88	72h	4.78	9Fh	5.68	CCh	6.58
19h	3	46h	3.9	73h	4.8	A0h	5.7	CDh	6.6
1Ah	3.02	47h	3.92	74h	4.82	A1h	5.72	CEh	6.62
1Bh	3.04	48h	3.94	75h	4.84	A2h	5.74	CFh	6.64
1Ch	3.06	49h	3.96	76h	4.86	A3h	5.76	D0h	6.66
1Dh	3.08	4Ah	3.98	77h	4.88	A4h	5.78	D1h	6.68
1Eh	3.1	4Bh	4	78h	4.9	A5h	5.8	D2h	6.7
1Fh	3.12	4Ch	4.02	79h	4.92	A6h	5.82	D3h	6.72
20h	3.14	4Dh	4.04	7Ah	4.94	A7h	5.84	D4h	6.74
21h	3.16	4Eh	4.06	7Bh	4.96	A8h	5.86	D5h	6.76
22h	3.18	4Fh	4.08	7Ch	4.98	A9h	5.88	D6h	6.78
23h	3.2	50h	4.1	7Dh	5	AAh	5.9	D7h	6.8
24h	3.22	51h	4.12	7Eh	5.02	ABh	5.92	D8h	6.82
25h	3.24	52h	4.14	7Fh	5.04	ACh	5.94	D9h	6.84
26h	3.26	53h	4.16	80h	5.06	ADh	5.96	DAh	6.86
27h	3.28	54h	4.18	81h	5.08	AEh	5.98	DBh	6.88
28h	3.3	55h	4.2	82h	5.1	AFh	6	DCh	6.9
29h	3.32	56h	4.22	83h	5.12	B0h	6.02	DDh	6.92
2Ah	3.34	57h	4.24	84h	5.14	B1h	6.04	DEh	6.94
2Bh	3.36	58h	4.26	85h	5.16	B2h	6.06	DFh	6.96
2Ch	3.38	59h	4.28	86h	5.18	B3h	6.08	E0h	6.98
								E1h	7

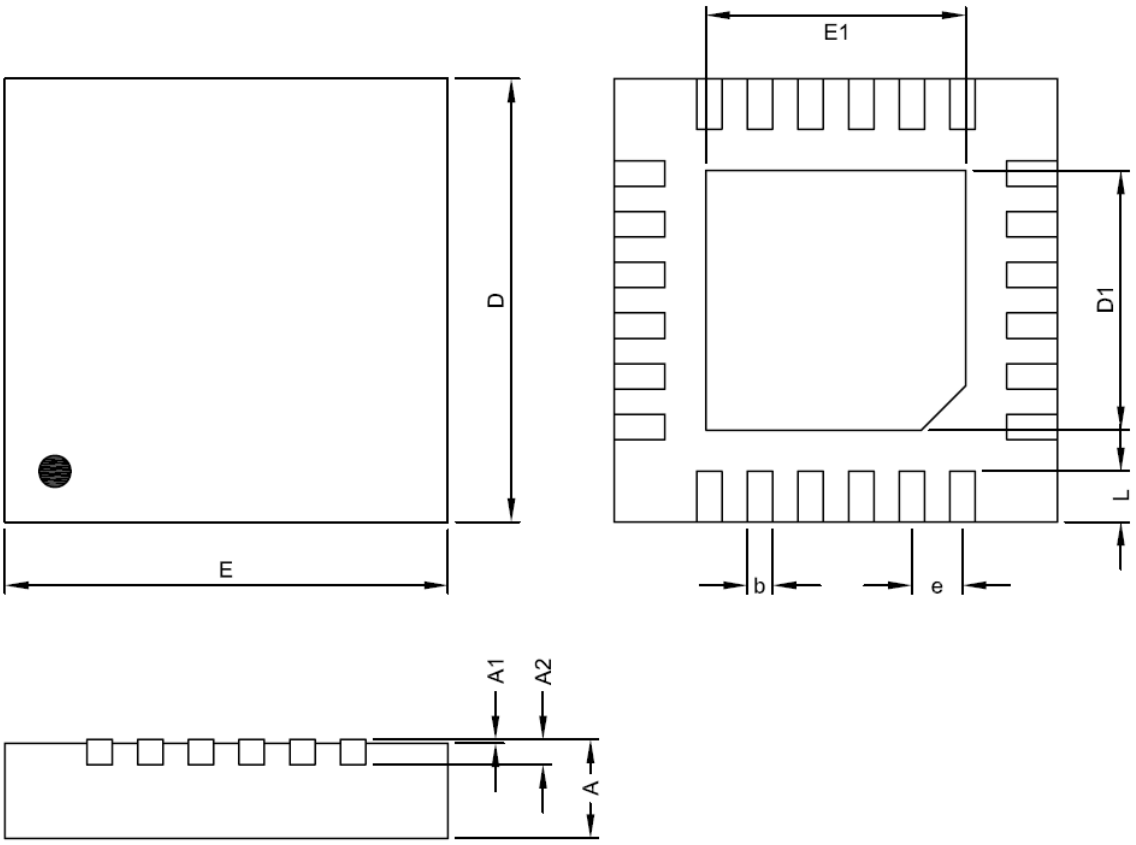
Configuration Parameter VCOM

DAC Value	VCOM Voltage (V)	DAC Value	VCOM Voltage (V)	DAC Value	VCOM Voltage (V)
00h	VCOM-(10mVx64)	2Bh	VCOM-(10mVx21)	56h	VCOM+(10mVx22)
01h	VCOM-(10mVx63)	2Ch	VCOM-(10mVx20)	57h	VCOM+(10mVx23)
02h	VCOM-(10mVx62)	2Dh	VCOM-(10mVx19)	58h	VCOM+(10mVx24)
03h	VCOM-(10mVx61)	2Eh	VCOM-(10mVx18)	59h	VCOM+(10mVx25)
04h	VCOM-(10mVx60)	2Fh	VCOM-(10mVx17)	5Ah	VCOM+(10mVx26)
05h	VCOM-(10mVx59)	30h	VCOM-(10mVx16)	5Bh	VCOM+(10mVx27)
06h	VCOM-(10mVx58)	31h	VCOM-(10mVx15)	5Ch	VCOM+(10mVx28)
07h	VCOM-(10mVx57)	32h	VCOM-(10mVx14)	5Dh	VCOM+(10mVx29)
08h	VCOM-(10mVx56)	33h	VCOM-(10mVx13)	5Eh	VCOM+(10mVx30)
09h	VCOM-(10mVx55)	34h	VCOM-(10mVx12)	5Fh	VCOM+(10mVx31)
0Ah	VCOM-(10mVx54)	35h	VCOM-(10mVx11)	60h	VCOM+(10mVx32)
0Bh	VCOM-(10mVx53)	36h	VCOM-(10mVx10)	61h	VCOM+(10mVx33)
0Ch	VCOM-(10mVx52)	37h	VCOM-(10mVx9)	62h	VCOM+(10mVx34)
0Dh	VCOM-(10mVx51)	38h	VCOM-(10mVx8)	63h	VCOM+(10mVx35)
0Eh	VCOM-(10mVx50)	39h	VCOM-(10mVx7)	64h	VCOM+(10mVx36)
0Fh	VCOM-(10mVx49)	3Ah	VCOM-(10mVx6)	65h	VCOM+(10mVx37)
10h	VCOM-(10mVx48)	3Bh	VCOM-(10mVx5)	66h	VCOM+(10mVx38)
11h	VCOM-(10mVx47)	3Ch	VCOM-(10mVx4)	67h	VCOM+(10mVx39)
12h	VCOM-(10mVx46)	3Dh	VCOM-(10mVx3)	68h	VCOM+(10mVx40)
13h	VCOM-(10mVx45)	3Eh	VCOM-(10mVx2)	69h	VCOM+(10mVx41)
14h	VCOM-(10mVx44)	3Fh	VCOM-(10mVx1)	6AH	VCOM+(10mVx42)
15h	VCOM-(10mVx43)	40h	VCOM	6BH	VCOM+(10mVx43)
16h	VCOM-(10mVx42)	41h	VCOM+(10mVx1)	6CH	VCOM+(10mVx44)
17h	VCOM-(10mVx41)	42h	VCOM+(10mVx2)	6DH	VCOM+(10mVx45)
18h	VCOM-(10mVx40)	43h	VCOM+(10mVx3)	6EH	VCOM+(10mVx46)
19h	VCOM-(10mVx39)	44h	VCOM+(10mVx4)	6FH	VCOM+(10mVx47)
1Ah	VCOM-(10mVx38)	45h	VCOM+(10mVx5)	70H	VCOM+(10mVx48)
1Bh	VCOM-(10mVx37)	46h	VCOM+(10mVx6)	71H	VCOM+(10mVx49)
1Ch	VCOM-(10mVx36)	47h	VCOM+(10mVx7)	72H	VCOM+(10mVx50)
1Dh	VCOM-(10mVx35)	48h	VCOM+(10mVx8)	73H	VCOM+(10mVx51)
1Eh	VCOM-(10mVx34)	49h	VCOM+(10mVx9)	74H	VCOM+(10mVx52)
1Fh	VCOM-(10mVx33)	4Ah	VCOM+(10mVx10)	75H	VCOM+(10mVx53)
20h	VCOM-(10mVx32)	4Bh	VCOM+(10mVx11)	76H	VCOM+(10mVx54)
21h	VCOM-(10mVx31)	4Ch	VCOM+(10mVx12)	77H	VCOM+(10mVx55)
22h	VCOM-(10mVx30)	4Dh	VCOM+(10mVx13)	78H	VCOM+(10mVx56)
23h	VCOM-(10mVx29)	4Eh	VCOM+(10mVx14)	79H	VCOM+(10mVx57)
24h	VCOM-(10mVx28)	4Fh	VCOM+(10mVx15)	7AH	VCOM+(10mVx58)
25h	VCOM-(10mVx27)	50h	VCOM+(10mVx16)	7BH	VCOM+(10mVx59)
26h	VCOM-(10mVx26)	51h	VCOM+(10mVx17)	7CH	VCOM+(10mVx60)
27h	VCOM-(10mVx25)	52h	VCOM+(10mVx18)	7DH	VCOM+(10mVx61)
28h	VCOM-(10mVx24)	53h	VCOM+(10mVx19)	7EH	VCOM+(10mVx62)
29h	VCOM-(10mVx23)	54h	VCOM+(10mVx20)	7FH	VCOM+(10mVx63)
2Ah	VCOM-(10mVx22)	55h	VCOM+(10mVx21)		

VCOM Delay Time Register – Address 0x13h [4:0]

DAC Value	Delay Time (ms)	DAC Value	Delay Time (ms)	DAC Value	Delay Time (ms)	DAC Value	Delay Time (ms)
00h	0	08h	40	10h	80	18h	120
01h	5	09h	45	11h	85	19h	125
02h	10	0Ah	50	12h	90	1Ah	130
03h	15	0Bh	55	13h	95	1Bh	135
04h	20	0Ch	60	14h	100	1Ch	140
05h	25	0Dh	65	15h	105	1Dh	145
06h	30	0Eh	70	16h	110	1Eh	150
07h	35	0Fh	75	17h	115	1Fh	155

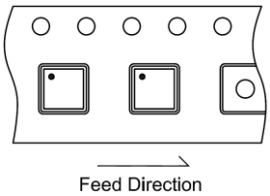
Package Information



TQFN3.5X3.5-24 Package

Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.0276	0.0295	0.0315
A1	0.00	---	0.05	0.0000	---	0.0020
A2	0.20 REF			0.0079 REF		
D	3.45	3.50	3.55	0.1358	0.1378	0.1400
E	3.45	3.50	3.55	0.1358	0.1378	0.1400
D1	1.90	2.05	2.15	0.0748	0.0807	0.0846
E1	1.90	2.05	2.15	0.0748	0.0807	0.0846
b	0.15	0.20	0.25	0.0059	0.0079	0.0098
e	0.40 BSC			0.0157 BSC		
L	0.35	0.40	0.45	0.0137	0.0157	0.0177

Taping Specification



PACKAGE	Q'TY/REEL
TQFN3.5X3.5-24	3,000 ea