Triple High-Voltage Scan Driver for TFT-LCD

Features

- **-20V to 40V High Output Level**
- **High Output Slew Rate to Drive Up to 5nF Load**
- **Power Off Discharge Function**
- **Over Temperature Protection**
- **Output Short Circuit Protection**
- **28-pin, TQFN (4mmx4mm) Package**
- **RoHS Compliant**

Applications

- **TFT LCD**

General Description

The G2583B is a 10-CH high voltage level shifter for TV and monitor LCD applications. It converts logic level signals from Timing Controller (T-CON) to high level signals used by the LCD panel. The outputs are switching from VGL to VGH, with capacitive loads up to 5nF. The G2583B also generates reset function. Once XOA reaches reset level, DISCH1 and DISCH2 will pulled to VGH.

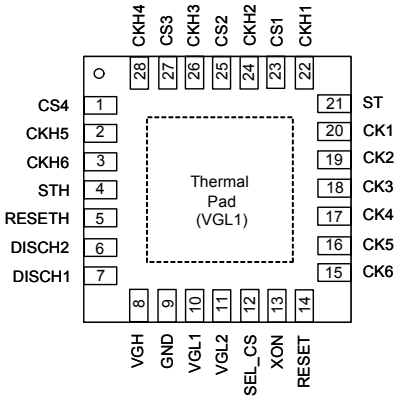
The G2583B features extensive protection functions that include SCP, OTP. It is available in a 4mmx4mm, 28-lead TQFN package.

Ordering Information

ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE (Green)
G2583BRV1U	2583B	-40°C to +85°C	TQFN4X4-28

Note: RV: TQFN4X4-28
1: Bonding Code
U: Tape & Reel
Green : Lead Free / Halogen Free

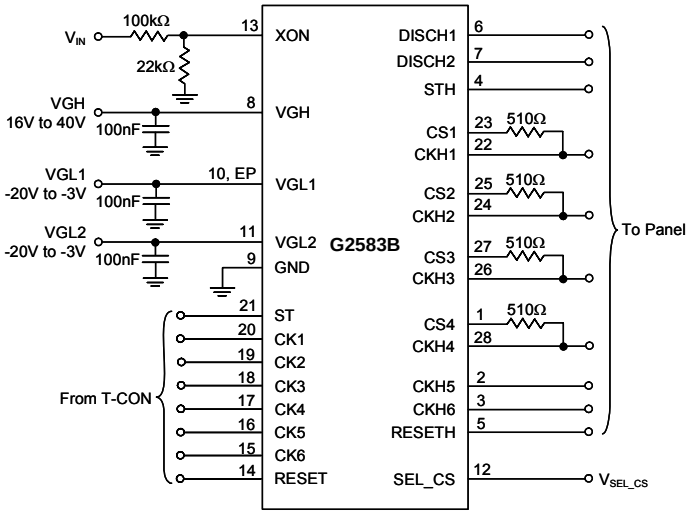
Pin Configuration



G2583B TQFN4X4-28

Note: Recommend connecting the Thermal Pad to the VGL1 for excellent power dissipation.

Typical Application Circuit



Absolute Maximum Ratings

VGH to GND . . . . . -0.3V to +45V
VGL1 to GND . . . . . -25V to +0.3V
VGL2 to GND . . . . . VGL1-0.3V to +0.3V
VGH to VGL . . . . . -0.3V to +62V
ST, RESET, CKx, SEL_CS, XON to GND
. . . . . -0.3V to +5.5V
STH, RESETH, CKHx, CSx, DISCH1 to VGL1
. . . . . -0.3V to VGH+0.3V
DISCH2 to VGL2 . . . . . -0.3V to VGH+0.3V
Thermal Resistance Junction to Ambient, (θ_{JA})
TQFN4X4-28. . . . . 52°C/W
Continuous Power Dissipation (T_A = +25°C)
TQFN4X4-28. . . . . 2000mW
Thermal Resistance Junction to Case, (θ_{JC})
TQFN4X4-28 . . . . . 7°C/W
Operating Temperature Range . . . . . -40°C to 85°C
Junction Temperature . . . . . 150°C
Storage Temperature Range . . . . . -65°C to 150°C
Reflow Temperature (soldering, 10s) . .. . 260°C
ESD Susceptibility
HBM (Human Body Mode) 2kV
MM (Machine Mode) 200V
CDM (Charge Device Mode) 700V

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{GH}=28V, V_{GL1}=V_{GL2}=-15V, GND=0, T_A=25°C)

The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified.

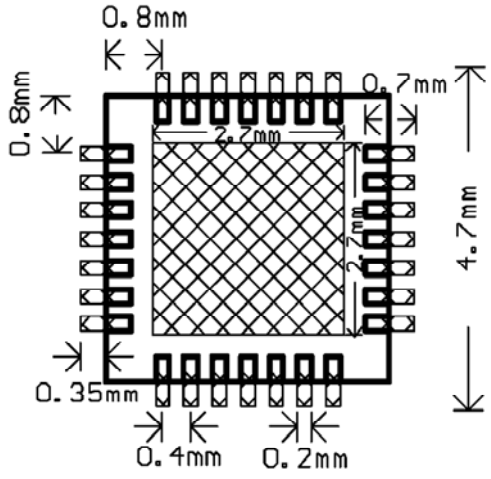
PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
High Voltage Level Shift						
VGH Input Voltage Range	V_{GH}		16	---	40	V
VGL Input Voltage Range	V_{GL}		-20	---	-3	V
Operating Frequency			---	---	100	kHz
CKx, ST Input Voltage	V_{IH}	High	2	---	---	V
	V_{IL}	Low	---	---	0.8	
Input Leakage Current	I_{IL}		-1	---	1	µA
VGH Quiescent Current	I_{VGH}		300	400	600	µA
CKH1 to CKH6 On-Resistance (P-MOSFET)	$R_{DS(ON)\_P}$	I_{LOAD}=10mA	---	12	25	Ω
CKH1 to CKH6 On-Resistance (N-MOSFET)	$R_{DS(ON)\_N}$	I_{LOAD}=10mA	---	8	15	Ω
DISCH1 On-Resistance (P-MOSFET)	$R_{DS(ON)\_P}$	I_{LOAD}=10mA	---	12	25	Ω
DISCH1 On-Resistance (N-MOSFET)	$R_{DS(ON)\_N}$	I_{LOAD}=10mA	---	3	10	Ω
DISCH2 On-Resistance (P-MOSFET)	$R_{DS(ON)\_P}$	I_{LOAD}=10mA	---	35	60	Ω
DISCH2 On-Resistance (N-MOSFET)	$R_{DS(ON)\_N}$	I_{LOAD}=10mA	---	10	20	Ω
STH, RESETH On-Resistance (P-MOSFET)	$R_{DS(ON)\_P}$	I_{LOAD}=10mA	---	35	60	Ω
Panel Discharge Detection Threshold	V_{XON}		1.14	1.2	1.26	V
STH, RESETH Falling Slew Rate	Slew-	C_{LOAD}=4.7nF	30	55	---	V/µs
STH, RESETH Rising Slew Rate	Slew+	C_{LOAD}=4.7nF	20	35	---	V/µs
STH, RESETH, CKHx Rising Propagation Delay	t_{pr}	C_{LOAD}=4.7nF	30	60	100	ns
STH, RESETH, CKHx Falling Propagation Delay	t_{pf}	C_{LOAD}=4.7nF	40	60	100	ns
CKHx Rising Charge Sharing Propagation Delay	t_{cspr}	C_{LOAD}=4.7nF	---	80	150	ns
CKHx Falling Charge Sharing Propagation Delay	t_{cspf}	C_{LOAD}=4.7nF	---	80	150	ns
CKHx Rising Slew Rate	Slew+	C_{LOAD}=4.7nF, R=50Ω	50	100	---	V/µs
CKHx Falling Slew Rate	Slew-	C_{LOAD}=4.7nF, R=50Ω	70	130	---	V/µs
Under Voltage Lockout Threshold	V_{UVLO}	VGH Rising	14	15	16	V
		VGH Falling	2	3.5	5	
Charge Sharing Selection Threshold	V_{SEL_CS}	Disable Charge Sharing	0	---	0.5	V
		Charge Sharing Selection1	1	---	2	
		Charge Sharing Selection2	2.8	---	5.5	
SEL_CS Internal Pull=Down Resistor	R_{SEL_CS}		50	100	200	kΩ
Thermal Shutdown Temperature	T_{SD}	Rising	130	150	170	°C
	T_{HYS}	Hysteresis	---	20	---	
Short Circuit Protection threshold	I_{SCP}		60	---	200	mA

Pin Description

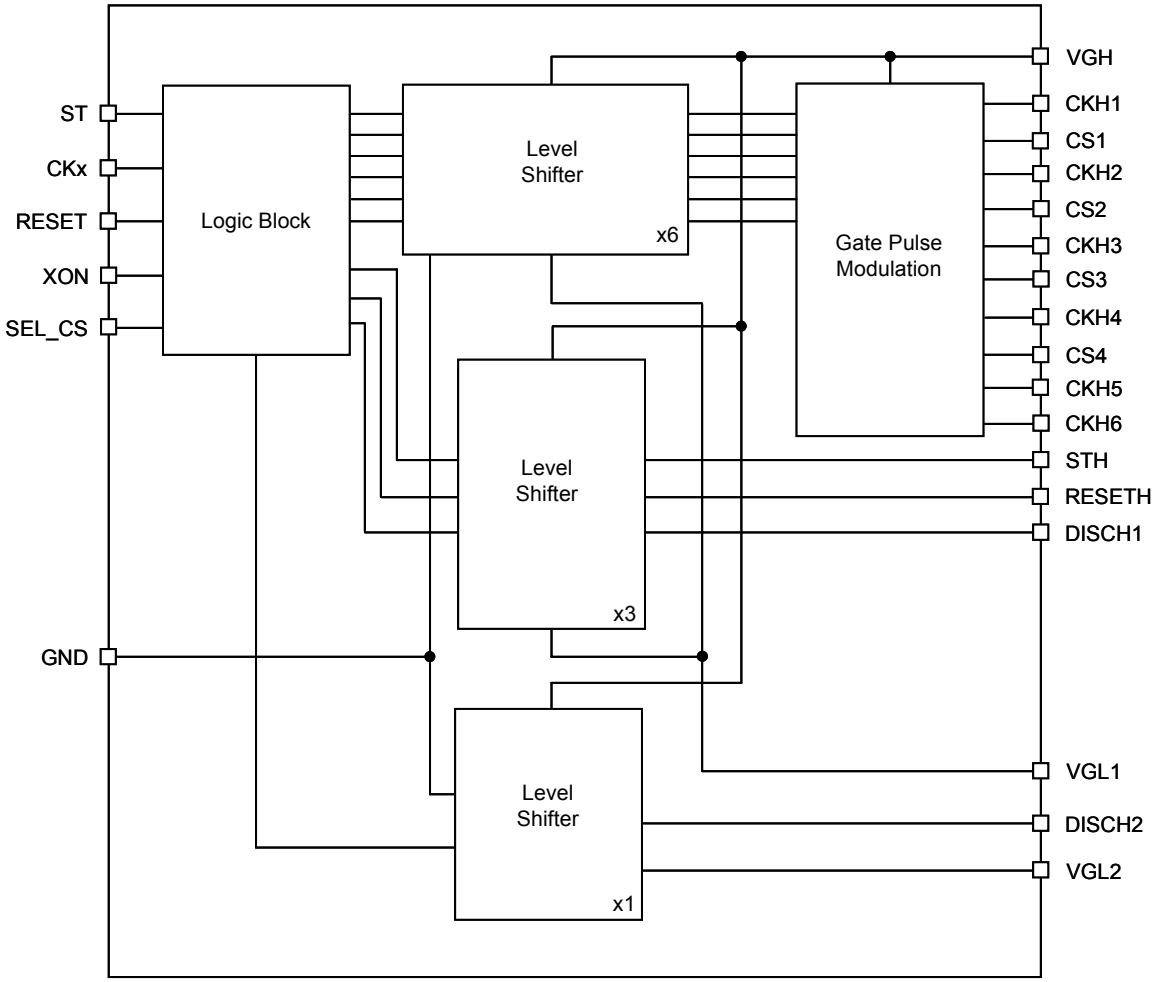
PIN	NAME	FUNCTION
1	CS4	Level Shift Output Charge Sharing.
2	CKH5	Level Shift Output.
3	CKH6	Level Shift Output.
4	STH	Start Pulse Output.
5	RESETH	Reset Output.
6	DISCH2	Discharge Output.
7	DISCH1	Discharge Output.
8	VGH	Level Shift Positive Input Power.
9	GND	Ground Pin.
10, EP	VGL1	Level Shift Negative Input Power, Lowest Voltage.
11	VGL2	Level Shift Negative Input Power.
12	SEL_CS	Charge Sharing Selection.
13	XON	XON Function Sense.
14	RESET	Reset Input.
15	CK6	Level Shift Input.
16	CK5	Level Shift Input.
17	CK4	Level Shift Input.
18	CK3	Level Shift Input.
19	CK2	Level Shift Input.
20	CK1	Level Shift Input.
21	ST	Start Pulse Input.
22	CKH1	Level Shift Output.
23	CS1	Level Shift Output Charge Sharing.
24	CKH2	Level Shift Output.
25	CS2	Level Shift Output Charge Sharing.
26	CKH3	Level Shift Output.
27	CS3	Level Shift Output Charge Sharing.
28	CKH4	Level Shift Output.

Minimum Footprint PCB Layout Section

TQFN4X4-28



Function Block Diagram



Timing Diagram

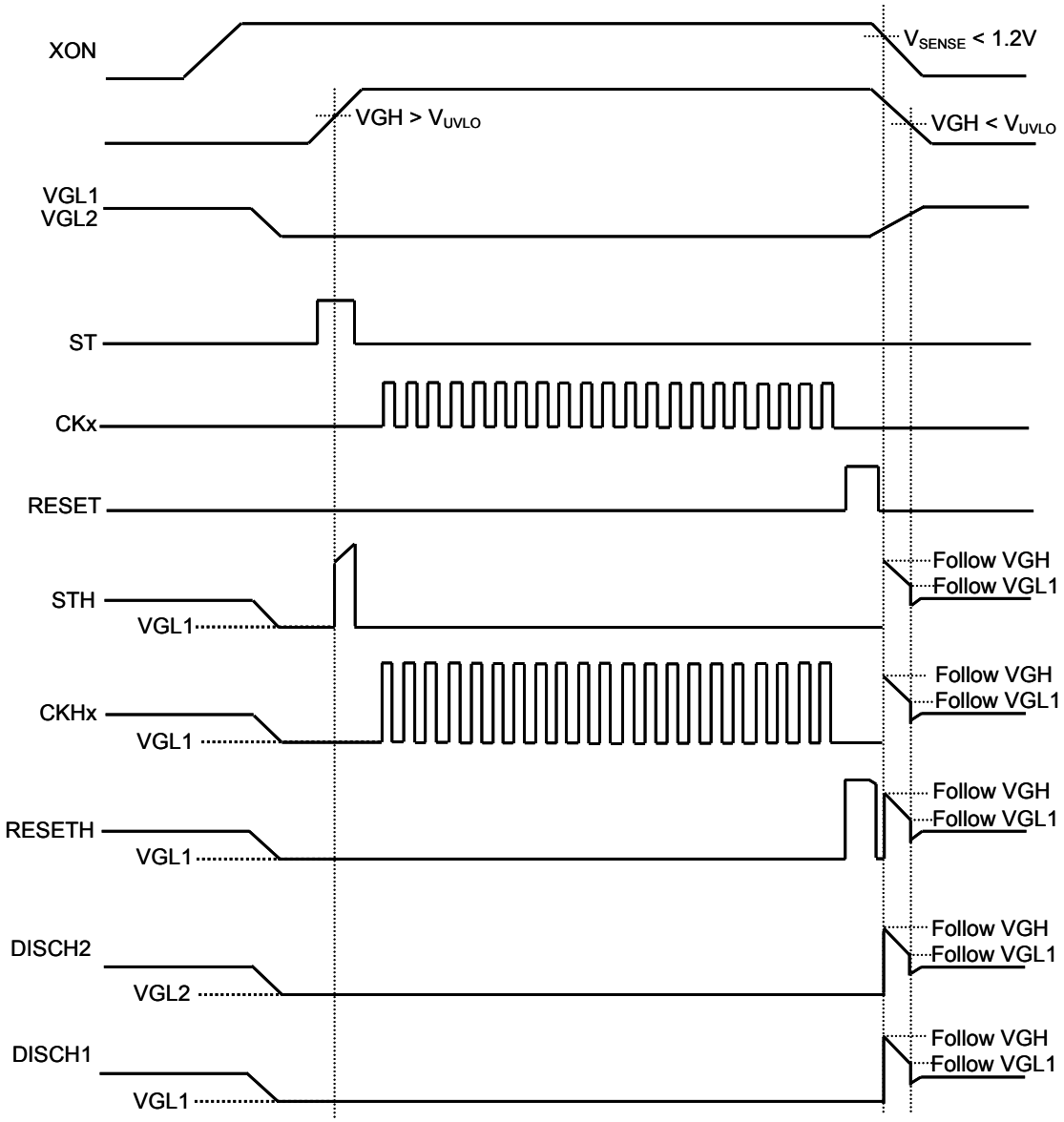


Figure 1. Power On/Off Sequence

Timing Diagram (continued)

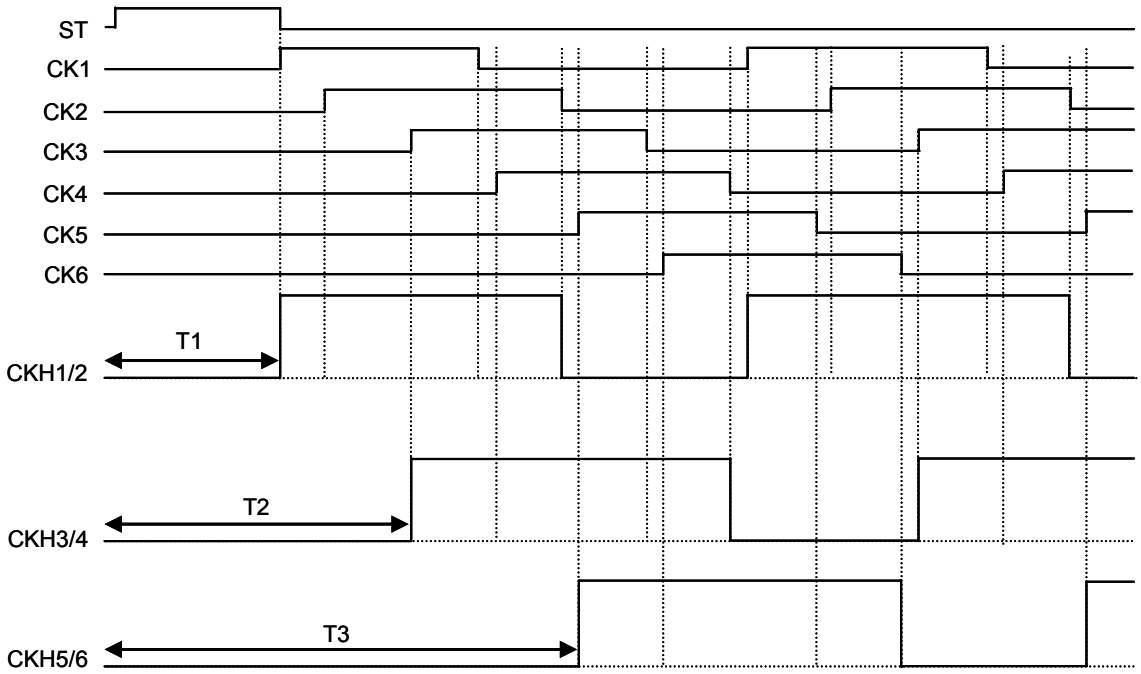


Figure 2. Disable Charge Sharing

Timing Diagram (continued)

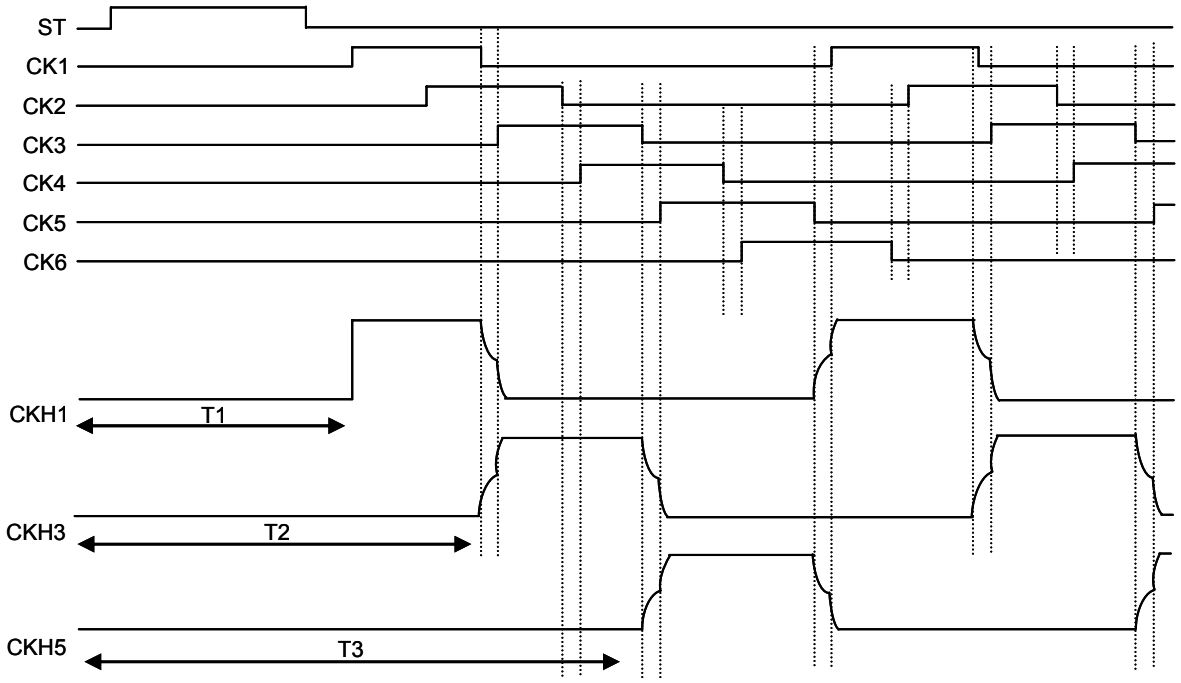


Figure 3. Charge Sharing Selection1

Match Eight Description:

1. Charge sharing of CKH1/CKH3 @ CK1 ↓ CK3 ↑ ;
2. Charge sharing of CKH5/CKH1 @ CK5 ↓ CK1 ↑ ;
3. Charge sharing of CKH3/CKH5 @ CK3 ↓ CK5 ↑ ;
4. Charge sharing of CKH2/CKH4/CKH6 @ the same concept.
5. ST rising of T1 period: voltage levels of CKH1 is VGL.
6. ST rising of T2 period: voltage levels of CKH3 is VGL.
7. ST rising of T3 period: voltage levels of CKH5 is VGL.

T1, T2 & T3 period of CKH2/CKH4/ CKH6 (at VGL level) @ the same concept.

Timing Diagram (continued)

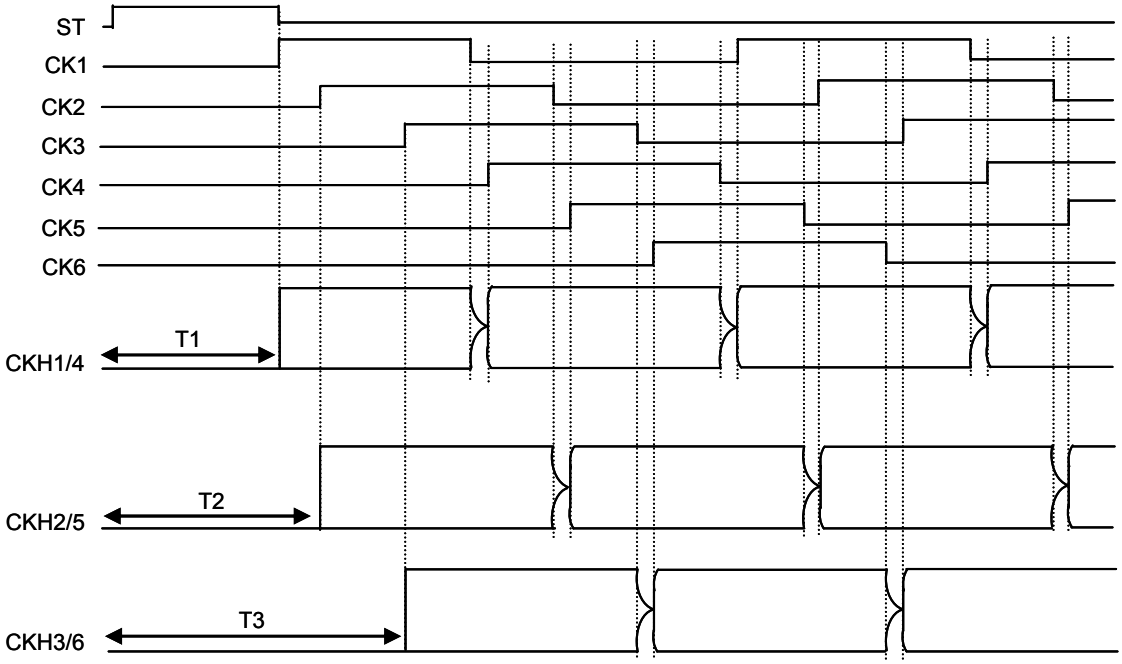


Figure 4. Charge Sharing Selection2

Match Six Description:

1. Charge sharing of CKH1/CKH4 @ CK1 ↓ CK4 ↑ & CK4 ↓ CK1 ↑ ;
2. Charge sharing of CKH2/CKH5 @ CK2 ↓ CK5 ↑ & CK5 ↓ CK2 ↑ ;
3. Charge sharing of CKH3/CKH6 @ CK3 ↓ CK6 ↑ & CK6 ↓ CK3 ↑ ;
4. ST rising of T1 period: voltage levels of CKH1 & CKH4 are VGL.
5. ST rising of T2 period: voltage levels of CKH2 & CKH5 are VGL.
6. ST rising of T3 period: voltage levels of CKH3 & CKH6 are VGL.

Timing Diagram (continued)

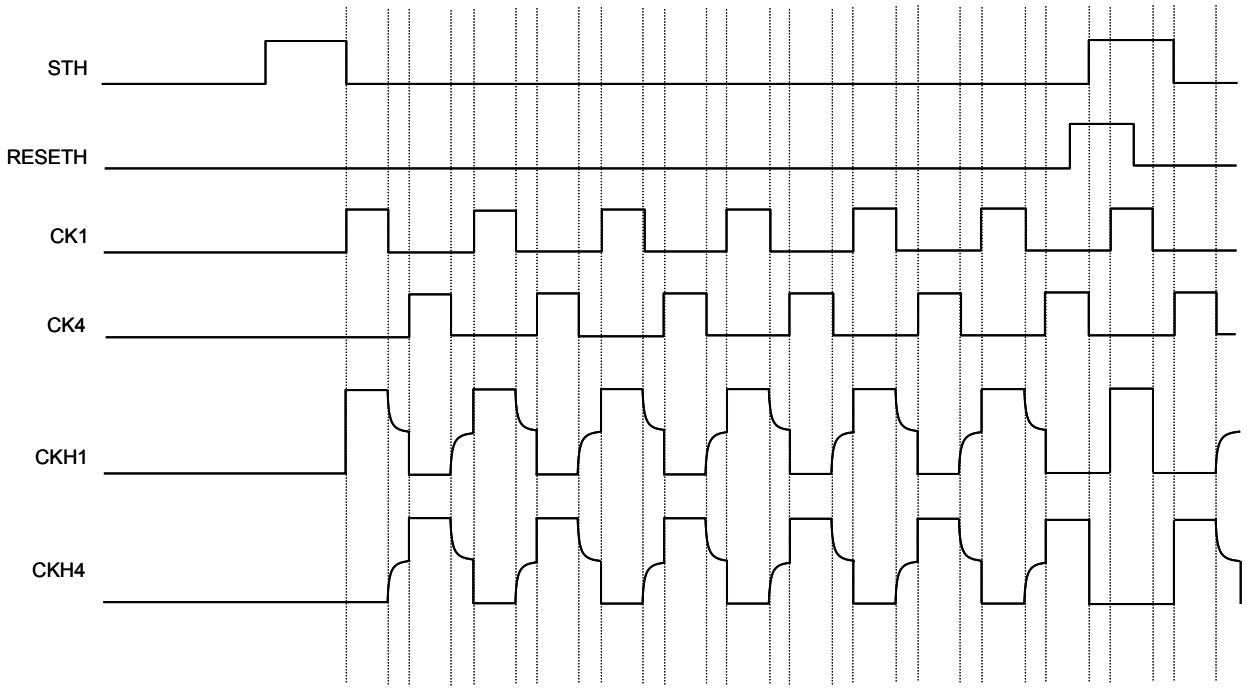


Figure 5. Frame Start/End Timing 1

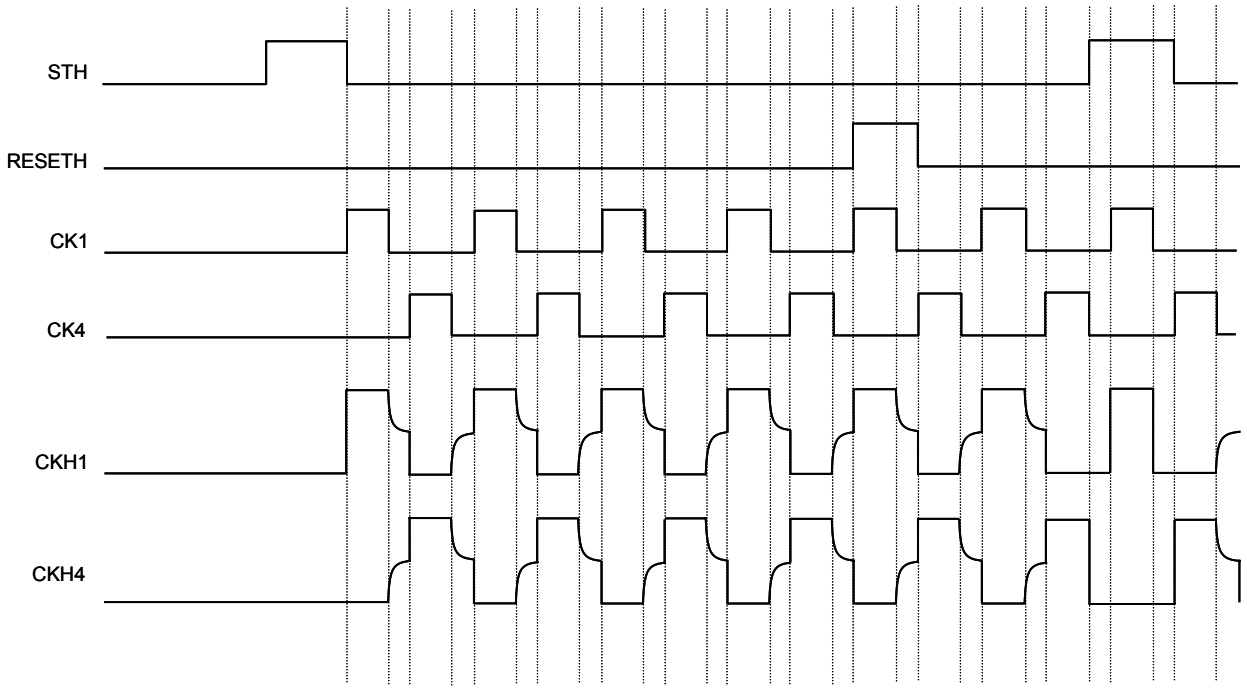


Figure 6. Frame Start/End Timing 2

Timing Diagram (continued)

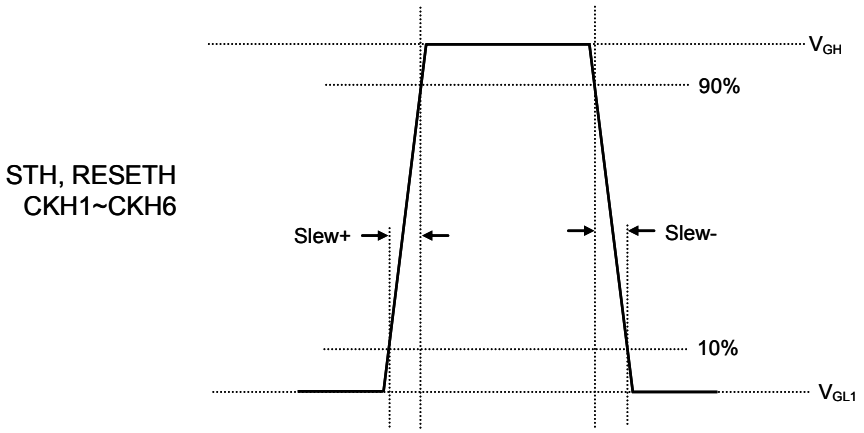


Figure 7. Rising and Falling Time

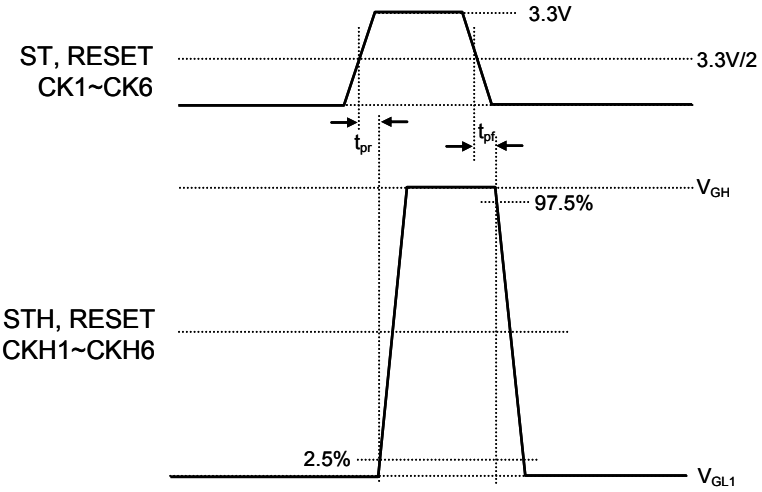


Figure 8. Propagation Delay

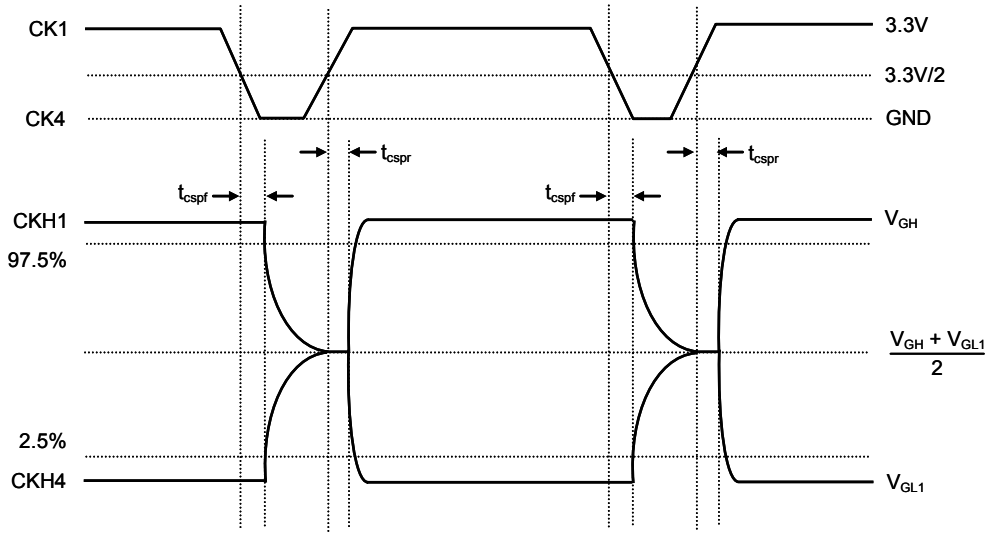


Figure 9. Charge Sharing of Propagation Delay

Power On and Off Sequence

Figure 1 shows the typical sequence of G2583B. VGL1 and VGL2 should power up prior to VGH. Before VGH ramp up arrived UVLO rising threshold of 15V, all clock outputs follow the VGL1 and VGL2. Before VGH start to rise, all clock outputs follows GND.

When the XON fall below the threshold of 1.2V, all clock outputs follow VGH, until the VGH drop below the UVLO falling threshold of 3.5V, the STH, RESETH, CKHx and DISCH1 follow the VGL1, DISCH2 follow VGL2.

If XON keep in high during power off, all clock outputs follow the clock input, until the VGH drop below the UVLO falling threshold 0f 3.5V, all clock outputs follow the VGL1, and DISCH1/DISCH2 always follows VGL1/VGL2 respectively.

STH output is blanked by VGH UVLO rising threshold of 15V, a rising edge of ST input after VGH exceed UVLO rising threshold will trigger the first STH output and CKHx outputs can follow the CKx inputs.

Panel Discharge Detection

The panel discharge detection is for detecting the input voltage of primary power manager. It is usually uses the resistor divider, connect the divided voltage to XON pin. The panel discharge detection threshold is 1.2V. If the XON is lower than 1.2V, all the output signals are pulled to VGH. See Figure 1 for power off sequence.

Level Shifter Outputs

The CKH1~CKH6, STH, RESETH, DISCH1, DISCH2 are output signals. The frame start/end timing diagram of the level shifter outputs are shown Figure 5, Figure 6.

The STH and RESETH only depend on the corresponding input signal (ST, RESET). CKHx follows the same logic level of CKx after the first valid ST rising edge.

The CKHx outputs have charge sharing function. SEL_CS pin determines the charge sharing mode. When the voltage of SEL_CS pin between 0V to 0.5V, the G2583B disable the charge sharing function, as shown in Figure 2. When the voltage of SEL_CS pin between 1V to 2V, it will enable the charge sharing function in mode 1, as shown in Figure 3. When the voltage of SEL_CS pin between 2.8V to 5.5V, it will operate in mode 2, as shown in Figure 4.

Over Temperature Protection

The G2583B has thermal protection function to prevent excessive power dissipation from overheating. When the junction temperature exceeds 150°C, it will shuts down the device and the output will keep high impedance. Recycle the VGH power or XON will clear the latch state.

Short Circuit Protection

Short circuit protection function is to prevent overload on each output channels. When one channel output transit from logic low to high and vice versa, short circuit detection begin after 2us blanking time. If the output loading over the SCP threshold and last 20us denoise time, the device will latch all the outputs to high impedance state. Recycle the VGH power or XON will clear the latch state. The SCP function is shown in Figure10.

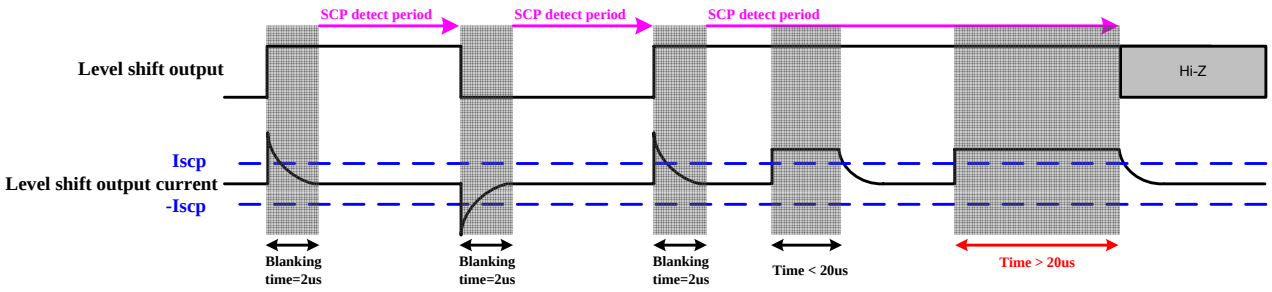
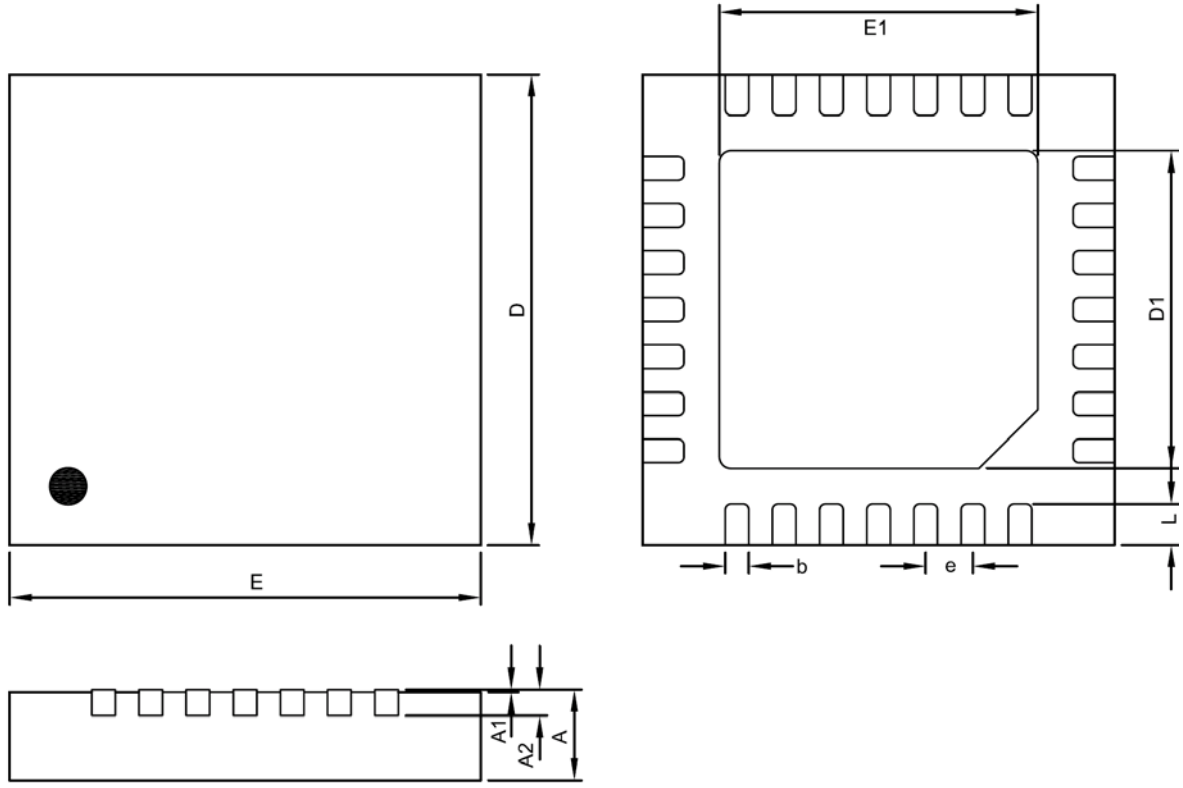


Figure 10. Short Circuit Protection Function

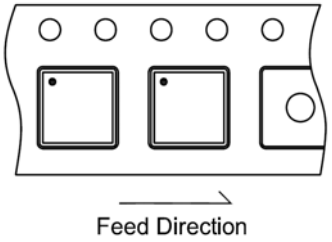
Package Information



TQFN4X4-28 Package

Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.0276	0.0295	0.0315
A1	0.00	- - -	0.05	0.0000	- - -	0.0020
A2	0.20 REF			0.0079 REF		
D	3.95	4.00	4.05	0.1555	0.1575	0.1594
E	3.95	4.00	4.05	0.1555	0.1575	0.1594
D1	2.55	2.65	2.75	0.1004	0.1043	0.1083
E1	2.55	2.65	2.75	0.1004	0.1043	0.1083
b	0.15	0.20	0.25	0.0059	0.0079	0.0098
e	0.40 BSC			0.0157 BSC		
L	0.30	0.40	0.45	0.0118	0.0157	0.0177

Taping Specification



PACKAGE	Q'TY/REEL
TQFN4X4-28	3,000 ea