Ultra-Low On-Resistance Load Switch with Controlled Turn-On

Features

- **Integrated Single Channel Load Switch**
- **Input Voltage Range: 0.7V to 5.7V**
- **Ultra-low ON-Resistance (14mΩ)**
  - **$R_{DS(on)}$ = 14mΩ at V_{IN} = 5V (V_{BIAS} = 5V)**
- **6A Maximum Continuous Switch Current**
- **Adjustable Undervoltage Lockout Threshold (UVLO)**
- **Adjustable Voltage Supervisor with Power Good (PG) Indicator**
- **Low Quiescent Current <50μA**
- **Low Threshold Control Inputs**
- **Adjustable Slew-rate Control**
- **Quick Output Discharge Transistor**
- **10 Pin TDFN Package with Thermal Pad**

General Description

The G2892 is a single N-channel MOSFET power switch designed for high-side load-switching application. The device has a typical $R_{DS(ON)}$ of 14mΩ and can support a maximum continuous current of 6A. The G2892 is controlled by an on/off input EN pin, which is suitable for interfacing directly with low-voltage I/O ports. The EN pin can also be configured via an external resistor divider to adjust under voltage lockout (UVLO) threshold.

In the G2892, a 15Ω on-chip load resistor is added for quick output discharge (QOD) when the switch is turned off. Moreover, the controlled rise time can be adjusted by using a ceramic capacitor on the CT pin in order to prevent in-rush current at start-up time.
The G2892 is available in 10 pin TDFN package.

Applications

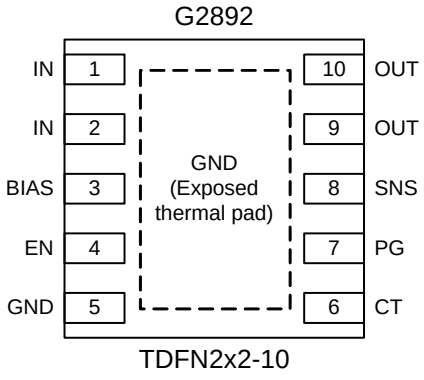
- **Notebooks / Netbooks**
- **Tablet PCs**
- **Consumer Electronics**
- **Set-Top-Boxes**
- **Industrial Systems**
- **Telecom Systems**

Ordering Information

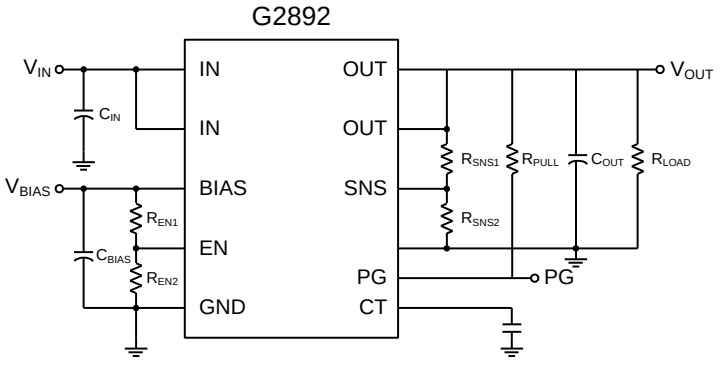
ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE (Green)
G2892K21D	2892	-40°C to +85°C	TDFN2X2-10

Note: K2: TDFN2X2-10
1: Bonding Code
D : Tape & Reel
Green: Lead Free / Halogen Free

Pin Configuration



TDFN2x2-10



Absolute Maximum Ratings

V_{IN} to GND . . . . . -0.3V to +6V
EN to GND . . . . . -0.3V to +6V
V_{OUT} to GND . . . . . -0.3V to +6V
CT GND . . . . . -0.3V to +12V
V_{BIAS} to GND . . . . . -0.3V to +6V
Continuous Switch Current (I_{MAX}). 6A
Junction Temperature . . . . . .150°C
Thermal Resistance Junction to Ambient, (θ_{JA})
TDFN2X2-10 . . . . . .63.5°C/W
Thermal Resistance Junction to Case, (θ_{JC})
TDFN2X2-10 . . . . . .81.6°C/W
Operating Temperature Range . . . . . -40°C to 85°C
Storage Temperature Range . . . . . .-65°C to 150°C
Reflow Temperature (soldering, 10sec) . . . . . .260°C
ESD(HBM) . . . . . .2KV(1)
ESD(CDM) . . . . . .±1000V

Note 1：Human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.

Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Input voltage range	V_{IN}	0.7	---	V_{BIAS}	V
Bias voltage range	V_{BIAS}	2.5	---	5.7	V
VOUT Output Current	I_{OUT}	0	---	6	A
Maximum Pulsed Switch Current, Pulse<300μs,1% Duty Cycle		---	8	---	A
EN, SNS, PG voltage range	V_{EN}, V_{SNS}, V_{PG}	0	---	5.7	V
Output voltage range	V_{OUT}	---		5.7	V
Input Capacitor	$C_{IN1,2}$	1*	---	---	μF

*Note: 1μF input capacitor is sufficient in most application cases. If the distance of power trace on PCB is longer than general design, larger input capacitor is highly recommended for normal operation.

Electrical Characteristics

(V_{IN} = 0.7V to 5V, V_{BIAS}= 5V, T_A = –40ºC to 85ºC (unless otherwise noted)

PARAMETER		SYMBOL	Conditions		MIN	TYP	MAX	UNITS
Input Voltage Range		V_{IN}			0.7	---	V_{BIAS}	V
Bias Voltage Range		V_{BIAS}			2.5	---	5.7	V
V_{EN}	Rising Threshold	$V_{IH,EN}$	V_{IN} = 0.7V to V_{BIAS}		650	700	750	mV
	Falling Threshold	$V_{IL,EN}$	V_{IN} = 0.7V to V_{BIAS}		560	600	640	mV
V_{SNS}	Rising Threshold	$V_{IH,SNS}$	V_{IN} = 0.7V to V_{BIAS}		465	515	565	mV
	Falling Threshold	$V_{IL,SNS}$	V_{IN} = 0.7V to V_{BIAS}		410	455	500	mV
Bias Quiescent Current		$I_{Q,BIAS}$	I_{OUT} = 0, V_{IN} = 0.7V to V_{BIAS}, V_{EN} = V_{BIAS} = 5V		---	25	50	μA
			I_{OUT} = 0, V_{IN} = 0.7V to V_{BIAS}, V_{EN} = V_{BIAS} = 3.3V		---	18	35	
			I_{OUT} = 0, V_{IN} = 0.7V to V_{BIAS}, V_{EN} = V_{BIAS} = 2.5V		---	16	25	
Bias Shutdown Current		$I_{SD,BIAD}$	V_{EN} = V_{OUT} = 0V, V_{BIAS} = 5V		---	4	7	μA
			V_{EN} = V_{OUT} = 0V, V_{BIAS} = 3.3V		---	4	6	
			V_{EN} = V_{OUT} = 0V, V_{BIAS} = 2.5V		---	4	5	
Input Shutdown Current		$I_{SD,IN}$	V_{EN} = V_{OUT} = 0V	V_{IN}= 5V	---	0.1	13	μA
				V_{IN}= 3.3V	---	0.1	10	
				V_{IN}= 1.8V	---	0.1	10	
				V_{IN}= 1.2V	---	0.1	8	
				V_{IN}= 0.7V	---	0.1	8	

Electrical Characteristics (Continued)

PARAMETER	SYMBOL	Conditions	MIN	TYP	MAX	UNITS
EN pin Input leakage Current	I_{EN_LEAK}	$V_{EN}<V_{BIAS}$	---	0.1	1	µA
SNS pin Input leakage Current	I_{SNS_LEAK}	$V_{SNS}<V_{BIAS}$	---	0.1	1	µA
Output Discharge Resistance	R_{DIS}	$V_{IN}=V_{OUT}=V_{BIAS}$, $V_{EN}=0$	---	15	30	Ω
On-Resistance	$R_{DS(on)}$	I_{OUT} = 200mA, V_{IN} = 0.7V to V_{BIAS}, V_{EN} = V_{BIAS} = 5V	---	14	20	mΩ
		I_{OUT} = 200mA, V_{IN} = 0.7V to V_{BIAS}, V_{EN} = V_{BIAS} = 3.3V	---	15	21	
		I_{OUT} = 200mA, V_{IN} = 0.7V to V_{BIAS}, V_{EN} = V_{BIAS} = 2.5V	---	16	23	
Thermal Shutdown	T_{SD}	Junction Temperature Rising	---	150	---	°C
Thermal Shutdown Hysteresis	T_{SDHYS}	Junction Temperature Falling	---	20	---	°C
Blanking time for EN and SNS	t_{BLANK}	EN or SNS Rising	---	100	---	µs
Deglitch time for EN and SNS	$t_{DEGLITCH}$	EN or SNS Falling	---	5	---	µs
Output Restart time	$t_{RESTART}$	SNS Falling	---	2	---	ms

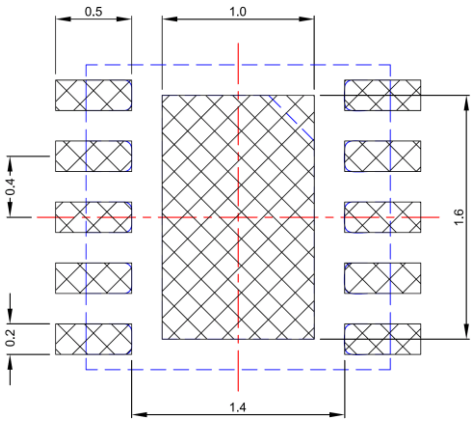
Switching Characteristics

(Switching characteristics shown below are only valid for the power-up sequence where VIN and VBIAS are already in steady state condition before the EN terminal is asserted high.)

PARAMETER		Test Conditions	MIN	TYP	MAX	UNITS
V_{IN}=5V, V_{EN}=V_{BIAS}=5V, T_A=25°C						
t_{ON}	Turn on time	R_L= 10Ω, C_L= 0.1µF, C_T= 1000pF	670	1100	1530	µs
t_{OFF}	Turn off time	R_L= 10Ω, C_L= 0.1µF, C_T= 1000pF	8	12	16	
t_R	V_{OUT} rising time	R_L= 10Ω, C_L= 0.1µF, C_T= 1000pF	860	1280	1700	
t_F	V_{OUT} falling time	R_L= 10Ω, C_L= 0.1µF, C_T= 1000pF	1.0	3.1	10.0	
t_D	ON delay time	R_L= 10Ω, C_L= 0.1µF, C_T= 1000pF	220	460	700	
V_{IN}=5V, V_{EN}=V_{BIAS}=5V, T_A=25°C						
t_{ON}	Turn on time	R_L= 10Ω, C_L= 0.1µF, C_T= 0pF	106	280	464	µs
t_{OFF}	Turn off time	R_L= 10Ω, C_L= 0.1µF, C_T= 0pF	7	11	15	
t_R	V_{OUT} rising time	R_L= 10Ω, C_L= 0.1µF, C_T= 0pF	100	200	360	
t_F	V_{OUT} falling time	R_L= 10Ω, C_L= 0.1µF, C_T= 0pF	0.8	1.7	5.0	
t_D	ON delay time	R_L= 10Ω, C_L= 0.1µF, C_T= 0pF	90	195	350	

Minimum Footprint PCB Layout Section (Unit: mm)

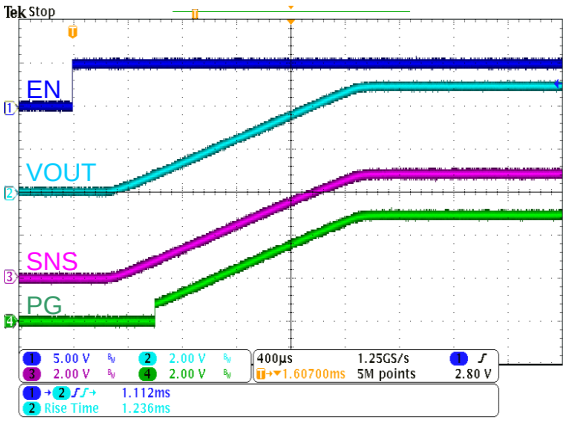
TDFN2X2-10



Typical Performance Characteristics

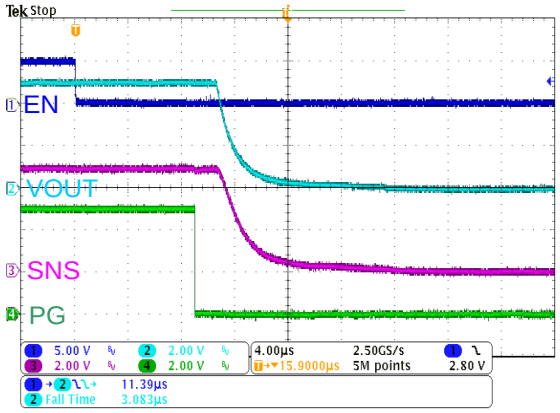
T_A = 25°C

Power On from EN



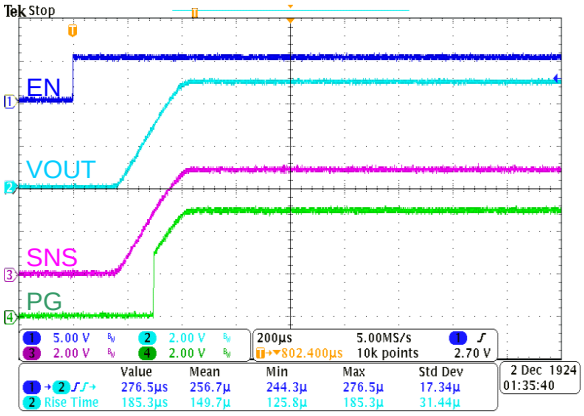
V_{BIAS}=5V;V_{IN}=5V;C_T=1000pF;C_{IN}=1µF;C_L=0.1µF;R_L=10Ω

Power Off from EN



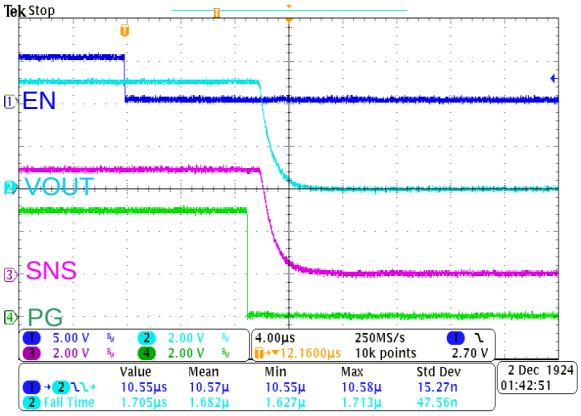
V_{BIAS}=5V;V_{IN}=5V;C_T=1000pF;C_{IN}=1uF;C_L=0.1µF;R_L=10Ω

Power On from EN



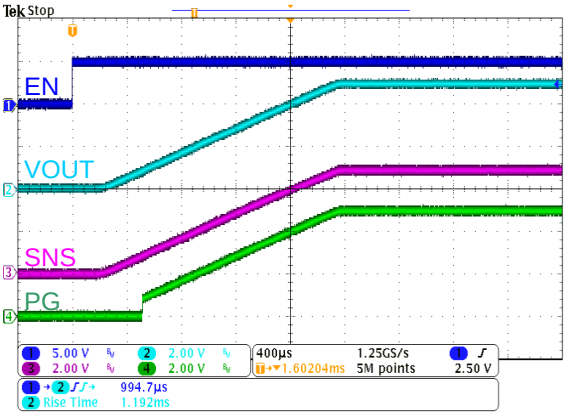
V_{BIAS}=5V;V_{IN}=5V;C_T=0pF;C_{IN}=1µF;C_L=0.1µF;R_L=10Ω

Power Off from EN



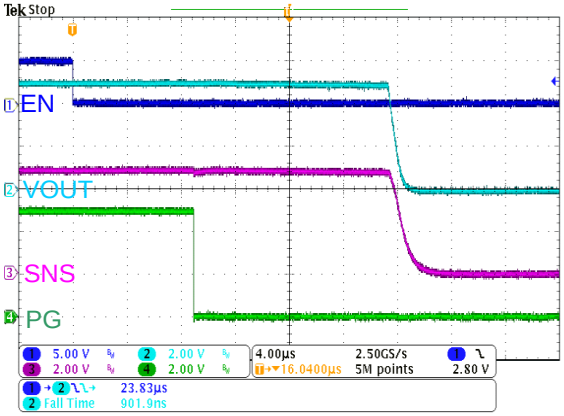
V_{BIAS}=5V;V_{IN}=5V;C_T=0pF;C_{IN}=1µF;C_L=0.1µF;R_L=10Ω

Power On from EN



V_{BIAS}=5V;V_{IN}=5V;C_T=1000pF;C_{IN}=1µF;C_L=0.1µF;No Load

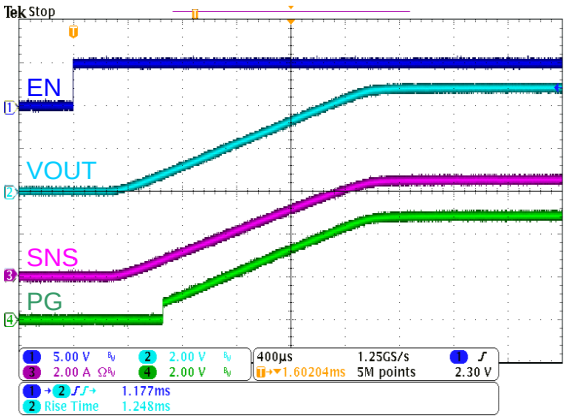
Power Off from EN



V_{BIAS}=5V;V_{IN}=5V;C_T=1000pF;C_{IN}=1µF;C_L=0.1µF;No Load

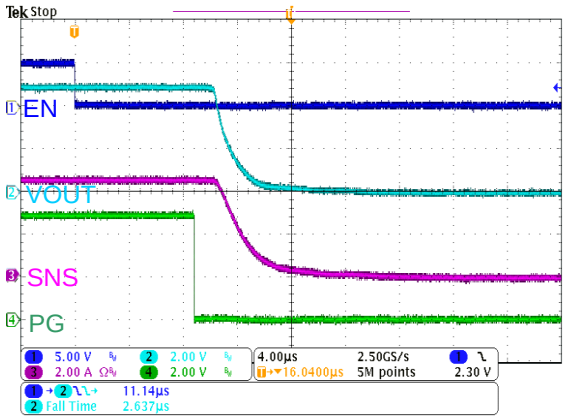
Typical Performance Characteristics (Continued)

Power On from EN



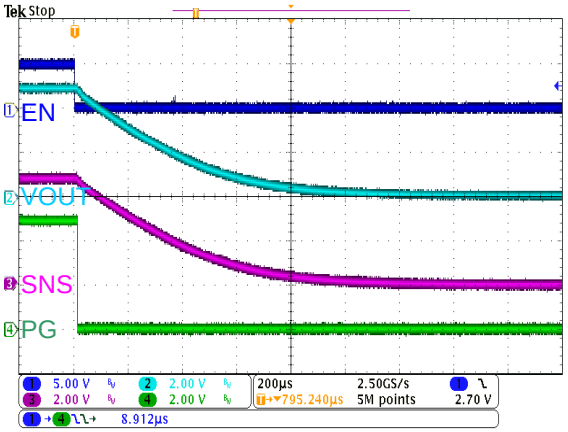
V_{BIAS}=5V;V_{IN}=5V;C_T=1000pF;C_{IN}=1µF;C_L=0.1µF;R_L=1Ω

Power Off from EN



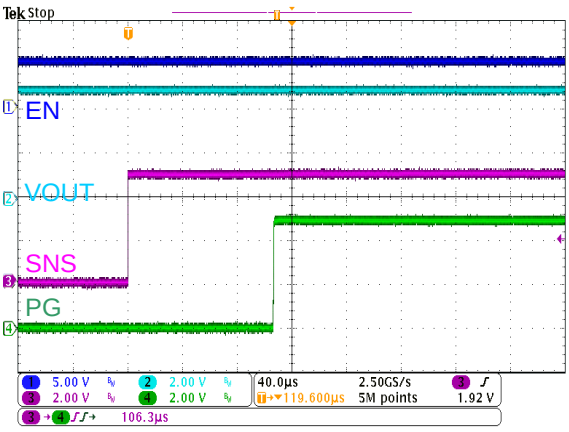
V_{BIAS}=5V;V_{IN}=5V;C_T=1000pF;C_{IN}=1µF;C_L=0.1µF;R_L=1Ω

PG Response to EN Falling ($t_{DEGLITCH}$)



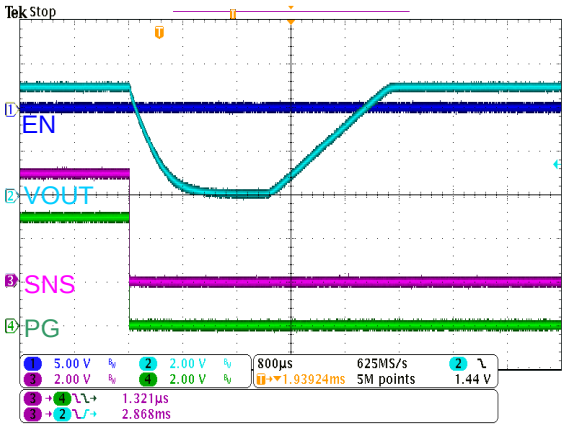
V_{BIAS}=5V;V_{IN}=5V;C_T=1000pF;C_{IN}=1µF;C_L=100µF;R_L=10Ω

PG Response to SNS Rising (t_{BLANK})



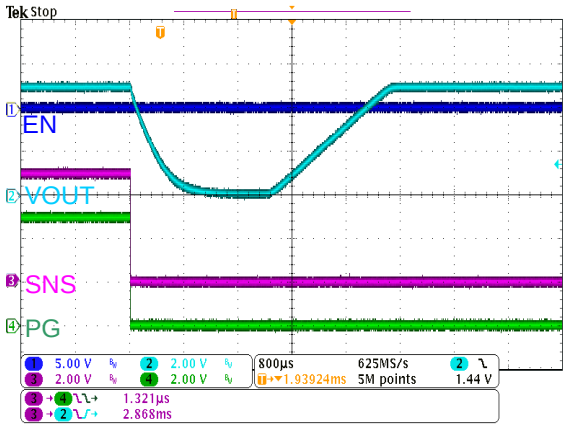
V_{BIAS}=5V;V_{IN}=5V;C_T=1000pF;C_{IN}=1µF;C_L=100µF;R_L=10Ω

PG Response to SNS Falling with Auto-Restart ($t_{DEGLITCH}$ and $t_{RESTART}$)



V_{BIAS}=5V;V_{IN}=5V;C_T=1000pF;C_{IN}=1µF;C_L=100µF;R_L=10Ω

Quick Output Discharge of 100-µF Load (t_{DIS})

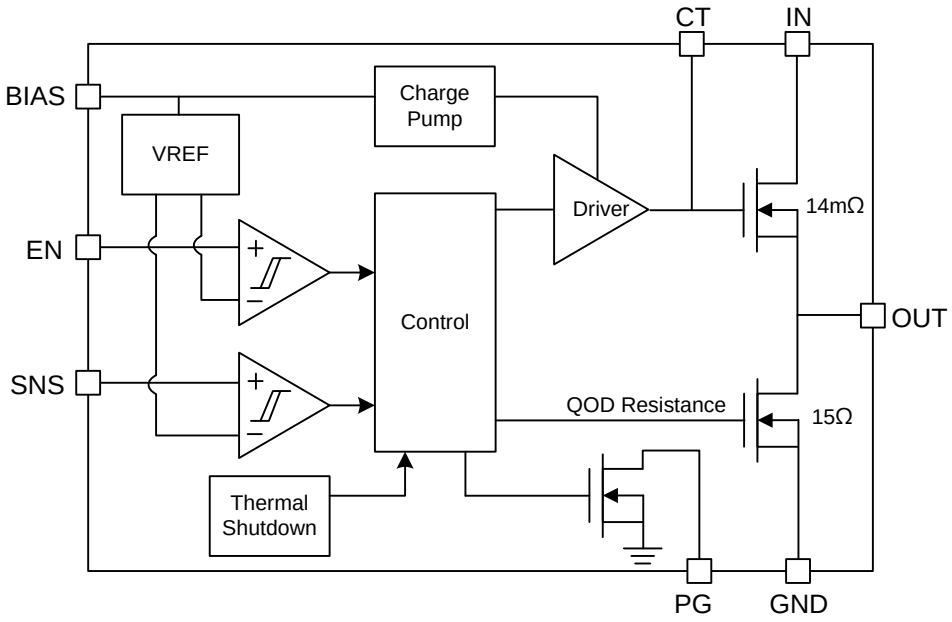


V_{BIAS}=5V;V_{IN}=5V;C_T=1000pF;C_{IN}=1µF;C_L=100µF;No Load

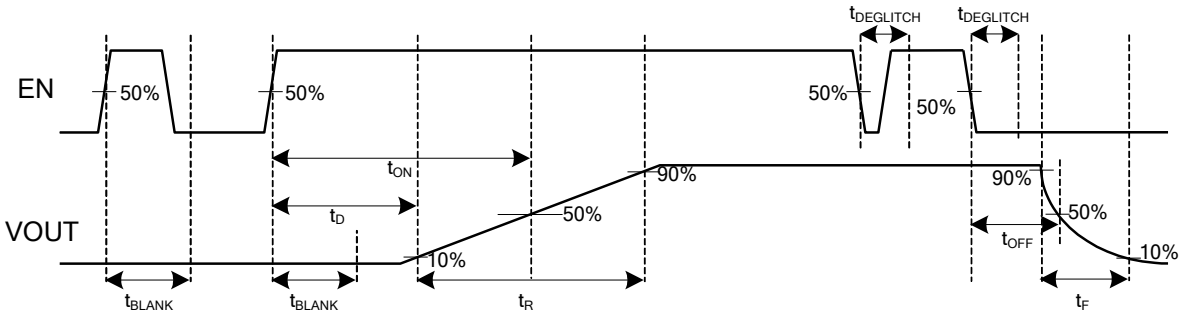
Pin Description

PIN NO.	PIN NAME	I/O	DESCRIPTION
1	IN	I	Switch Input. Bypass IN and GND with ceramic capacitor
2	IN	I	Switch Input. Bypass IN and GND with ceramic capacitor
3	BIAS	I	Supply input for the device
4	EN	I	Enable input. Switch is on when EN is pulled high. Also acts as the input UVLO pin. Use External resistor divider to adjust the UVLO level. Do not leave floating
5	GND	---	Ground
6	CT	O	V_{OUT} slew rate control
7	PG	O	Power good. This pin is open drain which will pull low when the voltage on EN or SNS is below their respective VIL level
8	SNS	I	Sense pin. Use External resistor divider to adjust the power good level. Do not leave floating
9	OUT	O	Switch Output
10	OUT	O	Switch Output
---	Thermal Pad	---	The exposed bottom pad must be connected to GND

Block Diagram



Timing Diagram



Function Description

On and Off Control (EN pin)

The EN pin controls the state of the switch. When the voltage on EN has exceeded $V_{IH,EN}$ the switch is enabled. When EN goes below $V_{IL,EN}$ the switch is disabled.

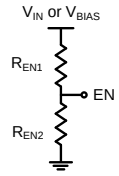
The EN pin has a blanking time of t_{BLANK} on the rising edge once the $V_{IH,EN}$ threshold has been exceeded. It also has a de-glitch time of $t_{DEGLITCH}$ when the voltage has gone below $V_{IL,EN}$.

The EN pin can also be configured via an external resistor divider to monitor a voltage signal for input UVLO.

$$V_{IH,EN} = V_{IN} \times \frac{R_{EN2}}{R_{EN1} + R_{EN2}}$$

Where

- $V_{IH,EN}$ is the rising threshold of the EN pin
- V_{IN} is the input voltage being monitored (this could be V_{IN}, V_{BIAS}, or an external power supply)
- R_{EN1}, R_{EN2} is the resistor divider values

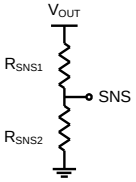


Voltage Monitoring (SNS pin)

The SNS pin of the device can be used to monitor the output voltage of the device or another voltage rail. The pin can be configured with an external resistor divider to set the desired trip point for the voltage being monitored or be tied to OUT directly. If the voltage on the SNS pin exceeds $V_{IH,SNS}$, the voltage being monitored on the SNS pin is considered to be valid high. The voltage on the SNS pin must be greater than $V_{IH,SNS}$ for at least t_{BLANK} before PG is asserted high. If the voltage on the SNS pin goes below $V_{IL,SNS}$, then the switch powers cycle (i.e., the switch is disabled and re-enabled). For proper functionality of the device, this pin must not be left floating. If a resistor divider is not being used for voltage sensing, this pin can be tied directly to VOUT.

The SNS pin has a blanking time of t_{BLANK} on the rising edge once the $V_{IH,SNS}$ threshold has been exceeded. It has a de-glitch time of $t_{DEGLITCH}$ when the voltage has gone below $V_{IL,SNS}$.

$$V_{IH,SNS} = V_{OUT} \times \frac{R_{SNS2}}{R_{SNS1} + R_{SNS2}}$$



Thermal Shutdown

If the junction temperature of the device exceeds T_{SD}, the switch is disabled. The device is enabled once the junction temperature drops by T_{SDHYS} as long as EN is still greater than $V_{IH,EN}$.

Power Good (PG pin)

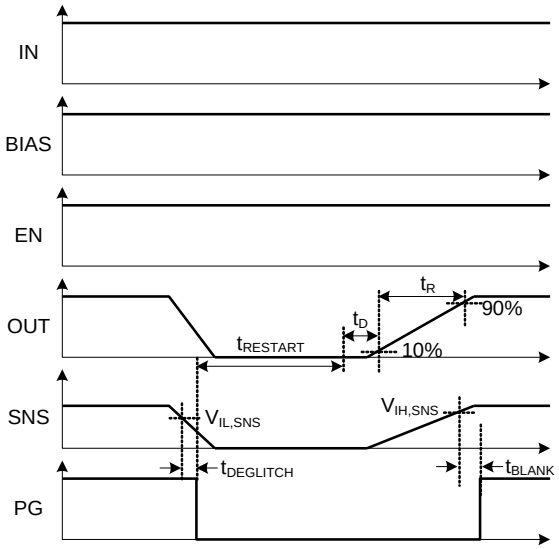
The PG pin is only asserted high when the voltage on EN has exceeded $V_{IH,EN}$ and the voltage on SNS has exceeded VIH,SNS. There is a t_{BLANK} time, typically 100µs, between the SNS voltage exceeding $V_{IH,SNS}$ and PG being asserted high. If the voltage on EN goes below $V_{IL,EN}$ or the voltage on SNS goes below VIL,SNS, PG is deasserted. There is a $t_{DEGLITCH}$ time, typically 5µs, between the EN voltage or SNS voltage going below their respective VIL levels and PG being pulled low.

PG is an open drain pin and must be pulled up with a pull-up resistor. Be sure to never exceed the maximum operating voltage on this pin. If PG is not being used in the application, tie it to GND for proper device functionality.

For proper PG operation, the BIAS voltage must be within the recommended operating range. In systems that are very sensitive to noise or have long PG traces, it is recommended to add a small capacitance from PG to GND for decoupling.

Supervisor Fault Detection and Automatic Restart (SNS pin)

The falling edge of the SNS pin below $V_{IL,SNS}$ is considered a fault case and causes the load switch to be disabled for $t_{RESTART}$ (typically 2ms). After the $t_{RESTART}$ time, the switch is automatically re-enabled as long as EN is still above $V_{IH,EN}$. In the case the SNS pin is being used to monitor V_{OUT} or a downstream voltage, the restart helps to protect against excessive over-current if there is a quick short to GND.

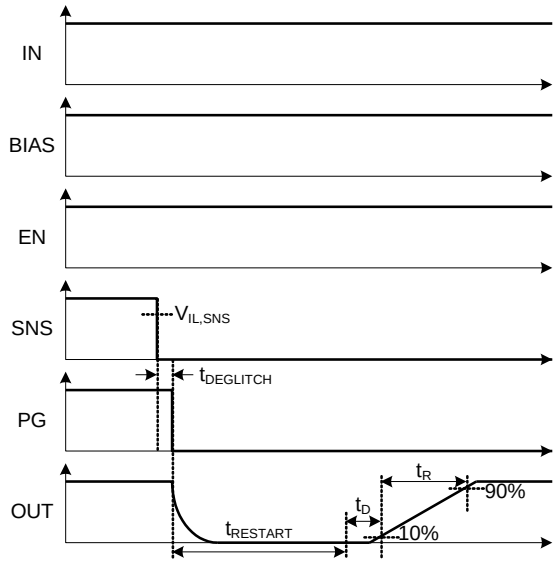


Automatic Restart after Quick Short to GND

Function Description (Continued)

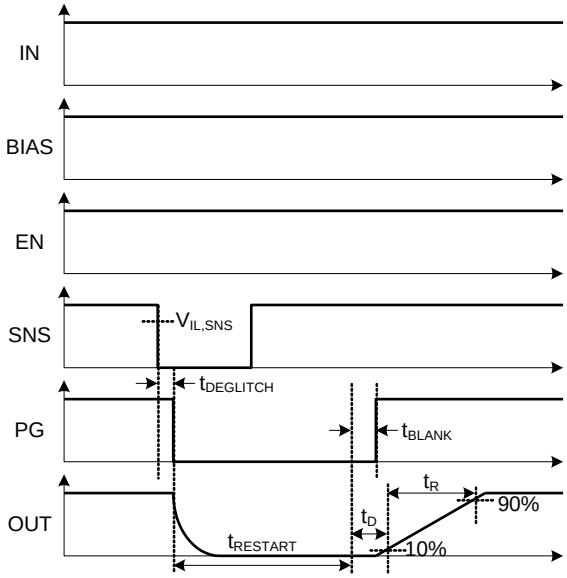
Manual Restart (SNS pin)

The falling edge of the SNS pin below $V_{IL,SNS}$ is considered a fault case and causes the load switch to be disabled for $t_{RESTART}$ (typically 2ms). The SNS pin can be driven by an MCU to manually reset the load switch. After the $t_{RESTART}$ time, the switch is automatically re-enabled as long as EN is still above $V_{IH,EN}$, even is SNS is held low. The PG pin stays low until the switch is re-enabled and the SNS pin rises above $V_{IH,SNS}$.



Manual Restart (SNS Held Low)

If the SNS pin is brought above $V_{IH,SNS}$ within the $t_{RESTART}$ time, the switch still waits to re-enable. The PG pin also stays low until t_{BLANK} after switch is re-enabled. In this case, PG indicates when the switch is enabled and capable of being reset again.

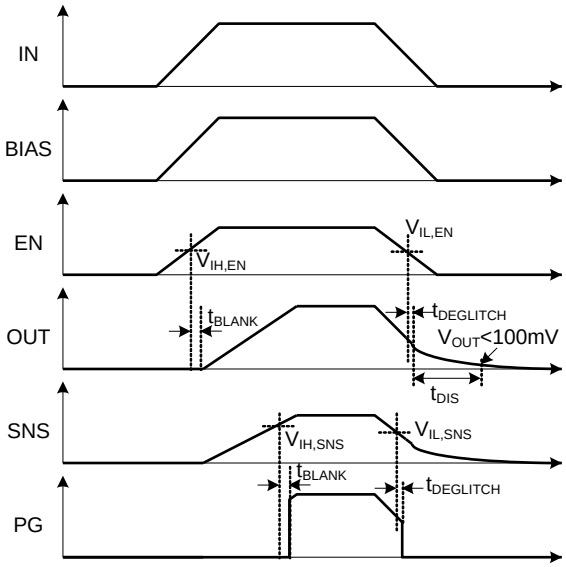


Manual Restart (SNS Toggled Low to High)

Quick Output Discharge (QOD)

The quick output discharge (QOD) transistor is engaged indefinitely whenever the switch is disabled and the recommended V_{BIAS} voltage is met. During this state, the QOD resistance (R_{PD}) discharges V_{OUT} to GND. It is not recommended to apply a continuous DC voltage to OUT when the device is disabled.

The QOD transistor can remain active for a short period of time even after V_{BIAS} loses power. This brief period of time is defined as t_{DIS}. For best results, it is recommended the device get disabled before V_{BIAS} goes below the minimum recommended voltage. The waveform below shows the behavior when power is applied and then removed in a typical application.



Power Applied and then Removed in a Typical Application

Adjustable Rise Time (CT pin)

A capacitor to GND on the CT pin sets the slew rate for V_{OUT}. An appropriate capacitance value must be placed on CT such that the I_{MAX} and I_{PLS} specifications of the device are not violated. The capacitor to GND on the CT pin must be rated for 25V or higher. An approximate formula for the relationship between CT (except for CT=open) and the slew rate for any V_{BIAS} is shown below.

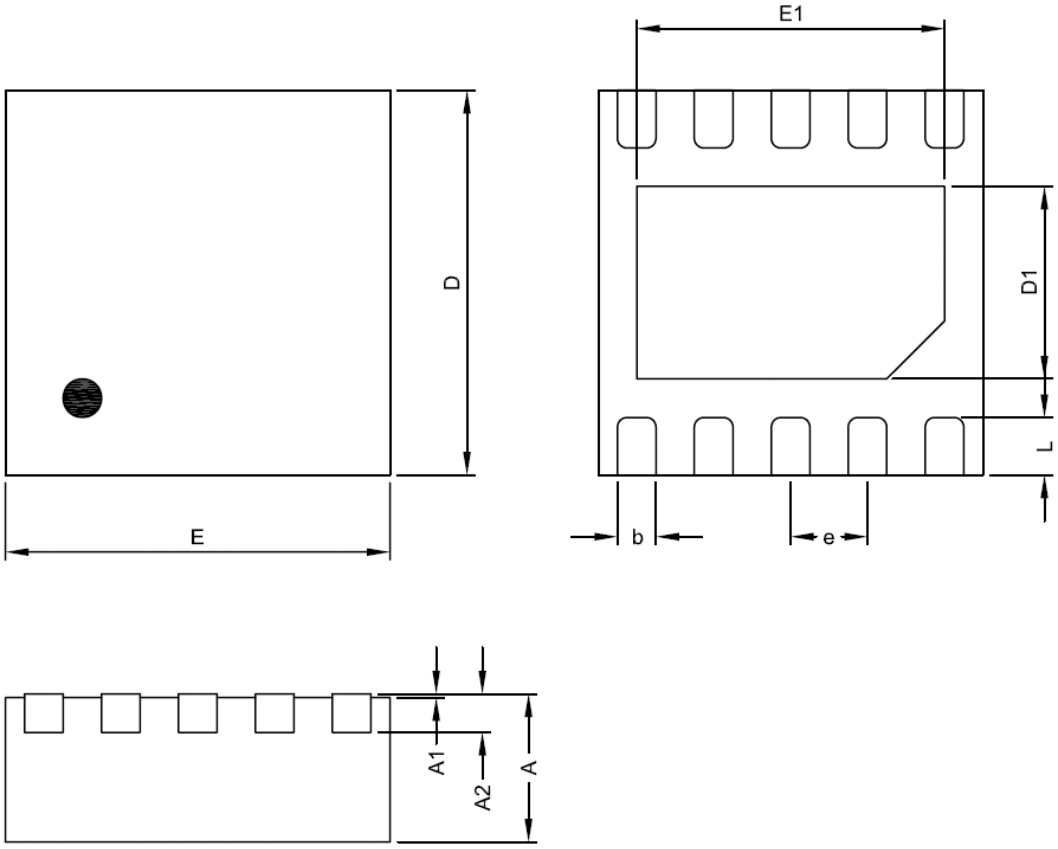
$$SR = 0.27 \times CT + 50$$

Where

- SR is the slew rate (in µs/V)
- CT is the capacitance value on the CT pin (in pF)
- The units for the constant 50 are µs/V
- The units for the constant 0.35 are µs/(V*pF)

Rise time can be calculated by multiplying the input voltage (typically 10% to 90%) by the slew rate.

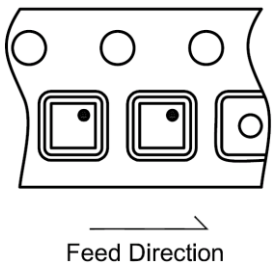
Package Information



TDFN2X2-10 Package

Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.0276	0.0295	0.0315
A1	0.00	---	0.05	0.0000	---	0.0020
A2	0.20 REF			0.0079 REF		
D	1.95	2.00	2.05	0.0768	0.0787	0.0807
E	1.95	2.00	2.05	0.0768	0.0787	0.0807
D1	0.85	0.95	1.05	0.0334	0.0374	0.0413
E1	1.35	1.50	1.65	0.0531	0.0591	0.0650
b	0.15	0.20	0.25	0.0059	0.0079	0.0098
e	0.40 BSC			0.0157 BSC		
L	0.20	0.30	0.35	0.0079	0.0118	0.0138

Taping Specification



PACKAGE	Q'TY/REEL
TDFN2X2-10	3,000 ea