Dual Fast Turn On Load Switch

Features

- **10µs ≤ EN asserted to V_{OUT} stable ≤ 65µs**
- **V_{IN} Range: 0.7V to 2.2V**
- **Dual Ultra-low ON-Resistance**
  - **$R_{DS(on)}$ = 24mΩ at V_{IN} = 1.8V (V_{BIAS} = 5V)**
  - **$R_{DS(on)}$ = 23mΩ at V_{IN} = 1.5V (V_{BIAS} = 5V)**
  - **$R_{DS(on)}$ = 20mΩ at V_{IN} = 1.05V (V_{BIAS} = 5V)**
- **4A Continuous Switch Current per channel**
- **Low Quiescent Current**
- **Quick Output Discharge**
- **14 Pin TDFN Package with Thermal Pad**

Applications

- **Notebooks**
- **Tablet PCs**

General Description

The G2894 is dual N-channel MOSFET power switch designed for high-side load-switching application. The device has a typical $R_{DS(ON)}$ of 20mΩ and the output current is limited to 4A. Each channel is controlled by an on/off input (EN1, EN2) independently, which is suitable for interfacing directly with low-voltage I/O ports.

In the G2894, a 220Ω on-chip load resistor is added for quick output discharge (QOD) when the switch is turned off.

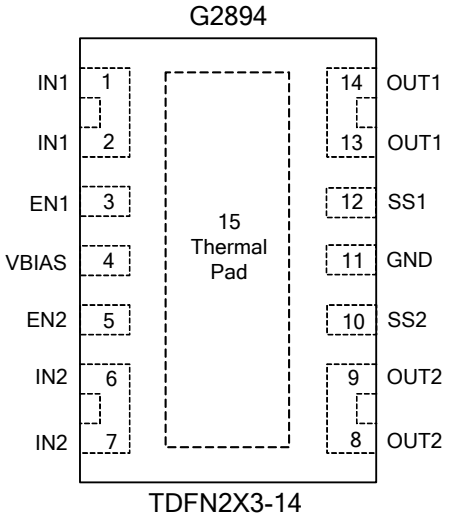
The G2894 is available in 14 pin TDFN package.

Ordering Information

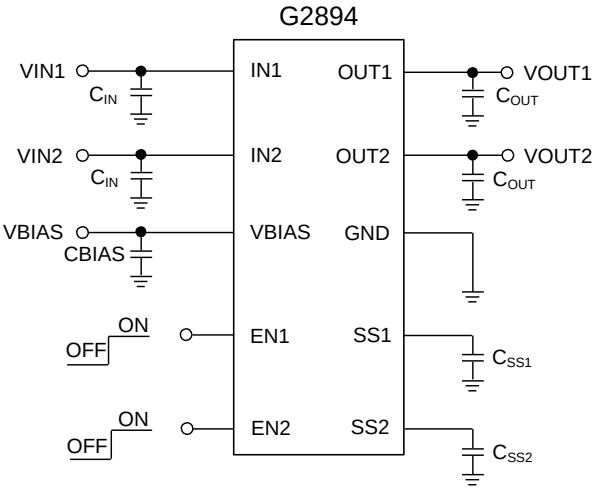
ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE (Green)
G2894KD1U	2894	-40°C to 85°C	TDFN2X3-14

Note: KD: TDFN2X3-14
1: Bonding Code
U: Tape & Reel
Green : Lead Free / Halogen Free.

Pin Configuration



Typical Application Circuit



Absolute Maximum Ratings

VBIAS to GND . . . . . -0.3V to +6V
IN1, IN2 to GND . . . . . -0.3V to +6V
EN1, EN2 to GND . . . . . -0.3V to +6V
OUT1, OUT2 to GND . . . . . -0.3V to +6V
SS1, SS2 to GND . . . . . -0.3V to +6V
Continuous Switch Current (I_{MAX}) 4A
Junction Temperature . . . . . 150°C
Thermal Resistance Junction to Ambient, (θ_{JA}) *
TDFN2X3-14 . . . . . 69°C/W
Continuous Power Dissipation (T_A = +25°C)*
TDFN2X3-14 . . . . . 1.9W
Thermal Resistance Junction to Case, (θ_{JC})
TDFN2X3-14 . . . . . 45°C/W
Operating Temperature Range . . . . . -40°C to 85°C
Storage Temperature Range . . . . . -65°C to 150°C
Reflow Temperature (soldering, 10 sec) . . . . . 260°C
ESD(HBM) 2kV
ESD(CDM) 1kV

*Please refer to Minimum Footprint PCB Layout Section.

Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Bias Voltage Range	V_{BIAS}	4.5	---	5.5	V
Input Voltage Range	$V_{IN1,2}$	0.7	---	2.2	V
Output Voltage Range	$V_{OUT1,2}$	---	---	VIN1,2	V
EN Voltage Range	EN1,2	0	---	V_{BIAS}	V
VOUT Output Current (Single Channel)	I_{OUT}	0	---	4	A
Maximum Pulsed Switch Current, Pulse<300μs,1% Duty Cycle (Single Channel)		---	6	---	A
Input Capacitor	$C_{IN1,2}$	*(1)	---	---	μF

Electrical Characteristics

(V_{IN1} = V_{IN2} = 1.05V, V_{BIAS}= 5V, T_A = 25 ºC (unless otherwise noted)

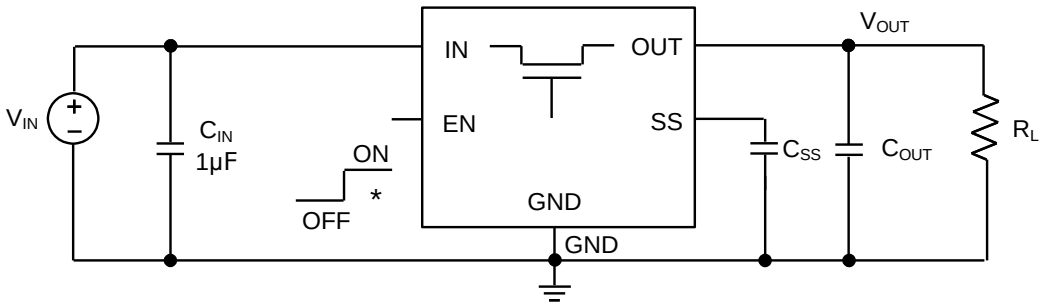
PARAMETER	SYMBOL	Conditions		MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}			0.7	---	2.2	V
Bias Voltage Range	V_{BIAS}			4.5	---	5.5	V
Bias Current	I_{BIAS}	IOUT1 = IOUT2 = 0A, EN1 = EN2 = V_{BIAS} = 5V		---	40	---	μA
Shutdown Bias Current	I_{SHDN}	ENx = GND, VOUTx = 0V		---	3	---	μA
Off-state Supply Current	I_{IN_OFF}	ENx = GND, VOUTx = 0V,		---	1	10	μA
EN pin Input leakage Current	I_{EN_LEAK}	EN=5V		---	---	1	μA
On -Resistance	$R_{DS(on)}$	ENx = VBIAS = 5V IOUTx = -500mA	VINx=1.8V	---	24	32	mΩ
			VINx=1.5V	---	23	31	
			VINx=1.05V	---	20	28	
			VINx=0.7V	---	19	27	
Discharge Resistance	R_{DIS}	ENx = 0V, IOUTx = 1mA		---	220	290	Ω
High level input voltage on EN pin	VIH			1.2	---	---	V
Low level input voltage on EN pin	VIL			---	---	0.5	V
Over Temperature Threshold	OT			---	155	---	ºC
Turn-ON Delay Time	t_D	R_L=10Ω, C_{OUT}=0.1μF, C_{SS}=Open		5	14	27	μs
Turn-ON Rise Time	t_R			12	22	37	
Turn-ON Time	t_{ON}			---	33	58	
Turn-OFF Fall Time *(2)	t_F			---	2	---	
Turn-OFF Time	t_{OFF}			---	2	---	
V_{OUT} ramp up slew rate *(2)	SR	VOUTx = 10%*V_{IN} to 90%*V_{IN}		---	---	100	mV/μs

Note

(1):1μF C_{IN} is sufficient in most application cases. If the distance of power trace on PCB is longer than general design, larger C_{IN} is highly recommended for normal operation.

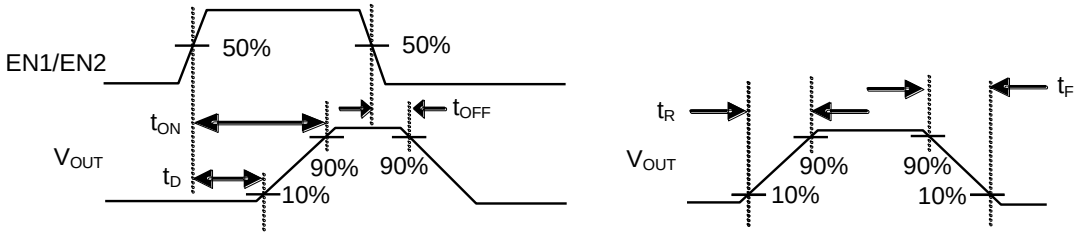
(2):Turn-OFF fall time and V_{OUT} ramp up slew rate is guaranteed by calculation

Parametric Measurement Information



(Single channel shown for clarity)

Test Circuit



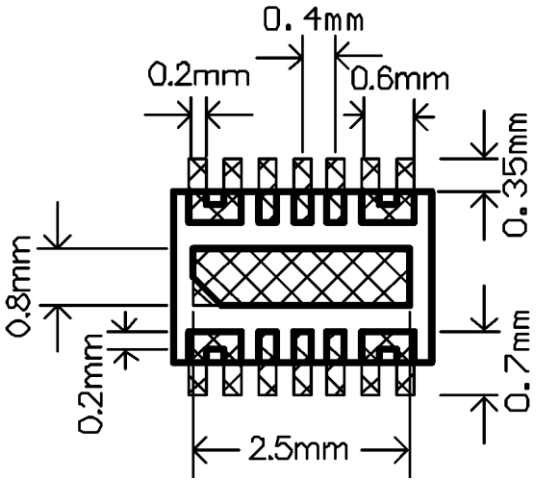
t_{ON} /t_{OFF} WAVEFORMS

*. Rising and falling time of control signal EN1,EN2 is 100ns

Figure 1. Test Circuit and t_{ON} / t_{OFF} Waveforms

Minimum Footprint PCB Layout Section

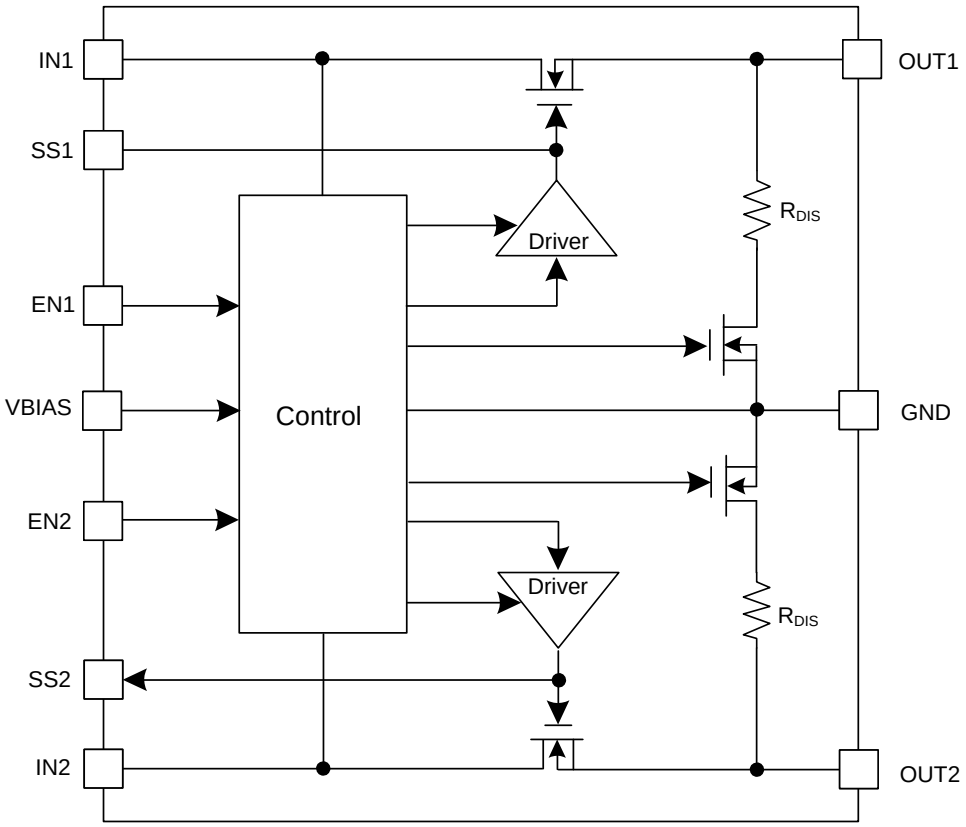
TDFN2X3-14



Pin Description

PIN NO.	PIN NAME	I/O	DESCRIPTION
1	IN1	I	Switch1 Input
2	IN1	I	Switch1 Input
3	EN1	I	Switch 1 Control Input
4	VBIAS	I	Input Bias Supply
5	EN2	I	Switch 2 Control Input
6	IN2	I	Switch 2 Input
7	IN2	I	Switch 2 Input
8	OUT2	O	Switch 2 Output
9	OUT2	O	Switch 2 Output
10	SS2	O	Switch2 Ramp capacitor input
11	GND	-	Ground
12	SS1	O	Switch 1 Ramp capacitor input
13	OUT1	O	Switch 1 Output
14	OUT1	O	Switch 1 Output
15	Thermal Pad	-	Exposed Pad to alleviate thermal stress. Solder to GND in PCB layout.

Block Diagram



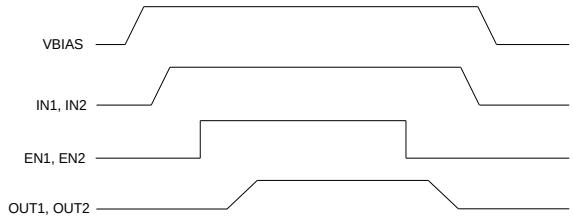
Application Information

V_{BIAS} and V_{IN} voltage range

For optimal $R_{DS(on)}$ performance, make sure $V_{IN}+3 \leqq V_{BIAS}$. Be sure to never exceed the maximum voltage rating for V_{BIAS} and V_{IN}.

Power Sequence

To operate safely, the VBIAS of G2894 must be ready firstly. Then, IN1 and IN2 can be applied. After VBIAS and IN1/IN2 are ready completely, the switch can be ON/OFF properly by asserting and deasserting EN1/EN2. VBIAS should maintain ON until IN1 / IN2 are OFF.



Input capacitor (optional)

To limit the voltage drop on the input supply caused by transient inrush currents when the switch turns on into a discharge load capacitor or short-circuit, a capacitor need to be placed between V_{IN} and GND. A 1μF ceramic capacitor, C_{IN}, placed close to the pins, is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop during high-current application. When switching heavy loads, it is recommended to have a C_{IN} about 10 times higher than the C_{OUT} to avoid excessive voltage drop.

Output capacitor (optional)

Due to the integrated body diode in the NMOS switch, a C_{IN} greater than C_{OUT} is highly recommended. A C_{OUT} greater than C_{IN} can cause V_{OUT} to exceed V_{IN} when the system supply is removed.

This could result in current flow through the body diode from V_{OUT} to V_{IN}. A C_{IN} to C_{OUT} ratio of 10 to 1 is recommended for minimizing V_{IN} dip caused by inrush currents during startup, however a 10 to 1 ratio for capacitance in not required for proper functionality of the device. A ratio smaller than 10 to 1 (such as 1 to 1) could cause slightly more V_{IN} dip upon turn due to inrush currents. This can be mitigated by increasing the capacitance on the SS pins for a longer rise time.

Parallel Application

For the application of requiring lower $R_{DS(on)}$, G2894 OUT1 and OUT2 can be tied together for obtaining lower $R_{DS(on)}$. In the parallel application, Both EN1 and EN2 must connect together, also, C_{SS1} and C_{SS2} must connect together too.

Adjustable V_{OUT} rise time

A capacitor to GND on the SS pins sets the slew rate for each channel. To ensure desired performance, a capacitor with a minimum voltage rating of 25V should be used on the SS pin. An approximate formula for the relationship between SS and slew rate is (the equation below accounts for 10% to 90% measurement on V_{OUT} and does NOT apply for C_{SS} = 0pF. Use table below to determine rise times for when C_{SS}=0pF):

$$Tr\ (\mu s) \approx (0.15 \times C_{SS}+27) \times V_{IN}$$

Where,

C_{SS} = the capacitance on the SS pin (in pF)

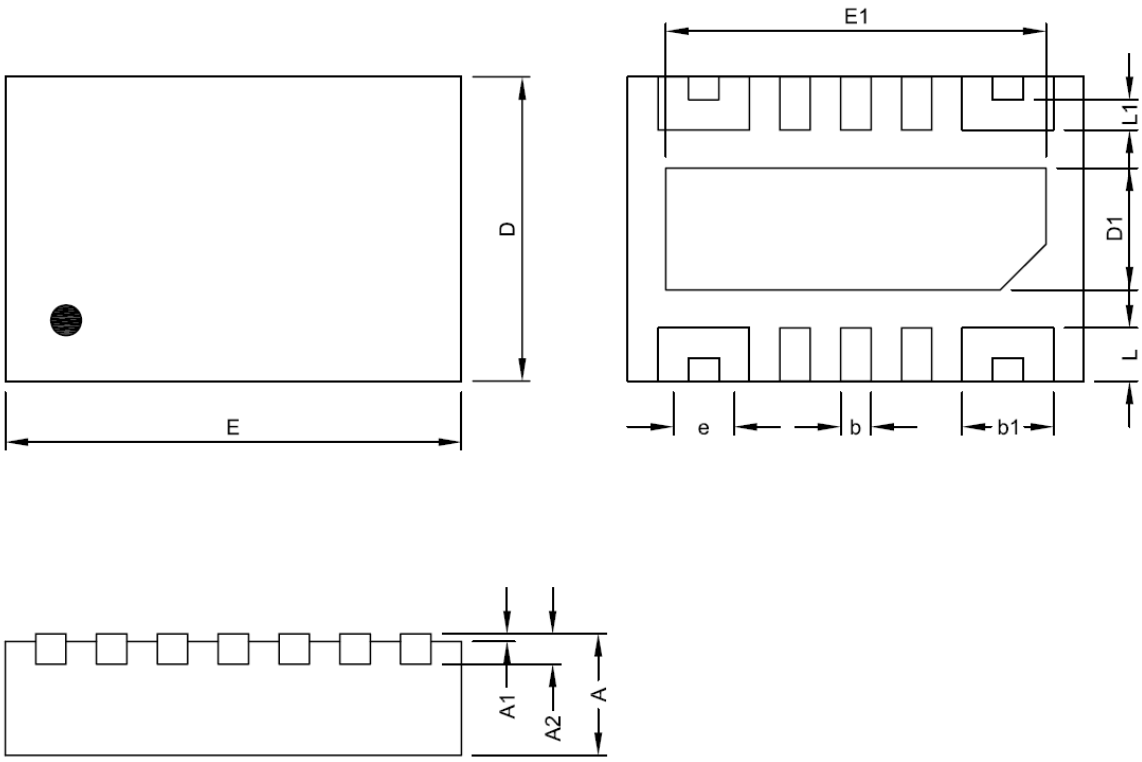
Rise time can be calculated by multiplying the input voltage by the slew rate. The table below contains rise time values measured on a typical device. Rise times shown below are only valid for the power-up sequence where V_{IN} and V_{BIAS} are already in steady state condition and the EN pin is asserted high.

C_{SS} (pF)	Rise time, Tr (μs) 10% - 90% of V_{IN}, C_L=0.1μF, C_{IN}=1μF, R_L=10Ω Typical values at 25ºC, V_{BIAS}=5V			
	1.8V	1.5V	1.05V	0.7V
N.C.	40	35	27	25
470	173	146	105	81
1,000	325	285	200	150
2,200	660	580	400	300
4,700	1390	1230	830	590

PCB Layout Guidelines

1. To have lower voltage drop in field application, short and wide PCB trace is recommended. The IN / OUT pins are located in corner of IC. It is beneficial to route a wide and short PCB trace.
2. To absorb voltage bounce that is caused by parasitic inductor of PCB trace at quick load transient, placing C_{IN} / C_{OUT} close to IN / OUT pin of IC is recommended.
3. The wide trace of V_{IN} / V_{OUT} and GND can help minimize the parasitic electrical effects and the case to ambient thermal impedance. Using thermal vias located under the exposed thermal pad helps thermal dissipation of the device

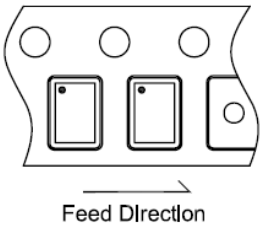
Package Information



TDFN2X3-14 Package

Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.0276	0.0295	0.0315
A1	0.00	- - -	0.05	0.0000	- - -	0.0020
A2	0.20 REF			0.0079 REF		
D	1.95	2.00	2.05	0.0768	0.0787	0.0807
E	2.95	3.00	3.05	0.1161	0.1181	0.1201
D1	0.75	0.85	0.95	0.0295	0.0335	0.0374
E1	2.45	2.50	2.55	0.0965	0.0984	0.1004
b	0.15	0.20	0.25	0.0059	0.0079	0.0098
b1	0.60 REF			0.0236 REF		
e	0.40 BSC			0.0157 BSC		
L	0.30	0.35	0.40	0.0118	0.0138	0.0157
L1	0.20 BSC			0.0079 BSC		

Taping Specification



PACKAGE	Q'TY/BY REEL
TDFN2X3-14	3,000 ea