

Dual Ultra-Low On-Resistance Load Switch with Controlled Turn-On

Features

- Integrated Dual Channel Load Switch
- Input Voltage Range: 0.7V to 5.5V
- Dual Ultra-low ON-Resistance (16mΩ)
 - $R_{DS(on)} = 17m\Omega$ at $V_{IN} = 5V$ ($V_{BIAS} = 5V$)
 - $R_{DS(on)} = 16m\Omega$ at $V_{IN} = 3.6V$ ($V_{BIAS} = 5V$)
 - $R_{DS(on)} = 16m\Omega$ at $V_{IN} = 1.8V$ ($V_{BIAS} = 5V$)
 - $R_{DS(on)} = 15m\Omega$ at $V_{IN} = 0.8V$ ($V_{BIAS} = 5V$)
- 6A Continuous Switch Current per channel
- Low Quiescent Current
 - 65μA (Both Channel)
 - 55μA (Single Channel)
- Low Threshold Control Inputs
- Adjustable Slew-rate Control
- Quick Output Discharge Transistor
- 14 Pin TDFN Package with Thermal Pad

General Description

The G2898 is dual N-channel MOSFET power switch designed for high-side load-switching application. The device has a typical $R_{DS(ON)}$ of 16mΩ and the output current is limited to 6A. Each channel is controlled by an on/off input (EN1, EN2) independently, which is suitable for interfacing directly with low-voltage I/O ports.

In the G2898, a 250Ω on-chip load resistor is added for quick output discharge (QOD) when the switch is turned off. Moreover, the controlled rise time can be adjusted by using a ceramic capacitor on the CTx pins in order to prevent in-rush current at start-up time.

The G2898 is available in 14 pin TDFN package.

Applications

- Notebooks / Netbooks
- Tablet PCs
- Consumer Electronics
- Set-Top-Boxes
- Industrial Systems
- Telecom Systems

Ordering Information

ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE (Green)
G2898KD1U	2898	-40°C to 85°C	TDFN2X3-14

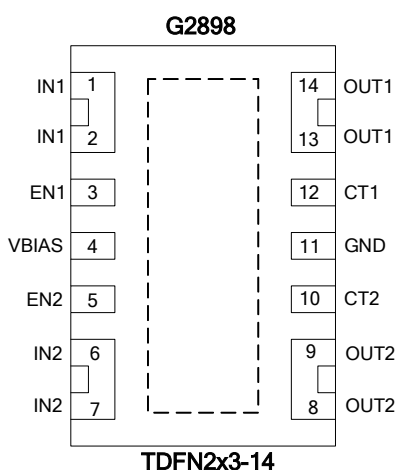
Note: KD: TDFN2X3-14

1: Bonding Code

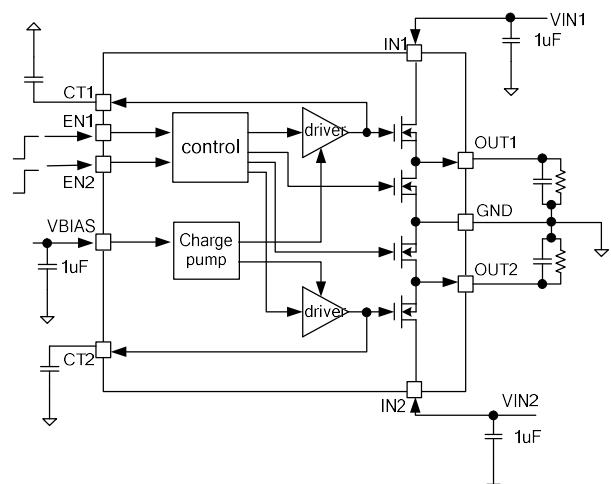
U: Tape & Reel

Green : Lead Free / Halogen Free.

Pin Configuration



Typical Application Circuit



Absolute Maximum Ratings

V_{IN1}, V_{IN2} to GND -0.3V to +6V
 $EN1, EN2$ to GND -0.3V to +6V
 V_{OUT1}, V_{OUT2} to GND -0.3V to +6V
 $CT1, CT2$ to GND -0.3V to +12V
 V_{BIAS} to GND -0.3V to +6V
 Continuous Switch Current (I_{MAX}) 6A
 Junction Temperature 150°C

Operating Temperature Range -40°C to 85°C
 Storage Temperature Range -65°C to 150°C
 Reflow Temperature (soldering, 10sec) 260°C
 ESD(HBM) 2KV⁽¹⁾
 ESD(CDM) ±1000V

Note 1 : Human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.

Thermal Information

THERMAL METRIC		TDFN2X3-14	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance	55.3	°C/W
$R_{\theta JC_top}$	Junction to case top thermal resistance	83.8	°C/W
$R_{\theta JB}$	Junction to board thermal resistance	21.7	°C/W
Ψ_{JT}	Junction to top characterization parameter	2.7	°C/W
Ψ_{JB}	Junction to board characterization parameter	21.8	°C/W
$R_{\theta JC_bot}$	Junction to case bottom thermal resistance	6.7	°C/W

- Package thermal metric is obtained using the method described in JEDEC specification JESD51-7, using a four-layer board.
- The maximum power dissipation is $P_{D(MAX)} = \frac{(T_{JMAX} - T_A)}{R_{\theta JA}}$, Exceeding the maximum allowable power dissipation results in excessive die temperature, and the device will enter thermal shutdown.

Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Input voltage range	$V_{IN1,2}$	0.7	---	V_{BIAS}	V
Bias voltage range	V_{BIAS}	2.5	---	5.6	V
VOOUT Output Current (Single Channel)	I_{OUT}	0	---	6	A
Maximum Pulsed Switch Current, Pulse<300μs, 1% Duty Cycle (Single Channel)		---	8	---	A
ON voltage range	$EN1,2$	0	---	5.5	V
Output voltage range	$V_{OUT1,2}$	---	---	$V_{IN1,2}$	V
High-level input voltage, EN1, EN2	V_{IH}	1.2	---	5.5	V
Low-level input voltage, EN1, EN2	V_{IL}	---	---	0.5	V
Input Capacitor	$C_{IN1,2}$	1*	---	---	μF

*Note: 1μF input capacitor is sufficient in most application cases. If the distance of power trace on PCB is longer than general design, larger input capacitor is highly recommended for normal operation.

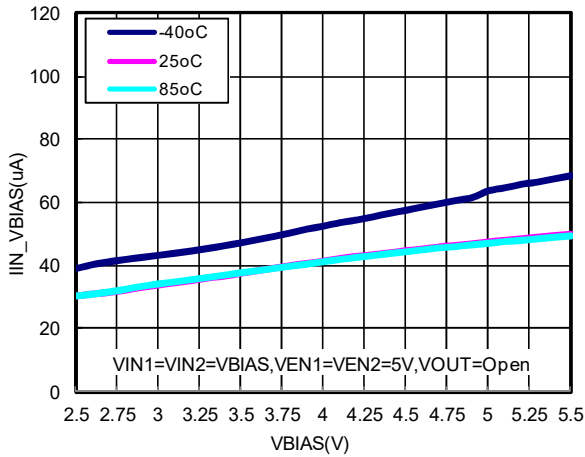
Electrical Characteristics

($V_{IN1} = 0.7V$ to $5.5V$, $V_{IN2} = 0.7V$ to $5.5V$, $V_{BIAS} = 5V$, $T_A = -40^{\circ}C$ to $85^{\circ}C$ (unless otherwise noted))

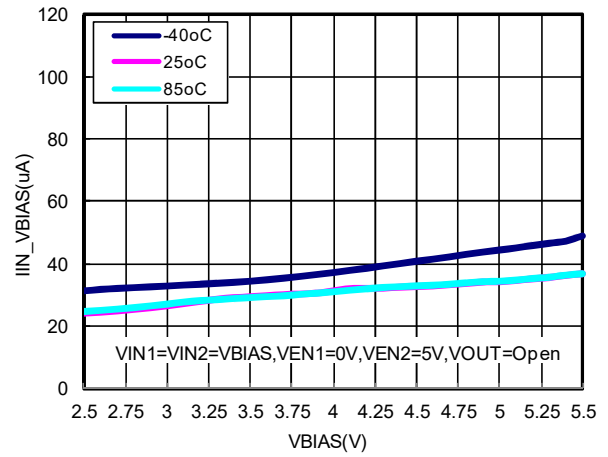
PARAMETER	SYMBOL	Conditions		T _A	MIN	TYP	MAX	UNITS
Input Voltage Range	V _{IN}			---	0.7	---	V _{BIAS}	V
Bias Voltage Range	V _{BIAS}			---	2.5	---	5.6	V
Bias Current	I _{BIAS}	IOUT1 = IOUT2 = 0, VIN1 = VIN2 = 5V EN1 = EN2 = V _{BIAS} = 5V		Full	---	65	80	μA
		IOUT1 = IOUT2 = 0, VIN1 = VIN2 = 5V EN1 = V _{BIAS} = 5V, EN2 = 0V		Full	---	53	---	μA
		IOUT1 = IOUT2 = 0, VIN1 = VIN2 = 2.5V EN1 = EN2 = V _{BIAS} = 2.5V		Full	---	40	48	μA
		IOUT1 = IOUT2 = 0, VIN1 = VIN2 = 2.5V EN1 = V _{BIAS} = 2.5V, EN2 = 0V		Full	---	33	---	μA
Shutdown Bias Current	I _{SHDN}	ENx = GND, VOUTx = 0V		Full	---	---	1	μA
Off-state Supply Current	I _{IN_OFF}	ENx = GND, VOUTx = 0V, VINx= 0.7 to 5V		Full	---	0.5	8	μA
EN pin Input leakage Current	I _{EN_LEAK}	EN=5.5V		Full	---	---	1	μA
On -Resistance	R _{DS(on)}	Enx = VBIAS, IOUTx = -200mA VBIAS = 5V,	VINx=5V	25 °C	---	17	23	mΩ
				Full	---	---	27	
			VINx=3.6V	25 °C	---	16	23	
				Full	---	---	27	
			VINx=1.8V	25 °C	---	16	23	
				Full	---	---	27	
			VINx=0.8V	25 °C	---	15	23	
				Full	---	---	27	
On -Resistance	R _{DS(on)}	Enx =VBIAS, IOUTx = -200mA VBIAS = 2.5V,	VINx=2.5V	25 °C	---	18	25	mΩ
				Full	---	---	30	
			VINx=1.8V	25 °C	---	17	25	
				Full	---	---	30	
			VINx=1.2V	25 °C	---	16	25	
				Full	---	---	30	
			VINx=0.8V	25 °C	---	15	25	
				Full	---	---	30	
Discharge Resistance	R _{DIS}	VINx = 5.0V,ENx = 0V, IOUTx = 1mA		Full	---	250	330	Ω
High level input voltage on EN pin	VIH				1.2	---	5.5	V
Low level input voltage on EN pin	VIL				---	0	0.5	V
Over Temperature Threshold	OT				---	155	---	°C
Over Temperature Hysteresis					---	25	---	°C

Typical Performance Characteristics
($T_A=25^\circ\text{C}$)

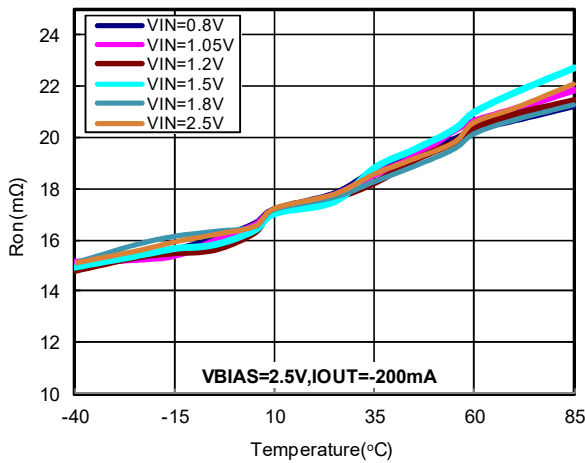
QUIESCENT CURRENT vs. V_{BIAS}
(BOTH CHANNELS)



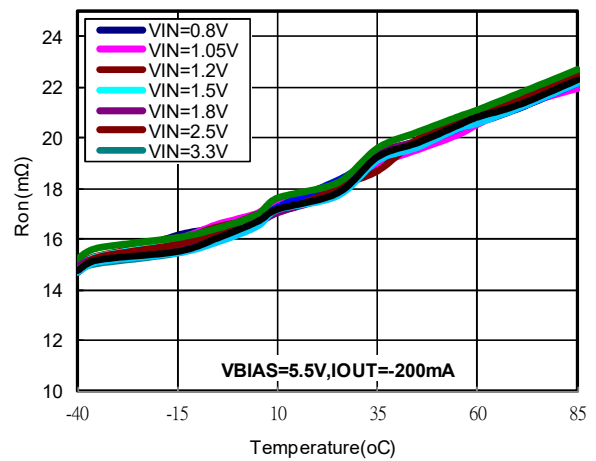
QUIESCENT CURRENT vs. V_{BIAS}
(SINGLE CHANNEL)



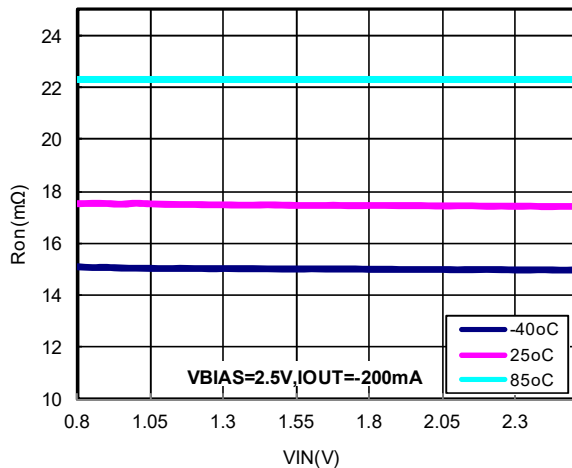
R_{ON} vs. TEMPERATURE
($V_{BIAS}=2.5\text{V}$, SINGLE CHANNEL)



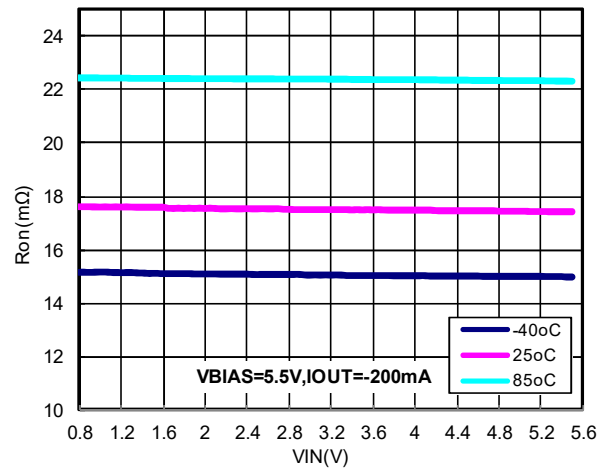
R_{ON} vs. TEMPERATURE
($V_{BIAS}=5.5\text{V}$, SINGLE CHANNEL)



R_{ON} vs. V_{IN} ($V_{BIAS}=2.5\text{V}$, SINGLE CHANNEL)

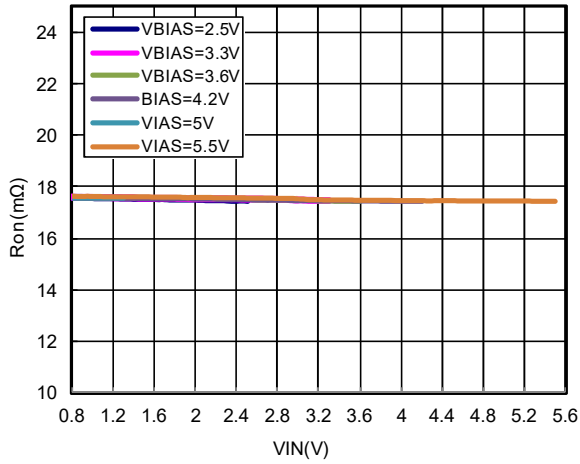


R_{ON} vs. V_{IN} ($V_{BIAS}=5.5\text{V}$, SINGLE CHANNEL)

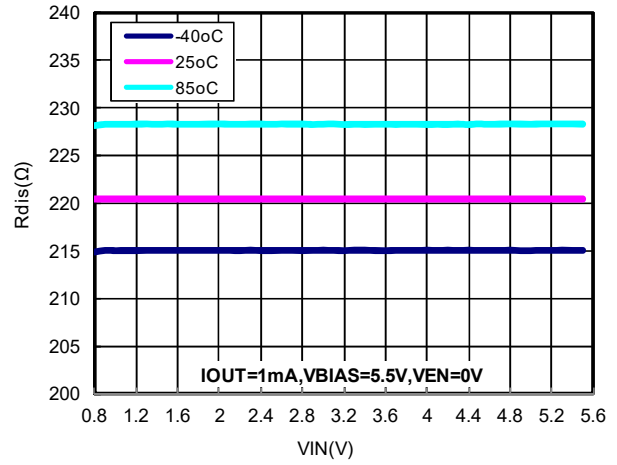


Typical Performance Characteristics (continued)

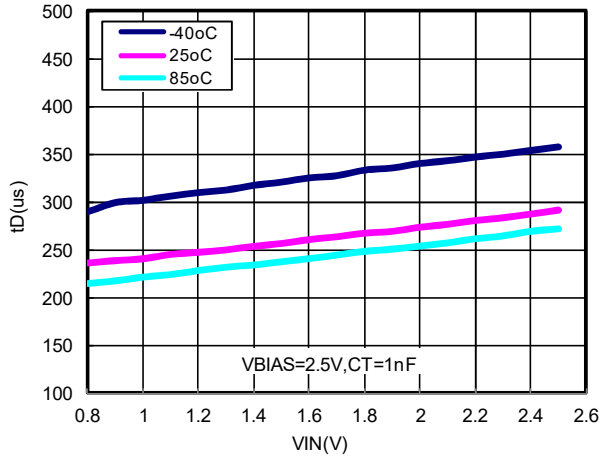
R_{ON} vs. V_{IN} (T_A=25°C, SINGLE CHANNEL)



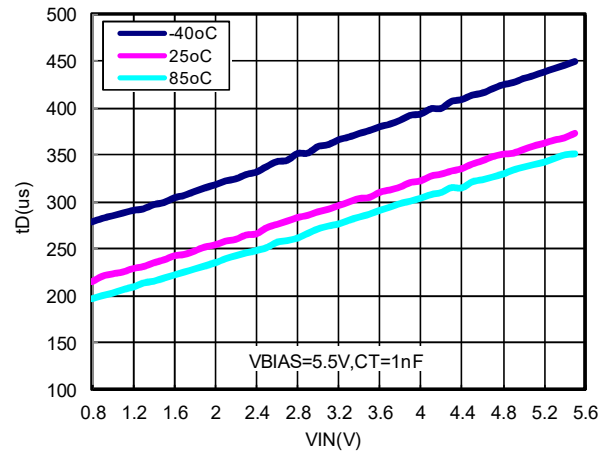
R_{DIS} vs. V_{IN} (V_{BIAS}=5.5V, SINGLE CHANNEL)



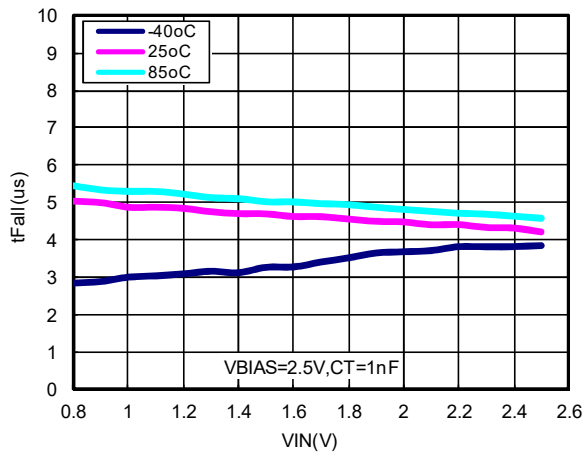
T_D vs. V_{IN} (V_{BIAS}=2.5V, CT=1nF)



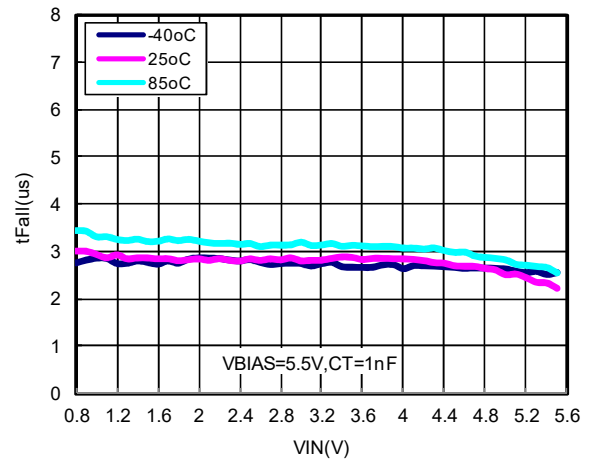
T_D vs. V_{IN} (V_{BIAS}=5.5V, CT=1nF)



T_F vs. V_{IN} (V_{BIAS}=2.5V, CT=1nF)

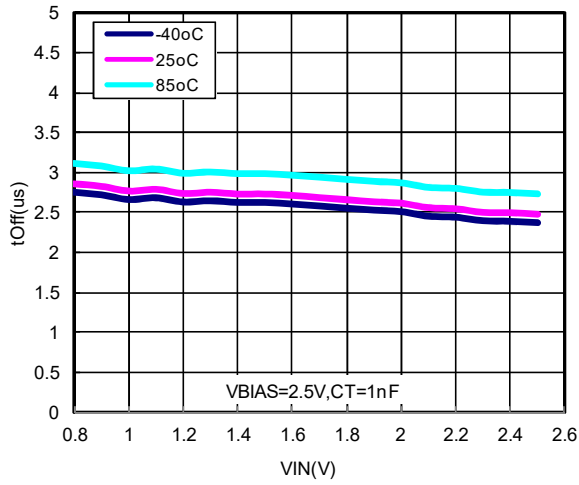


T_F vs. V_{IN} (V_{BIAS}=5.5V, CT=1nF)

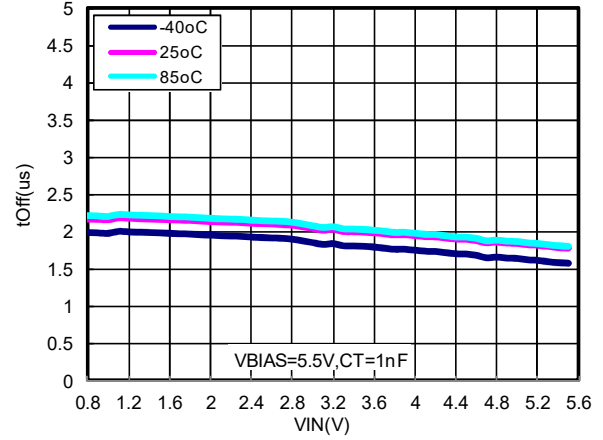


Typical Performance Characteristics (continued)

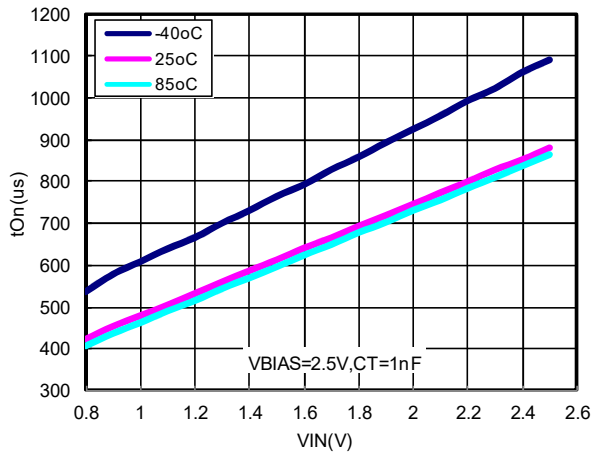
T_{OFF} vs. V_{IN} ($V_{BIAS}=2.5V, C_T=1nF$)



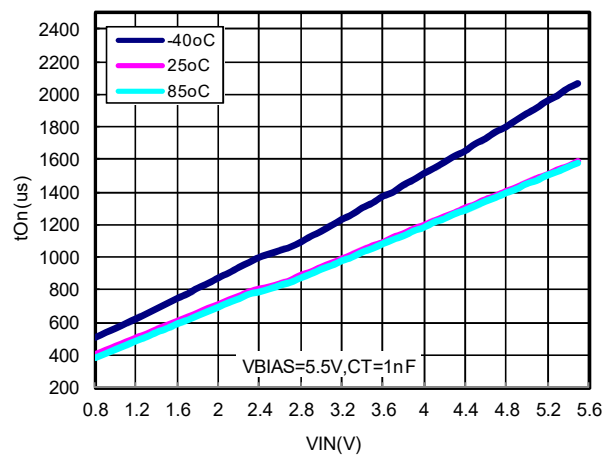
T_{OFF} vs. V_{IN} ($V_{BIAS}=5.5V, C_T=1nF$)



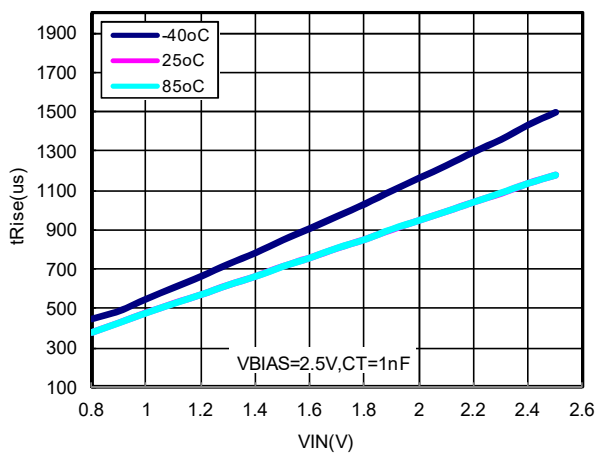
T_{ON} vs. V_{IN} ($V_{BIAS}=2.5V, C_T=1nF$)



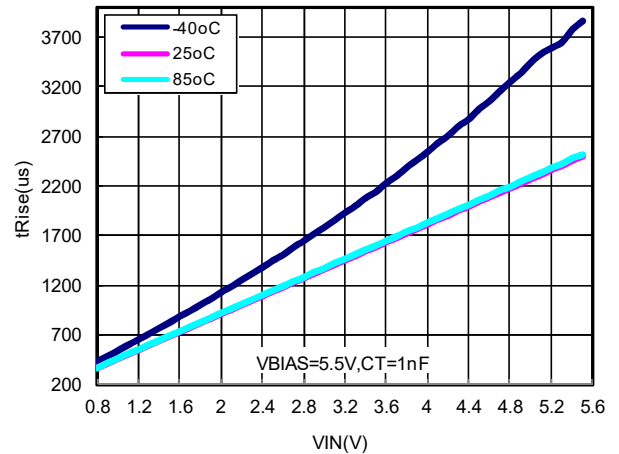
T_{ON} vs. V_{IN} ($V_{BIAS}=5.5V, C_T=1nF$)



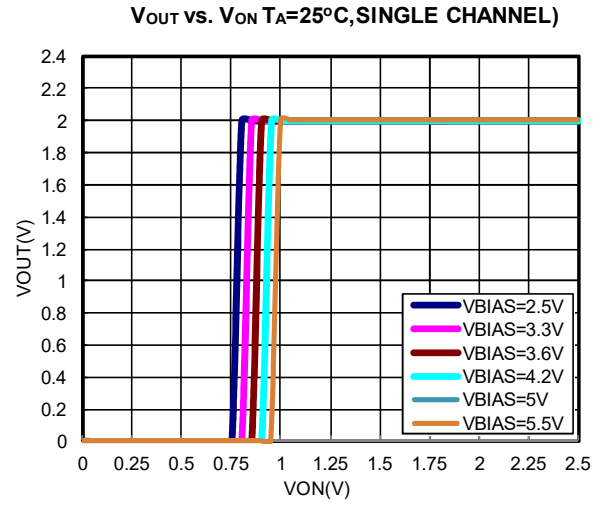
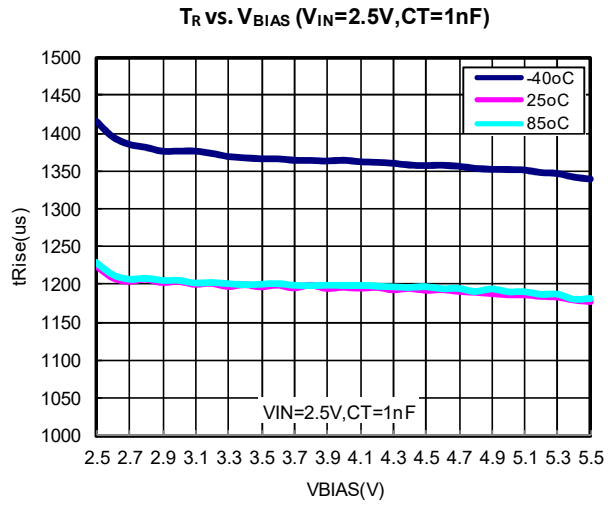
T_R vs. V_{IN} ($V_{BIAS}=2.5V, C_T=1nF$)

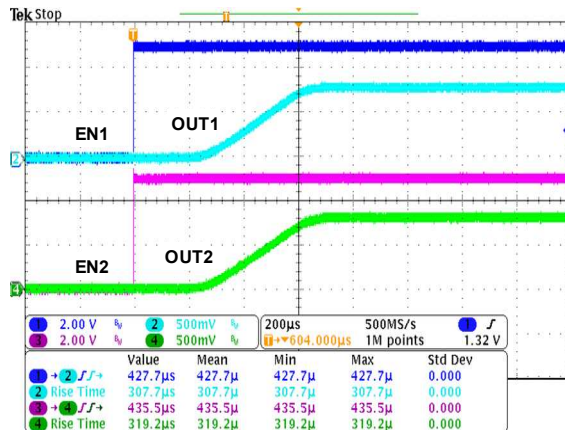
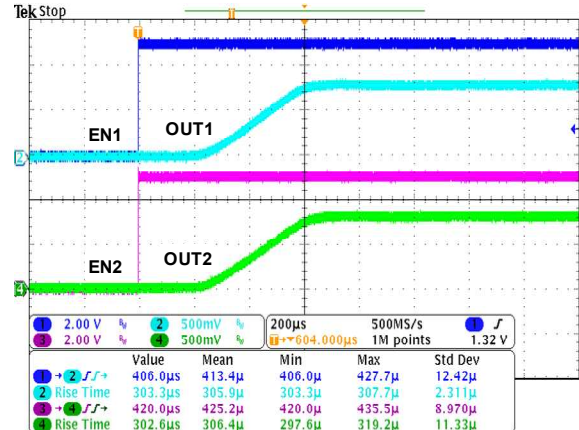
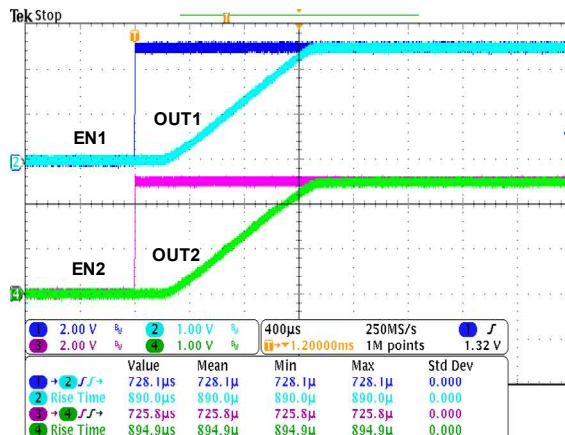
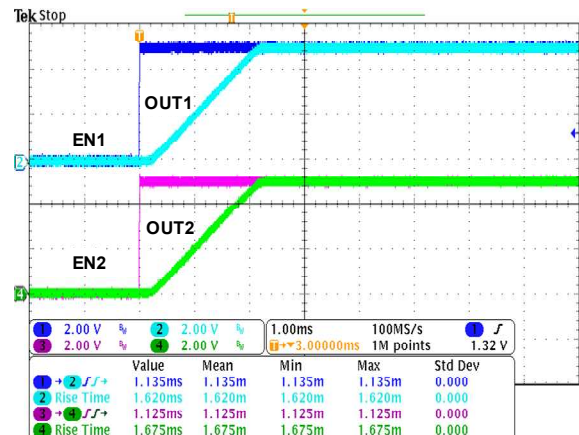
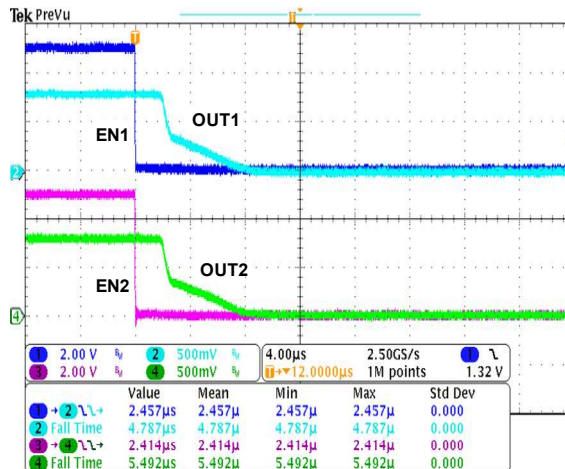
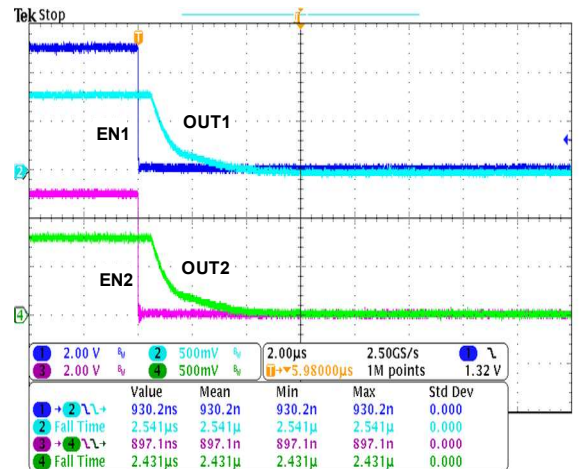


T_R vs. V_{IN} ($V_{BIAS}=5.5V, C_T=1nF$)



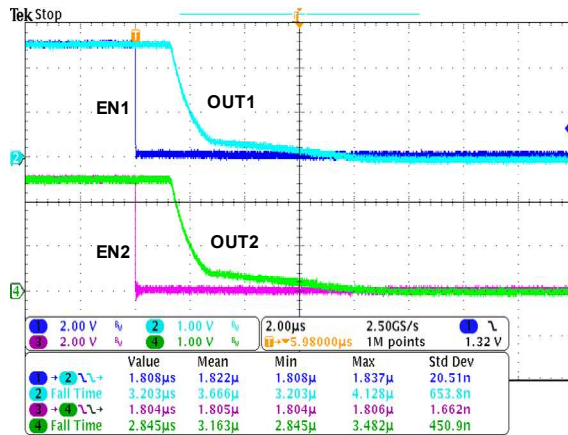
Typical Performance Characteristics (continued)



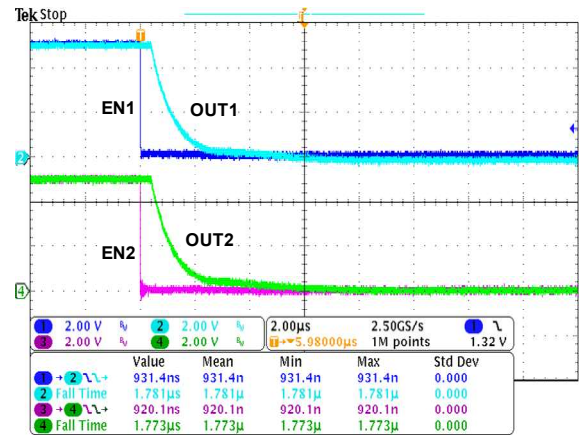
Typical Performance Characteristics (continued)
TURN-ON RESPONSE TIME($V_{IN}=0.8V, V_{BIAS}=2.5V$)

TURN-ON RESPONSE TIME($V_{IN}=0.8V, V_{BIAS}=5V$)

TURN-ON RESPONSE TIME($V_{IN}=2.5V, V_{BIAS}=2.5V$)

TURN-ON RESPONSE TIME($V_{IN}=5V, V_{BIAS}=5V$)

TURN-OFF RESPONSE TIME($V_{IN}=0.8V, V_{BIAS}=2.5V$)

TURN-OFF RESPONSE TIME($V_{IN}=0.8V, V_{BIAS}=5V$)


Typical Performance Characteristics (continued)

TURN-OFF RESPONSE TIME($V_{IN}=2.5V, V_{BIAS}=2.5V$)

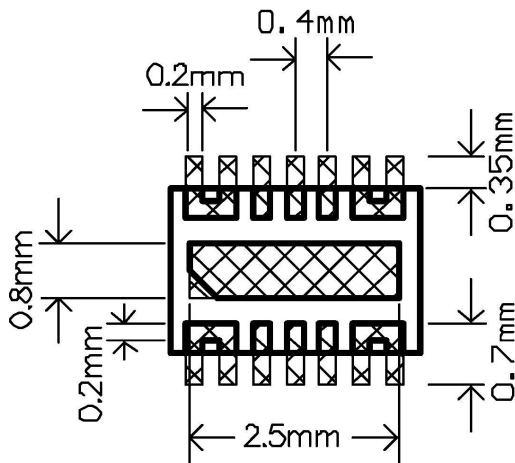


TURN-OFF RESPONSE TIME($V_{IN}=5V, V_{BIAS}=5V$)



Minimum Footprint PCB Layout Section

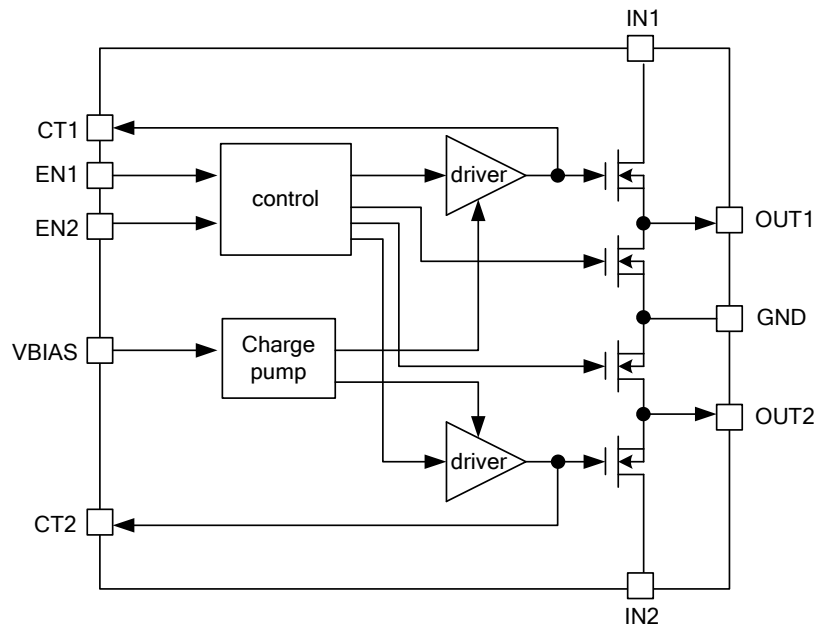
TDFN2X3-14



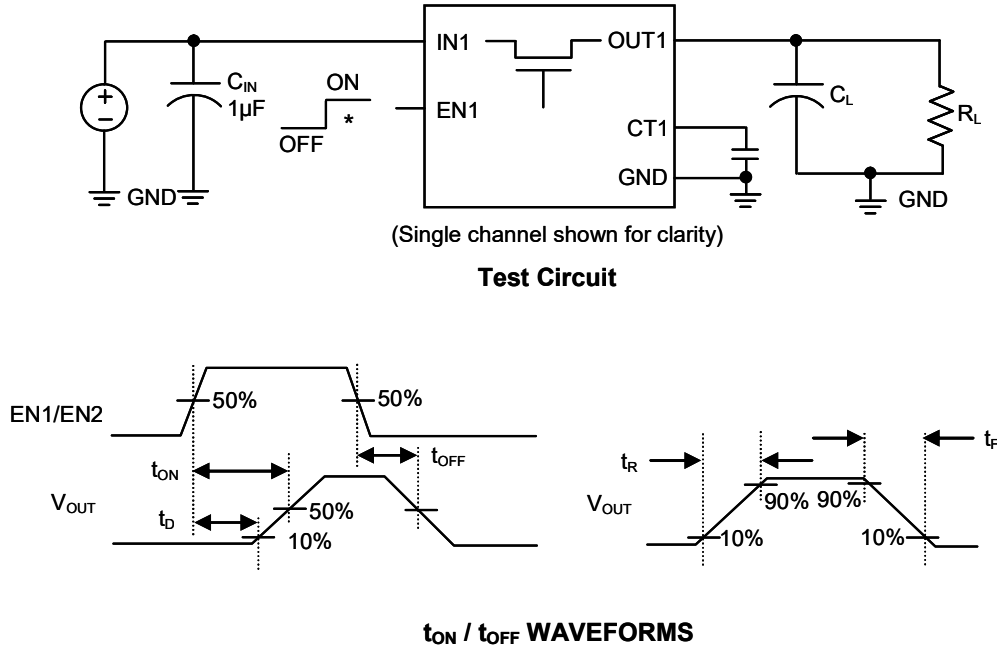
Pin Description

PIN NO.	PIN NAME	I/O	DESCRIPTION
1	IN1	I	Switch1 Input
2	IN1	I	Switch1 Input
3	EN1	I	Switch 1 Control Input
4	VBIAS	I	Input Bias Supply
5	EN2	I	Switch 2 Control Input
6	IN2	I	Switch 2 Input
7	IN2	I	Switch 2 Input
8	OUT2	O	Switch 2 Output
9	OUT2	O	Switch 2 Output
10	CT2	O	Switch2 Ramp capacitor input
11	GND	-	Ground
12	CT1	O	Switch 1 Ramp capacitor input
13	OUT1	O	Switch 1 Output
14	OUT1	O	Switch 1 Output
15	Thermal Pad	O	Exposed Pad to alleviate thermal stress. Solder to GND in PCB layout.

Block Diagram



Parametric Measurement Information



*. Rising and falling time of control signal EN1,EN2 is 100ns

Figure 1. Test Circuit and t_{ON} / t_{OFF} Waveforms

SWITCHING CHARACTERISTICS

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{IN}=V_{EN}=V_{BIAS}=5V, T_A=25°C (unless otherwise noted)					
t _{ON}	R _L =10Ω, C _L =0.1μF, C _T =1000pF	---	1210	---	μs
t _{OFF}	R _L =10Ω, C _L =0.1μF, C _T =1000pF	---	1	---	
t _R	R _L =10Ω, C _L =0.1μF, C _T =1000pF	---	1600	---	
t _F	R _L =10Ω, C _L =0.1μF, C _T =1000pF	---	2	---	
t _D	R _L =10Ω, C _L =0.1μF, C _T =1000pF	---	410	---	
V_{IN}=0.8V, V_{EN}=V_{BIAS}=5V, T_A=25°C (unless otherwise noted)					
t _{ON}	R _L =10Ω, C _L =0.1μF, C _T =1000pF	---	440	---	μs
t _{OFF}	R _L =10Ω, C _L =0.1μF, C _T =1000pF	---	1	---	
t _R	R _L =10Ω, C _L =0.1μF, C _T =1000pF	---	315	---	
t _F	R _L =10Ω, C _L =0.1μF, C _T =1000pF	---	3	---	
t _D	R _L =10Ω, C _L =0.1μF, C _T =1000pF	---	280	---	
V_{IN}=2.5V, V_{EN}=5V, V_{BIAS}=2.5V, T_A=25°C (unless otherwise noted)					
t _{ON}	R _L =10Ω, C _L =0.1μF, C _T =1000pF	---	790	---	μs
t _{OFF}	R _L =10Ω, C _L =0.1μF, C _T =1000pF	---	2	---	
t _R	R _L =10Ω, C _L =0.1μF, C _T =1000pF	---	870	---	
t _F	R _L =10Ω, C _L =0.1μF, C _T =1000pF	---	3	---	
t _D	R _L =10Ω, C _L =0.1μF, C _T =1000pF	---	360	---	
V_{IN}=0.8V, V_{EN}=5V, V_{BIAS}=2.5V, T_A=25°C (unless otherwise noted)					
t _{ON}	R _L =10Ω, C _L =0.1μF, C _T =1000pF	---	460	---	μs
t _{OFF}	R _L =10Ω, C _L =0.1μF, C _T =1000pF	---	2	---	
t _R	R _L =10Ω, C _L =0.1μF, C _T =1000pF	---	330	---	
t _F	R _L =10Ω, C _L =0.1μF, C _T =1000pF	---	3	---	
t _D	R _L =10Ω, C _L =0.1μF, C _T =1000pF	---	300	---	

Application Information

V_{IN} and V_{BIAS} voltage range

For optimal $R_{DS(on)}$ performance, make sure $V_{IN} \leq V_{BIAS}$. The device will still be functional if $V_{IN} > V_{BIAS}$ but it will exhibit $R_{DS(on)}$ greater than what is listed in the Electrical characteristics table. See Figure below for an example for a typical device. Notice the increasing $R_{DS(on)}$ as V_{IN} exceeds V_{BIAS} voltage. Be sure to never exceed the maximum voltage rating for V_{IN} and V_{BIAS} .

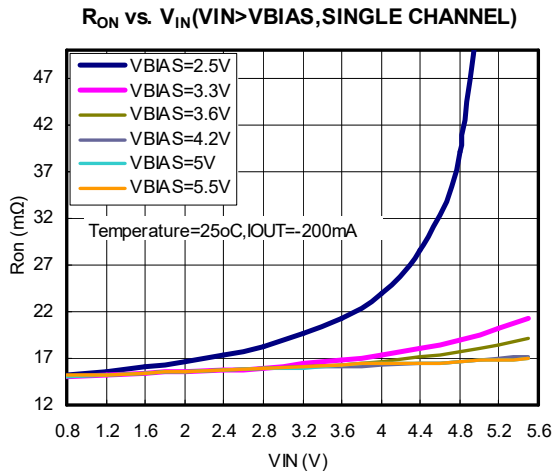


Figure 2. $R_{DS(on)}$ vs. V_{IN} ($V_{IN} > V_{BIAS}$ Single Channel)

Adjustable rise time

A capacitor to GND on the CT pins sets the slew rate for each channel. To ensure desired performance, a capacitor with a minimum voltage rating of 25V should be used on the CT pin. An approximate formula for the relationship between CT and slew rate is (the equation below accounts for 10% to 90% measurement on VOUT and does NOT apply for CT = 0pF. Use table below to determine rise times for when CT=0pF):

$$SR = 0.37 \times CT + 17.8$$

Where,

SR = slew rate (in $\mu\text{s/V}$)

CT = the capacitor value on the CT pin (in pF)

The units for the constant 17.8 is in $\mu\text{s/V}$.

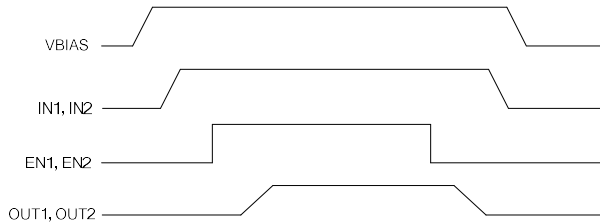
Rise time can be calculated by multiplying the input voltage by the slew rate. The table below contains rise time values measured on a typical device. Rise times shown below are only valid for the power-up sequence where V_{IN} and V_{BIAS} are already in steady state condition and the EN pin is asserted high.

CTx(pF)	Rise time (μs) 10% - 90%, $C_L=0.1\mu\text{F}$, $C_{IN}=1\mu\text{F}$, $R_L=10\Omega$ Typical values at 25°C, $V_{BIAS}=5\text{V}$						
	5V	3.3V	1.8V	1.5V	1.2V	1.05V	0.8V
0	99	72	50	44	39	36	32
220	496	338	198	170	142	128	103
470	920	616	348	298	246	220	177
1000	1708	1148	658	556	456	408	328
2200	4250	2770	1550	1290	1052	940	736
4700	8520	5680	3160	2650	2160	1910	1520
10000	18400	12280	6860	5760	4700	4230	3360

Application Information

Power Sequence

To operate safely, the VBIAS of G2898 must be ready firstly. Then, IN1 and IN2 can be applied. After VBIAS and IN1/IN2 are ready, the switch can be ON/OFF properly by asserting and de-asserting EN1/EN2. VBIAS should maintain ON until IN1/IN2 are OFF.



Input capacitor (optional)

To limit the voltage drop on the input supply caused by transient in-rush currents when the switch turns on into a discharge load capacitor or short-circuit, a capacitor need to be placed between V_{IN} and GND. A $1\mu F$ ceramic capacitor, C_{IN} , placed close to the pins, is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop during high-current application. When switching heavy loads, it is recommended to have an input capacitor about 10 times higher than the output capacitor to avoid excessive voltage drop.

Output capacitor (optional)

Due to the integrated body diode in the NMOS switch, a C_{IN} greater than C_L is highly recommended. A C_L greater than C_{IN} can cause V_{OUT} to exceed V_{IN} when the system supply is removed. This could result in current flow through the body diode from V_{OUT} to V_{IN} . A C_{IN} to C_L ratio of 10 to 1 is recommended for minimizing V_{IN} dip caused by

inrush currents during startup, however a 10 to 1 ratio for capacitance is not required for proper functionality of the device. A ratio smaller than 10 to 1 (such as 1 to 1) could cause slightly more V_{IN} dip upon turn due to inrush currents. This can be mitigated by increasing the capacitance on the CT pin for a longer rise time.

Quick Output Discharge(QOD)

In the G2898, a 250Ω on-chip load resistor is embedded for quick output discharge (QOD) when the switch is turned off to avoid any unknown state caused by the floating supply to the downstream load. The power dissipation of each channel QOD is approximately 0.15 watt for 100ms.

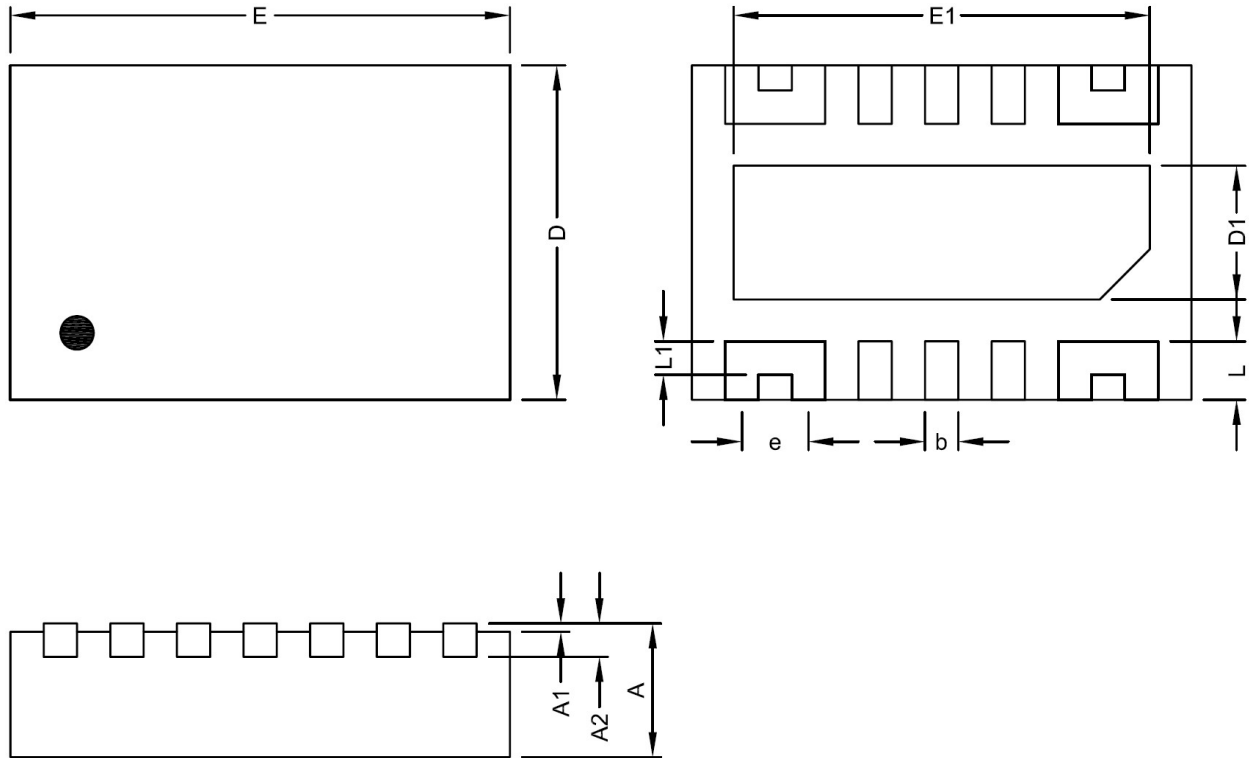
Thermal Shutdown

Thermal Shutdown protects the part from internally or externally generated excessive temperatures. When the device temperature exceeds OT (typical $155^{\circ}C$), the switch is turned off. The switch automatically turns on again if the temperature of the die drops 25 degrees below the OT threshold.

PCB Layout Guidelines

1. To have lower voltage drop in field application, short and wide PCB trace is recommended. The IN/OUT pins are located in corner of IC. It is beneficial to route a wide and short PCB trace.
2. To absorb voltage bounce that is caused by parasitic inductor of PCB trace at quick load transient, placing C_{IN}/C_{OUT} close to IN/OUT pin of IC is recommended.
3. The wide trace of V_{IN}/V_{OUT} and GND can help minimize the parasitic electrical effects and the case to ambient thermal impedance. Using thermal vias located under the exposed thermal pad helps thermal dissipation of the device

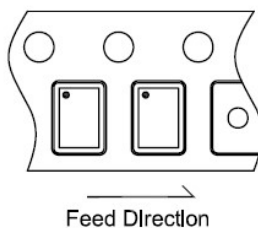
Package Information



TDFN2X3-14 Package

Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.0276	0.0295	0.0315
A1	0.00	---	0.05	0.0000	---	0.0020
A2	0.20 REF			0.0079 REF		
D	1.95	2.00	2.05	0.0768	0.0787	0.0807
E	2.95	3.00	3.05	0.1161	0.1181	0.1201
D1	0.75	0.85	0.95	0.0295	0.0335	0.0374
E1	2.45	2.50	2.55	0.0965	0.0984	0.1004
b	0.15	0.20	0.25	0.0059	0.0079	0.0098
e	0.40 BSC			0.0157 BSC		
L	0.30	0.35	0.40	0.0118	0.0138	0.0157
L1	0.20 BSC			0.0079 BSC		

Taping Specification



PACKAGE	Q'TY/BY REEL
TDFN2X3-14	3,000 ea

GMT Inc. does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and GMT Inc. reserves the right at any time without notice to change said circuitry and specifications.