# G2986

# LPDDR2/LPDDR3/DDR4 Termination Regulator

## Features

- **Support 1.2V LPDDR2/LPDDR3/DDR4 (0.6VTT) and DDR 3L (0.675VTT) Requirements**
- **Input Voltage Range: 3V to 5.5V**
- **VLDOIN Voltage Range: 1.1V to 3.6V**
- **Requires Only 20µF Ceramic Output Capacitance**
- **Supports High-Z in S3 and Soft-Off in S5**
- **Integrated Divider Tracks 1/2 VDDQSNS for Both VTT and VTTREF**
- **Remote Sensing (VTTSNS)**
- **±20mV Accuracy for VTT and VTTREF**
- **10mA Buffered Reference (VTTREF)**
- **Built-In Soft-Start**
- **Over Current Protection**
- **Thermal Shutdown Protection**
- **TDFN2X2-10 Package**

## General Description

The G2986 is a 3A sink/source tracking termination regulator. It is specifically designed for low-cost/ low-external component count systems. The G2986 maintains a high speed operational amplifier that provides fast load transient response and only requires 20µF (2×10µF) of ceramic output capacitance. The G2986 supports remote sensing functions and all features required to power the LPDDR2 /LPDDR3/DDR4 /DDR 3L VTT bus termination according to the JEDEC specification. In addition, the G2986 includes integrated sleep-state controls placing VTT in High-Z in S3 (suspend to RAM) and soft-off for VTT and VTTREF in S5 (Shutdown). The G2986 is available in the thermally efficient TDFN2X2-10.

## Applications

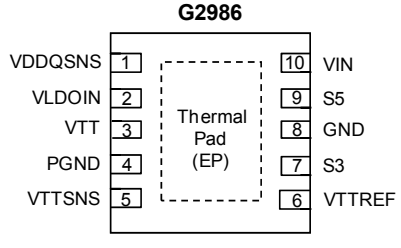
- **DDR 3L Memory Termination**
- **LPDDR2/LPDDR3/DDR4 Memory Termination**
- **SSTL−2, SSTL−18**
- **HSTL Termination**

## Ordering Information

| ORDER NUMBER | MARKING | TEMP. RANGE | PACKAGE (Green) | REMARK |
|---|---|---|---|---|
| G2986K21U | 2986 | -40°C~85°C | TDFN2X2-10 | |
| G2986K21D | 2986 | -40°C~85°C | TDFN2X2-10 | **OBSOLETE** |

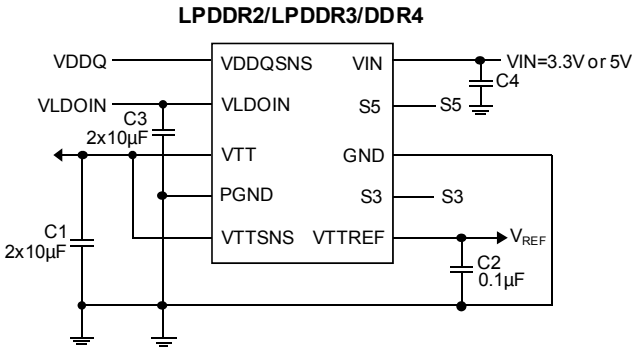
Note: K2:TDFN2X2-10
1: Bonding Code
U & D: Tape & Reel
Green : Lead Free / Halogen Free

## Pin Configuration




**TDFN2X2-10**
Note: Recommend connecting the Thermal Pad to the GND or let it keep floating.

## Typical Application Circuit



## Absolute Maximum Ratings (1)

**Supply Voltage Range**

VIN, VLDOIN, VTTSNS, VDDQSNS, S3, S5..-0.3V to +6V

PGND . . . . . -0.3V to 0.3V

**Output Voltage Range**

VTT, VTTREF . . . . . .-0.3V to VLDOIN+0.3V

Thermal Resistance of Junction to Ambient ($\theta_{JA}$)*

TDFN2X2-10. . . . . 127°C/W

Continuous Power Dissipation ($T_A$ = +25°C)*

TDFN2X2-10. . . . . .1.1W

Thermal Resistance Junction to Case, ($\theta_{JC}$)

TDFN2X2-10. . . . . .63°C/W

Maximum Junction Temperature, $T_J$ .. . . . . 160°C

Storage Temperature Range, $T_{STG}$. .-55°C to +160°C

Reflow Temperature (soldering, 10sec) . . . . . 260°C

* Measured on 1in$^2$ of 1oz PCB.

## Recommend Operating Range (1) (2)

VIN . . . . . 3V to 5.5V

S3, S5 . . . . . .-0.1V to 5.5V

VDDQSNS. . . . . .1.1V to 3.6V

VLDOIN . . . . . .1.1V to 3.6V

PGND . . . . . .-0.1V to 0.1V

**Operating Ambient Temperature Range**

$T_A$ . . . . . .. . . . .-40°C to 85°C

**Note:**

(1) All voltage values are with respect to the network ground terminal unless otherwise noted.

(2) VLDOIN, VTTSNS, VDDQSNS, S3, S5 must be lower than VIN on operation.

## Electrical Characteristics

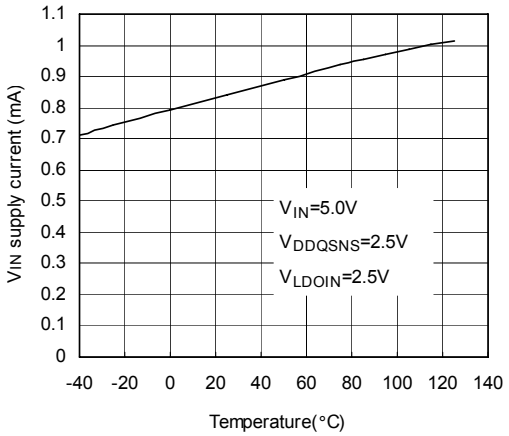
**Specifications with standard typeface are for $T_A$=25°C, $V_{IN}$=5V, VLDOIN=1.35V and VDDQSNS=1.35V. Unless otherwise specified.**

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Supply current, VIN | $I_{VIN}$ | $V_{VIN}$=5V, no load, S5=5V, S3 =5V | 0.5 | 0.8 | 2 | mA |
| Standby current, VIN | $I_{VINSTB}$ | $V_{VIN}$=5V, no load, S5=5V, S3 =0V | --- | 110 | 200 | µA |
| Shutdown current, VIN | $I_{VINSDN}$ | $V_{VIN}$=5V, no load, S5=0V, S3 =0V | --- | --- | 1 | µA |
| Supply current, VLDOIN | $I_{VLDOIN}$ | $V_{VIN}$=5V, no load, S5=5V, S3 =5V | --- | 0.03 | 2 | mA |
| Standby current, VLDOIN | $I_{VLDOINSTB}$ | $V_{VIN}$=5V, no load, S5=5V, S3 =0V | --- | 0.1 | 10 | µA |
| Shutdown current, VLDOIN | $I_{VLDOINSDN}$ | $V_{VIN}$=5V, no load, S5=0V, S3 =0V | --- | 0.1 | 1 | µA |
| VDDQSNS input Impedance | $Z_{VDDQSNS}$ | $V_{VIN}$=5V, S5=5V, S3 =5V | --- | 200 | --- | kΩ |
| VTTSNS input current | $I_{VTTSNS}$ | $V_{VIN}$=5V, S5=5V, S3 =5V | --- | 0.3 | 1 | µA |
| VTT output voltage | VTT | DDR3L | --- | 0.675 | --- | V |
| VTT Output Voltage Load Regulation (VTTREF-VTT) | $V_{OS}$VTT | $I_{VTT}$=0 | -20 | --- | 20 | mV |
| | | $\|I_{VTT}\|$<1.5A | -30 | --- | 30 | |
| | | $\|I_{VTT}\|$<3A | -40 | --- | 40 | |
| VTT Source Current limit | $I_{VTTOCLSRC}$ | VTT=VDDQSNS/2 *0.95, PGOOD=Hi | 3 | 4 | 6 | A |
| | | VTT=0 | 1.5 | 2 | 6 | |
| VTT Sink Current limit | $I_{VTTOCLSNK}$ | VTT=VDDQSNS/2 *1.05, PGOOD=Hi | 3 | 4 | 6 | A |
| | | VTT=$V_{VDDQSNS}$ | 1.5 | 2 | 6 | |
| VTT leakage current in S3 mode | $I_{VTTLK}$ | S3=0V, S5=5V | --- | 0.01 | --- | µA |
| VTT Discharge Current | $I_{DISCHARGE}$ | S5=0V, VDDQSNS=0, VTT=0.5V | 10 | 20 | --- | mA |
| VTTREF output voltage | $V_{TTREF}$ | DDR 3L | --- | 0.675 | --- | V |
| VTTREF Voltage Load Regulation | $\Delta V_{TTREF}$ | \|IVTTREF\|<10mA | -20 | --- | 20 | mV |
| High Level Input Voltage | $V_{IH}$ | S3 and S5 pin | 1.6 | --- | --- | V |
| Low Level Input Voltage | $V_{IL}$ | S3 and S5 pin | --- | --- | 1 | V |
| Logic input leakage current | $I_{ILEAK}$ | S3 and S5 pin | -1 | --- | 1 | µA |
| Thermal Shutdown | $T_{SD}$ | | --- | 160 | --- | °C |
| Thermal Shutdown Hystersis | | | --- | 20 | --- | °C |

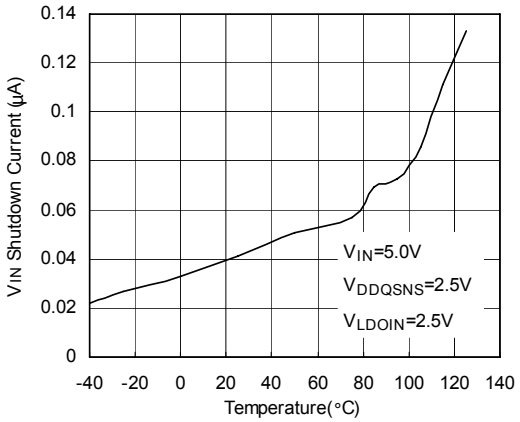
## Typical Performance Characteristics

**$C_{VLDOIN}$=10µF/MLCC/X5R, $C_{VIN}$=1µF/MLCC/X5R, $C_{VTTREF}$ =0.1µF,$C_{VTT}$=20µF/X5R/MLCC unless otherwise noted.**

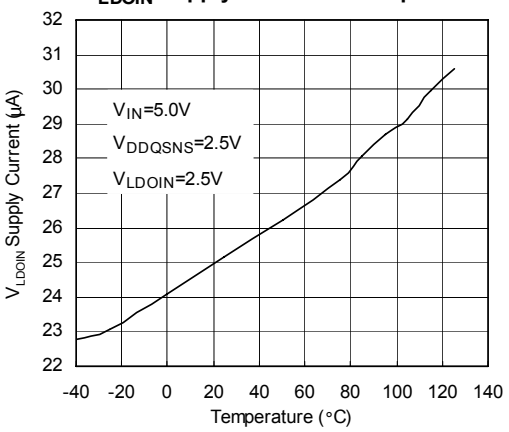
**$V_{IN}$ Supply Current vs Temperature**



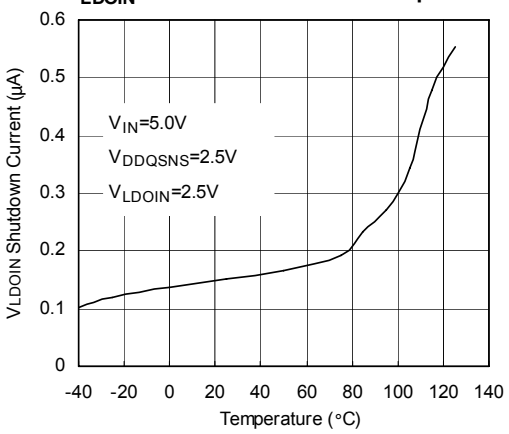

**$V_{IN}$ Shutdown Current vs Temperature**



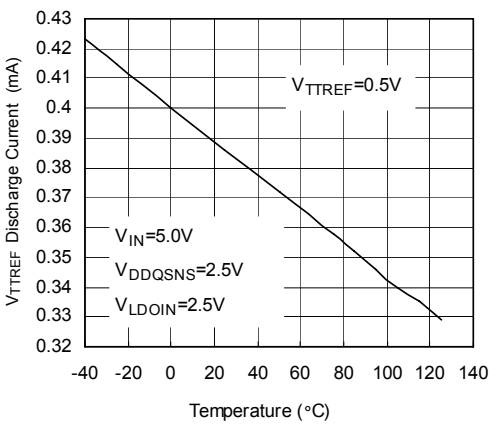

**$V_{LDOIN}$ Supply Current vs Temperature**



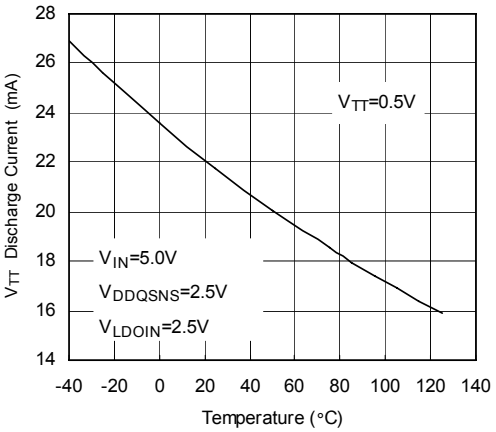

**$V_{LDOIN}$ Shutdown Current vs Temperature**




**$V_{TTREF}$ Discharge Current vs Temperature**

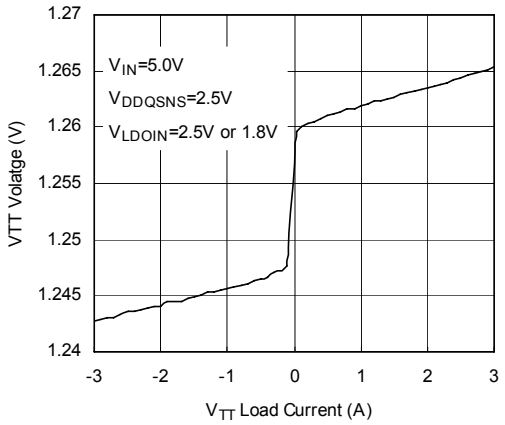



**$V_{TT}$ Discharge Current vs Temperature**

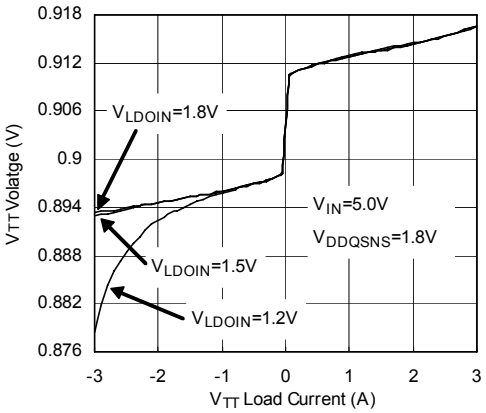


## Typical Performance Characteristics (continued)

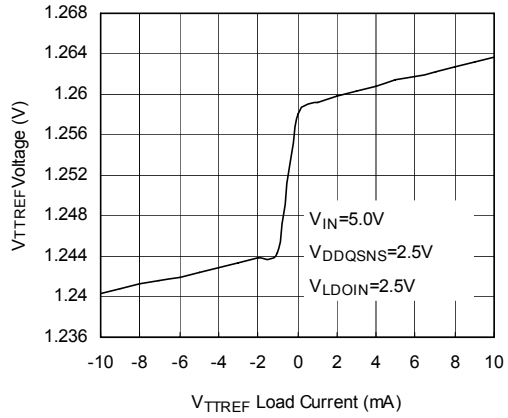
**$V_{TT}$ Voltage Regulation vs $V_{TT}$ Load Current (DDR I )**



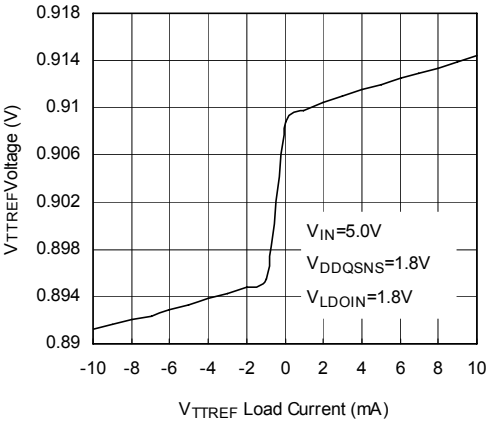

**$V_{TT}$ Voltage Regulation vs $V_{TT}$ Load Current (DDR II )**



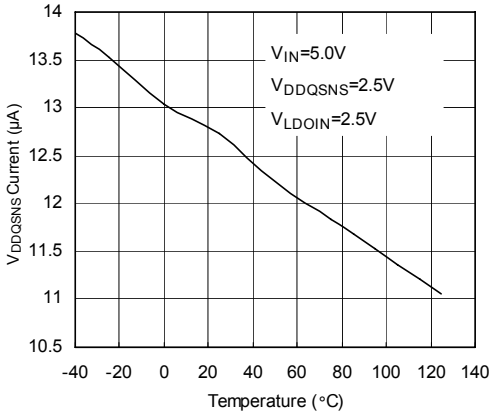

**$V_{TTREF}$ Voltage Load Regulation vs $V_{TTREF}$ Load Current (DDR I)**



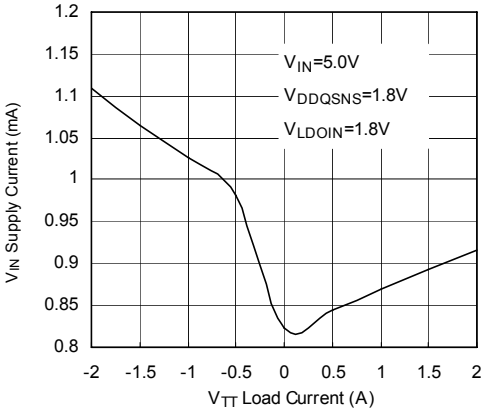

**$V_{TTREF}$ Voltage Load Regulation vs $V_{TTREF}$ Load Current (DDR II )**




**$V_{DDQSNS}$ Current vs Temperature**

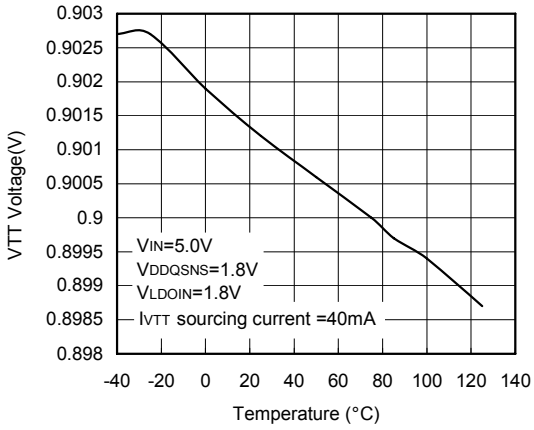



**$V_{IN}$ Supply Current vs $V_{TT}$ Load Current**

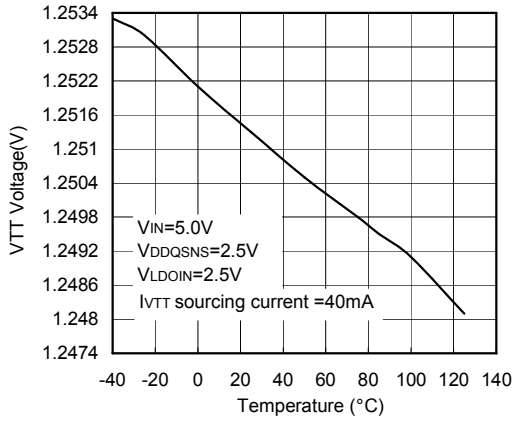


## Typical Performance Characteristics (continued)

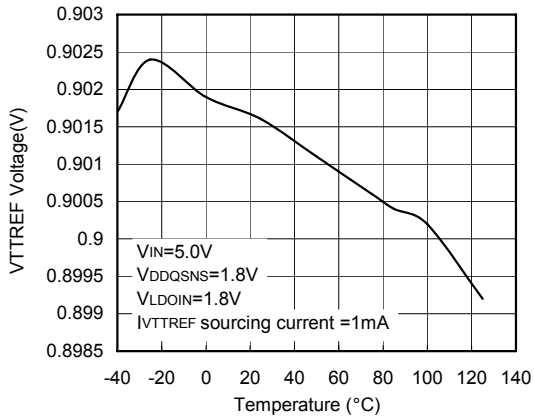
**$V_{TT}$ Voltage vs Temperature**



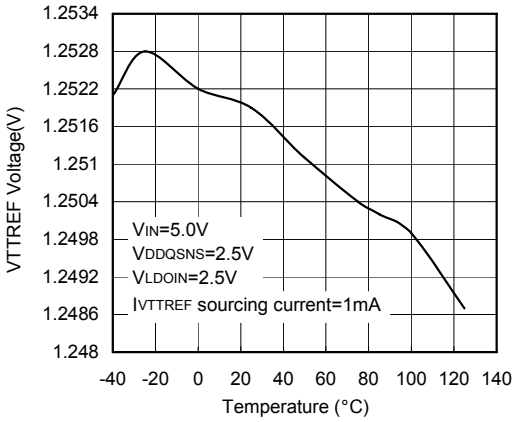

**$V_{TT}$ Voltage vs Temperature**




**$V_{TTREF}$ Voltage vs Temperature**

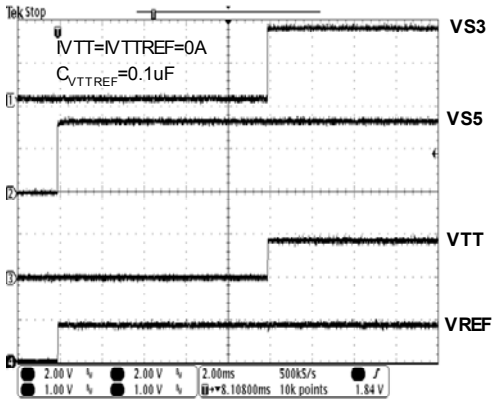



**$V_{TTREF}$ Voltage vs Temperature**

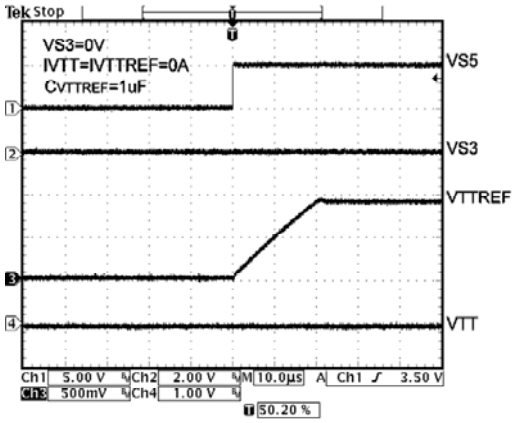


## Typical Performance Characteristics (continued)

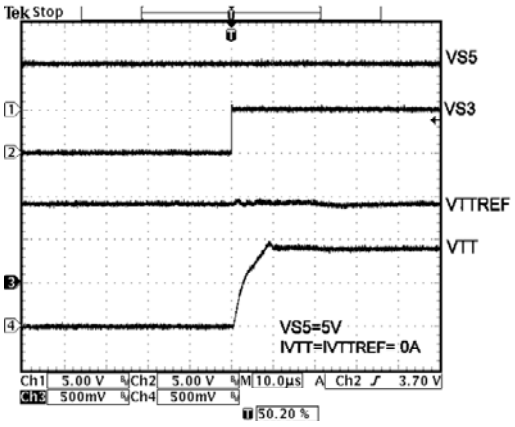
**Start Up Waveforms S5 Low to High**



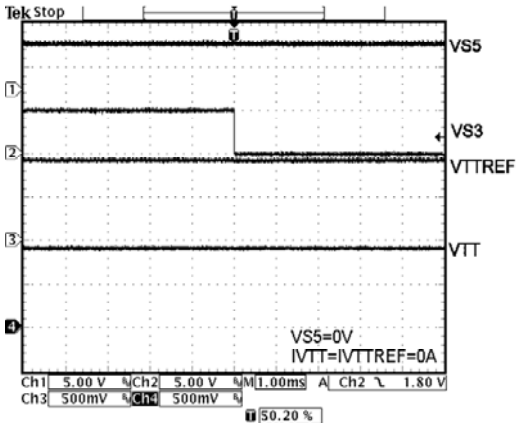

**Start Up Waveforms S5 Low to High**



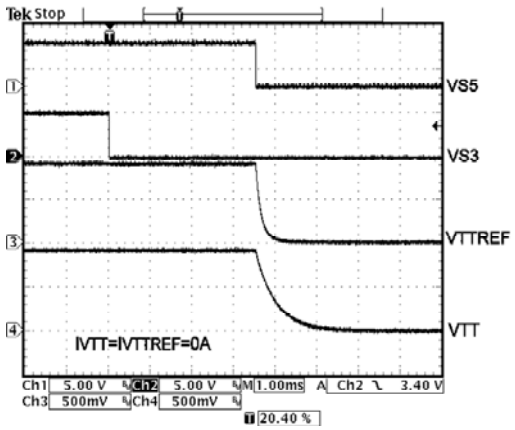

**Start Up Waveforms S3 Low to High**



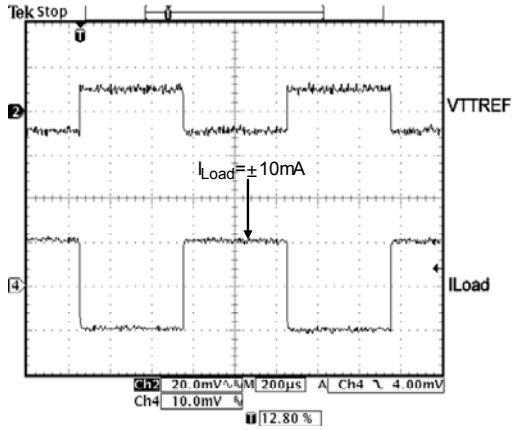

**Shutdown Waveforms S3 High to Low**




**Shutdown Waveforms S3 and S5 High to Low**

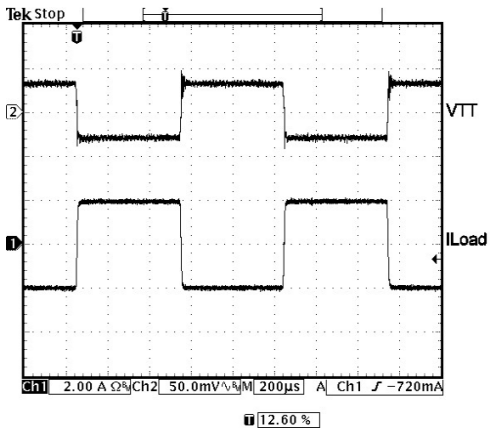



**$V_{TTREF}$ Voltage Transient Response**



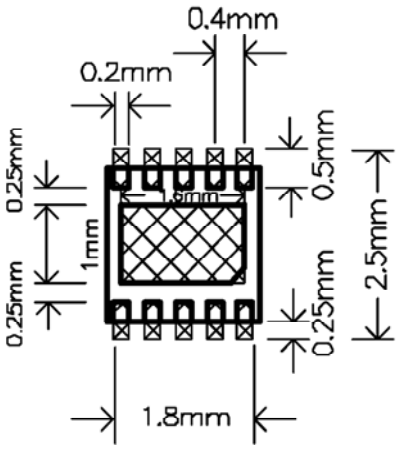
## Typical Performance Characteristics (continued)

**$V_{TT}$ Voltage Load Transient Response**

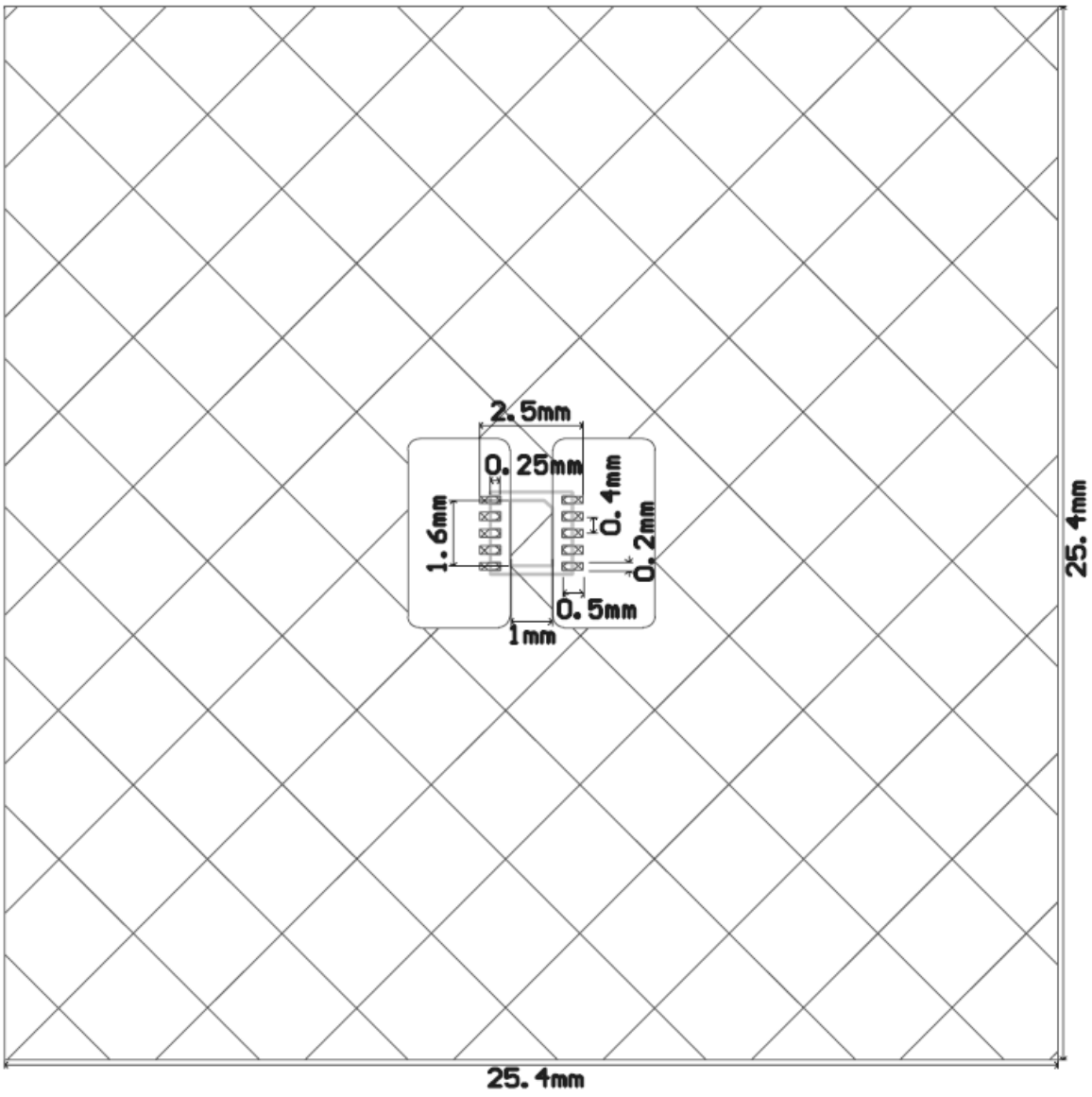



## Minimum Footprint PCB Layout Section

**TDFN2X2-10**



## 1in$^2$ of 1oz PCB Layout Section



## PCB Layout Guidelines.

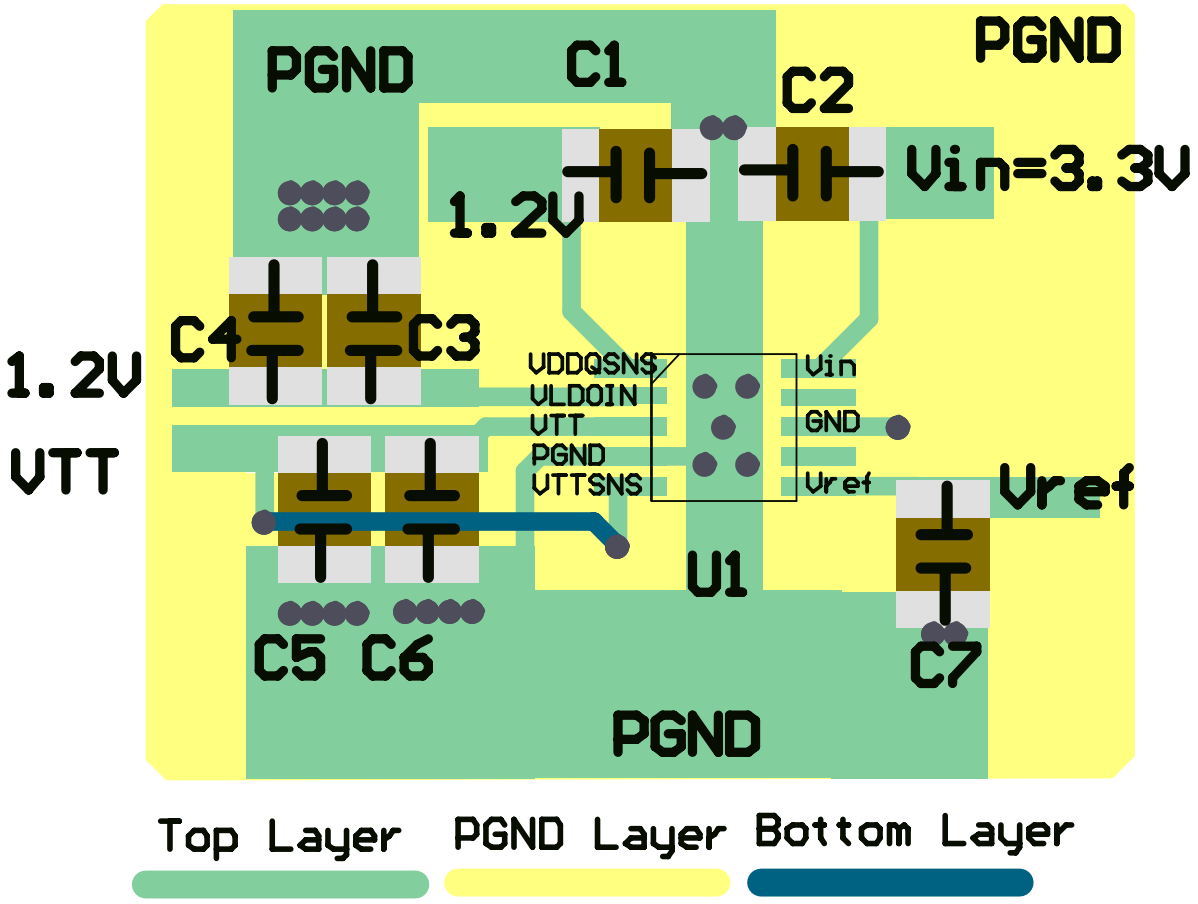
Place the input capacitors as close to VDLOIN pin as possible with short and wide connection.

Place the output capacitor as close to VTT pin as possible with short and wide connection.

Connect the VTTSNS pin to the positive node of output capacitors as a separate trace. In DDR VTT application, connect the VTT sense trace to DIMM side to ensure the VTT voltage at DIMM side is well regulated.

VTTSNS should be connected to the positive node of VTT output capacitor(s) as a separate trace from the high current power line and is strongly recommended to avoid additional ESR and/or ESL. If it is needed to sense the voltage of the point of the load, it is recommended to attach the output capacitor(s) at that point.

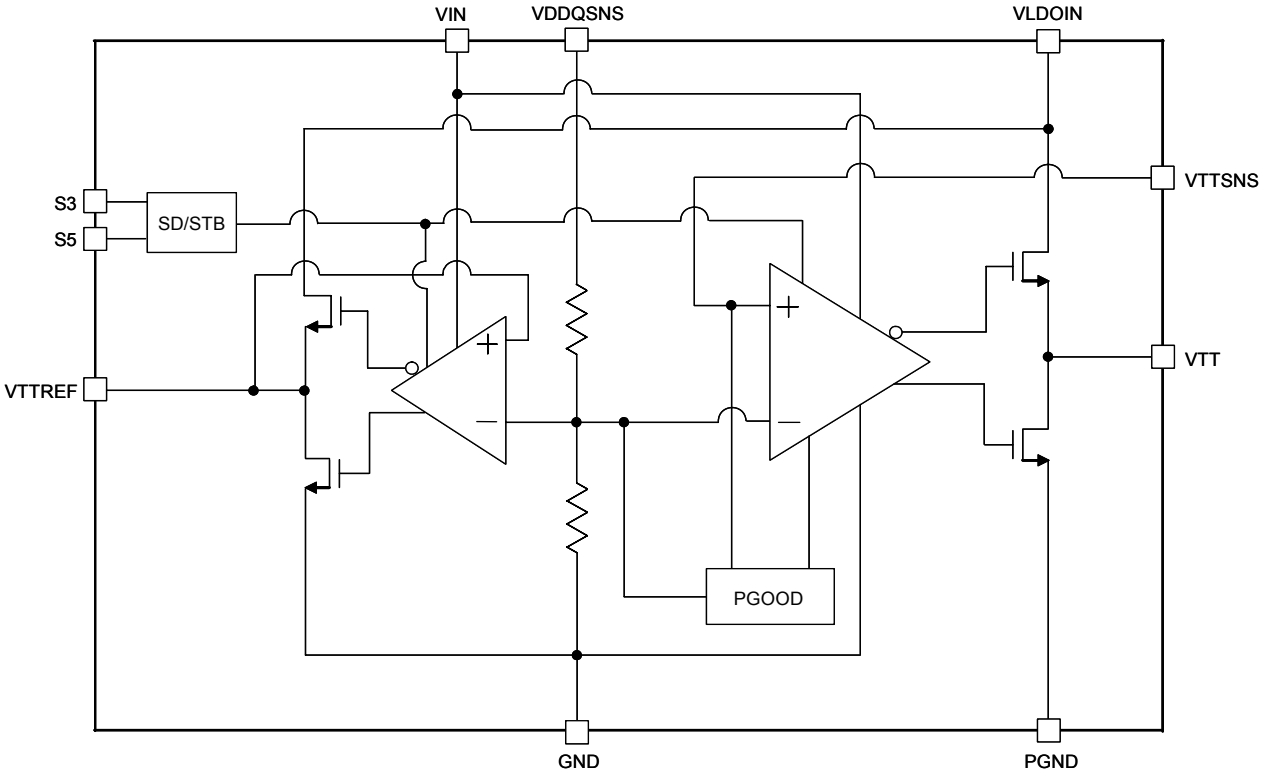
VDDQSNS can be connected separately from VLDOIN. Remember that this sensing potential is the reference voltage of VTTREF. Avoid any noise generative lines.



## Pin Description

| PIN | NAME | DESCRIPTIONS |
|---|---|---|
| 1 | VDDQSNS | VDDQ sense input |
| 2 | VLDOIN | Power supply for the VTT and VTTREF output stage |
| 3 | VTT | Output voltage for connection to termination resistors, equal to VDDQSNS/2 |
| 4 | PGND | Power ground output for the VTT output |
| 5 | VTTSNS | Voltage sense input for the VTT LDO. Connect to plus terminal of the output capacitor |
| 6 | VTTREF | Buffered output that is a reference output ,equal to VDDQSNS/2 |
| 7 | S3 | Active low suspend to RAM mode control pin, VTT is turned off and left Hi-Z |
| 8 | GND | Ground |
| 9 | S5 | Active low shutdown control pin, both VTT and VTTREF are turned off and discharged to ground |
| 10 | VIN | Analog input pin |
| Thermal Pad | | Recommend connecting the Thermal Pad to the GND for excellent power dissipation. |

## Block Diagram



## Description

### VTT SINK/SOURCE REGULATOR

The G2986 is a 3A sink/source tracking termination regulator designed specially for low-cost, low external components system where space is at premium such as notebook PC applications. The G2986 integrates high performance low-dropout linear regulator that is capable of sourcing and sinking current up to 3 A. This VTT linear regulator is implemented with ultimately fast response feedback loop so that small ceramic capacitors are enough to keep tracking to the VTTREF within 40mV at all conditions including fast load transient. To achieve tight regulation with minimum effect of trace resistance, a remote sensing terminal, VTTSNS, should be connected to the positive node of VTT output capacitor as a separate trace from the high current line from VTT.

### VTTREF REGULATOR

The VTTREF block consists of an on-chip 1/2 divider, LPF and buffer. This regulator can source/sink current up to 10mA. Bypass VTTREF to GND using a 0.1µF ceramic capacitor to ensure stable operation. To ensure better start-up and transient performance, the larger 1µF ceramic capacitors are recommended.

### Power on sequence

To operate safely, the G2986 must keep VIN voltage larger than other Input-PIN voltage .This condition is due to the internal parasitic diodes between VIN to others PIN for ESD issue. If the $V_{IN}$ voltage is lower than the other pins voltage, the G2986 will consume extra current through the parasitic diodes during the power-on period.

### Soft-Start

The soft-start function of the VTT is achieved via a current clamp, allowing the output capacitors to be charged with low and constant current that gives linear ramp up of the output voltage. The current limit threshold is changed in two stages using an internal powergood signal. When VTT is outside the powergood threshold, the current limit level is 2A. When VTT rises above (VTTREF - 5%) or falls below (VTTREF + 5%) the current limit level switches to 4 A. The thresholds are typically VTTREF 5% (from outside regulation to inside) and 10% (when it falls outside). The soft-start function is completely symmetrical and it works not only from GND to VTTREF voltage, but also from VDDQSNS to VTTREF voltage. Note that the VTT output is in a high impedance state during the S3 state (S3 = low, S5 = high) and its voltage can be up to VDDQSNS voltage depending on the external condition. Note that VTT does not start under a full load condition.

### S3, S5 Control and Soft-Off

The S3 and S5 terminals should be connected to SLP_S3 and SLP_S5 signals respectively. Both VTTREF and VTT are turned on at normal state (S3 = high, S5 = high). VTTREF is kept alive while VTT is turned off and left high impedance in standby state (S3 = low, S5 = high). Both VTT and VTTREF outputs are turned off and discharged to the ground through internal MOSFETs during shutdown state (S5 = low). The control function is showed on the Table 1.

**Table 1. S3 and S5 Control Table**

| STATE | S3 | S5 | VTT | VREF |
|---|---|---|---|---|
| **Normal** | Hi | Hi | 1.25V/0.9V | 1.25V/0.9V |
| **Standby** | Lo | Hi | 12mV/6mV (High-Z) | 1.25V/0.9V |
| **Shutdown** | Lo | Lo | 0V (Discharge) | 0V (Discharge) |
| **Shutdown** | Hi | Lo | 0V (Discharge) | 0V (Discharge) |

### VTT Current Protection

The LDO has a constant overcurrent limit (OCL) at 4A. This trip point is reduced to 2A before the outputvoltage comes within 5% of the target voltage or goes outside of 10% of the target voltage.

### Input Capacitor

Adding a capacitance close to VLDOIN pin can improve the VTT performance when fast load- transient. In general, 1/2 COUT is recommended for the VLDOIN capacitance. Separating the VDDQSNS and VLDOIN pins will get better transient performance. The recommended capacitor types are tabulated in the Table 2.

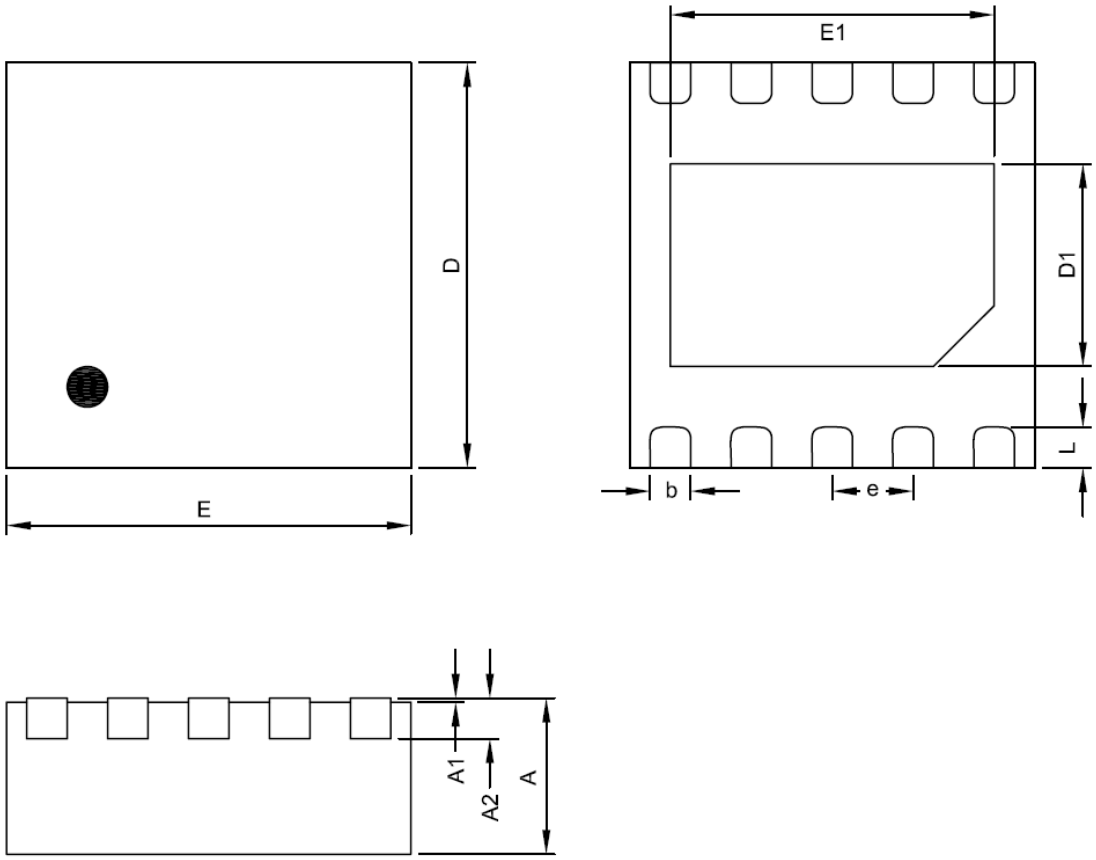
### Output Capacitor

For stable operation, total capacitance of the VTT output terminal can be equal or greater than 20µF. The output capacitor should be located near VTT output terminal as close as possible to minimize the effect of ESR and ESL. The recommended capacitor types are tabulated in the Table 2.

**Table 2.**

| CAP | MANUF | PART NUMBER |
|---|---|---|
| **C1** | TAYO YUDEN | EMK 325BJ106KD |
| **C2** | TAYO YUDEN | UMK 212BJ104KG |

## Package Information

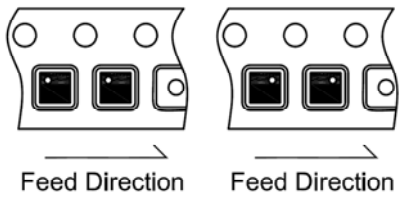



**TDFN2X2-10 Package**

| Symbol | DIMENSION IN MM | | | DIMENSION IN INCH | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 0.70 | 0.75 | 0.80 | 0.0276 | 0.0295 | 0.0315 |
| A1 | 0.00 | - - - | 0.05 | 0.0000 | - - - | 0.0020 |
| A2 | 0.20 REF | | | 0.0079 REF | | |
| D | 1.95 | 2.00 | 2.05 | 0.0768 | 0.0787 | 0.0807 |
| E | 1.95 | 2.00 | 2.05 | 0.0768 | 0.0787 | 0.0807 |
| D1 | 0.95 | 1.00 | 1.05 | 0.0374 | 0.0394 | 0.0413 |
| E1 | 1.55 | 1.60 | 1.65 | 0.0610 | 0.0630 | 0.0650 |
| b | 0.15 | 0.20 | 0.25 | 0.0059 | 0.0079 | 0.0098 |
| e | 0.40 BSC | | | 0.0157 BSC | | |
| L | 0.20 | 0.25 | 0.30 | 0.0079 | 0.0098 | 0.0118 |

## Taping Specification

**G2986K21U** **G2986K21D**




| PACKAGE | Q'TY/REEL |
|---|---|
| TDFN2X2-10 | 3,000 ea |