G2998/G2999

DDR Termination Regulator

Features

- **Support and DDR I (1.25VTT), DDR II (0.9 VTT) , DDR III (0.75 VTT) , and DDR IIIL (0.675VTT) Requirements**
- **Input Voltage Range: 3V to 5.5V**
- **VTT_IN Voltage Range: 1.2V to 3.6V**
- **Requires Only 20µF Ceramic Output Capacitance**
- **VTT Pulled Low by 2kΩ Resistor in Stand-By Mode (G2998 version)**
- **VTT Tri-State in Stand-By Mode (G2999 version)**
- **Integrated Divider Tracks 1/2 VDDQ for Both VTT and VREF**
- **Remote Sensing (VTTS)**
- **±20mV Accuracy for VTT**
- **±30mV Accuracy for VREF**
- **Built-In Soft-Start**
- **Over Current Protection**
- **Thermal Shutdown Protection**
- **MSOP-8 and SOP-8(Thermal Pad) Package**

Applications

- **DDR I/II/III/IIIL Memory Termination**
- **SSTL−2, SSTL−18**
- **HSTL Termination**

General Description

The G2998/G2999 is a 3A sink/source tracking termination regulator. It is specifically designed for low-cost/ low-external component count systems. The G2998/ G2999 maintains a high speed operational amplifier that provides fast load transient response and only requires 20µF (2 × 10µF) of ceramic output capacitance. The G2998/G2999 supports remote sensing functions and all features required to power the DDR I / DDR II / DDR III / DDR IIIL VTT bus termination according to the JEDEC specification. In addition, the G2998/ G2999 also has an Enable (EN) pin that provides Suspend to RAM (STR) functionality. When EN is pulled low, VREF will remain active, but VTT output will be turned off and discharged to the ground through internal MOSFETs in G2998 version and VTT output will be in tri-state in G2999 version. A power saving advantage can be obtained in this mode through lowering the quiescent current to150µA @ VCC=3.3V.

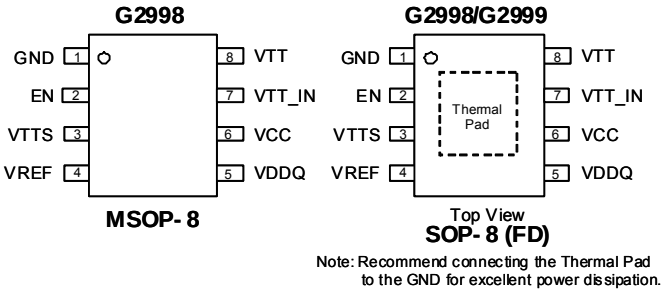
The G2998/G2999 is available in the MSOP-8 and SOP-8 package with the Thermal pad.

Ordering Information

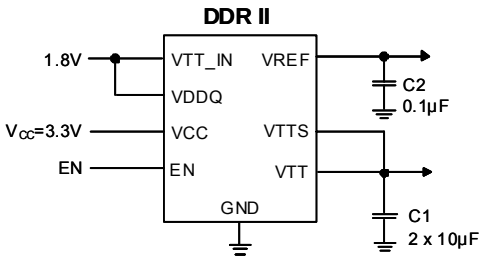
ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE (Green)	REMARK
G2998P81U	G2998	-40°C~85°C	MSOP-8	**OBSOLETE**
G2998F11U	G2998	-40°C~85°C	SOP-8 (FD)	
G2999F11U	G2999	-40°C~85°C	SOP-8 (FD)	

Note: P8: MSOP-8 F1: SOP-8 (FD)
1: Bonding Code
U: Tape & Reel
Green : Lead Free / Halogen Free

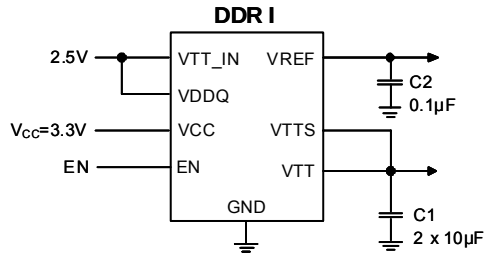
Pin Configuration

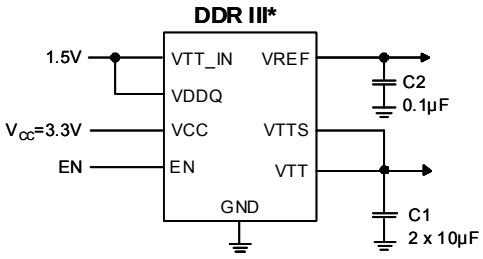


Note: Recommend connecting the Thermal Pad to the GND for excellent power dissipation.



Typical Application Circuit





* Recommended V_{CC} =3.3V

Absolute Maximum Ratings (1)

Supply Voltage Range
VCC, VTT_IN, VTTS, VDDQ, EN . . . . . .-0.3V to +6V
Output Voltage Range
VTT, VREF. . . . . -0.3V to VTT_IN +0.3V
Maximum Junction Temperature,T_J . . . . . 160°C
Storage Temperature Range, T_{STG}. . -55°C to +160°C
Reflow Temperature (soldering, 10sec) . . . . . 260°C
Thermal Resistance Junction to Ambient, (θ_{JA})
MSOP-8 . . . . . 190°C/W(4)
SOP-8 (FD) . . . . . 50°C/W(5)
Continuous Power Dissipation (T_A = +25°C)
MSOP-8 . . . . . 0.7W(4)
SOP-8 (FD) . . . . . 2.7W(5)
Thermal Resistance Junction to Ambient, (θ_{JC})
MSOP-8 . . . . . 55°C/W
SOP-8 (FD) . . . . . .12°C/W

Recommend Operating Range (1) (2)
VCC . . . . . 3V to 5.5V
EN . . . . . -0.1V to 5.5V
VDDQ. . . . . 1.3V to 3.6V
VTT_IN . . . . . .1.2V to 3.6V(3)

Operating Ambient Temperature Range
T_A . . . . . -40°C to 85°C

Note:
(1) All voltage values are with respect to the network ground terminal unless otherwise noted.
(2) VTT_IN, VDDQ must be lower than VCC on operation.
(3) VTT, VREF must be lower than VTT_IN on operation.
(4) Please refer to "Minimum Footprint PCB Layout Section".
(5) Please refer to PCB size described in EV2998-10.

Electrical Characteristics

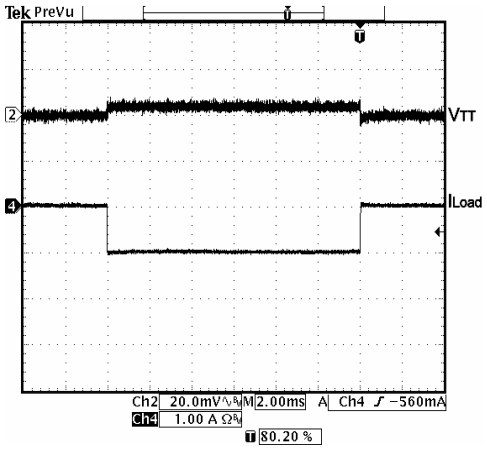
Specifications with standard typeface are for T_A=25°C, V_{CC}=3.3V, VTT_IN=1.8V and VDDQ=1.8V. Unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage (DDR I/ DDR II)	Vcc		3	---	5.5	V
Supply Voltage (DDR III/ DDR IIIL)			---	3.3	---	
Supply Current, VCC	I_{CC}	V_{CC}=3.3V, no load, V_{EN}=3.3V	0.5	0.9	4	mA
Standby Current, VCC	I_{CC}	V_{CC}=3.3V, no load, V_{EN}=0V	---	150	500	μA
VDDQ Input Impedance	Z_{VDDQ}	V_{CC}=3.3V, V_{EN}=3.3V	70	100	130	kΩ
VTTS Input Current	I_{VTTS}	V_{CC}=3.3V, no load, V_{EN}=3.3V	---	0.3	2	μA
VTT Output Voltage (DDR I)	VTT		---	1.25	---	V
VTT Output Voltage (DDR II)			---	0.9	---	
VTT Output Voltage (DDR III)			---	0.75	---	
VTT Output Voltage (DDR IIIL)			---	0.675	---	
VTT Output Voltage Load Regulation (V_{REF}-VTT)	V_{OS}VTT	I_{VTT}=0	-20	---	20	mV
		$\|I_{VTT}\|$<1.5A	-30	---	30	
		$\|I_{VTT}\|$<3A	-40	---	40	
VTT Source Current Limit	$I_{VTTOCLSRC}$	VTT=VDDQ/2 *0.95, PGOOD=Hi	3	4	---	A
		VTT=0	1.5	2	---	
VTT Sink Current Limit	$I_{VTTOCLSNK}$	VTT=VDDQ/2 *1.05, PGOOD=Hi	3	4	---	A
		VTT=VDDQ	1.5	2	---	
Line Regulation		V_{CC}=3.3V to 5.5V, I_{VTT}=1A to GND	---	1	20	mV
VTT Standby Discharge Resistance (G2998)		No load, V_{EN}=0V	0.5	2	8	kΩ
VTT Standby Discharge Resistance (G2999, VTT is in Hi-Z state)		No load, V_{EN}=0V	1000	---	---	kΩ
V_{REF} Output Voltage (DDR I)	V_{REF}		---	1.25	---	V
V_{REF} Output Voltage (DDR II)			---	0.9	---	
V_{REF} Output Voltage (DDR III)			---	0.75	---	
V_{REF} Output Voltage (DDR IIIL)			---	0.675	---	
V_{REF} Voltage Load Regulation	ΔV_{REF}	$\|I_{VREF}\|$<10mA	-30	---	30	mV
High Level Enable Input Voltage	V_{IH}	V_{CC}=3.3V	1.6	---	---	V
Low Level Enable Input Voltage	V_{IL}	V_{CC}=3.3V	---	---	0.8	V
Enable Pin Input Leakage Current	I_{EN}	V_{EN}=3V	-2	---	2	μA
UVLO Threshold Voltage	V_{UVLO}		2.0	2.32	2.7	V
Hysteresis Voltage			---	120	---	mV
Thermal Shutdown	T_{SD}		---	160	---	°C
Thermal Shutdown Hysteresis			---	20	---	°C

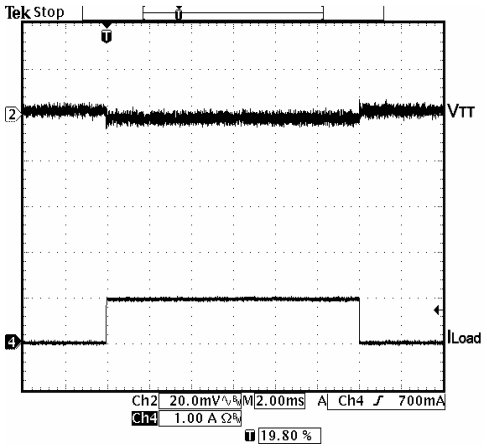
Typical Performances Characteristics

V_{CC}=3.3V, V_{TT_IN}=1.8V, V_{DDQ}=1.8V, V_{EN}=3.3V, C_{Vcc}=1μF, C_{VDDQ}=1μF, C_{VTT_IN}=10μF, C_{VREF} =0.1μF, C_{VTT} =20μF, T_A=25 °C, unless otherwise noted.

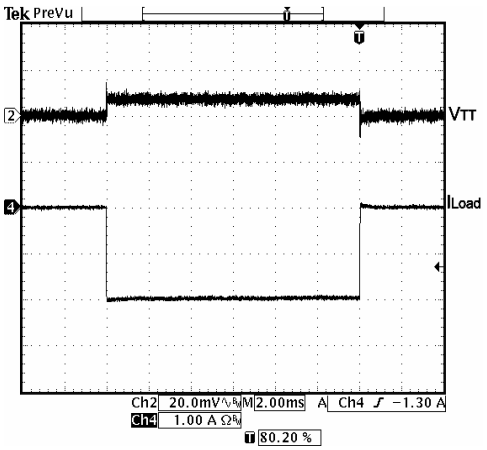
I_{Load}=1.0A Transient (Sinking)



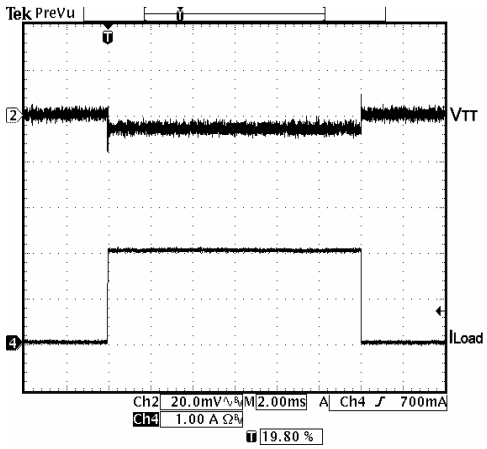
I_{Load}=1.0A Transient (Sourcing)



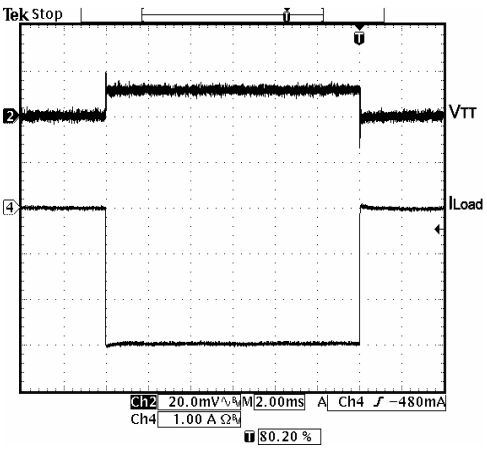
I_{Load}=2.0A Transient (Sinking)



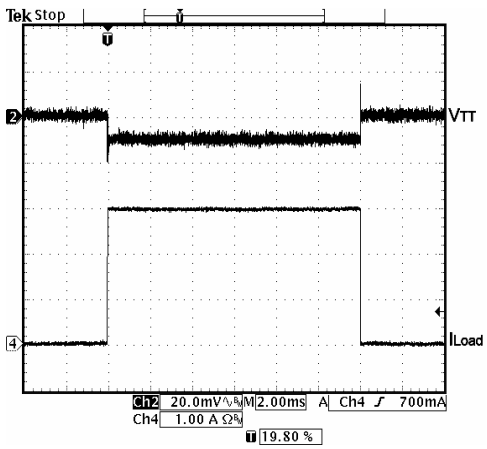
I_{Load}=2.0A Transient (Sourcing)



I_{Load}=3.0A Transient (Sinking)

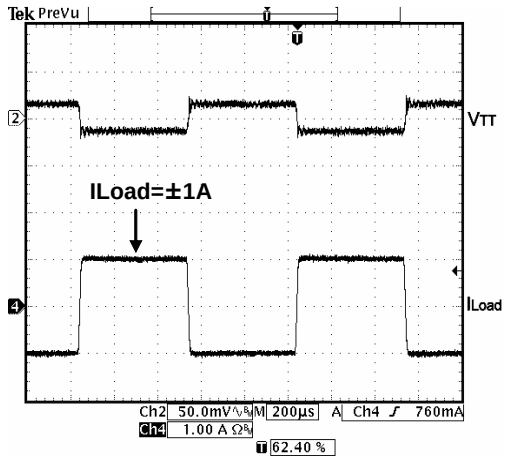


I_{Load}=3.0A Transient (Sourcing)

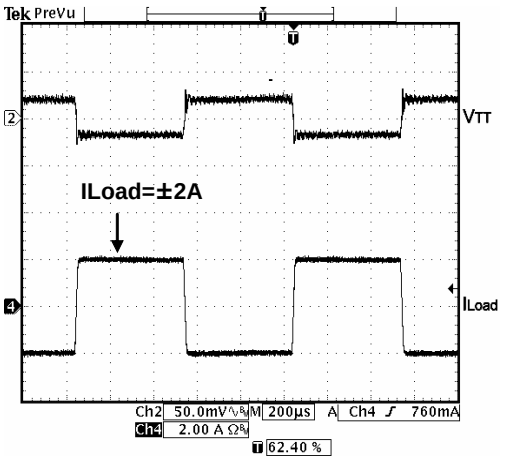


Typical Performances Characteristics (continued)

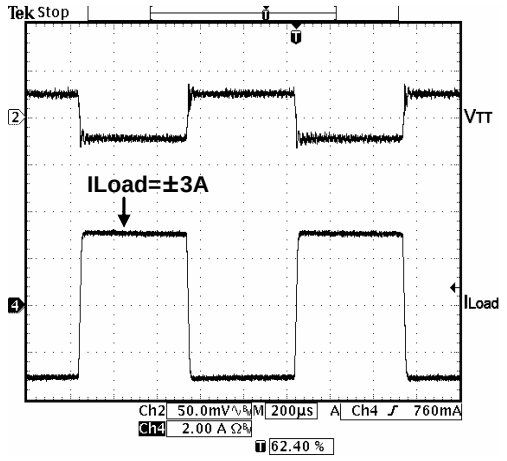
V_{TT} Voltage Transient Response



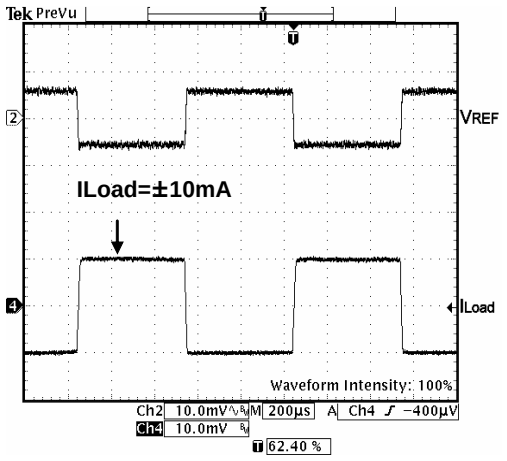
V_{TT} VoltageTransient Response



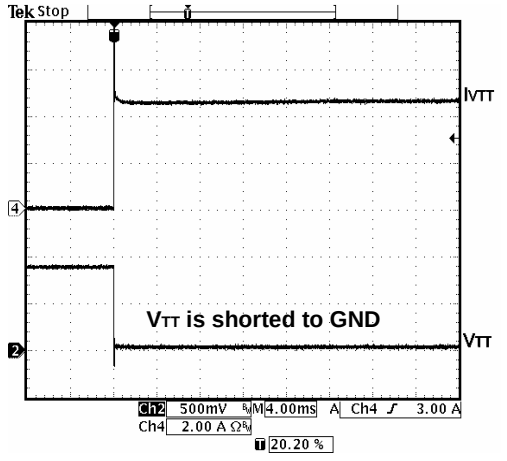
V_{TT} Voltage Transient Response



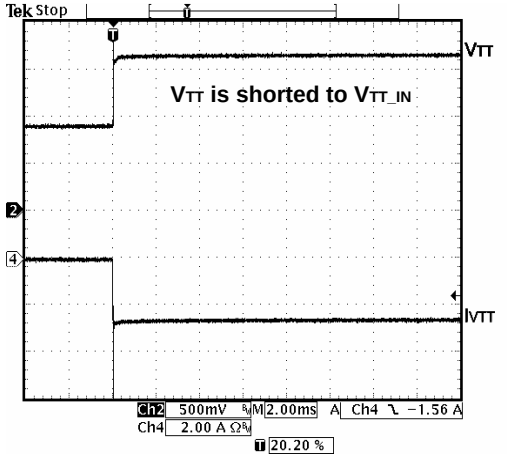
V_{REF} Voltage Transient Response



Output Short-Circuit Protection

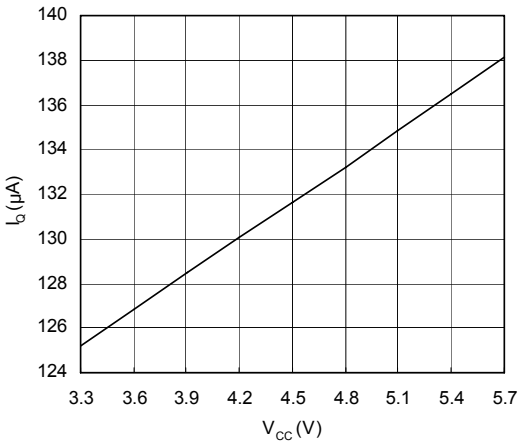


Output Short-Circuit Protection

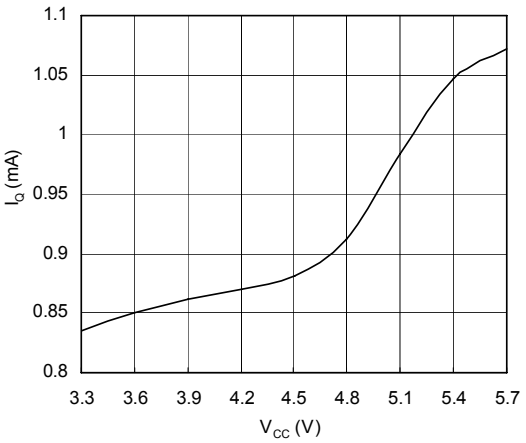


Typical Performances Characteristics (continued)

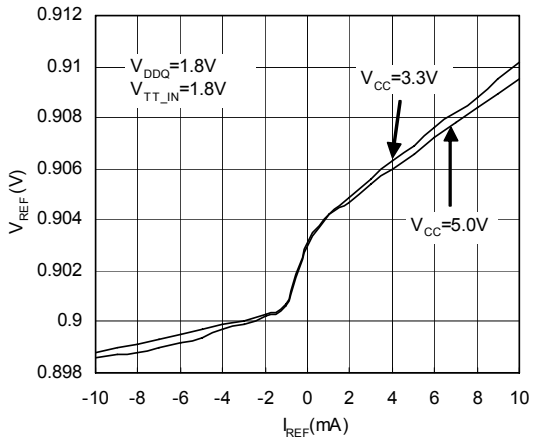
I_Q vs V_{CC} in SD



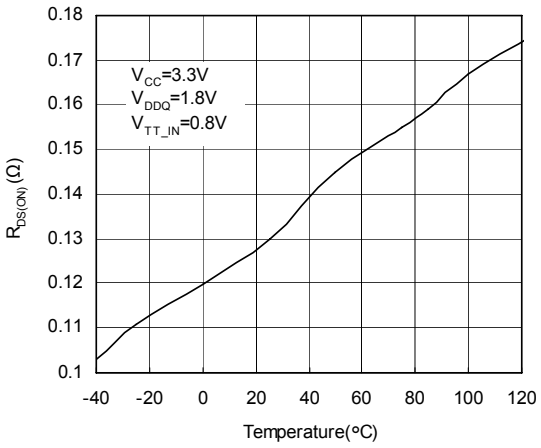
I_Q vs V_{CC}



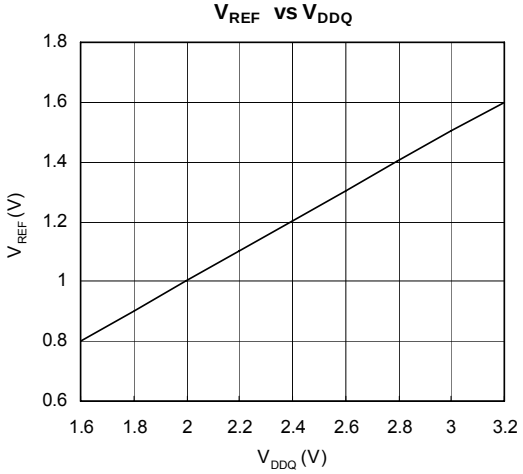
V_{REF} vs I_{REF}



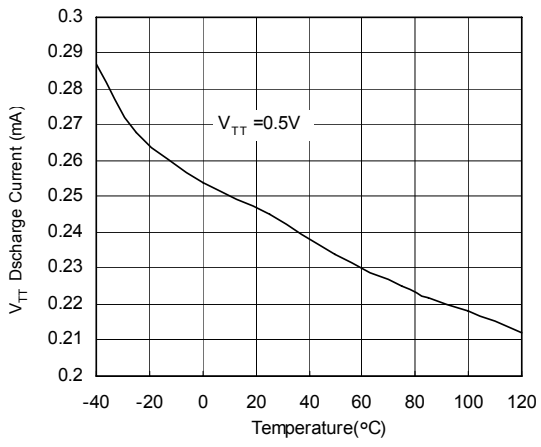
High side $R_{DS(ON)}$ vs Temperature



V_{REF} vs V_{DDQ}

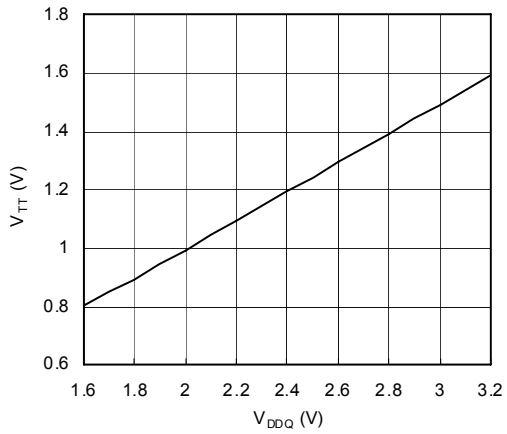


V_{TT} Discharge Current vs Temperature (only in G2998 version)

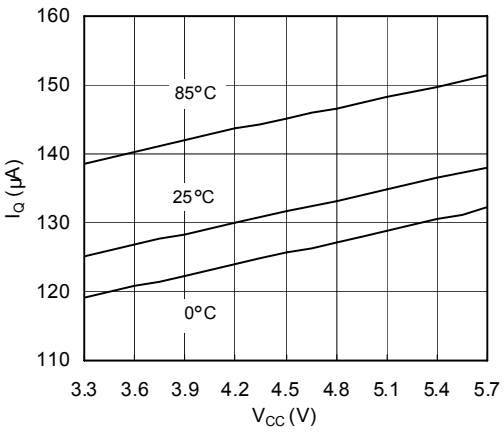


Typical Performances Characteristics (continued)

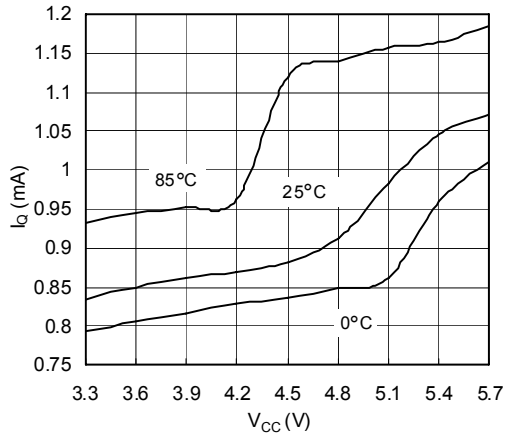
V_{TT} vs V_{DDQ}



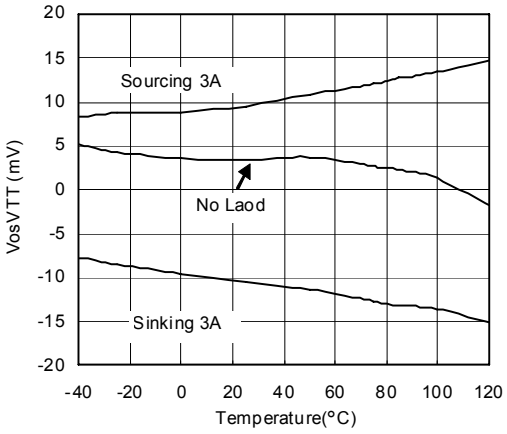
I_Q vs V_{CC} in S_D Temperature



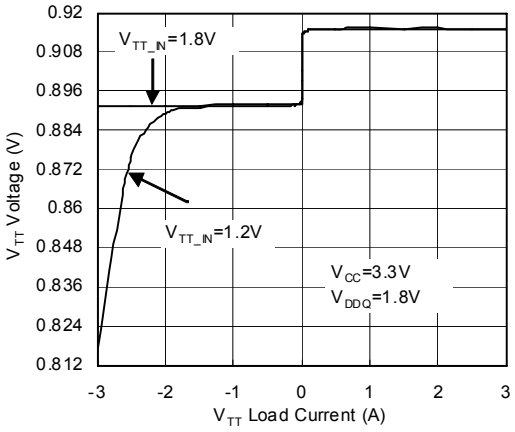
I_Q vs V_{CC} Temperature



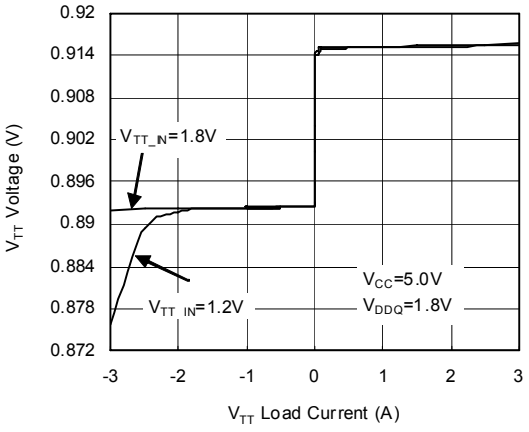
VosVTT vs Temperature



V_{TT} Voltage vs V_{TT} Load Current

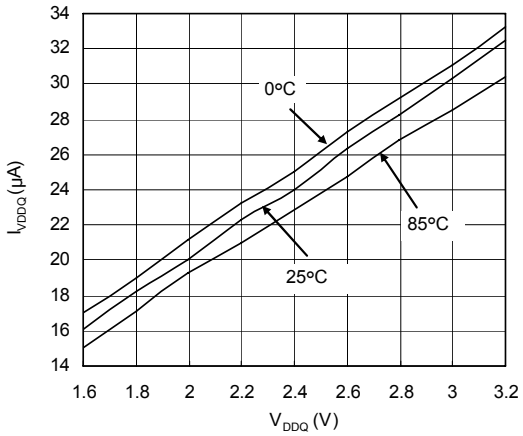


V_{TT} Voltage vs V_{TT} Load Current

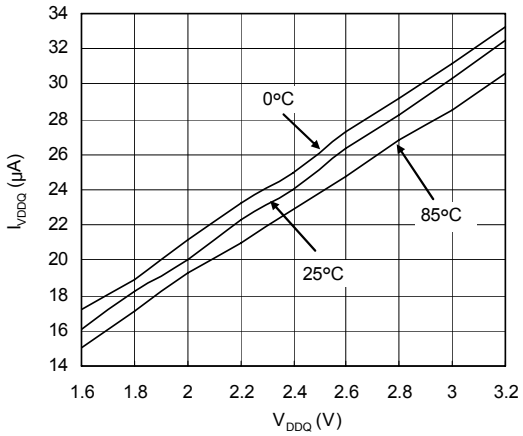


Typical Performances Characteristics (continued)

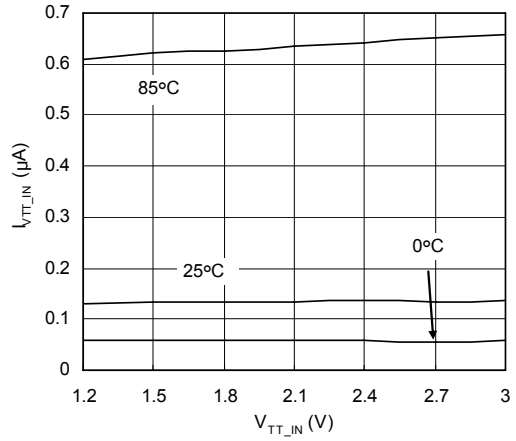
I_{VDDQ} vs V_{DDQ} in SD Temperature



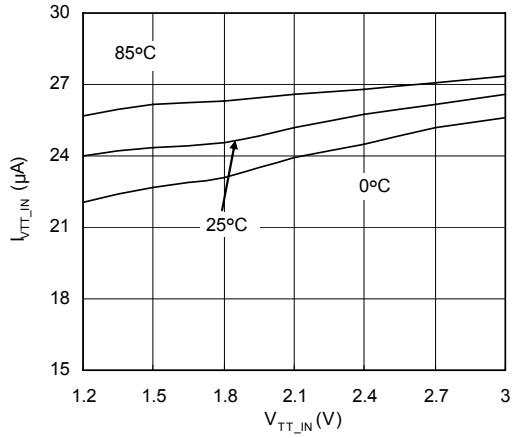
I_{VDDQ} vs V_{DDQ} Temperature



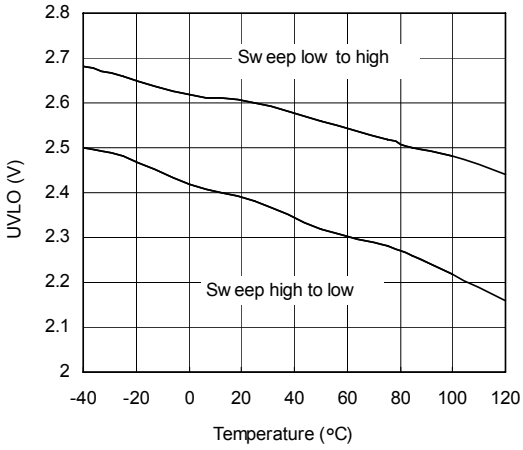
I_{VTT_IN} vs V_{TT_IN} in SD Temperature



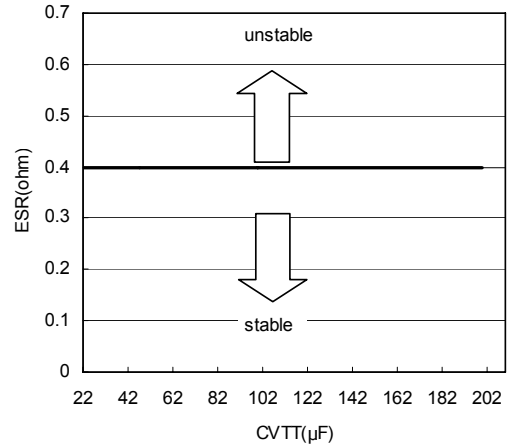
I_{VTT_IN} vs V_{TT_IN} Temperature



UVLO vs Temperature

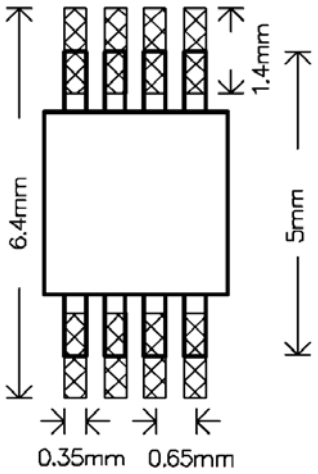


ESR Stable Range vs. C_{VTT}

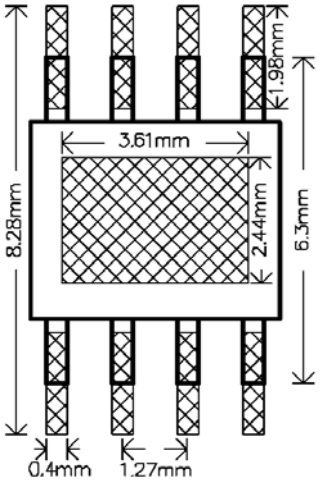


Minimum Footprint PCB Layout Section

MSOP-8



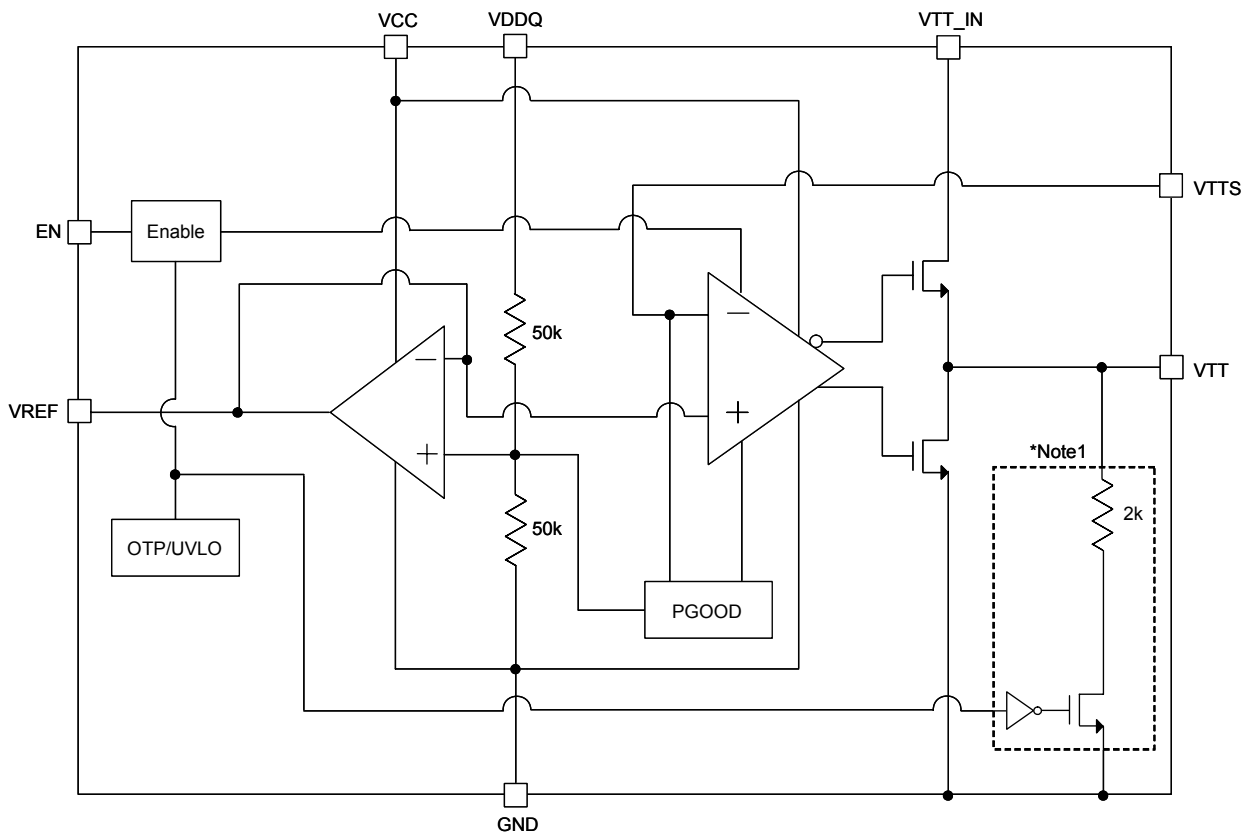
SOP-8 (FD)



Pin Description

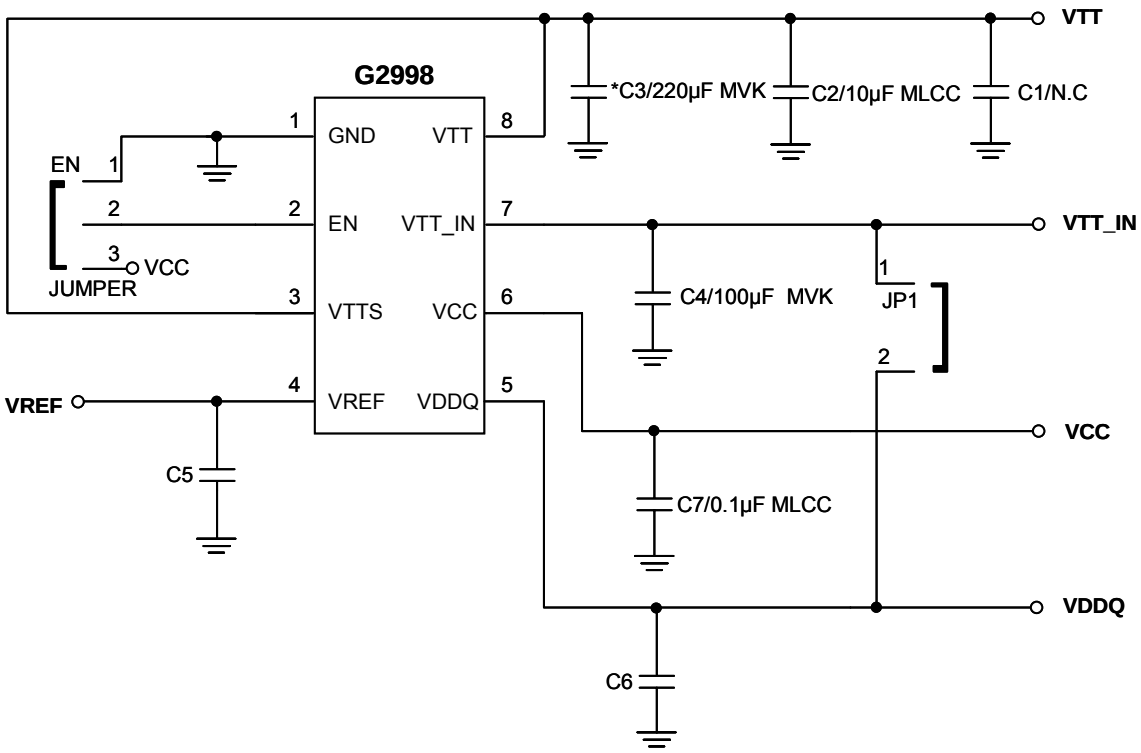
PIN		NAME	FUNCTION
MSOP-8	SOP-8 (FD)		
1	1	GND	Ground
2	2	EN	Active high enable control pin
3	3	VTTS	Feedback pin for regulating VTT
4	4	VREF	Buffered output that is a reference output of VDDQ/2
5	5	VDDQ	Power Input for internal reference
6	6	VCC	Analog input pin
7	7	VTT_IN	Power supply for the VTT output stage
8	8	VTT	Output voltage for connection to termination resistors, equal to VREF
	Thermal Pad		Recommend connecting the Thermal Pad to the GND for excellent power dissipation.

Block Diagram



* Note1: In stand-by mode, VTT will be pulled low by a 2k resistor in G2998 version. But in G2999 version, VTT will be Tri-state in stand-by mode.

Application Circuit



* To use AL-cap (ALUMINUM ELECTROLYTIC CAPACITORS) at VTT, recomment the Low-ESR.
The Size of capacitance (µF) should be optimized "based DDR characteristic",
try to use below value at VREF and VDDQ, for Noise elimination at VREF and VDDQ.
--> **C5=C6=2.2µF MLCC, or More high capacitance**

Description

VTT SINK/SOURCE Regulator

The G2998/G2999 is a 3A sink/source tracking termination regulator designed specially for low-cost, low external components system where space is at premium such as notebook PC applications. The G2998/G2999 integrates high performance low-dropout linear regulator that is capable of sourcing and sinking current up to 3A. This VTT linear regulator is implemented with ultimately fast response feedback loop so that small ceramic capacitors are enough to keep tracking to the VREF within 40mV at all conditions including fast load transient. To achieve tight regulation with minimum effect of trace resistance, a remote sensing terminal, VTTS, should be connected to the positive node of VTT output capacitor as a separate trace from the high current line from VTT.

Series Stub Termination Logic (SSTL) was created to improve signal integrity of the data transmission across the memory bus. This termination scheme is essential to prevent data error from signal reflections while transmitting at high frequencies encountered with DDR-SDRAM. The most common form of termination is Class II single parallel termination. This involves one RS series resistor from the chipset to the memory and one RT termination resistor, both 25Ω typically. The resistors can be changed to scale the current requirements from the G2998/G2999. This implementation can be seen below in Figure 1.

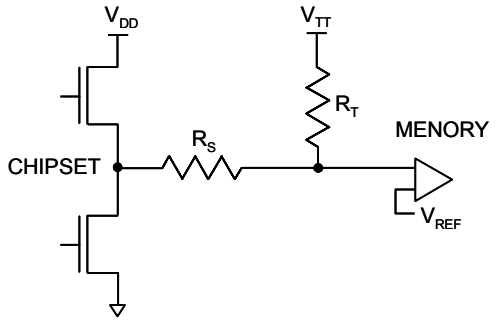


Figure 1. SSTL- Termination Scheme

VDDQ

A voltage divider of two 50kΩ is connected between VDDQ and ground, to create the internal reference voltage (VDDQ/2). This guarantees that VTT will track VDDQ/2 precisely.

VTTS

The VTTS pin is the feedback sensing pin of the operation amplifier which regulates the VTT voltage. In most motherboard applications, the termination resistors will connect VTT in a long plane. If using the remote sensing pin - VTTS to the middle of the bus, the significant long-trace IR drop resulting in a termination voltage which is lower at one end than the other can be avoided. This will provide a better distribution across the entire termination bus. If the remote load regulation is not used, the VTTS pin must still be connected to VTT for correct regulation. Care should be taken when a long VTTS trace is implemented in close proximity to the memory. Noise pickup in the VTTS trace can cause problems with precise regulation of VTT. A small 0.1µF ceramic capacitor placed next to the VTTS pin can help to filter any high frequency signals and preventing errors.

VREF Regulator

The VREF block consists of an on-chip 1/2 divider, LPF and buffer. This regulator can source/sink current up to 10mA. Bypass VREF to GND using a 0.1µF ceramic capacitor to ensure stable operation.

Power on sequence

To operate safely, the G2998/G2999 must keep VCC voltage larger than other Input-pin voltage .This condition is due to the internal parasitic diodes between VCC to other pins for ESD issue. If the VCC voltage is lower than the other pins voltage, the G2998/G2999 will consume extra current through the parasitic diodes during the power-on period.

Soft-Start

The soft-start function of the VTT is achieved via a current clamp, allowing the output capacitors to be charged with low and constant current that gives linear ramp up of the output voltage. The current limit threshold is changed in two stages using an internal powergood signal. When VTT is outside the power-good threshold, the current limit level is 2A. When VTT rises above (VREF - 5%) or falls below (VREF + 5%) the current limit level switches to 4 A. The thresholds are typically VREF ±5% (from outside regulation to inside) and ±10% (when it falls outside). The soft-start function is completely symmetrical and it works not only from GND to VREF voltage, but also from VDDQ to VREF voltage.

Enable Control and UVLO

Both VREF and VTT are turned on at normal state (EN PIN = Hi). In stand-by state (EN PIN = Lo), VREF is kept alive while VTT output will be turned off and discharged to the ground through internal MOSFETs in G2998 version and VTT output will be in tri-state in G2999 version. The UVLO function protects faulty function due to low voltage levels of VCC. VTT starts up when VCC reaches the UVLO threshold level and EN reach the threshold level.

VTT Current Protection

The LDO has a constant overcurrent limit (OCL) at 4A. This trip point is reduced to 2A before the output voltage comes within 5% of the target voltage or goes outside of 10% of the target voltage.

Input Capacitor

Adding a capacitance close to VTT_IN pin can improve the VTT performance when fast load- transient. In general, 1/2 COUT is recommended for the VTT_IN capacitance. Separating the VDDQ and VTT_IN pins will get better transient performance. The recommended capacitor types are tabulated in the Table 1.

Output Capacitor

For stable operation, total capacitance of the VTT output terminal can be equal or greater than 20μF. The output capacitor should be located near VTT output terminal as close as possible to minimize the effect of ESR and ESL. The recommended capacitor types are tabulated in the Table 1.

Table 1.

CAP	MANUF	PART NUMBER
C1	TAYO YUDEN	EMK 325BJ106KD
C2	TAYO YUDEN	UMK 212BJ104KG

Thermal Dissipation

When the current is sinking to or sourcing from VTT, the G2998/G2999 will generate internal power dissipation resulting in the heat. Care should be taken to prevent the device from damages caused by the junction temperature exceeding the maximum rating. The maximum allowable internal temperature rise (T_{RMAX}) can be calculated under the given maximum ambient temperature (T_{AMAX}) of the application and the maximum allowable junction temperature (T_{JMAX}).

$T_{RMAX} = T_{JMAX} - T_{AMAX}$

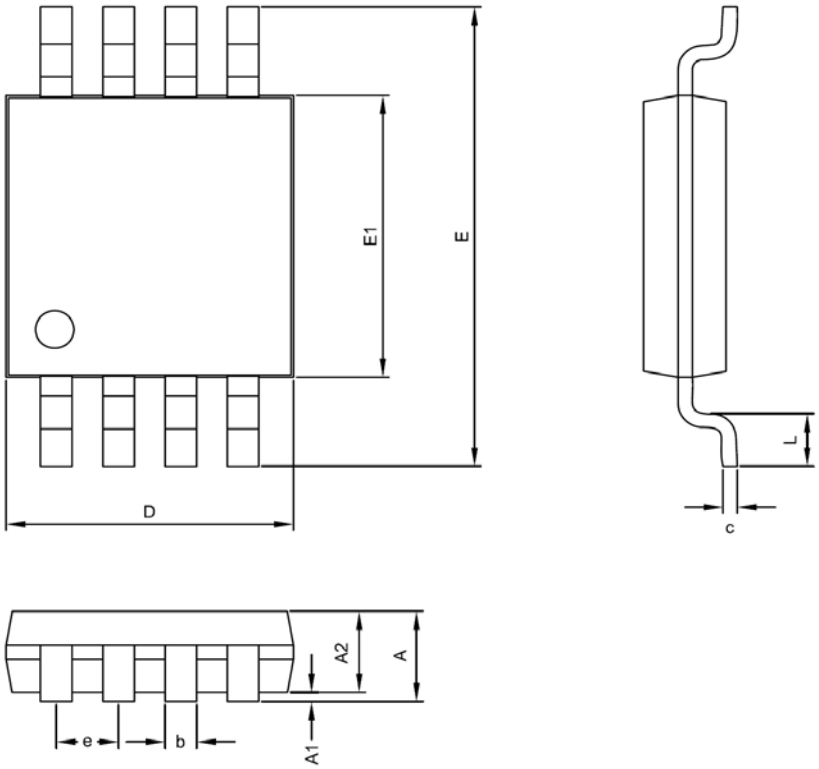
From this equation, the maximum power dissipation (P_{DMAX}) of the G2998/G2999 can be calculated:

$P_{DMAX} = T_{RMAX} / \theta_{JA}$

θ_{JA} of the G2998/G2999 will be dependent on several variables:

The packages used, the thickness and size of the copper, the number of vias and the airflow. In the package, the G2998/G2999 use the SOP-8 with Power-PAD to improve the θ_{JA} . If the layout of the PCB can put a larger size of copper to contact the Power-PAD of this device, the θ_{JA} will be further improved. The better θ_{JA} is not only protecting the device well, but also increasing the maximum current capability at the same ambient temperature.

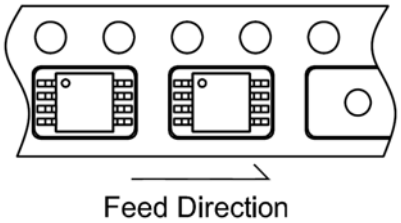
Package Information



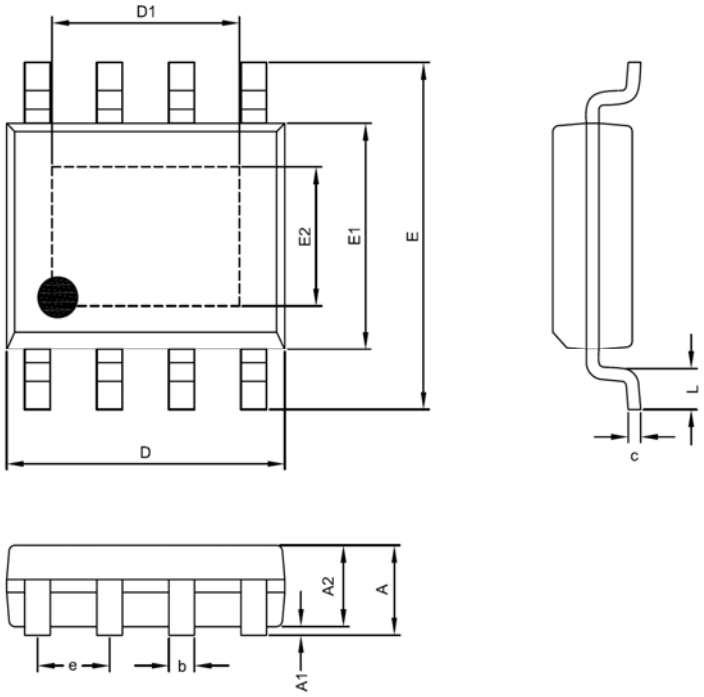
MSOP-8 Package

Symble	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.81	0.95	1.10	0.032	0.037	0.043
A1	0.00	---	0.15	0.000	---	0.006
A2	0.76	0.86	0.96	0.030	0.034	0.038
D	2.85	3.00	3.15	0.112	0.118	0.124
E	4.75	4.90	5.05	0.187	0.193	0.199
E1	2.85	3.00	3.15	0.112	0.118	0.124
c	0.13	0.15	0.23	0.005	0.006	0.009
b	0.28	0.30	0.38	0.011	0.012	0.015
e	0.65 BSC			0.026 BSC		
L	0.4	0.53	0.8	0.016	0.021	0.031

Taping Specification



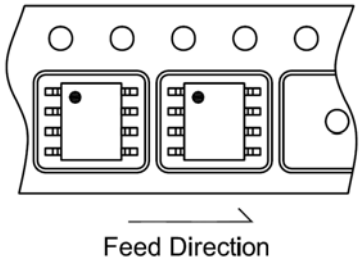
PACKAGE	Q'TY/REEL
MSOP-8	3,000 ea



SOP- 8 (FD) Package

Symble	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.35	1.55	1.65	0.053	0.061	0.065
A1	0.00	---	0.15	0.000	---	0.006
A2	1.15	1.35	1.50	0.045	0.053	0.059
D	4.80	4.90	5.00	0.189	0.192	0.197
D1	2.29	---	3.71	0.090	---	0.146
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.153	0.157
E2	2.29	---	2.64	0.090	---	0.104
c	0.19	0.23	0.27	0.007	0.009	0.011
b	0.33	0.43	0.53	0.013	0.017	0.021
e	1.27 BSC			0.050 BSC		
L	0.40	0.70	1.00	0.016	0.028	0.039

Taping Specification



PACKAGE	Q'TY/REEL
SOP-8 (FD)	2,500 ea