

24V/6A ORing-Dual Ideal Diode

Features

- 4.5 V to 24V Operating Range
- 20mΩ N-channel MOSFET
- 30mV Forward Drop in Regulation
- Smooth Switchover
- DFN3X3-10 Package

Applications

- Laptop/PC
- Multiple Input Power Supplies
- Redundant Power Supplies

General Description

The G3718 contains two power path ideal diodes that use two N-MOSFET replace for. The total capable of supplying is up to 6A with a typical forward conduction resistance of 20mΩ. It results in lower conduction forward voltage and lower power dissipation, smaller PCB layout size, and elimination of heatsink in high-power applications.

The G3718 operates from 4.5V to 24V and includes a charge pump to drive the high side N-channel MOSFET. The G3718 is easily ORing power supplies together to increase total system reliability. In the ORing Dual MOSFET application, the G3718 regulates the forward voltage drop of 30mV across the V_{IN} to V_{OUT} of internal MOSFET to ensure smooth current transfer from one path to the other without oscillation.

Ordering Information

ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE (Green)
G3718QE1U	3718	-40°C to +85°C	DFN3X3-10

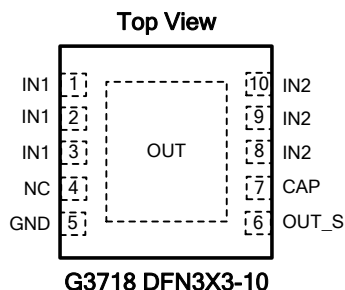
Note: QE: DFN3X3-10

1: Bonding Code

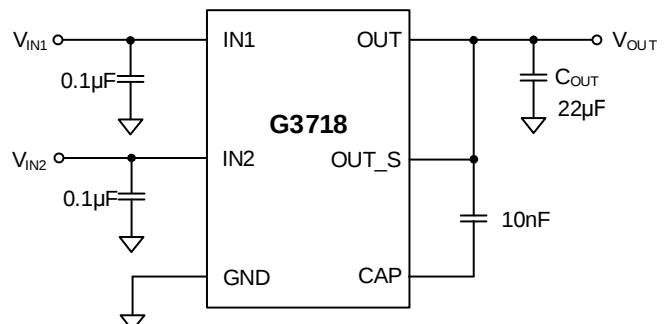
U: Tape & Reel

Green : Lead Free / Halogen Free

Pin Configuration



Typical Application Circuit



Absolute Maximum Ratings

IN1, IN2, OUT, OUT_S (OFF state) -0.3V to 28V
 CAP to OUT_S -0.3V to 7V
 Operating Temperature (T_A) -40°C to 85°C
 Operating Junction Temperature (T_J) . -40°C to 150°C
 Storage Temperature (T_{stg}) -65°C to 150°C

Recommended Operating Conditions

IN1, IN2, OUT, OUT_S 4.5V to 24V
 CAP to OUT_S 0V to 6V
 Output Current 6.0A
 Output Current (10ms) 11.4A
 ESD (HBM) ±2KV
 ESD (CDM) ±500V

Thermal Information

THERMAL METRIC		DFN3X3-10	UNIT
R _{θJA}	Junction to ambient thermal resistance	53.7	°C/W
R _{θJC_top}	Junction to case top thermal resistance	78.4	°C/W
R _{θJB}	Junction to board thermal resistance	23.9	°C/W
Ψ _{JT}	Junction to top characterization parameter	6.2	°C/W
Ψ _{JB}	Junction to board characterization parameter	23.9	°C/W
R _{θJC_bot}	Junction to case bottom thermal resistance	7.2	°C/W

- Package thermal metric is obtained using the method described in JEDEC specification JESD51-7, using a four-layer board.
- The maximum power dissipation is $P_{D(MAX)} = \frac{(T_{JMAX} - T_A)}{R_{\theta JA}}$, Exceeding the maximum allowable power dissipation results in excessive die temperature, and the device will enter thermal shutdown.

Electrical Characteristics

V_{IN1} & V_{IN2} = 20V, T_A = 25°C

The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input Voltage Range	V _{IN1/2}		4.5	---	24	V
Under Voltage Lockout Voltage	V _{UVLO}	IN Pin	---	3.73	---	V
Under Voltage Lockout Hysteresis Voltage	V _{HYS(UVLO)}		---	230	---	mV
CAP to OUT	VCAP-OUT	V _{IN} = 20V	---	5.3	---	V
Supply Current	I _{IN1}	V _{IN1} > V _{IN2} , No Load	---	180	---	μA
	I _{IN2}		---	---	10	
	I _{IN2}	V _{IN2} > V _{IN1} , No Load	---	180	---	
	I _{IN1}		---	---	10	
IN1/2 to OUT On resistance	R _{ON}	IVIN1/2 = 1A	---	20	24	mΩ
IN1/2 to OUT Regulation Voltage	V _{OL}	IVIN1/2 = 0.1A	15	30	45	mV

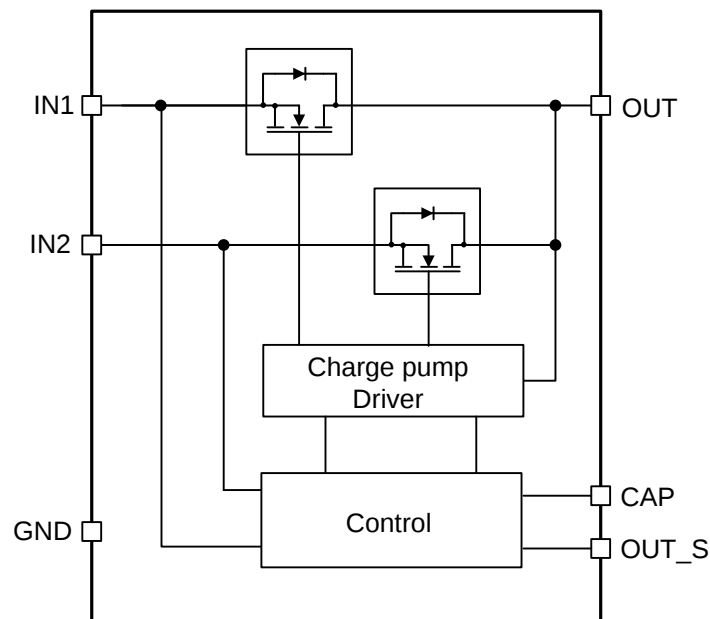
Note

*1 Guaranteed by designed

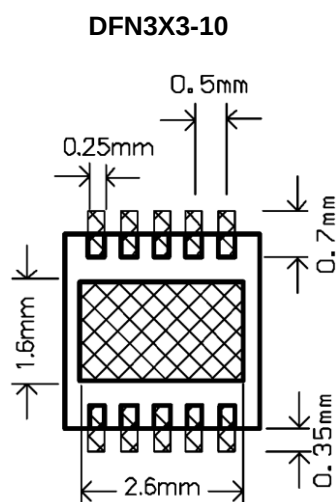
Pin Description

PIN	NAME	I/O	DESCRIPTION
1,2,3	IN1	I	Diode1 Anode, V_{IN1} input power supply terminal.
4	NC	I	No Connection.
5	GND		Ground.
6	OUT_S	O	Output voltage remote sense. This pin must be connected to OUT terminal.
7	CAP	O	The CAP pin is stand-alone connected to the OUT_S through a 10nF MLCC.
8,9,10	IN2	I	Diode2 Anode, V_{IN2} input power supply terminal.
Thermal Pad	OUT	O	OUT is the common power supply output terminal. The exposed pad is the cathode of the ideal diodes, It is also the drain of the internal N-channel MOSFETs.

Function Diagram



Minimum Footprint PCB Layout Section



Functional

IN1 and IN2

Both IN1 and IN2 are input power supply terminals. IN1 and IN2 is the anode of the ideal diode. It is also the source terminal of the internal N-channel MOSFETs.

OUT

OUT is the exposed pad which is the power supply output terminal. OUT is the common cathode of the ideal diodes, It is also the drain of the internal N-channel MOSFETs.

OUT_S

The OUT_S pin is the output voltage sense pin. It must be connected to the OUT pin.

CAP

The G3718 has an internal charge pump that pumps the internal gate-drive voltage high enough to fully turn on the ORing N-channel MOSFETs. Connect a 10nF external MLCC between CAP and OUT_S by an individual path.

Operation

The high stable power systems often use parallel connected or multi connected power supplies or battery for achieving redundant and enhance system reliability. ORing ideal diodes have been popular in connecting these supplies at the POL(point of load) or converter. The advantage of ORing ideal diodes is the lower forward voltage drop and the resulting lower power consumption loss. This drop reduces the available supply voltage and dissipates significant power. Using an N-channel MOSFET to replace a Schottky diode reduces the power dissipation and eliminates the need for costly heat sinks or large thermal layout in high power applications.

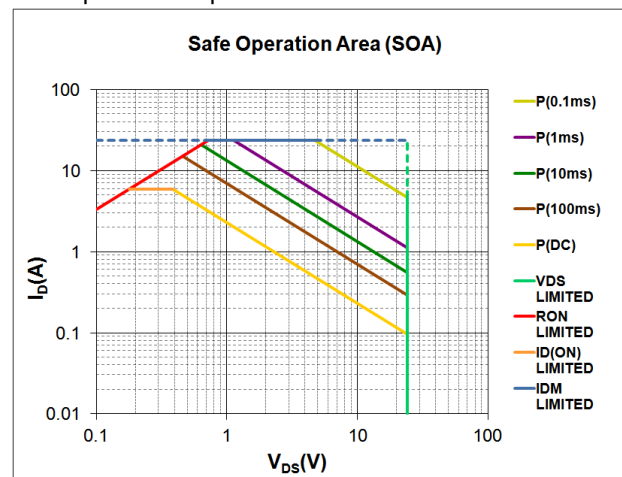
The G3718 operates from 4.5V to 24V and includes a charge pump to drive the high side N-channel MOSFET. During normal operation, the device will always try to regulate the V_{OUT} to be $V_{IN} - 30mV$. When the load current produces a forward drop voltage greater than 30mV, the gate control loop will drive the N-channel MOSFET to lower its $R_{DS(on)}$ to try to achieve the 30mV. In the heavy load condition, the gate control loop will keep increasing the gate driving current of the MOSFET until it is fully on and remains fully on if the forward drop voltage at that time still exceeds 30mV. The MOSFET is driven fully on and the voltage drop is equal to

$$R_{DS(on)} * I_{LOAD}$$

In light load condition, If the load current is reduced causing the forward drop to fall below 30mV, the gate control loop will reduce the gate driving current to increase the $R_{DS(on)}$ to try to achieve the 30mV drop voltage.

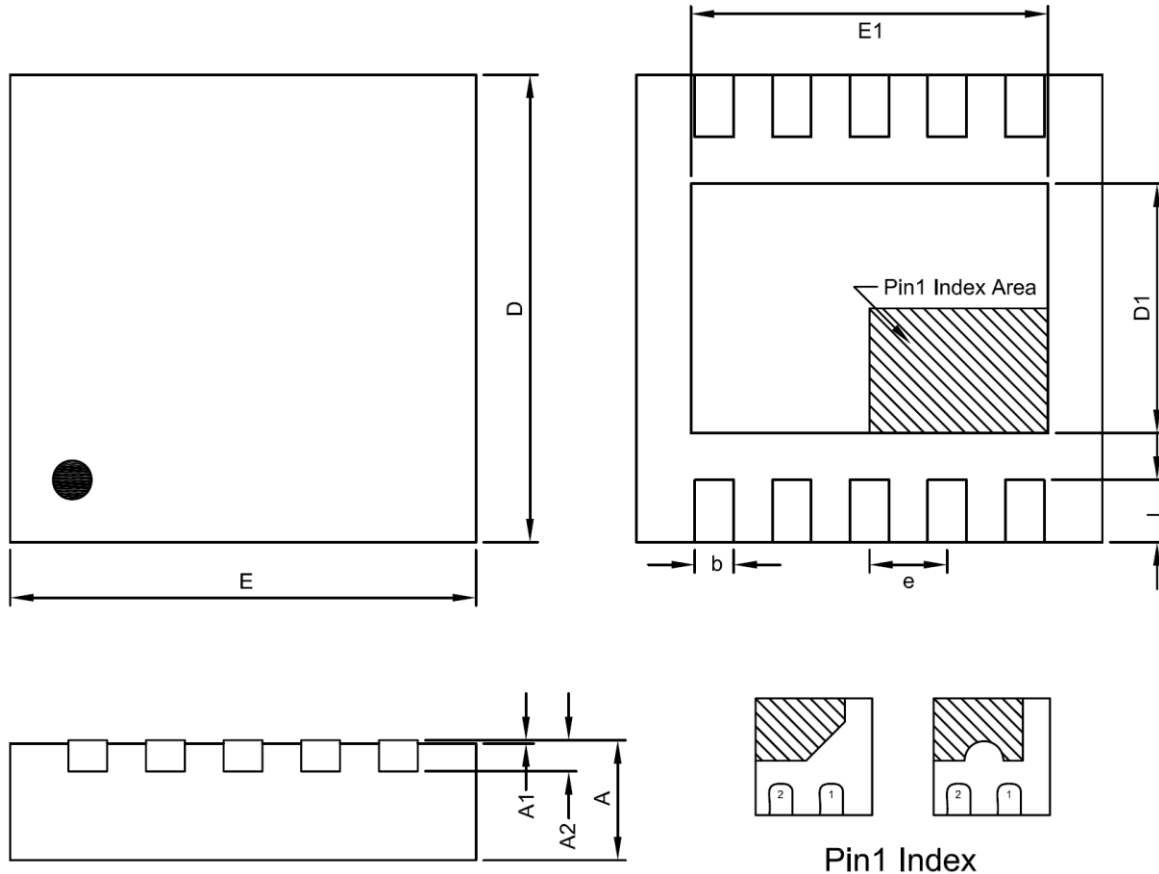
Safe Operating Area, SOA

The Safe Operation Area, SOA specification combines the various limitations of the device — maximum voltage, current, power, and junction temperature into one curve, allowing the simplified design of protection circuitry. The illustration of SOA is the combination of voltage and current below the line that can be tolerated, in addition to the continuous rating, separate SOA curves are also plotted for different single duration pulse conditions (100 ms, 10 ms pulse, etc.) The SOA curve is a graphical representation of the power handling capability of the device under various conditions. The SOA curve takes into account the wire bond current carrying capability, junction temperature, and internal power dissipation limitations.

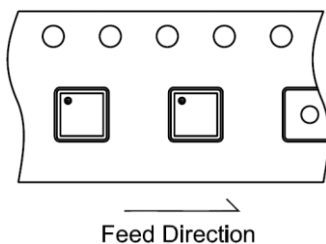


Application

The G3718's layout should be considered: The OUT pin should be connected as closely as possible to the exposed pad (the cathode of the ideal diodes, the drain of the MOSFETs) for good accuracy. Keep the traces (polygon shapes) to the IN1/IN2 and OUT short and wide. The PCB traces associated with the power path through the MOSFET should have low resistance. The OUT acts as a heatsink to remove the heat from the device. The CAP pin is stand-alone connected to the OUT_S through a 10nF MLCC.

Package Information

DFN3X3-10 Package

Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.90	1.00	0.0315	0.0354	0.0394
A1	0.00	---	0.05	0.0000	---	0.0020
A2	0.20 REF			0.0079 REF		
D	2.95	3.00	3.05	0.1161	0.1181	0.1201
E	2.95	3.00	3.05	0.1161	0.1181	0.1201
D1	1.50	1.60	1.75	0.0591	0.0630	0.0689
E1	2.20	2.60	2.70	0.0866	0.1024	0.1063
b	0.18	0.25	0.30	0.0071	0.0098	0.0118
e	0.50 BSC			0.0197 BSC		
L	0.30	0.40	0.50	0.0118	0.0157	0.0197

Taping Specification


PACKAGE	Q'TY/REEL
DFN3X3-10	3,000 ea

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