eFuse with Over Voltage Protection and Blocking FET Control

Features

- **5-V eFuse**
  - **G3720H05FL/G3720H05F**
- **12-V eFuse**
  - **G3720H12FL/G3720H12F**
- **Fixed Over-Voltage Clamp**
  - **6.1V-Clamp: G3720H05FL/G3720H05F**
  - **15V-Clamp: G3720H12FL/G3720H12F**
- **Integrated 28mΩ Pass MOSFET**
- **1A to 5A Adjustable I_{LIMIT}**
- **±7.5% I_{LIMIT} Accuracy at 3.7A**
- **Reverse Current Blocking Support**
- **Programmable OUT Slew Rate, UVLO**
- **Built-in Thermal Shutdown**
- **Small Foot Print – DFN3X3-10**
- **UL 2367 Recognition-File NO. E232223**

Applications

- **Adapter Powered Devices**
- **HDD and SSD Drives**
- **Set Top Boxes**
- **Servers / AUX Supplies**
- **Fan Control**
- **PCI/PCIe Cards**

General Description

The G3720 series of eFuses is a highly integrated circuit protection and power management solution in a tiny package. The devices use few external components and provide multiple protection modes. They are a robust defense against overloads, shorts circuits, voltage surges, excessive inrush current, and reverse current.

Current limit level can be set with a single external resistor. Over voltage events are limited by internal clamping circuits to a safe fixed maximum, with no external components required. Applications with particular voltage ramp requirements can set dV/dT with a single capacitor to ensure proper output ramp rates.

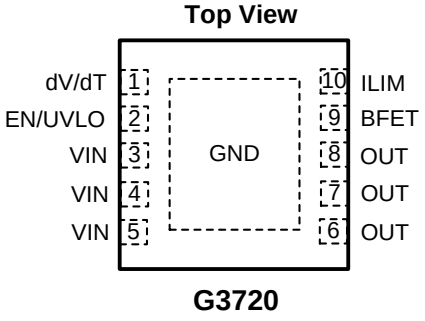
Many systems, such as SSDs, must not allow holdup capacitance energy to dump back through the FET body diode onto a drooping or shorted input bus. The BFET pin is for such systems. An external NFET can be connected “Back to Back (B2B)” with the G3720 output and the gate driven by BFET to prevent current flow from load to source.

Ordering Information

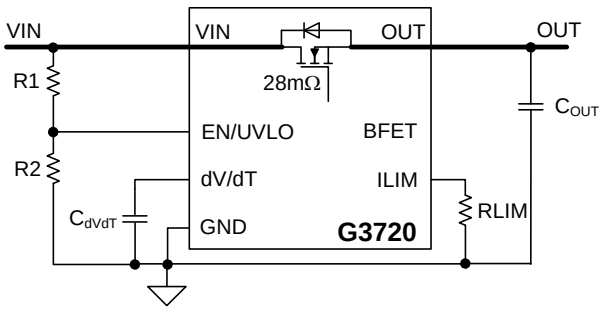
Order Number	Marking	Output Voltage Clamp	Response to Thermal Shutdown (TSD)	Enable	Temp. Range	Package (Green)
G3720H05FLQE1D	30BA	6.1	Latch-off	Active high	-40°C to +85°C	DFN3X3-10
G3720H05FQE1D	30BB	6.1	Auto-retry	Active high	-40°C to +85°C	DFN3X3-10
G3720H12FLQE1D	30CA	15	Latch-off	Active high	-40°C to +85°C	DFN3X3-10
G3720H12FQE1D	30CB	15	Auto-retry	Active high	-40°C to +85°C	DFN3X3-10

Note: QE:DFN3X3-10
1: Bonding Code
D: Tape & Reel
Green: Lead Free / Halogen Free

Pin Configuration



Typical Application Circuit



Absolute Maximum Ratings

Supply Voltage

VIN . . . . . -0.3V to 20V
VIN (10msTransient) 22V

Output Voltage

OUT . . . . . .-0.3V to VIN+0.3V
OUT (Transient<1μs) . . . . . .-1.2V

Voltage

ILIM . . . . . -0.3V to 7V
EN/UVLO . . . . . -0.3V to 7V
dV/dT. . . . . -0.3V to 7V
BFET. . . . . -0.3V to 30V
ESD(HBM) . . . . . .±2.5KV
ESD(CDM) . . . . . ±500V

Recommended Operating Conditions

Input Voltage

VIN . . . . . 4.5V to 12V
BFET . . . . . 0V to VIN+6V
dV/dT, EN/UVLO. . . . . 0V to 6V
ILIM. . . . . 0V to 3V
Continuous output current (I_{OUT}). . . . . 0A to 5A
Resistance (ILIM) . . . . . .10kΩ to 162kΩ

External capacitance

OUT . . . . . 0.1 to 1000μF
dV/dT. 1000nF
Operating Junction Temperature (T_J). .-40°C to 125°C
Operating Ambient Temperature (T_A). . .-40°C to 85°C
Storage Temperature (T_{STG}) . . . . . -65°C to 150°C

Thermal Information

THERMAL METRIC		DFN3X3-10	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance	52.2	°C/W
$R_{\theta JC\_top}$	Junction to case top thermal resistance	74.7	°C/W
$R_{\theta JB}$	Junction to board thermal resistance	22.1	°C/W
Ψ_{JT}	Junction to top characterization parameter	2.4	°C/W
Ψ_{JB}	Junction to board characterization parameter	22.1	°C/W
$R_{\theta JC\_bot}$	Junction to case bottom thermal resistance	4.1	°C/W

1. Package thermal metric is obtained using the method described in JEDEC specification JESD51-7, using a four-layer board.
2. The maximum power dissipation is $P_{D(MAX)} = \frac{(T_{JMAX} - T_A)}{R_{\theta JA}}$, Exceeding the maximum allowable power dissipation results in excessive die temperature, and the device will enter thermal shutdown.

Electrical Characteristics

(–40°C≤T_J≤ +125°C, V_{IN}=5V, $V_{EN/UVLO}$=2V, RILIM=100kΩ, CdV/dT=OPEN. All voltages referenced to GND)

The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
VIN (Input Supply)							
UVLO Threshold	V_{UVR}	Rising		4.15	4.3	4.45	V
	V_{UV_HYS}	Hysteresis		---	5%	---	
Quiescent Current	I_Q	$V_{EN/UVLO}$=2V		0.3	0.42	0.55	mA
Shutdown Current	I_{SHDN}	$V_{EN/UVLO}$=0V		---	0.1	0.225	mA
Over-Voltage Clamp	V_{OVC}	G3720H05FL	V_{VIN}>6.75V, I_{OUT}=10mA	5.5	6.1	6.75	V
		G3720H05F					
		G3720H12FL	V_{VIN}>16.5V, I_{OUT}=10mA	13.8	15	16.5	
		G3720H12F					
OUT (Pass FET Output)							
FET ON Resistance	$R_{DS(on)}$	T_J=25°C		21	28	37	mΩ
		T_J=125°C		---	39	48	
OUT Bias Current in off State	$I_{OUT\_OFF\_LKG}$	$V_{EN/UVLO}$=0V, V_{OUT}=0V (sourcing)		–5	0	1.2	µA
	$I_{OUT\_OFF\_SINK}$	$V_{EN/UVLO}$=0V, V_{OUT}=300mV (sinking)		10	15	20	
Turnon Delay	T_{DLY_ON}	Enabling of chip to I_D = 100 mA with 1 A resistive load		---	220	---	µs
Turnoff Delay	T_{DLY_OFF}			---	0.4	---	
EN/UVLO (Enable/UVLO Input)							
EN Threshold Voltage	V_{ENR}	Rising		1.37	1.4	1.44	V
	V_{ENF}	Falling		1.32	1.35	1.39	V
EN Input Leakage Current	I_{EN}	0V≤V_{EN}≤5V		–0.1	0	0.1	µA

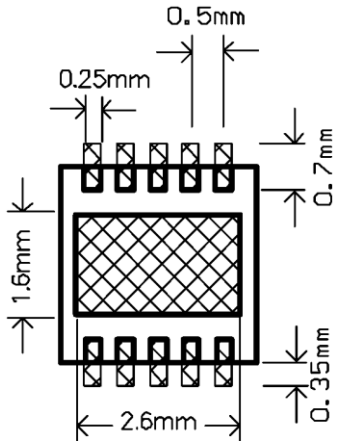
Electrical Characteristics (Continued)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
dV/dT (Output Slew Rate Control)							
dV/dT Charging Current	$I_{dV/dT}$	$V_{dV/dT}$=0V		---	220	---	nA
dV/dT Discharging Resistance	R_{dV/dT_disch}	$V_{EN/UVLO}$=0V, $I_{dV/dT}$=10mA sinking		50	75	100	Ω
dV/dT to OUT Gain	$GAIN_{dV/dT}$	$\Delta V_{dV/dT}$		---	4.85	---	V/V
Output Ramp Time	$t_{dV/dT}$	Enable to V_{OUT}=4.9V, $C_{dV/dT}$ =0		0.28	0.42	0.52	ms
		Enable to V_{OUT}= 4.9V, $C_{dV/dT}$=1nF		---	5	---	
		Enable to V_{OUT}=11.7V, $C_{dV/dT}$ =0		0.7	1	1.3	
		Enable to V_{OUT}=11.7V, $C_{dV/dT}$=1nF		---	12	---	
ILIM (Current Limit)							
ILIM Bias Current	I_{ILIM}	V_{ILIM}=0V		---	10	---	µA
Overload Current Limit	I_{OC}	R_{ILIM}=10kΩ, $V_{VIN-OUT}$=1V		---	1.02	---	A
		R_{ILIM}=45.3kΩ, $V_{VIN-OUT}$=1V		1.79	2.10	2.42	
		R_{ILIM}=100kΩ, $V_{VIN-OUT}$=1V		3.46	3.75	4.03	
		R_{ILIM}=150kΩ, $V_{VIN-OUT}$=1V		4.5	5.1	5.7	
	$I_{OC\_R\_Short}$	R_{ILIM}=0Ω, $V_{VIN-OUT}$=1V		---	0.84	---	A
	$I_{OC\_R\_Open}$	R_{ILIM}=OPEN, $V_{VIN-OUT}$=1V		---	0.73	---	A
Short-Circuit Current Limit	I_{SC}	G3720H05FL G3720H05F	R_{ILIM}=10kΩ, $V_{VIN-OUT}$=5V	---	1.01	---	A
			R_{ILIM}=45.3kΩ, $V_{VIN-OUT}$=5V	1.72	2.05	2.42	
			R_{ILIM}=100kΩ, $V_{VIN-OUT}$=5V	3.14	3.56	3.98	
			R_{ILIM}=150kΩ, $V_{VIN-OUT}$=5V	4.22	4.95	5.69	
		G3720H12FL G3720H12F	R_{ILIM}=10kΩ, $V_{VIN-OUT}$=12V	---	0.98	---	
			R_{ILIM}=100kΩ, $V_{VIN-OUT}$=12V	2.9	3.32	3.85	
			R_{ILIM}=45.3kΩ, $V_{VIN-OUT}$=12V	1.62	1.98	2.37	
			R_{ILIM}=150kΩ, $V_{VIN-OUT}$=12V	3.7	4.5	5.5	
Fast-Trip Comparator Level w.r.t. Overload Current Limit		$I_{FASTRIP}$: I_{OC}		---	160%	---	
Fast-Trip Comparator Delay	$t_{FASTOffDly}$	I_{OUT} > $I_{FASTRIP}$ to I_{OUT}=0 (Switch off)		---	300	---	ns
ILIM Open Detect Threshold	V_{ILIM_OPEN}			---	3.1	---	V
BFET (Blocking FET Gate Driver)							
BFET Charging Current	I_{BFET}	V_{BFET}=V_{OUT}		---	2	---	µA
BFET Discharging Resistance	R_{BFET_disch}	$V_{EN/UVLO}$=0 V, I_{BFET}=100mA		15	26	36	Ω
BFET Clamp Voltage	V_{BFET_MAX}			---	V_{VIN} + 6.4	---	V
BFET Turnon Time	t_{BFET_ON}	Enable to V_{BFET}=12V, C_{BFET}=1nF			4.2		ms
		Enable to VBFET=12V, C_{BFET}=10nF			42		
BFET Turnoff Time	t_{BFET_OFF}	$V_{EN/UVLO}$=0V to V_{BFET}=1V, C_{BFET}=1nF			0.4		µs
		$V_{EN/UVLO}$=0V to V_{BFET}=1V, C_{BFET}=10nF			1.4		
TSD (Thermal Shut Down)							
Thermal Shutdown Temperature	T_{SHDN}	Rising		---	150	---	°C
	T_{SD_HYS}	Hysteresis		---	10	---	°C
Retry Delay After TSD Recovery	T_{SD_DLY}	G3720H05F		---	0.1	---	ms
		G3720H12F					
		G3720H05FL		Latch-off			
		G3720H12FL					

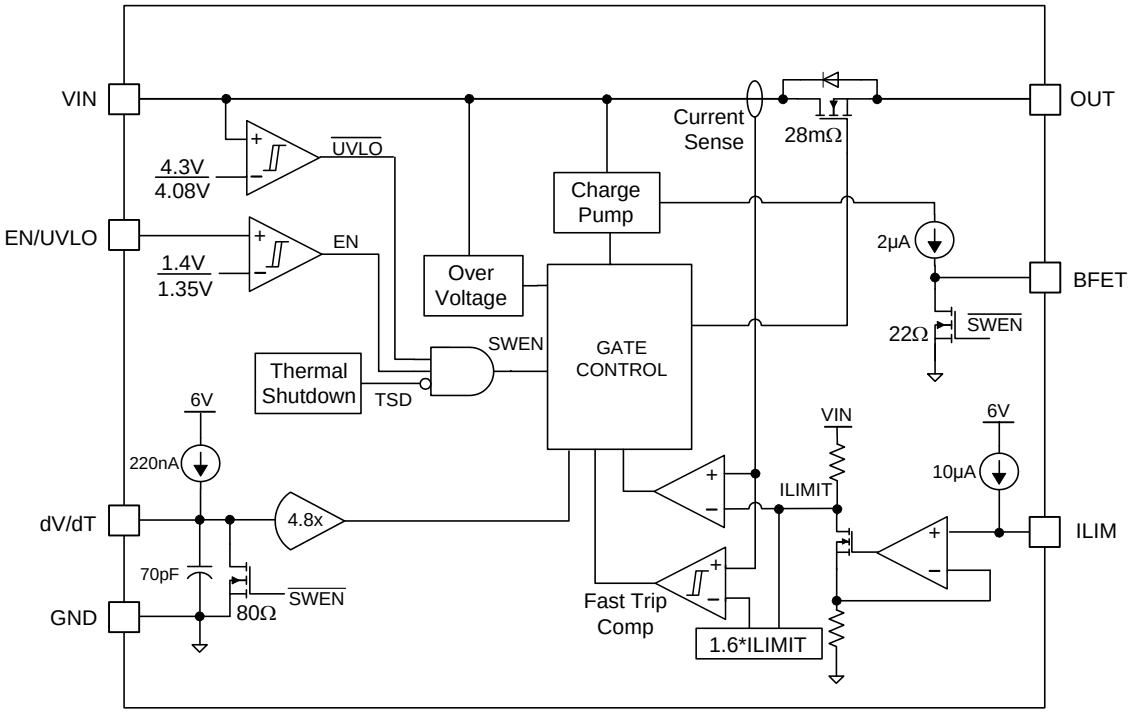
Pin Description

PIN	NAME	I/O	DESCRIPTION
1	dV/dT	O	Tie a capacitor from this pin to GND to control the ramp rate of OUT at device turnon
2	EN/UVLO	I	This is a dual function control pin. When used as an ENABLE pin and pulled down, it shuts off the internal pass MOSFET and pulls BFET to GND. When pulled high, it enables the device and BFET. As an UVLO pin, it can be used to program different UVLO trip point via external resistor divider
3,4,5	VIN	I	Input supply voltage
6,7,8	OUT	O	Output of the device
9	BFET	O	Connect this pin to the gate of a blocking NFET. See the Feature Description section. Leave this pin floating if it is not used
10	ILIM	O	A resistor from this pin to GND sets the overload and short circuit limit
Thermal Pad	GND	Ground	GND

Minimum Footprint PCB Layout Section



Block Diagram



Typical Applications

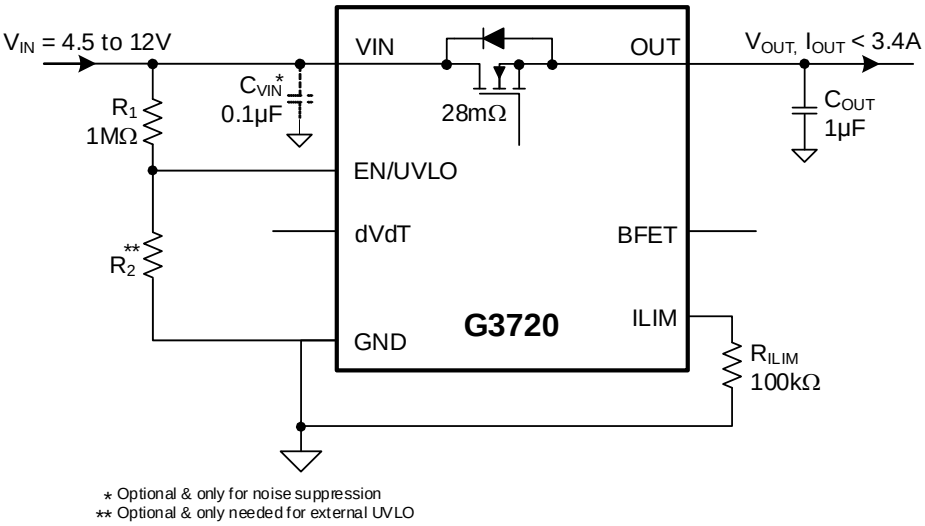


Figure 1. Simple 3.4A eFuse

Typical Applications (continued)

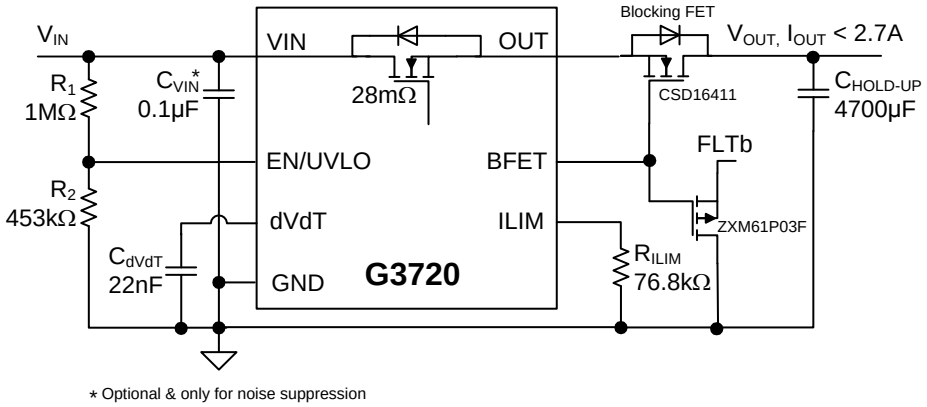


Figure 2. Inrush and Reverse Current Protection for Hold-Up Capacitor Application

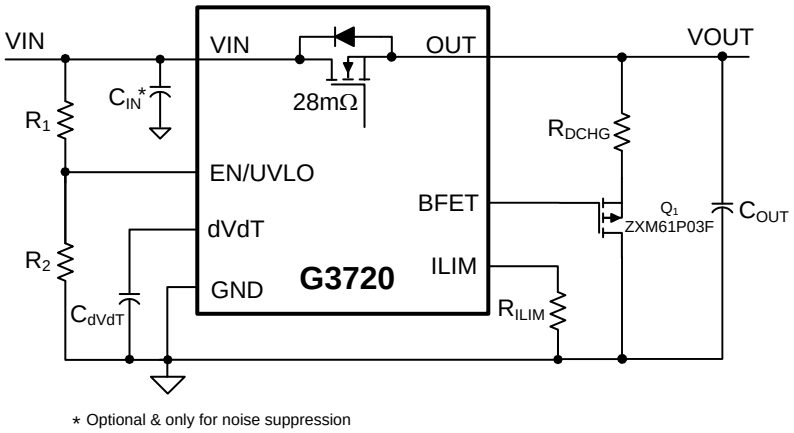


Figure 3. Circuit Implementation with Quick Output Discharge Function

Function Description

Slew Rate and Ramp time (dV/dT)

Connect a capacitor from this pin to GND to control the output voltage at power-on. This pin can be left floating to obtain a predetermined slew rate (minimum $T_{dV/dT}$) on the output. The total ramp time ($T_{dV/dT}$) for 0 to VIN can be calculated using Equation 1.

$$T_{dV/dT} = 10^6 \times V_{IN} \times (C_{dV/dT} + 70pF) \quad (1)$$

R_{ILIM} Selection

The R_{ILIM} resistor at the ILIM pin sets the over load current limit, this can be set as follows.

$$R_{ILIM}=(I_{OC}-0.7) / (3x10^{-5}) \quad (2)$$

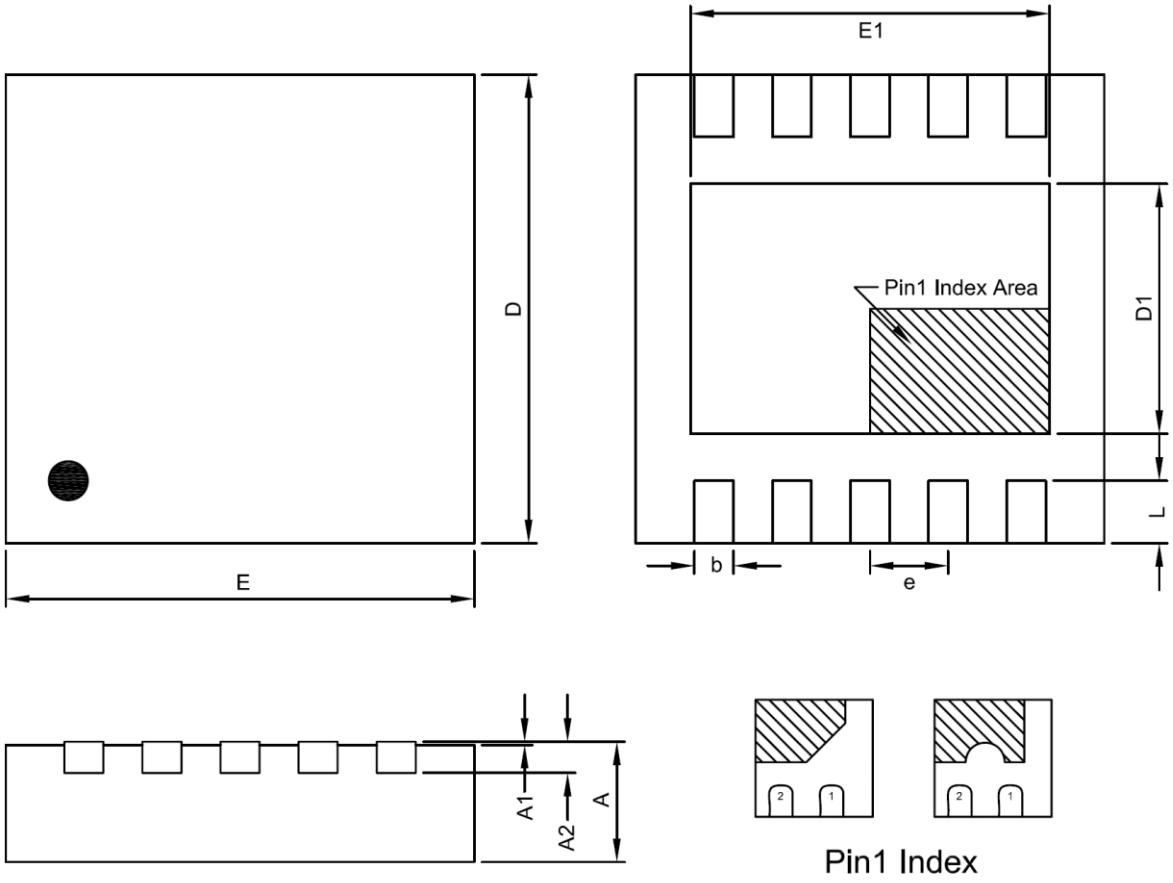
BFET

Connect this pin to an external NFET that can be used to disconnect input supply from rest of the system in the event of power failure at VIN. The BFET pin is controlled by either input UVLO (V_{UVR}) event or EN/UVLO (see Table 1). BFET can source charging current of 2µA (TYP) and sink (discharge) current from the gate of the external FET via a 26Ω internal discharge resistor to initiate fast turnoff, typically <1µs. Due to 2µA charging current, it is recommended to use >10MΩ impedance when probing the BFET node.

Table 1. BFET

EN/UVLO > V_{ENR}	VIN > V_{UVR}	BFET MODE
H	H	Charge
X	L	Discharge
L	X	Discharge

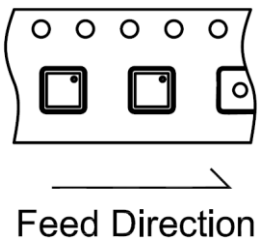
Package Information



DFN3X3-10 Package

Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.90	1.00	0.0315	0.0354	0.0394
A1	0.00	- - -	0.05	0.0000	- - -	0.0020
A2	0.20 REF			0.0079 REF		
D	2.95	3.00	3.05	0.1161	0.1181	0.1201
E	2.95	3.00	3.05	0.1161	0.1181	0.1201
D1	1.50	1.60	1.75	0.0591	0.0630	0.0689
E1	2.20	2.60	2.70	0.0866	0.1024	0.1063
b	0.18	0.25	0.30	0.0071	0.0098	0.0118
e	0.50 BSC			0.0197 BSC		
L	0.30	0.40	0.50	0.0118	0.0157	0.0197

Taping Specification



PACKAGE	Q'TY/BY REEL
DFN3X3-10	3,000 ea