12-Channel, 16-Bit, Enhanced Spectrum, PWM, RGB, LED Driver with 3.3-V Linear Regulator

Features

- **Power Supply Range:**
  Internal linear Regulator: 6V to 17V
  Direct Power Supply: 3V to 5.5V
- **12 constant-current output channels**
- **Drive up to 60mA Each Channel**
- **Grayscale Control with Enhanced PWM:**
  16-bit (65536 steps)
- **Global Brightness Control :**
  7-bit (128 steps) for each color group
- **LED Supply Voltage: up to 17V**
- **Excellent Current Accuracy:**
  Between Channels: ±1%(typ.)
  Between ICs: ±1%(typ.)
- **Data Transfer Rate: 20MHz**
- **Linear Regulator: 3.3V**
- **Auto Display Repeat Function**
- **Display Timing Reset Function**
- **Internal/External Selectable GS Clock**
- **Thermal Shutdown with Auto Restart**
- **Available in QFN 4X4-24 Package**
- **RoHS Compliant**

General Description

The G5031 is a 12-channels, constant-current sink driver, which is designed for RGB LED cluster lamp applications using internal Pulse Width Modulation (PWM) control with 16-bit color depth. Each output channel has individually adjustable currents with 65536 PWM grayscale (GS) steps. Also, each color group can be controlled by 128 constant-current sink steps with the global brightness control (BC) function. GS control and BC are accessible via a two-wire signal interface. The maximum current value for each channel is set by a single external resistor. All constant-current outputs are turned off when the IC is in an over-temperature condition.

Applications

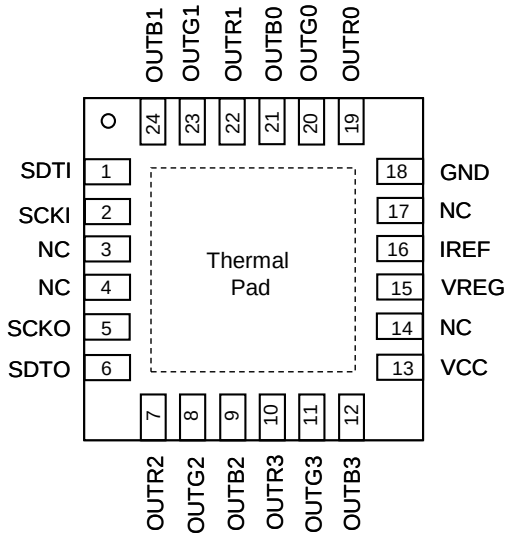
- **RGB LED Cluster Lamp Displays**

Ordering Information

ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE (Green)
G5031Q51D	5031	-40°C to +85°C	QFN4X4-24

Note: Q5:QFN4X4-24
1: Bonding Code
U: Tape & Reel
Green : Lead Free / Halogen Free

Pin Configuration

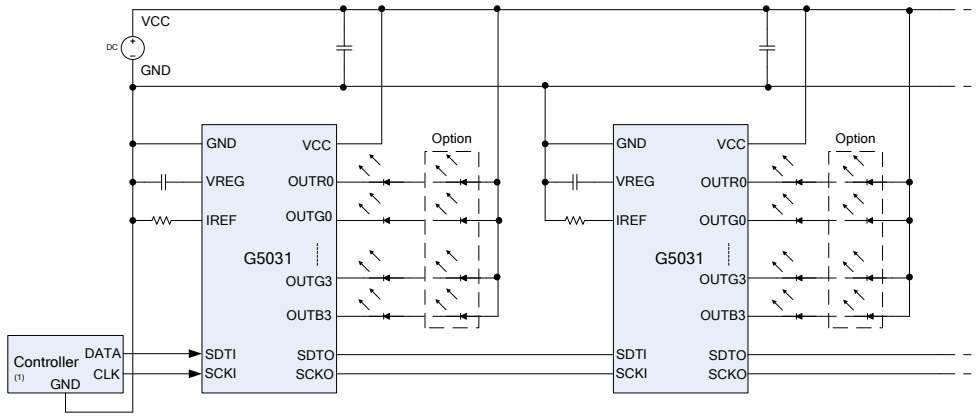


G5031 QFN4X4-24

Note: Recommend connecting the Thermal Pad to the GND for excellent power dissipation.

Typical Application Circuit

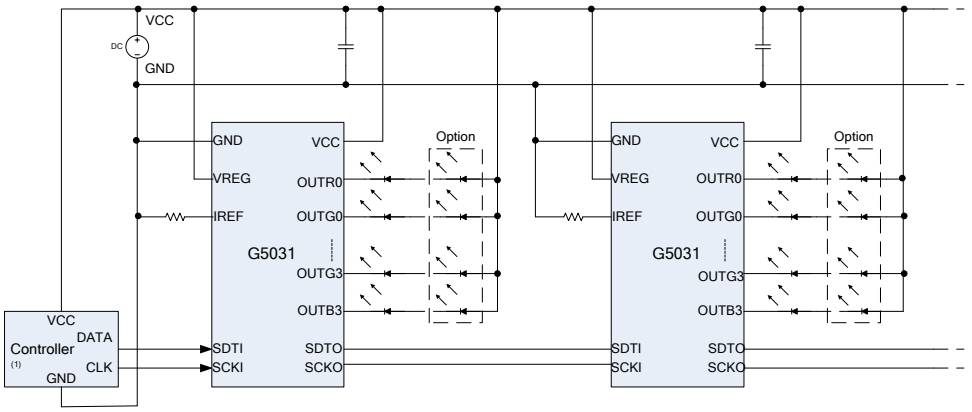
Typical Application Circuit Example (Internal Linear Regulator Using VCC=6V to 17V)



(1) The output voltage range is from 0V to 3.3V

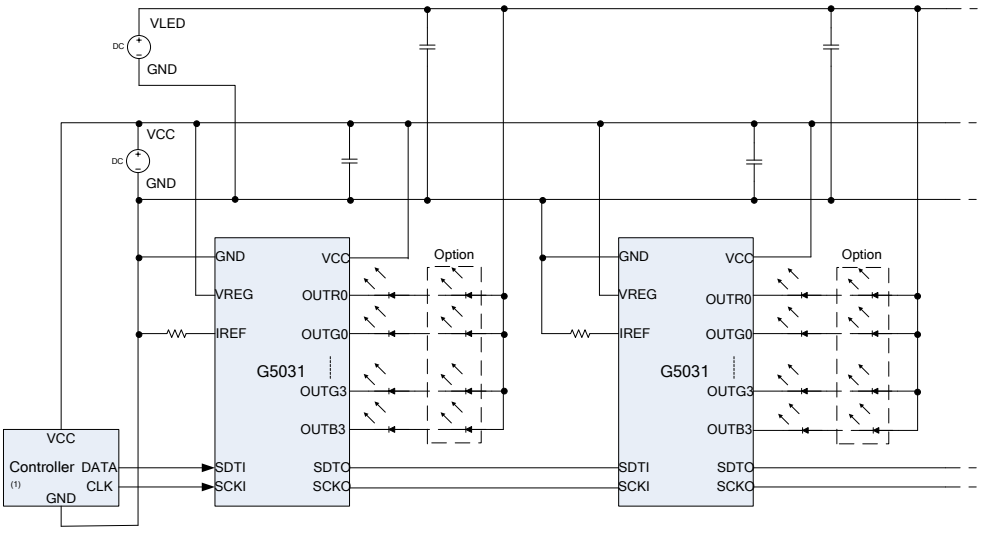
Note: The number of LEDs in series changes, depending on the VCC voltage.

Typical Application Circuit Example (Direct Power Supplying VCC=3V to 5.5V)



(1) The output operating voltage range is from 0V to VCC

Typical Application Circuit Example (Direct Power Supplying VCC=3V to 5.5V, V_{LED}=15V)



(1) The output operating voltage range is from 0V to VCC

Absolute Maximum Ratings

Supply Voltage, VCC . . . . . .-0.3V to 18V
Input Voltage
IREF. . . . . .-0.3V to VREG + 0.3V
SDTI,SCKI. . . . . .-0.3V to VREG + 0.6V
Output Voltage
OUTR0 to OUTR3, OUTG0 to OUTG3, OUTB0 to OUTB3 . . . . . -0.3V to + 18V
SDTO,SCKO. . . . . .-0.3V to VREG + 0.3V
VREG. . . . . .-0.3V to + 6V
Output Current (DC)
OUTR0 to OUTR3, OUTG0 to OUTG3, OUTB0 to OUTB3 . . . . . 75mA
VREG. . . . . .-30mA
Operating junction Temperature $T_{J(max)}$ . . . . . +150°C
Storage Temperature T_{stg} . . . . . -55°C to + 150°C
Electrostatic Discharge Rsting
Human body mode (HBM) 4kV
Machine mode (MM) 200V

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

Recommended Operating Conditions

At T_A=–40°C to +85°C, and VCC=6V to 17V or VCC=VREG=3 V to 5.5 V, unless otherwise noted.

PARAMETER	SYMBOL	MIN	NOM	MAX	UNIT
DC Characteristics					
Supply voltage, internal voltage regulator used	VCC	6		17	V
Supply voltage, VREG connected to VCC	VREG	3	3.3	5.5	V
Voltage applied to output (OUTR0 to OUTR3, OUTG0 to OUTG3, OUTB0 to OUTB3)	V_O	---	---	17	V
High-level input voltage (SDTI, SCKI)	V_{IH}	0.7×VREG	---	VREG	V
Low-level input voltage (SDTI, SCKI)	V_{IL}	GND	---	0.3×VREG	V
Input voltage hysteresis (SDTI, SCKI)	V_{IHYS}	---	0.2×VREG	---	V
High-level output current (SDTO)	I_{OH}	---	---	–2	mA
Low-level output current (SDTO)	I_{OL}	---	---	2	mA
Constant output sink current (OUTR0 to OUTR3, OUTG0 to OUTG3, OUTB0 to OUTB3)	I_{OLC}	---	---	60	mA
Voltage regulator output current (VREG)	I_{REG}	---	---	–25	mA
Operating free temperature range	T_A	–40	---	+85	°C
Operating junction temperature	T_J	–40	---	+125	°C
AC Characteristics					
Data clock frequency and GS control clock frequency, SCKI	$f_{CLK\ (SCKI)}$	0.007	---	20	MHz
Pulse duration, SCKI	t_{WH}/t_{WL}	10	---	---	ns
Setup time, SDTI – SCKI↑	t_{SU}	5	---	---	ns
Hold time, SDTI – SCKI↑	t_H	3	---	---	ns

Electrical Characteristics

V_{CC}=6V to 17V or VCC=VREG=3V to 5.5V, VLED=5V, and C_{VREG}=1μF. Typical values are at T_A =+25°C and VCC=12V. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-level output voltage, SDTO/SCKO	V_{OH}	IOH=–2mA	VREG–0.4	---	VREG	V
Low-level output voltage, SDTO/SCKO	V_{OL}	IOL=2mA	0	---	0.4	V
Input current, SDTI/SCKI	I_I	VI=VREG or GND	–1	---	1	μA
Supply current	I_{CC}	SDTI/SCKI=low, BLANK=1, GSn=FFFFh, BCX=7Fh, V_{OUTXn}=1V, R_{IREF}=25kΩ (I_{OLCMax}=2mA)	---	2	4	mA
	I_{CC1}	SDTI/SCKI=low, BLANK=1, GSn=FFFFh, BCX=7Fh, V_{OUTXn}=1V, R_{IREF}=1.7 kΩ (I_{OLCMax}=30mA)	---	6	9	mA
	I_{CC2}	SDTI=10MHz, SCKI=20MHz, BLANK=0, auto repeat enable, external GS clock selected, GSn=FFFFh, BCX=7Fh, V_{OUTXn} =1V, R_{IREF}=1.7kΩ (IOLCMax=30mA)	---	14	22	mA
	I_{CC3}	SDTI=10MHz, SCKI=20MHz, BLANK=0, auto repeat enable, external GS clock selected, GSn=FFFFh, BCX=7Fh, V_{OUTXn} =1V, R_{IREF}=0.83kΩ (I_{OLCMax}=60mA)	---	21	36	mA
Constant output current, OUTXn	I_{OLC}	All OUTXn on, BCX=7Fh, V_{OUTXn}=1V, V_{OUTfix}=1V, R_{IREF}=0.83kΩ (I_{OLCMax}=60mA)	56.3	60.5	64.7	mA
Leakage output current, OUTXn	I_{OLKG}	All OUTXn off, BCX=7Fh, VOUTXn=17V, V_{OUTfix}=17V, R_{IREF}=0.83kΩ (I_{OLCMax}=60mA)	---	---	0.1	μA
Constant-current error(1) (channel-to-channel in same color group), OUTXn	ΔI_{OLC}	All OUTXn on, BCX=7Fh, V_{OUTXn}=V_{OUTfix}=1V, R_{IREF}=0.83kΩ (I_{OLCMax}=60mA)	---	±1	±3	%
Constant current error(2) (device-to-device in same color group), OUTXn	ΔI_{OLC1}	All OUTXn on, BCX=7Fh, VOUTXn=V_{OUTfix} = 1V, R_{IREF}=0.83kΩ (I_{OLCMax}=60mA), at same grouped color output of OUTR0-3, OUTG0-3, and OUTB0-3	---	±1	±4	%
Line regulation of constant-current output, OUTXn(3)	ΔI_{OLC2}	All OUTn on, BCX=7Fh, V_{OUTXn}=V_{OUTfix}=1V, R_{IREF}=0.83kΩ (I_{OLCMax}=60 mA)	---	±0.5	±1	%/V
Load regulation of constant-current output, OUTXn(4)	ΔI_{OLC3}	All OUTn on, BCX=7Fh, V_{OUTXn}=V_{OUTfix} =1V, R_{IREF}=0.83kΩ (I_{OLCMax}=60 mA)	---	±1	±3	%/V
Thermal shutdown temperature	T_{TSD}	Junction temperature(5)	130	145	160	°C
Thermal shutdown hysteresis	T_{HYS}	Junction temperature(5)	10	20	30	°C
Reference voltage output, I_{REF}	V_{IREF}	R_{IREF}=0.83kΩ	1.195	1.225	1.255	V
Linear regulator output voltage, VREG	V_{REG}	VCC=6V to 1 V, IREG=0mA to –25mA	3.1	3.3	3.5	V
Line regulation of linear regulator, VREG	ΔV_{REG}	VCC=6V to 17V, IREG=0mA	---	---	90	mV
Load regulation of linear regulator, VREG	ΔV_{REG1}	VCC=12V, IREG=0mA to –25mA	---	---	120	mV
Undervoltage lockout release, VREG	V_{STR}		2.5	2.7	2.9	V
Undervoltage lockout hysteresis, VREG	V_{HYS}		300	400	500	mV

(1) The deviation of each output in the same color group (OUTR0-OUTR3 or OUTG0-OUTG3 or OUTB0-OUTB3) from the average current from the same color group. Deviation is calculated by the formula:

$$\Delta(\%) = \left(\frac{I_{OLCXn}}{\frac{(I_{OLCX0} + I_{OLCX1} + I_{OLCX2} + I_{OLCX3})}{4}} - 1 \right) \times 100$$

Where: X=R/G/B, and n = 0-3

(2) The deviation of each color group constant-current average from the ideal constant-current value.
Deviation is calculated by the following formula:

$$\Delta(\%) = \left(\frac{\frac{I_{OLCX0} + I_{OLCX1} + I_{OLCX2} + I_{OLCX3}}{4} - (\text{Ideal Output Current})}{\text{Ideal Output Current}} \right) \times 100$$

Where: X=R/G/B.
Ideal current is calculated by the following formula for the OUTRn and OUTGn groups:

$$I_{OLCXN(IDEAL)}, (mA) = 41X \left(\frac{1.225}{R_{IREF}(\Omega)} \right)$$

Where: X=R/G/B.

(3) Line regulation is calculated by this equation:

$$\Delta(\%/V) = \left(\frac{(I_{OLCXn} \text{ at } VCC = 5.5V) - (I_{OLCXn} \text{ at } VCC = 3V)}{(I_{OLCXn} \text{ at } VCC = 3V)} \right) \times \frac{100}{5.5V - 3V}$$

Where: X=R/G/B, n = 0-3

(4) Load regulation is calculated by the equation:

$$\Delta(\%/V) = \left(\frac{(I_{OLCXn} \text{ at } V_{OUTXn} = 3V) - (I_{OLCXn} \text{ at } V_{OUTXn} = 1V}{(I_{OLCXn} \text{ at } V_{OUTXn} = 1V)} \right) \times \frac{100}{3V - 1V}$$

Where: X=R/G/B, n = 0-3

(5) Not tested, specified by design.

Switching Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Rise time, SDTO/SCKO	t_{R0}		---	3	10	ns
Rise time, OUTXn	t_{R1}	BCX=7Fh	---	5	15	ns
Fall time, SDTO/SCKO	t_{F0}		---	3	10	ns
Fall time, OUTXn	t_{F1}	BCX=7Fh	---	15	25	ns
Propagation delay	t_{D0}	SCKI↑ to SDTO↑↓	10	25	60	ns
	t_{D1}	SCKI↑ to SCKO↑	5	15	40	ns
	$t_{D2(1)}$	SCKO↑ to SDTO↑↓	5	10	20	ns
	t_{D3}	SCKI↑ to OUTRn↑↓, BLANK=0, BCXn=7Fh, OUTTMG=1 or SCKI↓ to OUTRn↑↓, BLANK=0, BCXn=7Fh, OUTTMG=0	10	25	60	ns
	t_{D4}	SCKI↑ to OUTGn↑↓, BLANK=0, BCXn=7Fh, OUTTMG=1 or SCKI↓ to OUTGn↑↓, BLANK=0, BCXn=7Fh, OUTTMG=0	25	50	90	ns
	t_{D5}	SCKI↑ to OUTBn↑↓, BLANK=0, BCXn=7Fh, OUTTMG=1 or SCKI↓ to OUTBn↑↓, BLANK=0, BCXn=7Fh, OUTTMG=0	40	75	120	ns
	$t_{D6(2)}$	Last SCKI↑ to internal latch pulse genaration	8/f_{OSC}	---	16384/ f_{OSC}	sec
Shift clock output one pulse width	$t_{W(SCKO)}$	SCKO↑ to SCKO↓	12	25	35	ns
Internal oscillator frequency	f_{OSC}		6	10	12	MHz

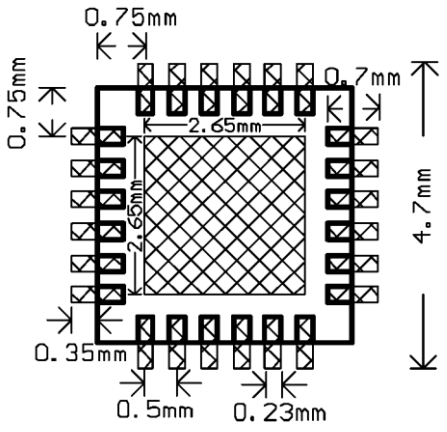
(1) The propagation delays are calculated by $t_{D2}=t_{D0}+t_{D1}$.
(2) The generation timing of the internal latch pulse changes depending on the SCKI clock frequency; see the *Internal Latch Pulse Generation Timing* section.

Pin Description

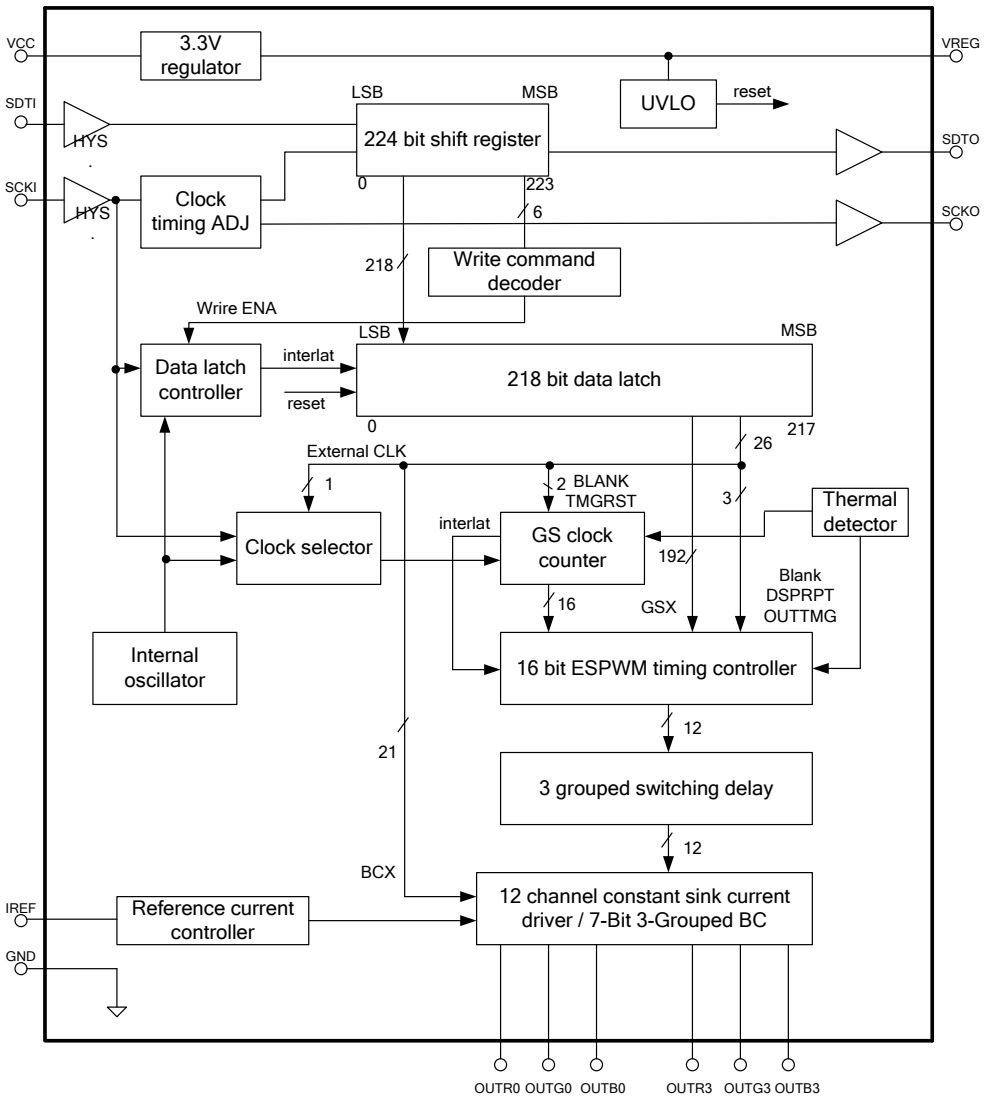
PIN	NAME	I/O	FUNCTION
1	SDTI	I	Serial data input for the 224-bit shift register
2	SCKI	I	Serial data shift clock input. Data present on SDTI are shifted to the LSB of the 224-bit shift register with the SCKI rising edge Data in the shift register are shifted toward the MSB at each SCKI rising edge. The MSB data of the shift register appear on SDTO.
5	SCKO	I/O	Serial data shift clock output. The input shift clock signal from SCKI is adjusted to the timing of the serial data output for SDTO and the signal is then output at SCKO.
6	SDTO	O	Serial data output of the 224-bit shift register. SDTO is connected to the MSB of the 224-bit shift register. Data are clocked out at the SCKI rising edge.
15	VREG	I/O	Internal linear voltage regulator output. A decoupling capacitor of 1 µF must be connected. This output can be used for external devices as a 3.3-V power supply. This terminal can be connected with the VREG terminal of other devices to increase the supply current. Also, this pin can be supplied with 3 V to 5.5 V from an external power supply by connecting it to VCC.
16	IREF	O	Maximum current programming terminal. A resistor connected between IREF and GND sets the maximum current for every constant-current output. The external resistor should be placed close to the device.
19	OUTR0	O	RED constant-current outputs. Multiple outputs can be configured in parallel to increase the constant-current capability. Different voltages can be applied to each output.
22	OUTR1	O	
7	OUTR2	O	
10	OUTR3	O	
20	OUTG0	O	GREEN constant-current outputs. Multiple outputs can be configured in parallel to increase the constant-current capability. Different voltages can be applied to each output.
23	OUTG1	O	
8	OUTG2	O	
11	OUTG3	O	
21	OUTB0	O	BLUE constant-current outputs. Multiple outputs can be configured in parallel to increase the constant-current capability. Different voltages can be applied to each output.
24	OUTB1	O	
9	OUTB2	O	
12	OUTB3	O	
13	VCC	-	Power-supply terminal
-	GND, PowerPAD(PWP)	-	Power ground terminal
18	GND, exposed thermal pad (RGE)	-	
3,4,14,17	NC	-	Not connected

Minimum Footprint PCB Layout Section

QFN4X4-24



Block Diagram



Parametric Measurement Information

Pin Equivalent Input/Output Schematics

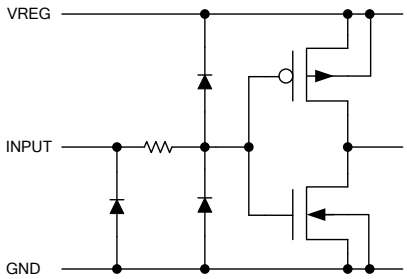


Figure 1. SDTI/SCKI

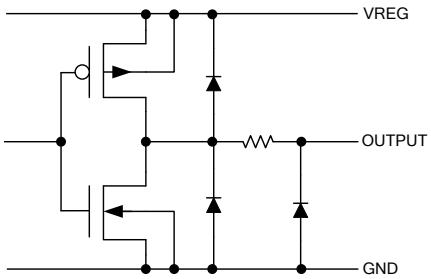


Figure 2. SDTO/SCKO

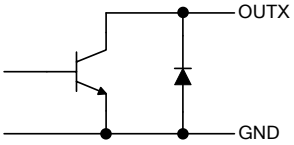


Figure 3. OUTR0 Through OUTB3

Test Circuits

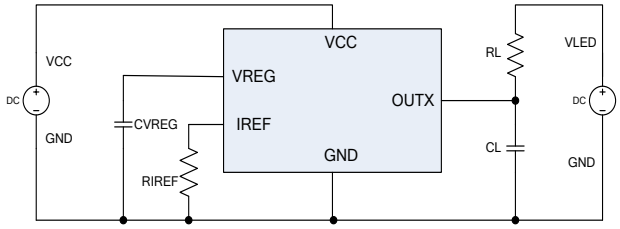


Figure 4. Rise/Fall Time Test Circuit for OUTXn

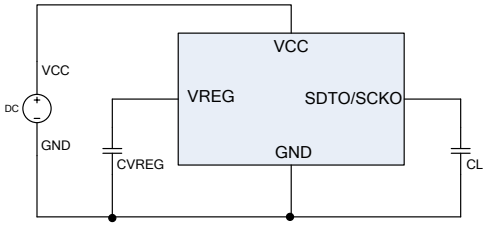


Figure 5. Rise/Fall Time Test Circuit for SDTO/SCKO

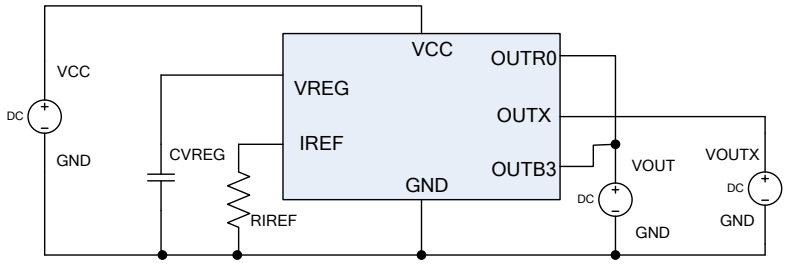
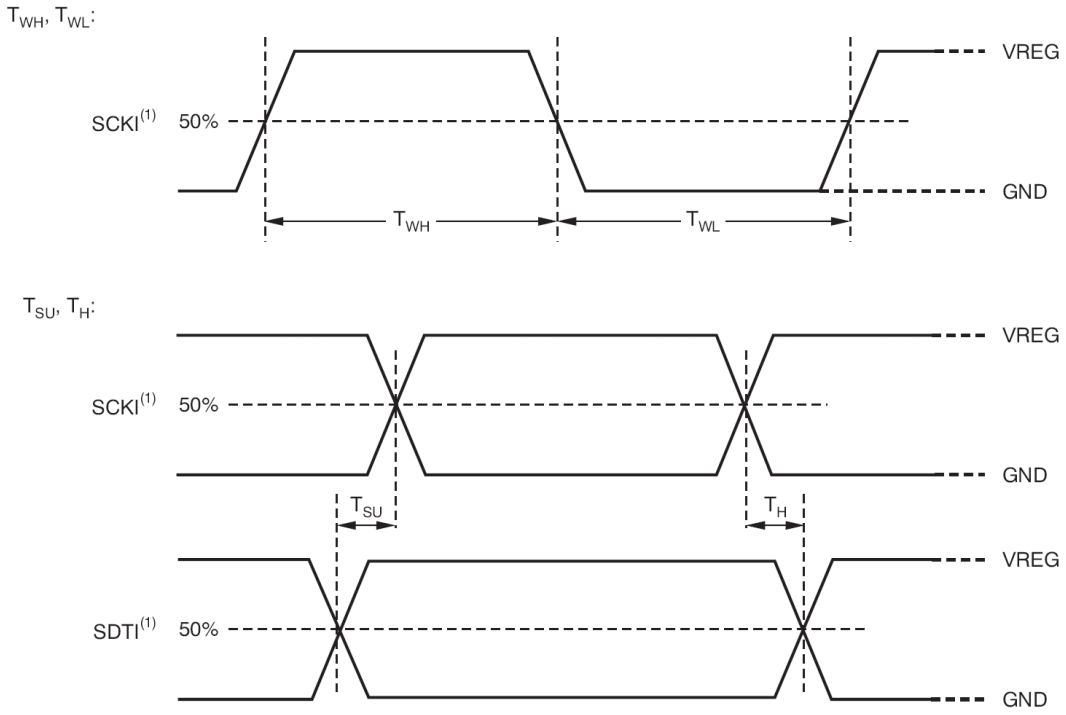


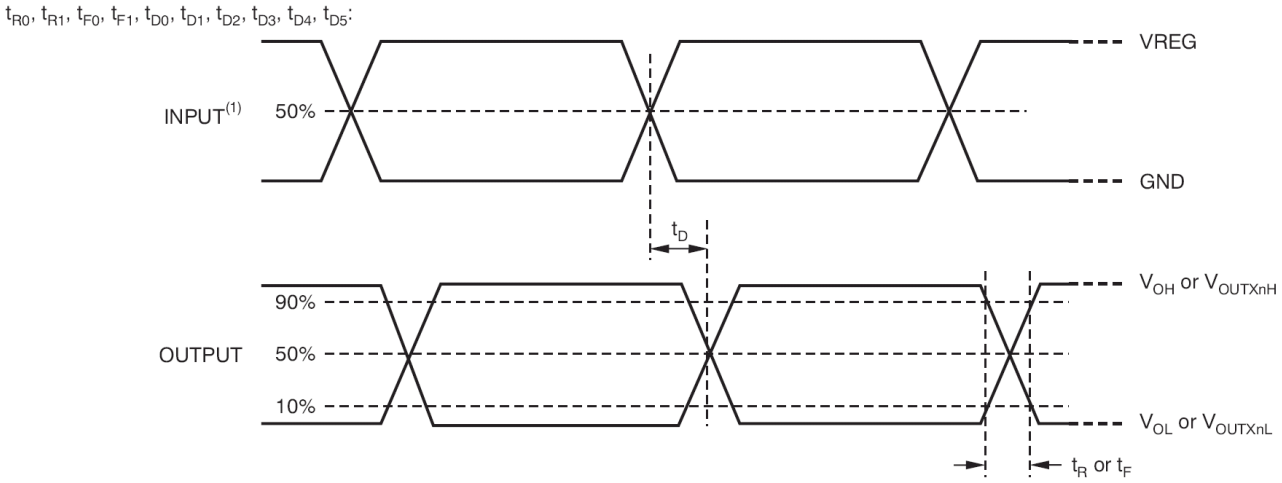
Figure 6. Constant-Current Test Circuit for OUTXn

Timing Diagrams



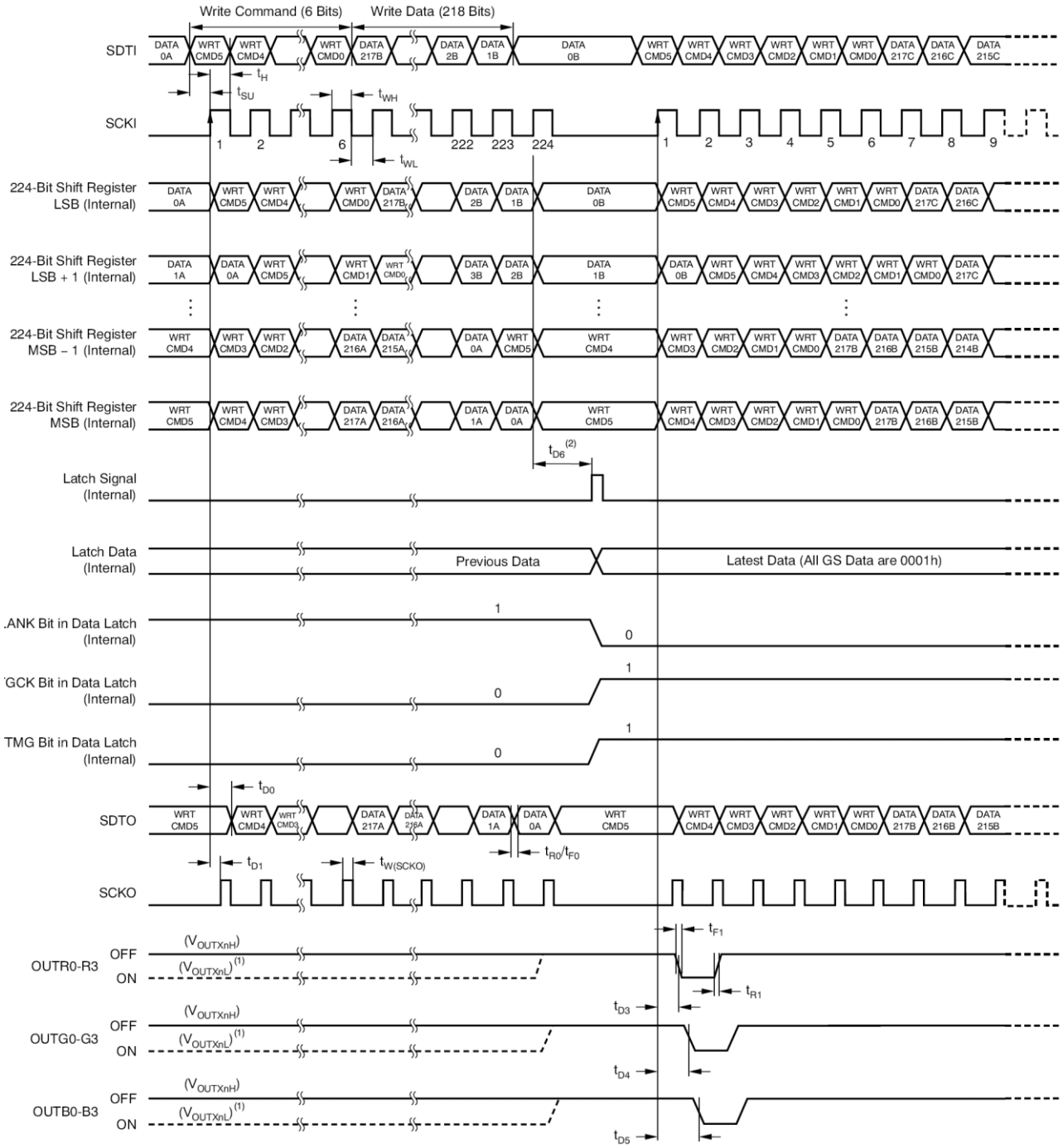
(1) Input pulse rise and fall time is 1ns to 3ns.

Figure 7. Input Timing



(1) Input pulse rise and fall time is 1ns to 3ns.

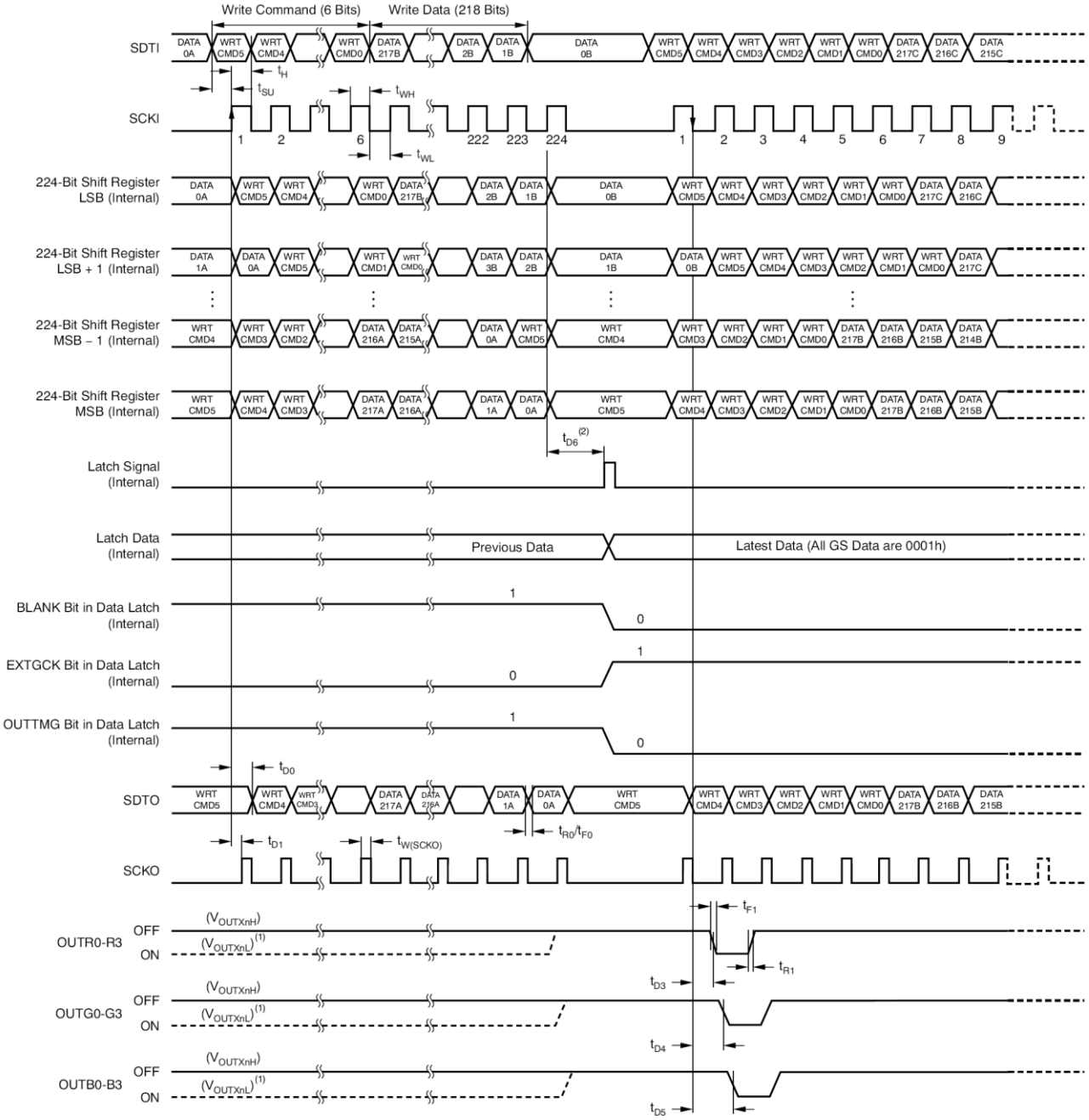
Figure 8. Output Timing



OUTXn on-off timing depends on previous GS data in the 218-bit data latch.

The propagation delay time shows the period from the rising edge of the last SCKI, not the 224th SCKI to the internal latch signal eration.

Figure 9. Data Write and OUTXn Switching Timing (OUTTMG = 1)



(1) OUTXn on-off timing depends on previous GS data in the 218-bit data latch.

(2) The propagation delay time shows the period from the rising edge of the last SCKI, not the 224th SCKI to the internal latch signal generation.

Figure 10. Data Write and OUTXn Switching Timing (OUTTMG = 0)

Application Information

Maximum Constant Sink Current Setting

The maximum constant sink current value for each channel, IOLCMax, is programmed through a single resistor, R_{IREF}, placed between IREF and GND. The desired value can be calculated with Equation 1:

$$R_{IREF}(k\Omega) = \frac{V_{IREF}\ (V)}{I_{OLCMax}\ (mA)} \times 41$$

Where:

V_{IREF} = the internal reference voltage on the IREF pin (1.225V, typically, when the global brightness control data are at maximum),

I_{OLCMax} = 2mA to 60Ma

I_{OLCMax} is the maximum current for each output. Each output sinks the I_{OLCMax} current when it is turned on and global brightness control data (BC) are set to the maximum value of 7Fh (127d).

R_{IREF} must be between 0.837 kΩ and 25.1 kΩ to hold I_{OLCMax} between 60mA (typical) and 2mA (typical).

Otherwise, the output may be unstable. Output currents lower than 2mA can be achieved by setting I_{OLCMax} to 2mA or higher and then using global brightness control to lower th output current. The constant-current sink values for specific external resistor values are shown in Figure 11 and Table 1.

Table 1. Maximum Constant-Current versus External Resistor Value

IOLCMax (mA)	R_{IREF} (kΩ, Typical)
60	0.837
55	0.913
50	1.005
45	1.12
40	1.26
35	1.44
30	1.67
25	2.01
20	2.51
15	3.35
10	5.02
5	10.04
2	25.1

Global Brightness Control (BC) Function (Sink Current Control)

The G5031 has the capability to adjust all output currents of each color group (OUTR0-3, OUTG0-3, and OUTB0-3) to the same current value. This function is called *global brightness (BC) control*. The BC data are seven bits long, which allows each color group output current to be adjusted in 128 steps from 0% to 100% of the maximum output current, IOLCMax. The BC data are set via the serial interface. When the BC data are changed, the output current is changed immediately.

When the IC is powered on, all outputs are forced off by BLANK (bit 213). BLANK initializes in the data latch but the data in the 224-bit shift register and the 218-bit data latch are not set to a default value, except for the BLANK bit. Therefore, BC data must be written to the data latch when BLANK is set to '0'.
Equation 2 determines each color group maximum output sink current:

$$I_{OUT}(mA)=I_{OLCMax}\ (mA)x\left[\frac{BCX}{127d}\right]$$

Where :
I_{OLCMax} = the maximum channel current for each channel determined by R_{IREF}
BC = the global brightness control value in the data latch for the specific color group
(BCX=0d to 127d, X=R/G/B)
Table 2 summarizes the BC data value versus the output current ratio and set current value.

Table 2. BC Data versus Current Ratio and Set Current Value

BC Data(Binary)	BC Data (Decimal)	BC Data (Hex)	Output Current Ratio to I_{OLCMax} (%, Typical)	60mA I_{OLCMax} (mA, Typical)	2mA I_{OLCMax} (mA, Typical)
000 0000	0	00	0	0	0
000 0001	1	01	0.8	0.47	0.02
000 0010	2	02	1.6	0.94	0.03
—	—	—	—	—	—
111 1101	125	7D	98.4	59.06	1.97
111 1110	126	7E	99.2	59.53	1.98
111 1111	127	7F	100	60	2

Grayscale GS Function (PWM Control)

The G5031 can adjust the brightness of each output channel using the enhanced spectrum pulse width modulation (ES-PWM) control scheme. The PWM bit length for each output is 16 bits. The use of the 16 bit length results in 65536 brightness steps from 0% to 100% brightness.

The PWM operation for all color groups is controlled by a 16 bit grayscale (GS) counter. The GS counter increments on each rising or falling edge of the external or internal GS reference clock that is selected by OUTTMG (bit 217) and EXTGCK (bit 216) in the data latch. When the external GS clock is selected, the GS counter uses the SCKI clock as the grayscale clock. The GS counter is reset to 0000h and all outputs are forced off when BLANK (bit 213) is set to '1' in the data latch and the counter value is held at '0' while BLANK is '1', even if the GS reference clock is toggled in between.

Equation 3 calculates each output (OUTXn) total on-time (t_{OUT_ON}):

t_{OUT_ON} (ns) = t_{GSCLK} (ns) GSXn

Where:

t_{GSCLK} = one period of the selected GS reference clock
(internal clock = 100ns typical, external clock = the period of SCKI)
GSXn = the programmed GS value for OUTXn (0d to 65535d) (3)

Table 3 summarizes the GS data values versus the output total on-time and duty cycle. When the IC is powered up, BLANK (bit 213) is set to '1' to force all outputs off; however, the 224 bit shift register and the 218-bit data latch are not set to default values. Therefore, the GS data must be written to the data latch when BLANK (bit 213) is set to '0'.

Table 3. Output Duty Cycle and Total On-Time versus GS Data

GS DATA (decimal)	GS DATA (hex)	ON-TIME DUTY (%)	GS DATA (decimal)	GS DATA (hex)	ON-TIME DUTY (%)
0	0	0	32768	8000	50.001
1	1	0.002	32769	8001	50.002
2	2	0.003	32770	8002	50.004
3	3	0.005	32771	8003	50.005
—	—	—	—	—	—
8191	1FFF	12.499	40959	9FFF	62.499
8192	2000	12.5	40960	A000	62.501
8193	2001	12.502	40961	A001	62.502
—	—	—	—	—	—
16383	3FFF	24.999	49149	BFFF	74.997
16384	4000	25	49150	C000	74.998
16385	4001	25.002	49151	C001	75
—	—	—	—	—	—
24575	5FFF	37.499	57343	DFFF	87.5
24576	6000	37.501	57344	E000	87.501
24577	6001	37.502	57345	E001	87.503
—	—	—	—	—	—
32765	7FFD	49.996	65533	FFFD	99.997
32766	7FFE	49.998	65534	FFFE	99.998
32767	7FFF	49.999	65535	FFFF	100

Enhanced Spectrum (ES) PWM Control

Enhanced spectrum (ES) PWM has the total display period divided into 128 display segments. The total display period refers the period between the first grayscale clock input to the 65536th grayscale clock input after BLANK (bit 213) is set to '0'. Each display period has 512 grayscale values, maximum. Each output on-time changes depending on the grayscale data. Refer to Table 4 for sequence information and Figure 23 for timing information.

Table 4. ES-PWM Drive Turn-On Time Length

GS DATA (dec)	GS DATA (hex)	OUTn DRIVER OPERATION
0	0000h	Does not turn on
1	0001h	Turns on during one GS clock period in the 1st display period
2	0002h	Turns on during one GS clock period in the 1st and 65th display period
3	0003h	Turns on during one GS clock period in the 1st, 33rd, and 65th display period
4	0004h	Turns on during one GS clock period in the 1st, 33rd, 65th, and 97th display period
5	0005h	Turns on during one GS clock period in the 1st, 17th, 33rd, 65th, and 97th display period
6	0006h	Turns on during one GS clock period in the 1st, 17th, 33rd, 65th, 81st, and 97th display period
—	—	The number of display periods that OUTXn is turned on during one GS clock is incremented by the GS data increasing in the following order. The order of display periods that the output turns on are: 1, 65, 33, 97, 17, 81, 49, 113, 9, 73, 41, 105, 25, 89, 57, 121, 5, 69, 37, 101, 21, 85, 53, 117, 13, 77, 45, 109, 29, 93, 61, 125, 3, 67, 35, 99, 19, 83, 51, 115, 11, 75, 43, 107, 27, 91, 59, 123, 7, 71, 39, 103, 23, 87, 55, 119, 15, 79, 47, 111, 31, 95, 63, 127, 2, 66, 34, 98, 18, 82, 50, 114, 10, 74, 42, 106, 26, 90, 58, 122, 6, 70, 38, 102, 22, 86, 54, 118, 14, 78, 46, 110, 30, 94, 62, 126, 4, 68, 36, 100, 20, 84, 52, 116, 12, 76, 44, 108, 28, 92, 60, 124, 8, 72, 40, 104, 24, 88, 56, 120, 16, 80, 48, 112, 32, 96, 64, and 128.
127	007Fh	Turns on during one GS clock period in the 1st to 127th display period, but does not turn on in the 128th display period
128	0080h	Turns on during one GS clock period in all display periods (1st to 128th)
129	0081h	Turns on during two GS clock periods in the 1st display period and one GS clock period in the next display period
—	—	The number of display periods where OUTn is turned on for two GS clocks is incremented by the increased GS data similar to the previous case where the GS value is 1 trough 127
255	00FFh	Turns on during two GS clock periods in the 1st to 127th display period, but only turns on during one GS clock period in the 128th display period
256	0100h	Turns on during two GS clock periods in all display periods (1st to 128th)
257	0101h	Turns on during three GS clock periods in the 1st display period and two GS clock periods in the next display period
—	—	Display periods with OUTn turned on is incremented by the increased GS data similar to 0101h operation
65478	FEFFh	Turns on during 511 GS clock periods in the 1st to 127th display period, but only turns on 510 GS clock periods in the 128th display period
65280	FF00h	Turns on during 511 GS clock periods in all display periods (1st to 128th)
65281	FF01h	Turns on during 512 GS clock periods in the 1st display period and 511 GS clock periods in the 2nd to 128th display periods
—	—	—
65534	FFFEh	Turns on during 512 GS clock periods in the 1st to 63th and 65th to 127th display periods, and turns on 511 GS clock periods in the 64th and 128th display periods
65535	FFFFh	Turns on during 512 GS clock periods in the 1st to 127th display period, but only turns on 511 GS clock periods in the 128th display period

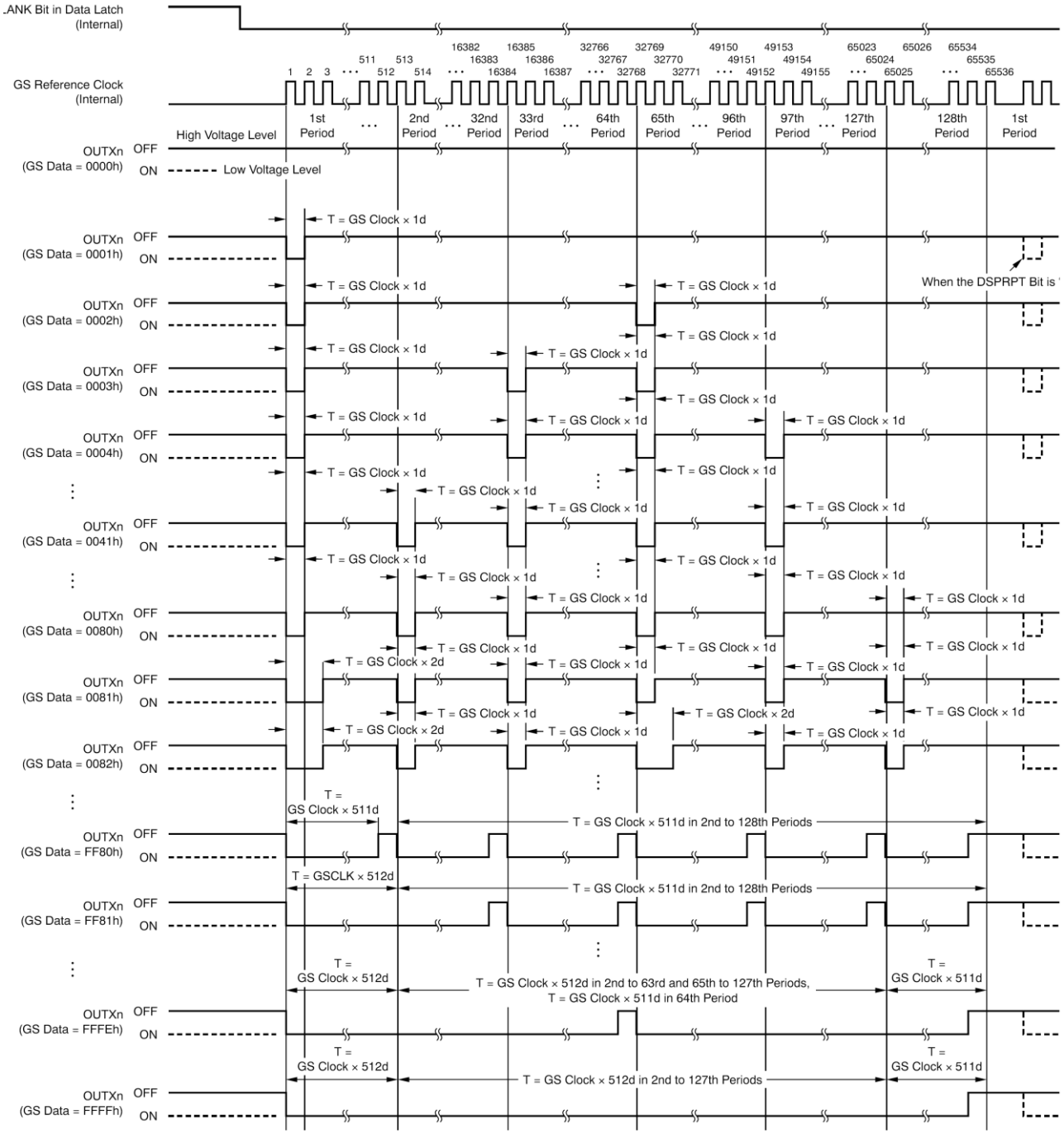


Figure 23. ES-PWM Operation

Register and Data Latch Configuration

The G5031 has a 224bit shift register and a 218 bit data latch that set grayscale (GS) data, global brightness control (BC), and function control (FC) data into the device. When the internal latch pulse is generated and the data of the six MSBs in the shift register are 25h, the 218 following data bits in the shift register are copied into the 218 bit data latch. If the data of the six MSBs is not 25h, the 218 data bits are not copied into the 218 bit data latch. The data in the data latch are used for GS, BC, and FC functions. Figure 24 shows the shift register and the data latch configuration.

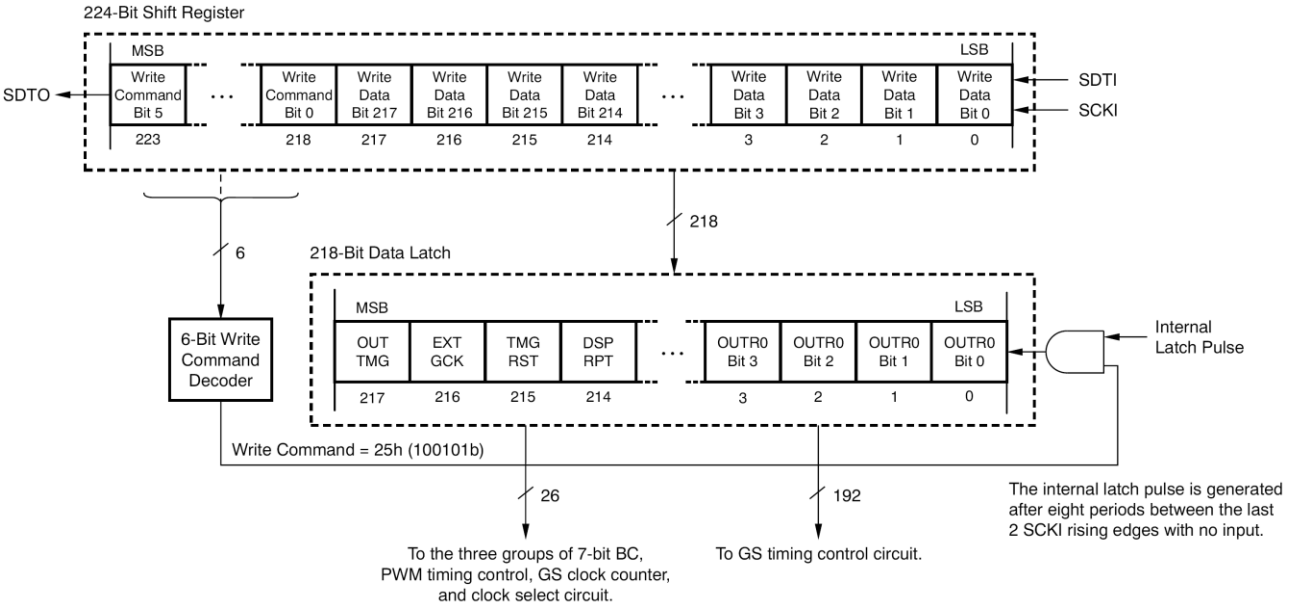


Figure 24. Common Shift Register and Control Data Latch Configuration

224 Bit Shift Register

The 224 bit shift register is used to input data from the SDTI pin with the SCKI clock into the G5031. The shifted data in this register is used for GS, BC, and FC. The six MSBs are used for the write command. The LSB of the register is connected to the SDTI pin and the MSB is connected to the SDTO pin. On each SCKI rising edge, the data on SDTI are shifted into the register LSB and all 224 bits are shifted towards the MSB. The register MSB is always connected to SDTO. When the device is powered up, the data in the 224 bit shift register is not set to any default value.

218 Bit Data Latch

The 218 bit data latch is used to latch the GS, BC, and FC data. The 218 LSBs in the 244 bit shift register are copied to the data latch when the internal latch pulse is generated with the 6-bit write command, 25h (100101b). When the device is powered up, the data in the latch are not reset except for BLANK (bit 213) which is set to '1' to force all outputs off. Therefore, GS, BC, and FC data must be set to the proper values before BLANK is set to '0'. The 218 bit data latch configuration is shown in Figure 25 and the data bit assignment is shown in Table 5.

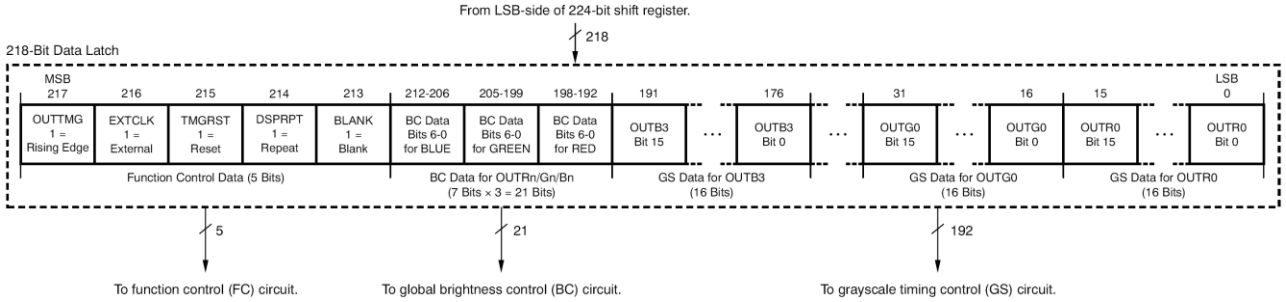


Figure 25. 218 Bit Data Latch Configuration

Table 5. Data Latch Bit Assignment

BIT NUMBER	BIT NAME	CONTROLLED CHANNEL/FUNCTIONS
15-0	GSR0	GS data bits 15 to 0 for OUTR0
31-16	GSG0	GS data bits 15 to 0 for OUTG0
47-32	GSB0	GS data bits 15 to 0 for OUTB0
63-48	GSR1	GS data bits 15 to 0 for OUTR1
79-64	GSG1	GS data bits 15 to 0 for OUTG1
95-80	GSB1	GS data bits 15 to 0 for OUTB1
111-96	GSR2	GS data bits 15 to 0 for OUTR2
127-112	GSG2	GS data bits 15 to 0 for OUTG2
143-128	GSB2	GS data bits 15 to 0 for OUTB2
159-144	GSR3	GS data bits 15 to 0 for OUTR3
175-160	GSG3	GS data bits 15 to 0 for OUTG3
191-176	GSB3	GS data bits 15 to 0 for OUTB3
198-192	BCR	BC data bits 6 to 0 for OUTR0-3
205-199	BCG	BC data bits 6 to 0 for OUTG0-3
212-206	BCB	BC data bits 6 to 0 for OUTB0-3
213	BLANK	Constant-current output enable bit in FC data (0 = output control enabled, 1 = blank). When this bit is '0', all constant-current outputs (OUTR0-OUTB3) are controlled by the GS PWM timing controller. When this bit is '1', all constant-current outputs are forced off. The GS counter is reset to '0', and the GS PWM timing controller is initialized. When the IC is powered on, this bit is set to '1'.
214	DSPRPT	Auto display repeat mode enable bit in FC data (0 = disabled, 1 = enabled). When this bit is '0', the auto repeat function is disabled. Each constant-current output is only turned on once, according the GS data after BLANK is set to '0' or after the internal latch pulse is generated with the TMGRST bit set to '1'. When this bit is '1', each output turns on and off according to the GS data every 65536 GS reference clocks.
215	TMGRST	Display timing reset mode enable bit in FC data (0 = disabled, 1 = enabled). When this bit is '1', the GS counter is reset to '0' and all constant-current outputs are forced off when the internal latch pulse is generated for data latching. This function is the same when BLANK is set to '0'. Therefore, BLANK does not need to be controlled by an external controller when this mode is enabled. When this bit is '0', the GS counter is not reset and no output is forced off even if the internal latch pulse is generated.
216	EXTGCK	GS reference clock select bit in FC data (0 = internal oscillator clock, 1 = SCKI clock). When this bit is '1', PWM timing refers to the SCKI clock. When this bit is '0', PWM timing refers to the internal oscillator clock.
217	OUTTMG	GS reference clock edge select bit for OUTXn on-off timing control in FC data (0 = falling edge, 1 = rising edge). When this bit is '1', OUTXn are turned on or off at the rising edge of the selected GS reference clock. When this bit is '0', OUTXn are turned on or off at the falling edge of the selected clock.

Internal Latch Pulse Generation Timing

The internal latch pulse is generated when the SCKI rising edge does not change for 8x the period between the last SCKI rising edge and the second to last SCKI rising edge if the data of the six MSBs in the 244 bit shift register are the command code 25h. The generation timing changes as a result of the SCKI frequency with the time range between 16384 times the internal oscillator period (2.74ms), maximum, and 8x the internal oscillator period (666 ns), minimum. Figure 26 shows the internal latch pulse generation timing.

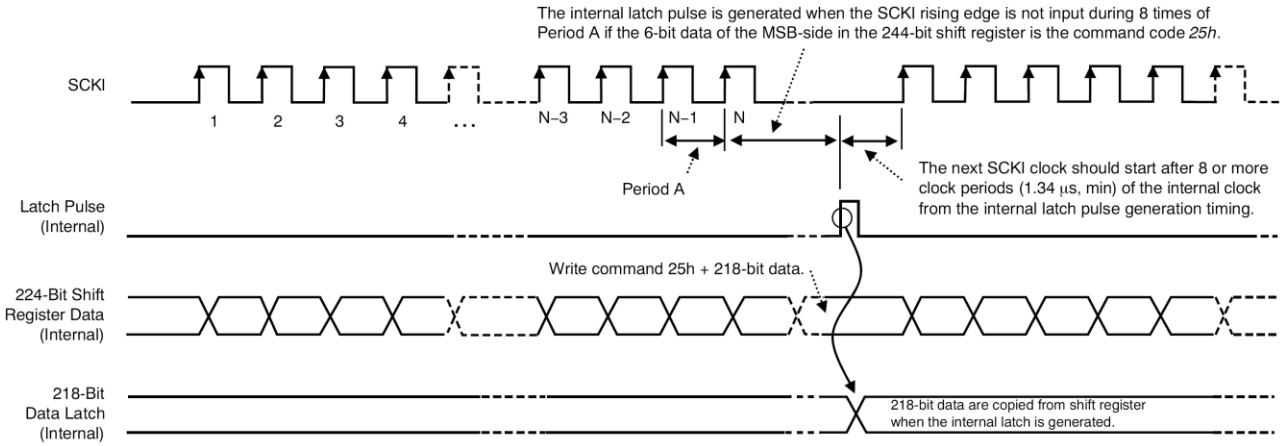


Figure 26. Data Latch Pulse Generation Timing

Auto Display Repeat Function

This function repeats the total display period without a BLANK bit change, as long as the GS reference clock is available. This function can be enabled or disabled with DSPRPT (bit 214) in the data latch. When the DSPRPT bit is '1', this function is enabled and the entire display period repeats without a BLANK bit data change. When the DSPRPT bit is '0', this function is disabled and the entire display period executes only once after the BLANK bit is set to '0' or the internal latch pulse is generated when the display timing reset function is enabled. Figure 27 shows the auto display repeat operation timing.

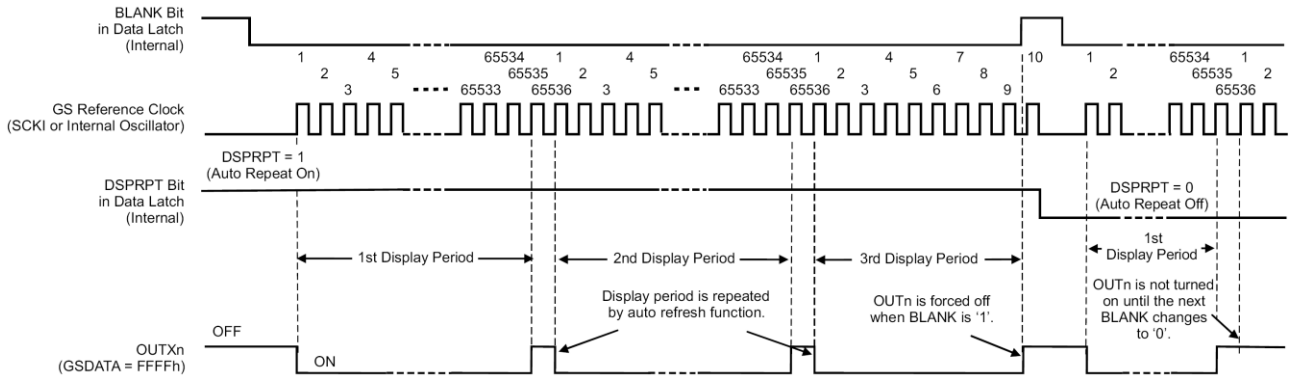


Figure 27. Auto Repeat Display Function

Display Timing Reset Function

This function allows the display timing to be initialized using the internal latch pulse, as shown in Figure 28. This function can be enabled or disabled by TMGRST (bit 215) in the data latch. When the TMGRST bit is '1', the GS counter is reset to '0' and all outputs are forced off when the internal latch pulse is generated. This function is the same when the BLANK bit changes (such as from '0' to '1' and from '1' to '0'). Therefore, the BLANK bit does not need to be controlled from an external controller to restart the PWM control from the next GS reference clock rising edge. When this bit is '0', the GS counter is not reset and no output is forced off even if the internal latch pulse is generated. Figure 28 shows the display timing reset operation.

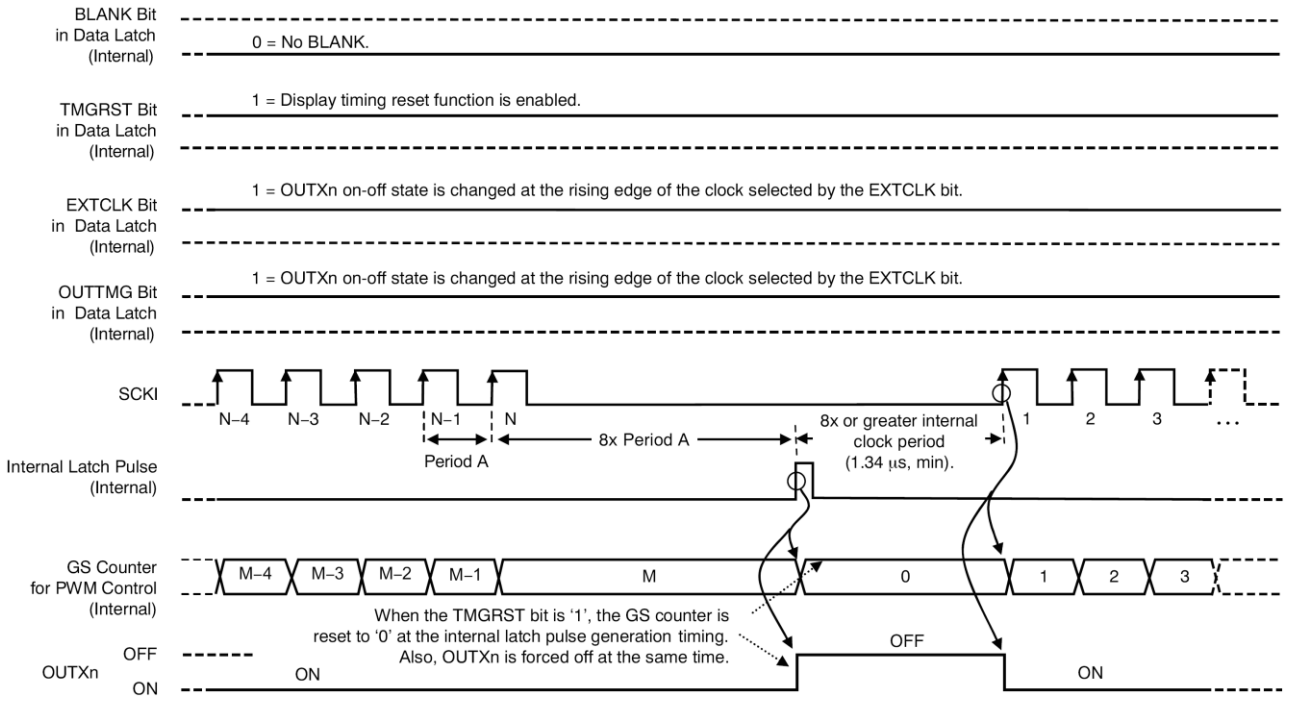


Figure 28 Display Timing Reset Function

Output Timing Select Function

This function selects the on-off change timing of the constant-current outputs (OUTXn) set by OUTTMG (bit 217) in the data latch. When this bit is '1', OUTXn are turned on or off at the rising edge of the selected GS reference clock. When this bit is '0', OUTXn are turned on or off at the falling edge of the selected clock. Electromagnetic interference (EMI) of the total system can be reduced using this bit setting. For example, when the odd number of devices in the system have this bit set to '0' and the even number of devices in the system have this bit set to '1', EMI is reduced because the devices change the OUTXn status at a deferent timing. Figure 29 and Figure 30 show the output switching timing when the OUTTMG bit is '1' and '0', respectively.

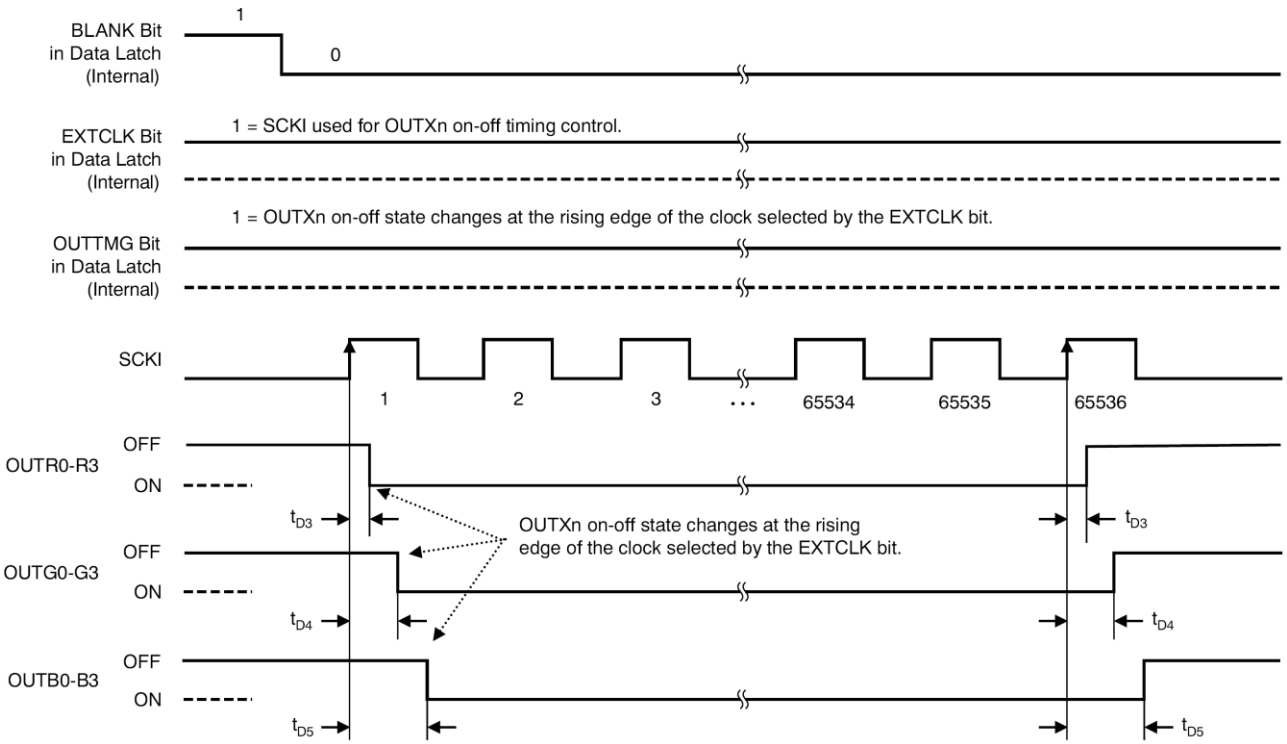


Figure 29. Output On-Off Timing with Four-Channel Grouped Delay (OUTTMG=1)

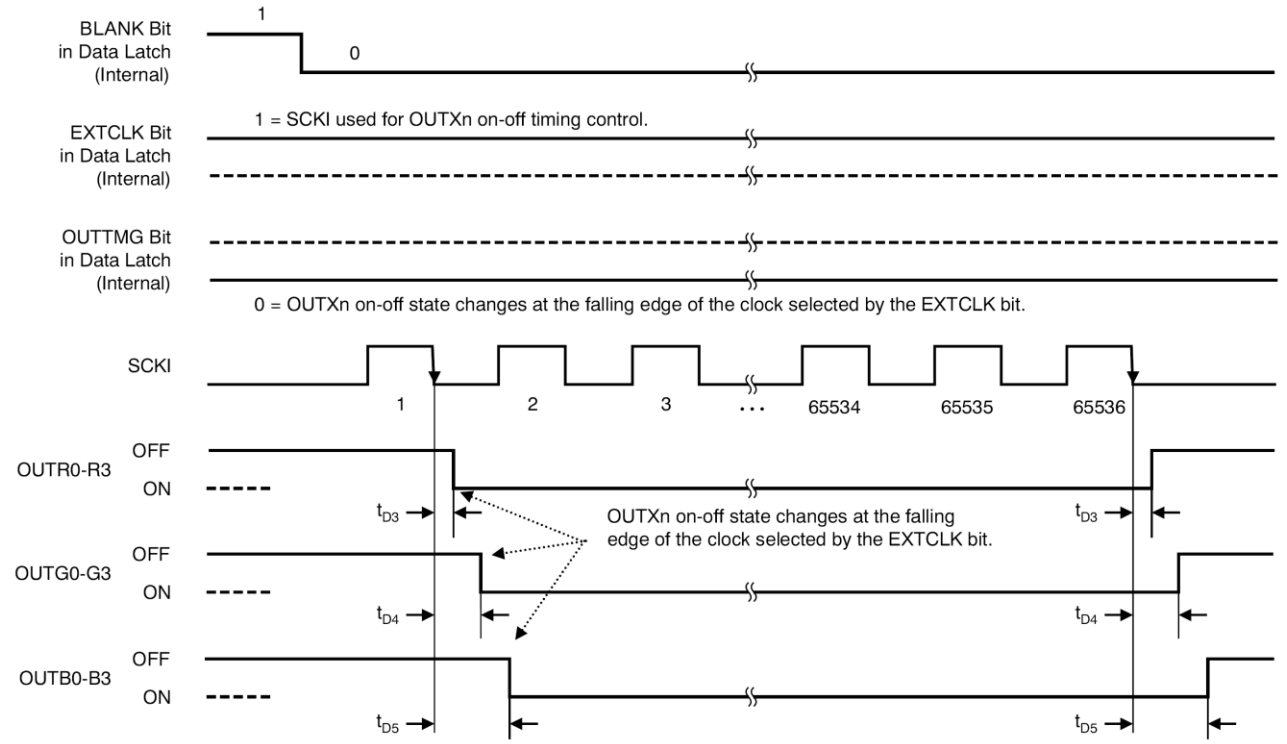


Figure 30. Output On-Off Timing with Four-Channel Grouped Delay (OUTTMG=0)

Thermal Shutdown

The thermal shutdown (TSD) function turns off all IC constant-current outputs when the junction temperature (T_J) exceeds the threshold (T_{TSD} = +145°C, typ). When the junction temperature drops below (T_{TSD} – T_{HYS}), the output control starts at the first GS clock in the next display period.

Noise Reduction

Large surge currents may flow through the IC and the board if all 12 outputs turn on simultaneously at the start of each GS cycle. These large current surges could induce detrimental noise and EMI into other circuits. The G5031 turns on the outputs for each color group independently with a 25 ns (typ) rise time. The output current sinks are grouped into three groups. The first group that is turned on/off are OUTR0-3; the second group that is turned on/off are OUTG0-3; and the third group is OUTB0-3. However, the state of each output is controlled by the selected GS clock; see the *Output Timing Select Function* section.

How to Control the G5031

To set each function mode, BC color, GS output, 6 bit write command, 5 bit FC data, 21 bit BC data for each color group, and 192 bit GS data for OUTXn, a total number of 224 bits must be written into the device. Figure 31 shows the 224 bit data packet configuration.

When *N* units of the G5031 are cascaded (as shown in Figure 32), N × 224 bits must be written from the controller into the first device to control all devices. The number of cascaded devices is not limited as long as the proper voltage is supplied to the device at VCC. The packets for all devices must be written again whenever the data in one packet is changed.

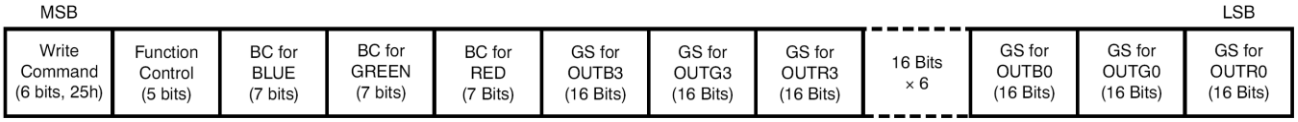


Figure 31. 224 Bit Data Packet Configuration

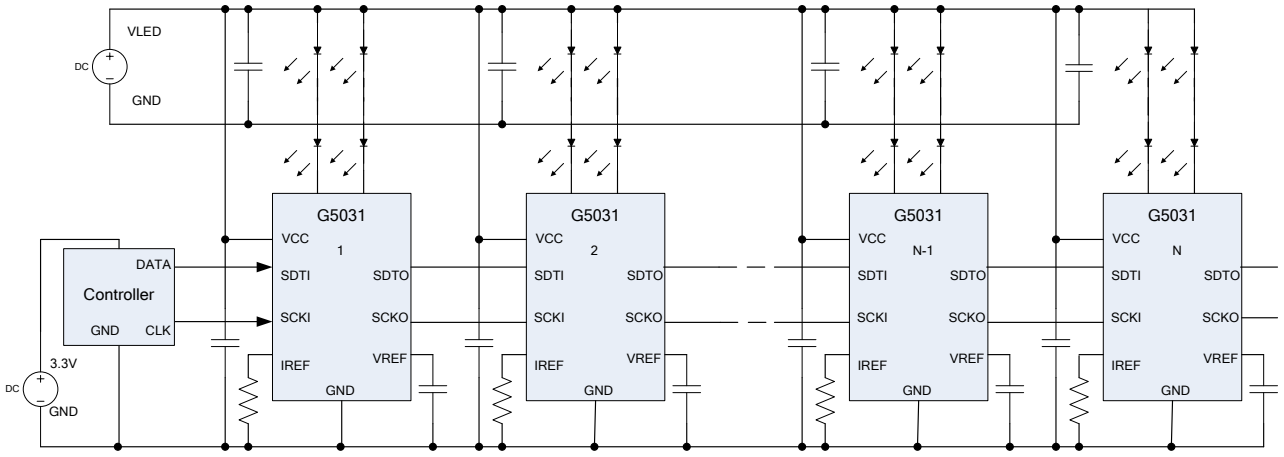


Figure 32. Cascading Connection of N G5031 Units

Data Write and PWM Control with Internal Grayscale Clock Mode

When the EXTCLK bit is '0', the internal oscillator clock is used for PWM control of OUTXn (X = R/G/B and n = 03) as the GS reference clock. This mode is ideal for illumination applications that change the display image at low frequencies. The data and clock timing is shown in Figure 9 and Figure 33. A writing procedure for the function setting and display control follows:

1. Power up VCC (VLED); all OUTXn are off because BLANK is set to '1'.
2. Write the 224 bit data packet (with MSB bit first) for the Nth G5031 using the SDTI and SCKI signals.
   The first six bits of the 224 bit data packet are used as the write command. The write command must be 25h (100101b); otherwise, the 218 bit data in the 224 bit shift register are not copied to the 218 bit data latch. The EXTCLK bit must be set to '0' for the internal oscillator mode. Also, the DSPRPT bit should be set to '1' to repeat the PWM timing control and BLANK set to '0' to start the PWM control.
3. Write the 224 bit data packet for the (N – 1) G5031 without delay after step 2.
4. Repeat the data write sequence until all G5031s have data. The total shift clock count (SCKI) is now 224 × N. After all device data are written, stop the SCKI at a high or low level for 8× the period between the last SCKI rising edge and the second to last SCKI rising edge. Then the 218 LSBs in the 224 bit shift resister are copied to the 218 bit data latch in all devices and the PWM control is started or updated at the same time.

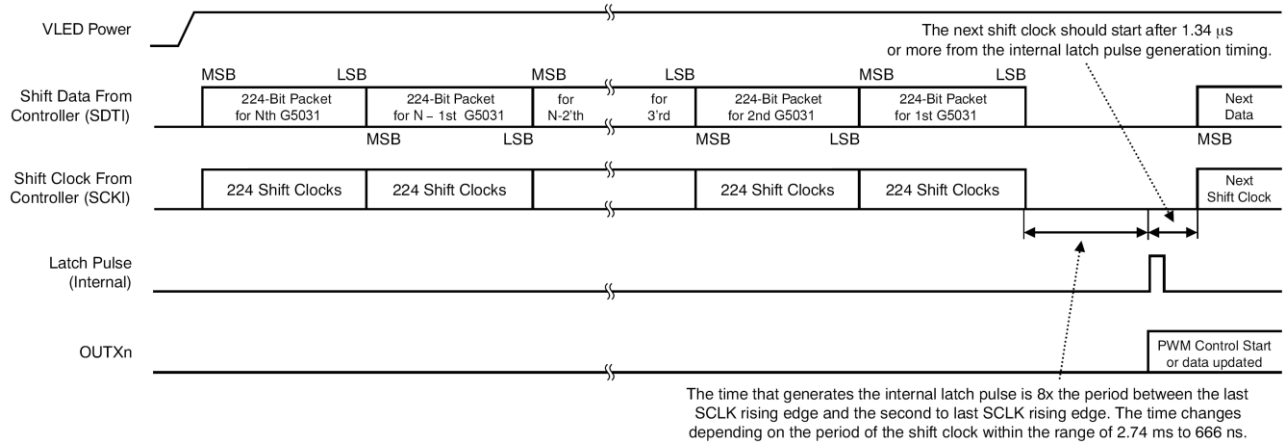


Figure 33. Data Packet and Display Start/Update Timing 1 (Internal Oscillator Mode)

Data Write and PWM Control with External Grayscale Clock Mode

When the EXTCLK bit is '1', the data shift clock (SCKI) is used for PWM control of OUTXn (X = R/G/B and n = 03) as the GS reference clock. This mode is ideal for video image applications that change the display image with high frequencies or for certain display applications that must synchronize all G5031s. The data and clock timing are shown in Figure 9 and Figure 34. A writing procedure for the display data and display timing control follows:

1. Power-up VCC (VLED); all OUTXn are off because BLANK is set to '1'.
2. Write the 224 bit data packet MSB-first for the Nth G5031 using the SDTI and SCKI signals. The first six bits of the 224 bit data packet are used as the write command. The write command must be 25h (100101b); otherwise, the 218 bit data in the 224 bit shift register are not copied to the 218 bit data latch. The EXTCLK bit must be set to '1' for the external oscillator mode. Also, the DSPRPT bit should be set to '0' so that the PWM control is not repeated, the TMGRST bit should be set to '1' to reset the PWM control timing at the internal latch pulse generation, and BLANK must be set to '0' to start the PWM control.
3. Write the 224 bit data for the (N – 1) G5031 without delay after step 2.
4. Repeat the data write sequence until all G5031s have data. The total shift clock count (SCKI) is 224 × N. After all device data are written, stop the SCKI at a high or low level for 8× the period between the last SCKI rising edge and the second to last SCKI rising edge. Then the 218 LSBs in the 224 bit shift resister are copied to the 218 bit data latch in all devices.
5. To start the PWM control, send one pulse of the SCKI clock with SDTI low after 1.34µs or more from step 4. The OUTXn are turned on when the output GS data are not 0000h.
6. Send the remaining 65535 SCKI clocks with SDTI low. Then the PWM control for OUTXn is synchronized with the SCKI clock and one display period is finished with a total of 65536 SCKI clock periods.
7. Repeat step 2 to step 6 for the next display period.

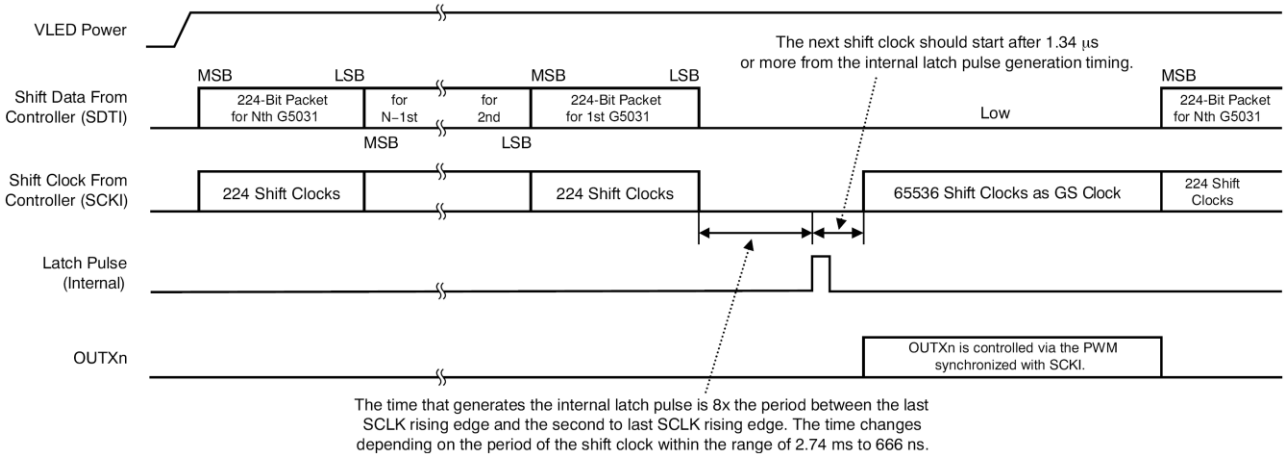


Figure 34. Data Packet and Display Start/Update Timing 2 (External Clock Mode)

There is another control procedure that is recommended for a long chain of cascaded devices. The data and clock timings are shown in Figure 9 and Figure 35. When 256 G5031 units are cascaded, use the following procedure:

1. Power up VCC (VLED); all OUTXn are off because BLANK is set to '1'.
2. Write the 224bit data packet MSB-first for the 256th G5031 using the SDTI and SCKI signals. The EXTCLK bit must be set to '1' for the external oscillator mode. Also, the DSPRPT bit should be set to '0' so that the PWM control does not repeat, the TMGRST bit should be set to '1' to reset the PWM control timing with the internal latch pulse, and BLANK must be set to '0' to start the PWM control.
3. Repeat the data write sequence for all G5031s. The total shift clock count (SCKI) is 57344 (224 × 256). After all device data are written, stop the SCKI signal at a high or low level for eight or more periods between the last SCKI rising edge and the second to last SCKI rising edge. Then the 218 LSBs in the 224 bit shift resister are copied to the 218 bit data latch in all devices.
4. To control the PWM, send 8192 SCKI clock periods with SDTI low after 1.34μs or more from step 3 (or step 7). These 8192 clock periods are used for the OUTXn PWM control.
5. Write the new 224 bit data packets to the 256th to first G5031s for the next display with 256 × 224 SCKI clock for a total of 57344 clocks. The PWM control for OUTXn remains synchronized with the SCKI clock and one display period is finished with a total of 65536 SCKI clocks. The SCKI clock signal is therefore used for PWM control and, at the same time, to write data into the shift registers of all cascaded parts.
6. Stop the SCKI signal at a high or low level for eight or more periods between the last SCKI rising edge and the second to last SCKI rising edge. Then the 218-bit LSBs in the 224 bit shift resister are copied to the 218bit data latch in all devices.
7. Repeat step 4 to step 6 for the next display periods.

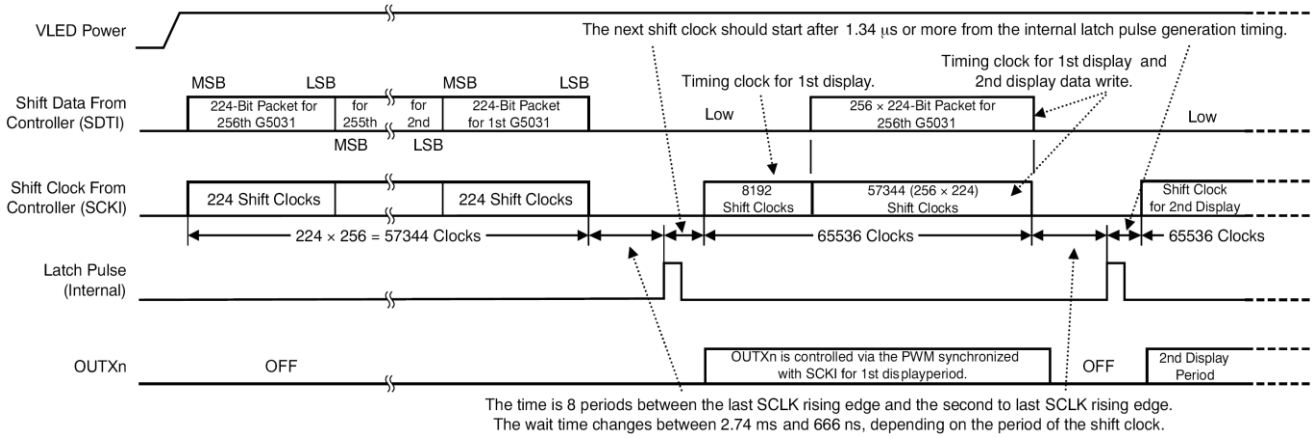
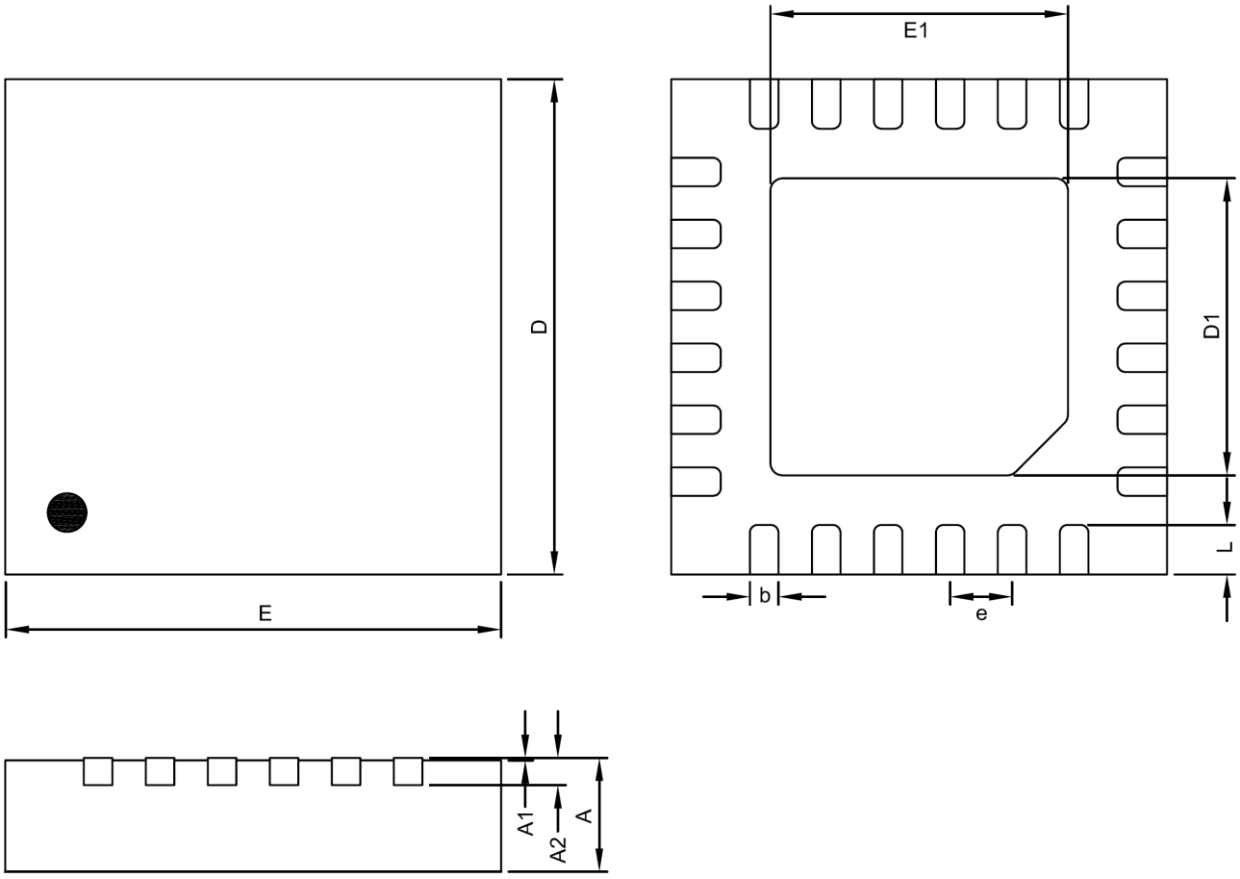


Figure 35. Data Packet and Display Start/Update Timing 3
(External Clock Mode with 256 Cascaded Devices)

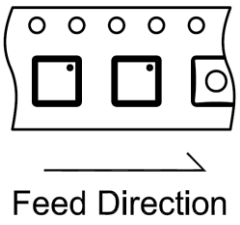
Package Information



QFN4X4-24 Package

Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.90	1.00	0.0315	0.0354	0.0394
A1	0.00	- - -	0.05	0.0000	- - -	0.0020
A2	0.20 REF			0.0079 REF		
D	3.95	4.00	4.05	0.1555	0.1575	0.1594
E	3.95	4.00	4.05	0.1555	0.1575	0.1594
D1	2.50	2.65	2.80	0.0984	0.1043	0.1102
E1	2.50	2.65	2.80	0.0984	0.1043	0.1102
b	0.18	0.23	0.30	0.0071	0.0091	0.0118
e	0.50 BSC			0.0197 BSC		
L	0.35	0.40	0.45	0.0138	0.0157	0.0177

Taping Specification



PACKAGE	Q'TY/REEL
QFN4X4-24	3,000 ea