G5288B

5V Electronic Fuse

Features

- **1A-7A Programmable-Current Limit**
- **N-channel on-resistance (typ): 40 mΩ**
- **En/Fault functions**
- **Output clamp voltage (typ):5.85V**
- **Internal undervoltage lockout**
- **Short-circuit limit**
- **Controlled output voltage ramp**
- **Programmable soft start function**
- **Thermal latch (typ): 165 °C**
- **Operating junction temp. - 40 °C to 125 °C**
- **Available in DFN10 (3x3 mm) package**

Applications

- **Hard disk drives**
- **Solid state drives (SSD)**
- **DVD and Blue-ray disc drivers**
- **Mother Board Power Management**

General Description

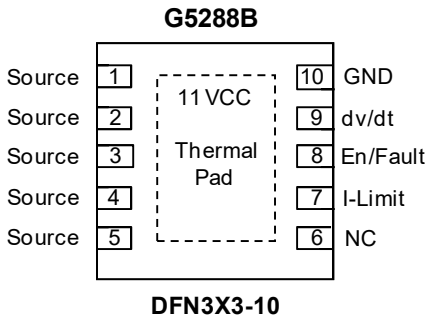
The G5288B is an integrated, cost-effective, electronic fuse optimized for monitoring output current and input voltage. Connected in series to a 5V power-rail, it is capable of protecting the electronic circuitry on its output from over current and overvoltage during output load transient and input voltage transient. If a continuous short-circuit is present on the board, when power is re-applied, G5288B initially limits the output current to a safe value to lower the power on G5288B and a thermal protection circuit is integrated as well. There is no degradation on G5288B after short-circuit/thermal protection events and it is reset either by recycling the supply voltage or using the En/Fault pin. G5288B also has a programmable delay to control turn on time.

Ordering Information

ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE (Green)
G5288BQE1U	5288B	-40°C~ +125°C	DFN3X3-10

Note: QE: DFN3X3-10
1: Bonding Code
U: Tape & Reel
Green : Lead Free / Halogen Free

Pin Configuration



DFN3X3-10

Note: Thermal Pad is the VCC Pin.

Absolute Maximum Ratings

VCC, Source, I_Limit . . . . . .-0.3V to +21V
En/Fault. . . . . -0.3V to +7V
dv/dt . . . . . .-0.3V to +7V
Operating junction temperature range(1)
. . . . . .-40°C to 125°C
Storage Temperature Range . . . . . .-65°C to 150°C
Lead temperature (soldering) 10 sec. . . . . 260°C
ESD (HBM). 2kV
ESD (CDM) 500V

(1) The thermal limit is set above the maximum thermal rating. It is not recommended to operate the device at temperatures greater than the maximum ratings for extended periods of time.

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

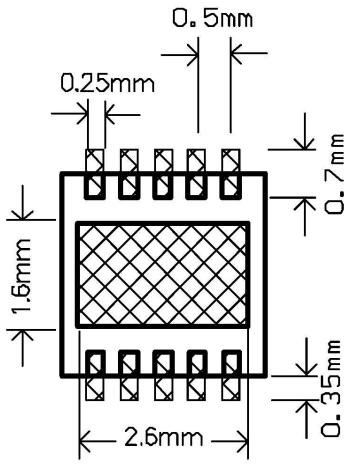
Thermal Information

THERMAL METRIC		DFN3X3-10	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance	57.5	°C/W
$R_{\theta JC\_top}$	Junction to case top thermal resistance	65.3	°C/W
$R_{\theta JB}$	Junction to board thermal resistance	27.0	°C/W
Ψ_{JT}	Junction to top characterization parameter	7.7	°C/W
Ψ_{JB}	Junction to board characterization parameter	27.1	°C/W
$R_{\theta JC\_bot}$	Junction to case bottom thermal resistance	6.0	°C/W

1. Package thermal metric is obtained using the method described in JEDEC specification JESD51-7, using a four-layer board.
2. The maximum power dissipation is $P_{D(MAX)} = \frac{(T_{JMAX} - T_A)}{R_{\theta JA}}$, Exceeding the maximum allowable power dissipation results in excessive die temperature, and the device will enter thermal shutdown.

Minimum Footprint PCB Layout Section

DFN3X3-10



Electrical Characteristics

(V_{CC} =5V, $V_{En/Fault}$ =3.3V, C_I =10µF, C_O =47µF, T_J =25°C.

The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified.

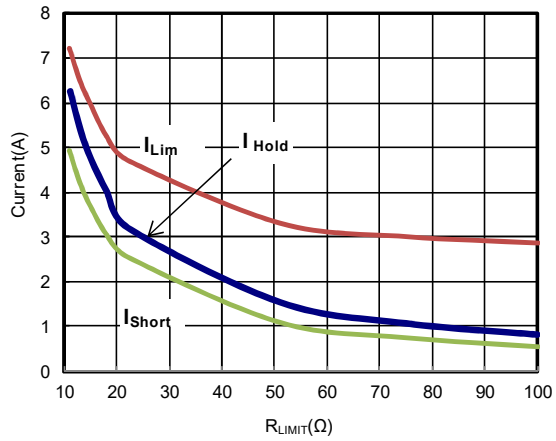
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Under/Overvoltage protection						
Output clamping voltage	V_{Clamp}	V_{CC}=8V	5.5	5.85	6	V
Under voltage lockout	V_{UVLO}	Turn-on, voltage rising	2.5	2.7	2.9	V
UVLO hysteresis	V_{Hyst}		---	0.15	---	V
Power MOSFET						
Delay time	T_{DLY}	Enabling of chip to I_D = 100mA with an 1A resistive load	---	500	---	µs
ON resistance	R_{DS_ON}	(1)	---	40	55	mΩ
		-40°C < T_J < 125°C(2)	---	52	---	
Off state output voltage	V_{OFF}	V_{CC}=8V, $V_{En/Fault}$=0, R_L=500Ω	---	50	120	mV
Continuous current	I_D	0.5in² pad, T_A=25°C (1)	---	4.2	---	A
		Minimum copper, T_A=80°C	---	2.3	---	
Current limit (For Direct Current-Sense)						
Short-circuit current limit	I_{Short}	R_{LIMIT} = 22Ω, SOURCE < 0.5V	---	2.2	---	A
Hold current limit	I_{Hold}	R_{LIMIT} = 22Ω	2.2	2.8	3.4	A
Overload current limit	I_{Lim}	R_{LIMIT} = 22Ω	---	4.3	---	A
Current limit (For Kelvin Sense)						
Short-circuit current limit	I_{Short}	R_{LIMIT} = 22Ω, SOURCE < 0.5V	---	1.8	---	A
Hold current limit	I_{Hold}	R_{LIMIT} = 22Ω	1.55	2.22	2.9	A
Trip current limit	I_{Lim}	R_{LIMIT} = 22Ω	---	3.3	---	A
dv/dt circuit						
Output voltage ramp time	dv/dt	$C_{dv/dt}$=1nF, 10% to 90%	2	3	4	ms
En/Fault						
Low level input voltage	V_{IL}	Output disabled	---	---	0.5	V
Intermediate level input voltage	$V_{I(INT)}$	Thermal fault, output disabled	0.82	1.4	1.95	V
High level input voltage	V_{IH}	Output enabled	2.5	---	---	V
High state maximum voltage	$V_{I(MAX)}$		3.4	4.3	5.4	V
Low level input current (sink)	I_{IL}	$V_{En/Fault}$=0V	---	-25	-35	µA
High level leakage current for external switch	I_I	$V_{En/Fault}$=3.3V	---	---	1	µA
Maximum fan-out for fault signal		Total numbers of chips that can be connected to this pin for simulta-neous shutdown	---	---	3	Units
Total device						
Bias current	I_{Bias}	Device operational	---	280	---	µA
		Shutdown	---	220	---	
Minimum operating voltage	V_{min}		---	---	2.55	V
Thermal latch						
Shutdown temperature	TSD	(1)	---	165	---	°C

1. Pulse test: Pulse width = 300µs, Duty cycle = 2%
2. Guaranteed by design, but not tested in production

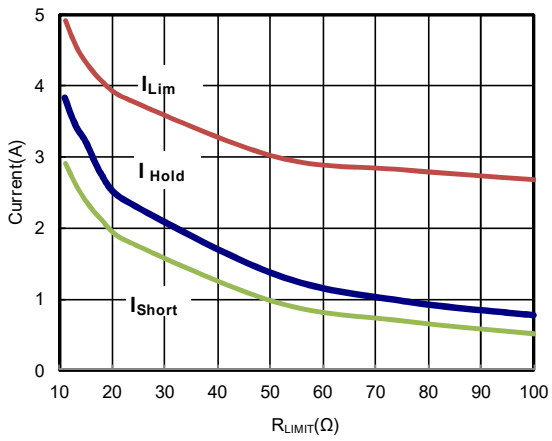
Typical Performance Characteristics

V_{CC}=5V, $V_{En/Fault}$=5V, R_{LIMIT}=13Ω, C_L=47uF, Cdv/dt=1nF, Direct Sense, T_A=T_J=25°C.

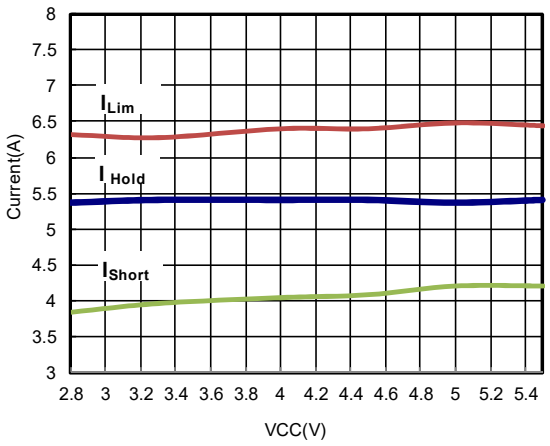
Trip Current, Hold Current, and Short Current vs. R_{LIMIT} Direct Sense VCC=5V



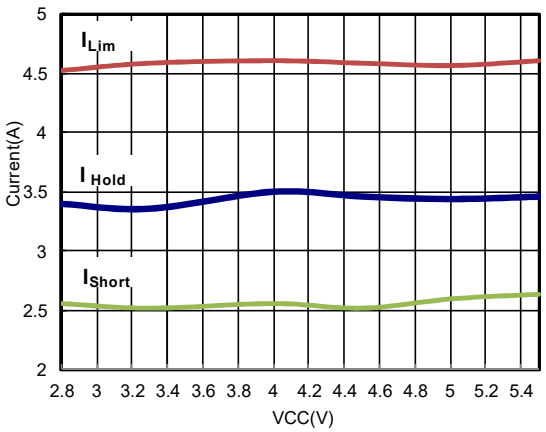
Trip Current, Hold Current, and Short Current vs. R_{LIMIT} Kelvin Sense VCC=5V



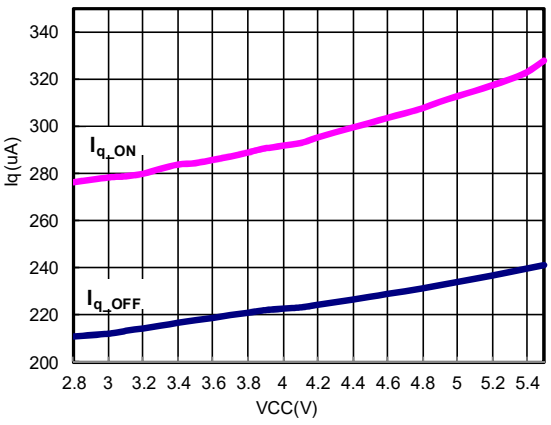
Trip Current, Hold Current, and Short Current vs. VCC Direct Sense R_{LIMIT}=13Ω



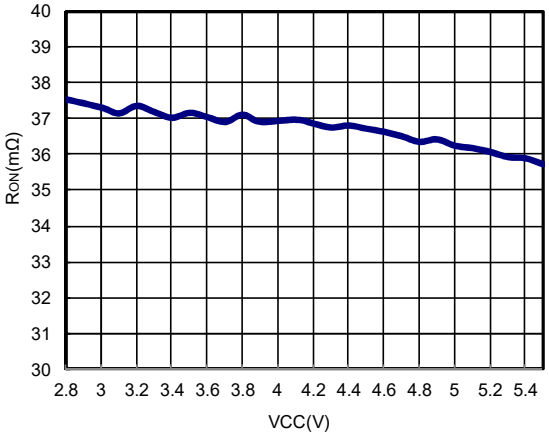
Trip Current, Hold Current, and Short Current vs. VCC Kelvin Sense R_{LIMIT}=13Ω



Iq (ON) & Iq (OFF) vs. VCC

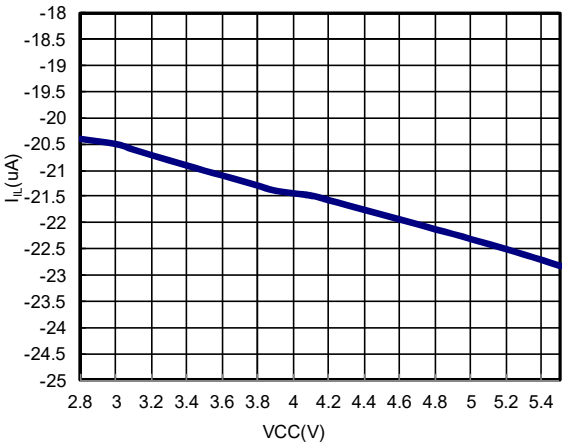


R_{DSon} vs. VCC

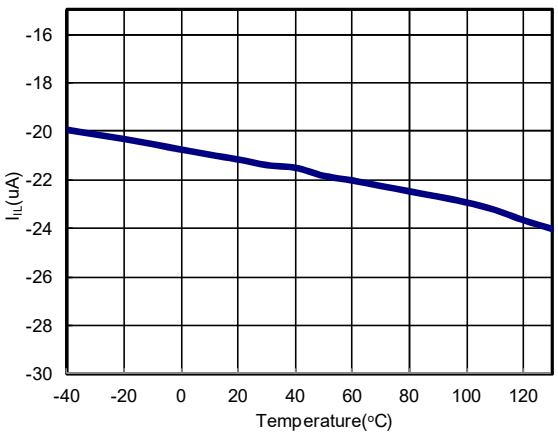


Typical Performance Characteristics (Continued)

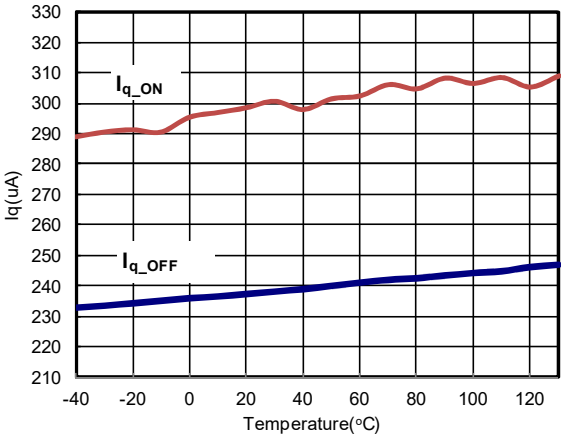
I_{IL} vs. VCC



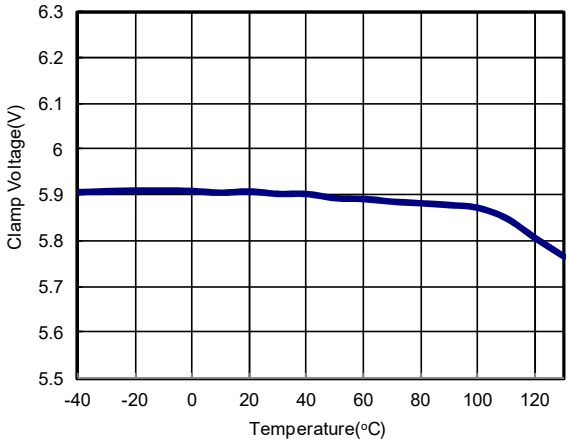
I_{IL} vs. Temperature



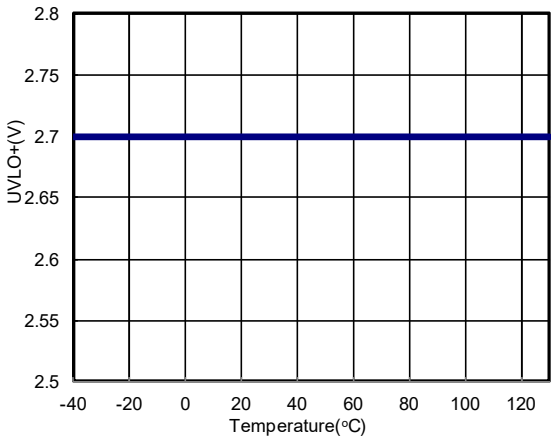
Iq(ON)&Iq(OFF) vs. Temperature
VCC=5V



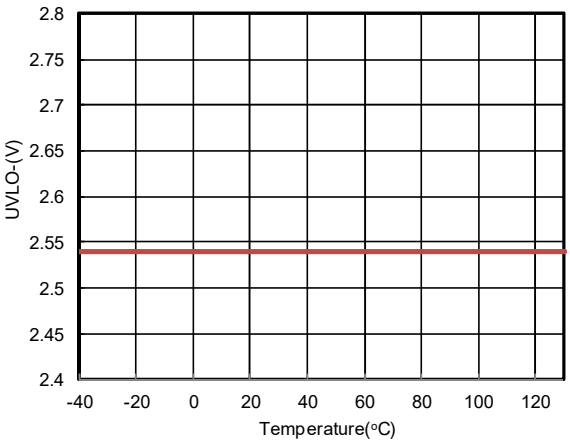
V_{Clamp} vs. Temperature
VCC=8V



UVLO vs. Temperature

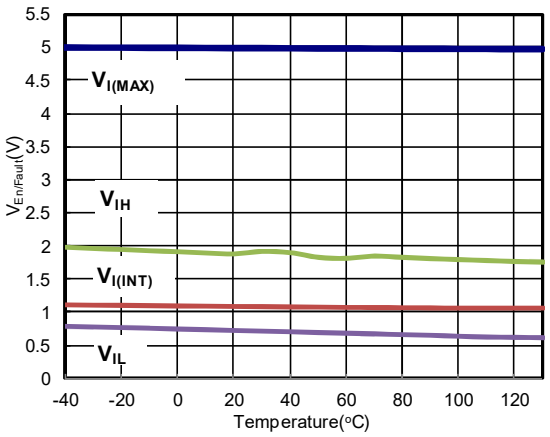


UVLO Hyst vs. Temperature

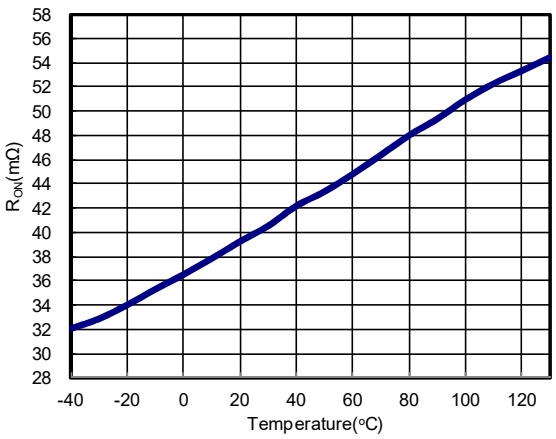


Typical Performance Characteristics (Continued)

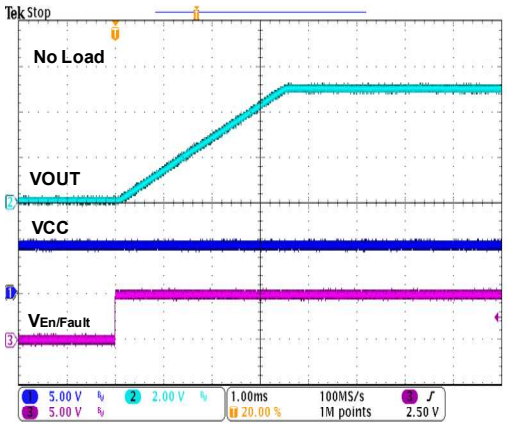
V_{IL}, $V_{I(INT)}$, V_{IH}, $V_{I(MAX)}$ vs. Temperature



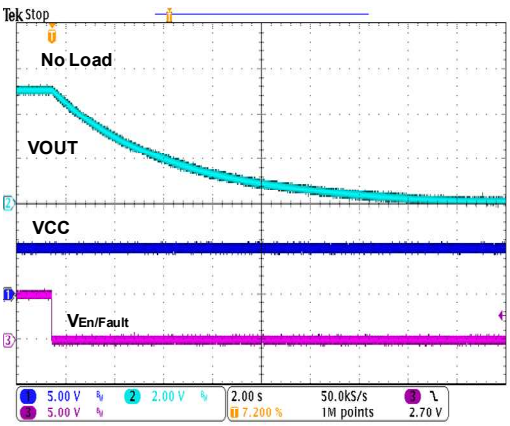
R_{DSon} vs. Temperature



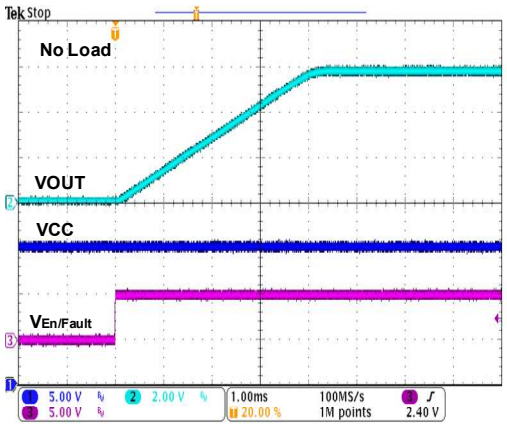
Startup through Enable



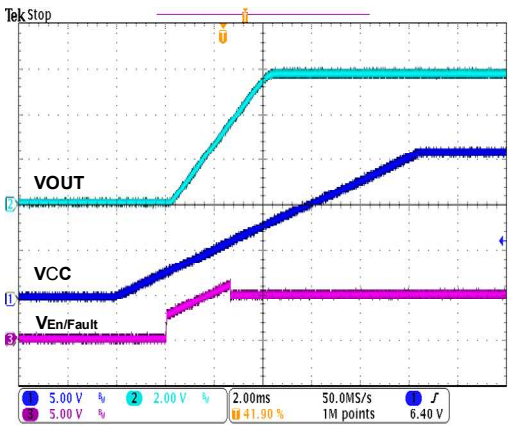
Shutdown through Enable



VOUT Clamping

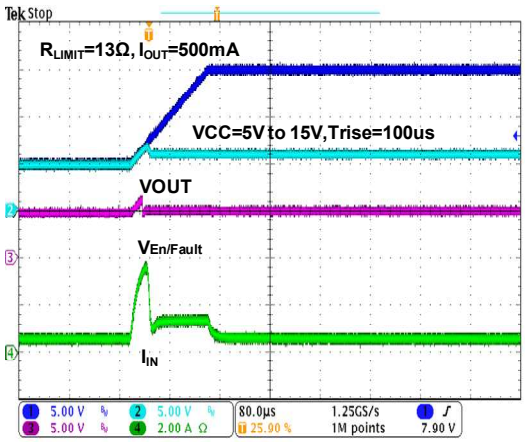


Startup into VOUT Clamping

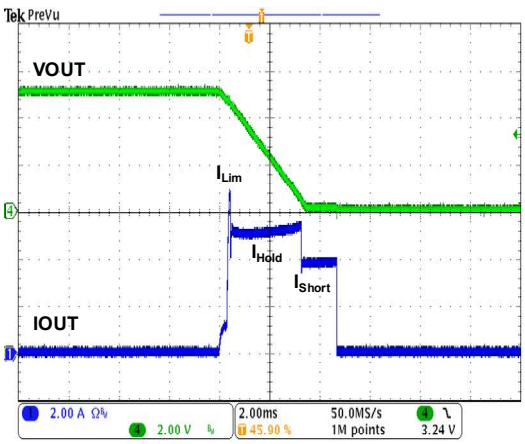


Typical Performance Characteristics (Continued)

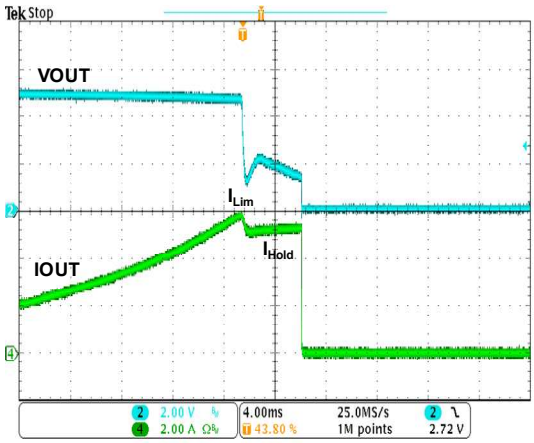
Line Transient



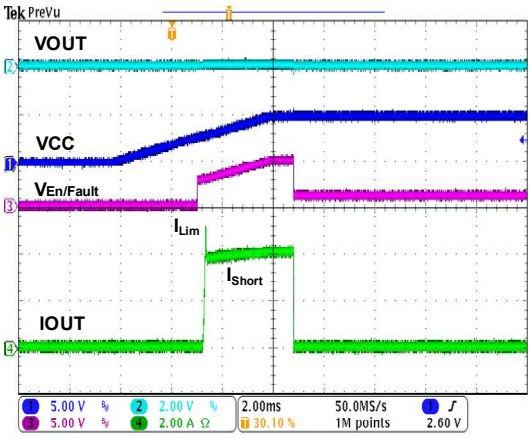
Current Limit



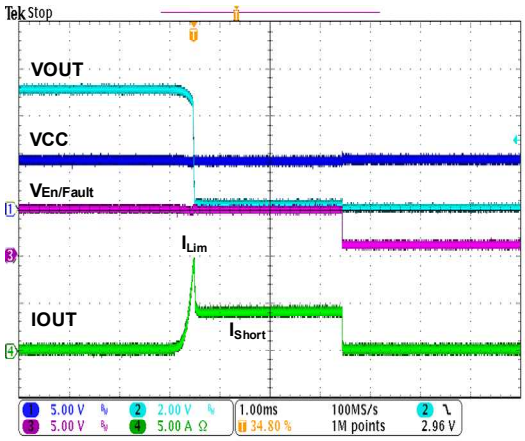
Current Limit



Startup into Short Circuit



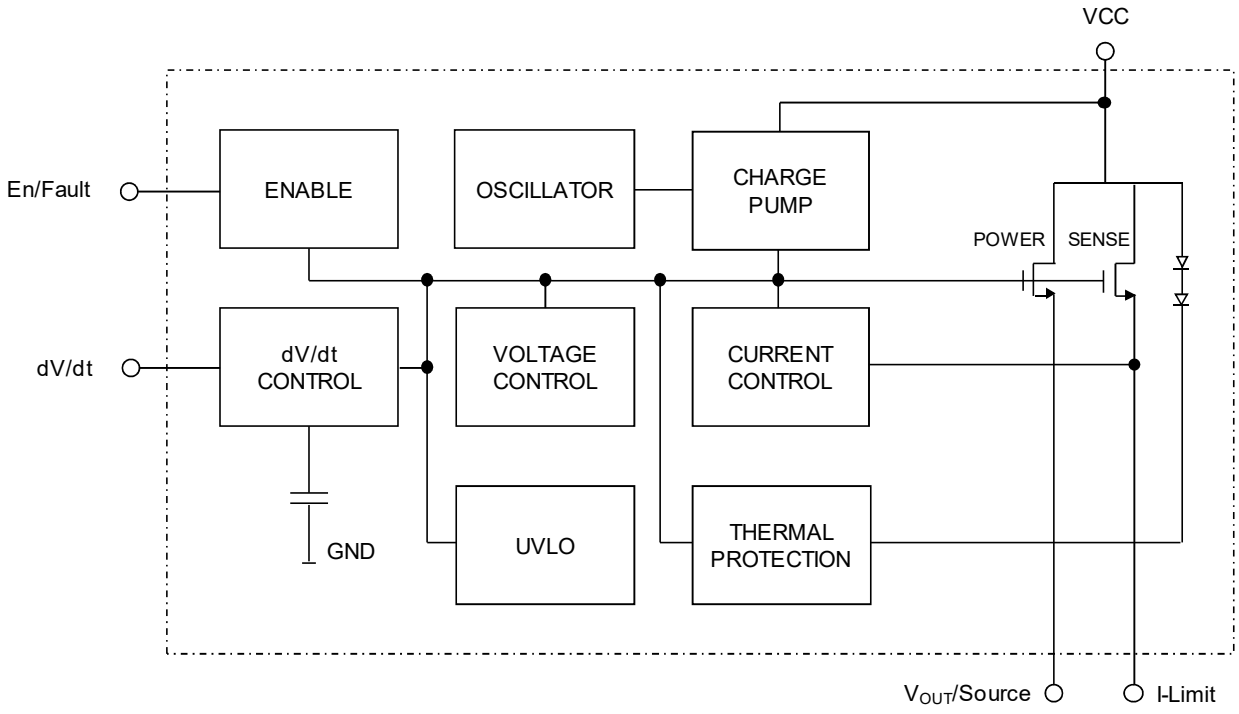
Short Circuit during Normal Operation



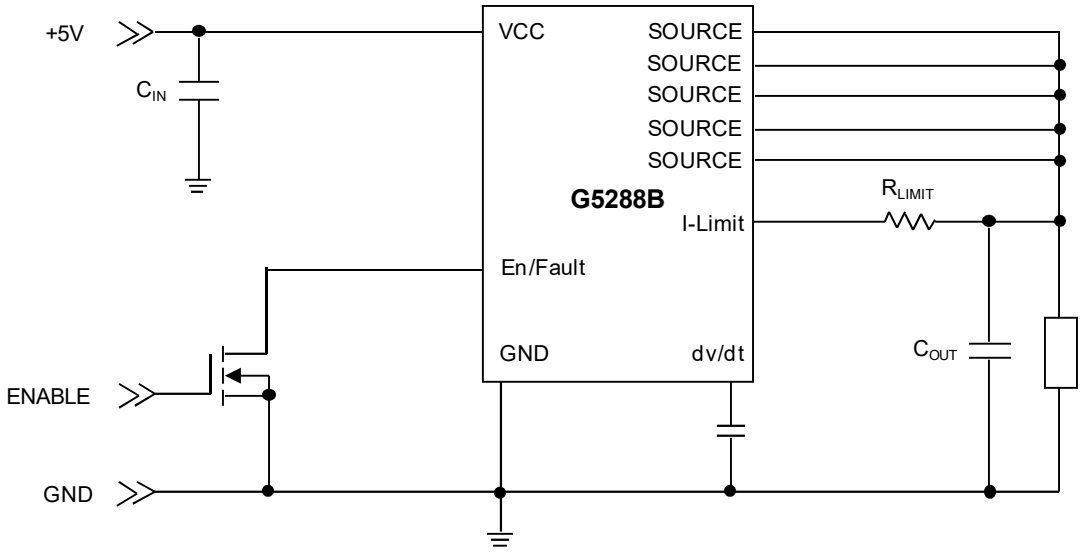
Pin Description

PIN	NAME	FUNCTION
1-5	Source	Connected to the source of the internal power MOSFET and to the output terminal of the fuse
6	NC	Not connected.
7	I-Limit	A resistor between this pin and the Source pin sets the overload and short-circuit current limit levels.
8	En/Fault	The En/Fault pin is a tri-state, bi-directional interface. During normal operation the pin must be left floating, or it can be used to disable the output of the device by pulling it to ground using an open drain or open collector device. If a thermal fault occurs, the voltage on this pin goes into an intermediate state to signal a monitor circuit that the device is in thermal shutdown. It can be connected to another device of this family to cause a simultaneous shutdown during thermal events.
9	dv/dt	The internal dv/dt circuit controls the slew rate of the output voltage at turn-on. An external capacitor can be added to this pin to increase the ramp time. If an additional capacitor is not required, this pin should be left open.
10	GND	Ground pin
11	VCC	Exposed pad. Positive input voltage must be connected to VCC.

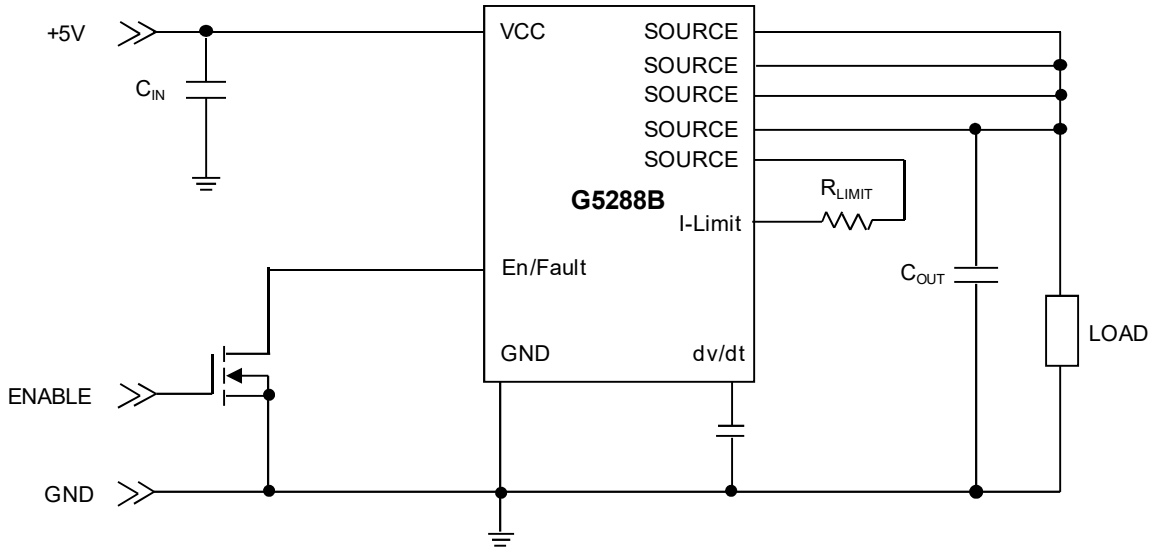
Block Diagram



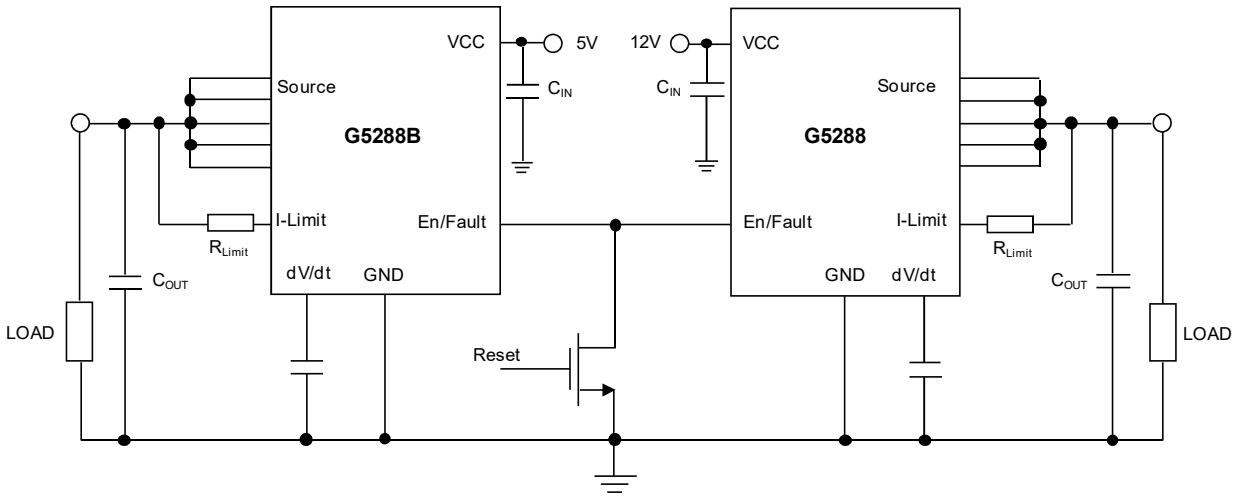
Typical application



Application Circuit with Direct Sense



Application Circuit with Kelvin Sense



Typical HDD Application Circuit

Operating modes

Turn-on

When the input voltage is applied, the En/Fault pin goes up to the high state, enabling the internal control circuit. After an initial delay time of typically 350 µs, the output voltage is supplied with a slope defined by the internal dv/dt circuit.

Normal operating condition

The G5288B buffers the circuitry on its output with the same voltage shown at its input, with a small voltage drop due to the N-channel MOSFET resistance.

Output voltage clamp

This internal protection circuit clamps the output voltage to a maximum safe value, typically 5.85V, if the input voltage exceeds this threshold.

Current limiting

When an overload event occurs, the current limiting circuit reduces the conductivity of the power MOSFET, in order to clamp the output current at the value selected externally by means of the limiting resistor R_{LIMIT}.

There are two methods to set up the application circuit for the G5288B as shown in typical application section.

Direct sense: connecting R_{LIMIT} between the current limit pin (I-limit) and the load. The resistance has an influence on the current limit value for a given resistor and may vary slightly depending on the impedance between the R_{LIMIT} and the source pins. The R_{DS_ON} of G5288B will be slightly lower in the method since all five source pins are connected in parallel.

Kelvin sense: using one of the source pins as the connection for R_{LIMIT}. This connection senses the voltage on the die and therefore any bond wire resistance and external impedance on the board have no effect on the current limit value. In this method, the R_{DS_ON} is slightly increased relative to the direct sense method since only four of the source pins are used. The tables as shown below list the examples of current limit values of the resistor value for both Kelvin sense and direct sense.

Thermal shutdown

If the device temperature exceeds the thermal latch threshold, typically 165 °C, the thermal shutdown circuitry turns the power MOSFET off, thus disconnecting the load. The En/Fault pin of the device is automatically set at an intermediate voltage, in order to signal the over temperature event. In this condition, G5288B can be reset either by cycling the supply voltage or by pulling down the En/Fault pin below the V_{IL} threshold and then releasing it.

Cdv/dt calculation

Connecting a capacitor between the dv/dt pin and GND allows the modification of the output voltage ramp-up time. Given the desired time interval Δt during which the output voltage goes from zero to its maximum value, the capacitance to be added on the dv/dt pin can be calculated using the following theoretical formula:

Equation 1

$$t_{slew} = 2.8 \times 10^6 \times (50pF + Cdv/dt)$$

$$Cdv/dt = \frac{t_{slew}}{2.8 \times 10^6} - 50pF$$

Where Cdv/dt is expressed in Farads and the time in seconds.

En/Fault pin

The En/Fault pin has the dual function of controlling the output of the device and, at the same time, of providing information about the device status to the application.

When it is used as a standard Enable pin, it should be connected to an external open-drain or open-collector device. In this case, when it is pulled at low logic level, it turns the output of the E-Fuse off.

If this pin is left floating, since it has internal pull-up circuitry, the output of G5288B is hold ON, in normal operating conditions.

In case of thermal fault, the pin is pulled to an intermediate state (Fig. 1). This signal can be provided to a monitor circuit, informing it that a thermal shutdown has occurred, or it can be directly connected to the En/Fault pins of other devices on the same application in order to achieve a simultaneous enable/disable feature.

When a thermal fault occurs, the device can be reset either by cycling the supply voltage or by pulling down the En/Fault pin below the V_{IL} threshold and then releasing it.

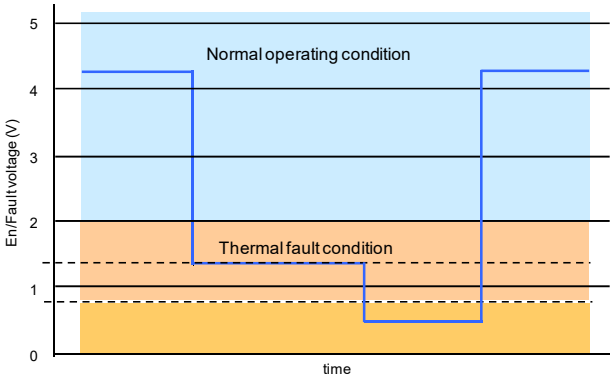


Fig. 1 En/Fault pin status

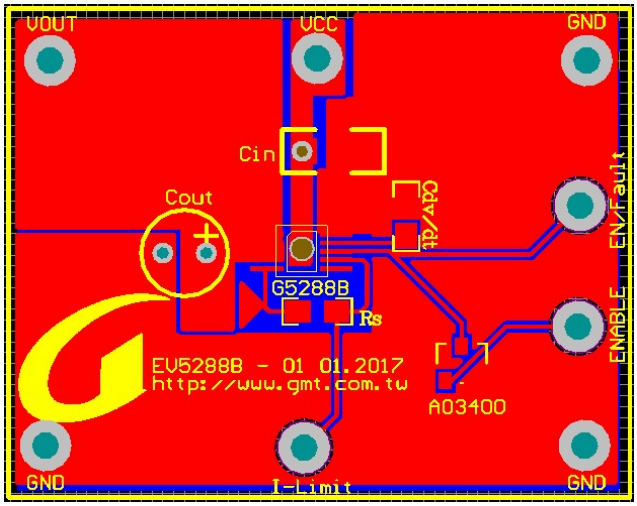
Table1: Current Limit vs. Current Limit Resistor (VCC=5V, Kelvin Sense)

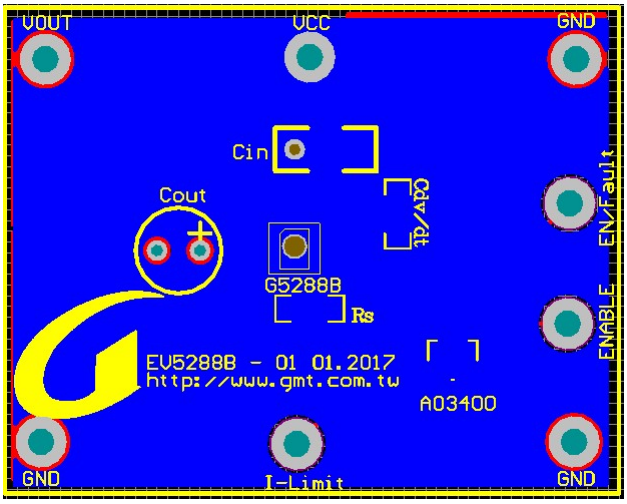
$R_{LIMIT}(\Omega)$	11	13	15	18	22	51	75	100
Trip Current (A)	4.66	4.38	4.1	3.76	3.6	2.74	2.54	2.44
Hold Current (A)	3.72	3.38	3.18	2.63	2.36	1.27	0.94	0.74

Table2: Current Limit vs. Current Limit Resistor (VCC=5V, Direct Sense)

$R_{LIMIT}(\Omega)$	11	13	15	18	22	51	75	100
Trip Current (A)	6.72	6	5.42	4.78	4.34	3.06	2.75	2.6
Hold Current (A)	6	5.1	4.54	3.76	3	1.44	1.03	0.81

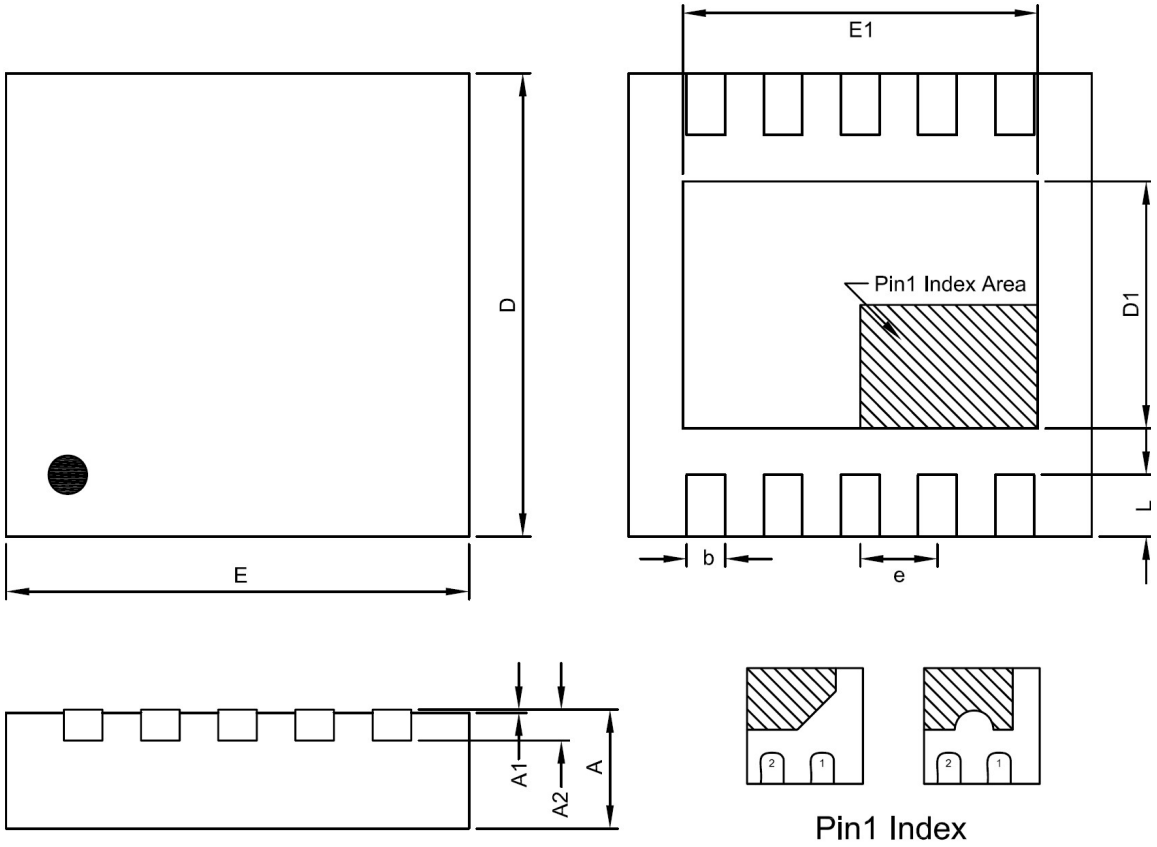
EV Board PCB Layout Section





DFN3X3-10 PCB	Information
Board Material	FR4
Size	36.3mm×28.7mm
Board Thickness	1.6mm
Layers	2
Copper Thickness	2 oz.

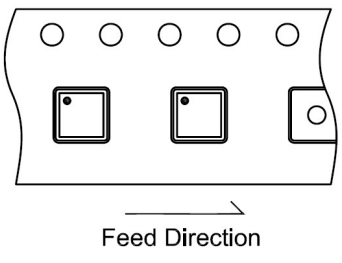
Package Information



DFN3X3-10 Package

Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.90	1.00	0.0315	0.0354	0.0394
A1	0.00	- - -	0.05	0.0000	- - -	0.0020
A2	0.20 REF			0.0079 REF		
D	2.95	3.00	3.05	0.1161	0.1181	0.1201
E	2.95	3.00	3.05	0.1161	0.1181	0.1201
D1	1.50	1.60	1.75	0.0591	0.0630	0.0689
E1	2.20	2.60	2.70	0.0866	0.1024	0.1063
b	0.18	0.25	0.30	0.0071	0.0098	0.0118
e	0.50 BSC			0.0197 BSC		
L	0.30	0.40	0.50	0.0118	0.0157	0.0197

Taping Specification



PACKAGE	Q'TY/REEL
DFN3X3-10	3,000 ea