High-Speed Step-Down Controller

Features

- **Ultra-High Efficiency**
- **4700ppm/°C $R_{DS(ON)}$ Current Sensing (without Current-Sense Resistor)**
- **Quasi-PWM with 100ns Load-Step Response**
- **Built-in 0.5% 0.7V Reference**
- **0.7V to 2.6V Adjustable Output Range**
- **4.5V to 28V Battery Input Range**
- **4 Selectable Frequency Setting**
- **Integrated Boost Switch**
- **OVP & UVP**
- **1.5ms Voltage Servo Soft-Start**
- **Drives Large Synchronous-Rectifier FETs**
- **Power-Good Indicator**
- **Thermal Shutdown (Non-latch)**

General Description

G5318 is a small-sized step-down controller uses constant on-time control scheme to handle wide input/output voltage ratios with ease and provides 100ns "instant-on" response to load transients while maintaining a relatively constant switching frequency. The G5318 achieves high efficiency at a reduced cost by eliminating the current-sense resistor found in traditional current-mode PWMs. Efficiency is further enhanced by an ability to drive very large synchronous rectifier MOSFETs. The G5318 is intended for CPU core, chipset, DRAM, or other low-voltage supplies as low as 0.7V. The G5318 is available in TDFN3X3-10 package.

Applications

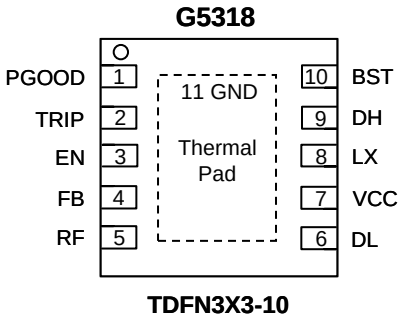
- **Notebook Computers**
- **CPU Core Supply**
- **I/O Supply**
- **Chipset/RAM Supply as Low as 0.7V**

Ordering Information

ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE (Green)
G5318RE1U	5318	-40°C to +85°C	TDFN3X3-10
G5318RE1D	5318	-40°C to +85°C	TDFN3X3-10

Note: RE: TDFN3X3-10
1: Bonding Code
U & D : Tape & Reel
Green: Lead Free / Halogen Free

Pin Configuration



TDFN3X3-10

Absolute Maximum Ratings

VCC to GND . . . . . -0.3V to 7V
EN, FB, PGOOD, RF to GND . . . . . -0.3V to 7V
TRIP GND . . . . . -0.3V to (VCC+0.3V)
BST to GND . . . . . -0.3V to 36V
DL to GND . . . . . -0.3V to 7V
<30ns . . . . . -6V to 7.5V
DH to LX . . . . . -0.3V to 6V
<30ns . . . . . -6V to 7.5V
LX to BST . . . . . -6V to 0.3V
LX to GND . . . . . -0.3V to 30V
<30ns . . . . . -6V to 36V

Thermal Resistance of Junction to Ambient, (θ_{JA})
TDFN3X3-10 . . . . . 68°C/W
Continuous Power Dissipation (T_A = +25°C)
TDFN3X3-10 . . . . . 1.47W
Thermal Resistance of Junction to Ambient, (θ_{Jc})
TDFN3X3-10 . . . . . 28°C/W
Junction Temperature . . . . . 150°C
Storage Temperature . . . . . -65°C to 150°C
Reflow Temperature (soldering, 10sec) . . . . . 260°C
ESD (HBM) 2kV
ESD (MM) 200V

Electrical Characteristics

(VIN=15V, V_{CC}=5V, EN= V_{CC}, T_A=25°C)

The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	V_{CC}		4.5	---	6.5	V
FB Regulation Voltage	Forced-PWM mode	FB = OUT	---	0.70	---	V
(DC Output Voltage Accuracy)	Skip mode		0.7005	0.704	0.7075	
FB Input Current	VFB=0.735V, skip mode		---	0.01	0.2	µA
Soft-Start Ramp Time	Rising edge of EN to VOUT=95%		1	1.5	2.2	ms
Switching Frequency	VIN=12V VOUT=1.1V	R_{RF} = 470kΩ	240	290	340	kHz
		R_{RF} = 200kΩ	290	340	390	
		R_{RF} = 100kΩ	330	380	430	
		R_{RF} = 39kΩ	380	430	480	
On Time	VIN=12V VOUT=1.1V	R_{PF} = 470kΩ	269	316	382	ns
		R_{PF} = 200kΩ	235	270	316	
		R_{PF} = 100kΩ	213	241	278	
		R_{PF} = 39kΩ	190	213	241	
Minimum On Time	VIN=19V VOUT=0.7V	R_{RF} = 39kΩ	---	80	---	ns
Minimum Off Time			---	400	---	ns
Quiescent Supply Current (V_{CC})	FB forced above the regulation point		---	500	750	µA
Shutdown Current (V_{CC})	EN=0V		---	---	1	µA
Output Shutdown Discharge Resistance	EN=0V, LX=0.5V		---	20	32	Ω
Overvoltage Trip Threshold	With respect to error comparator threshold		15	20	25	%
Overvoltage Fault Propagation Delay	FB forced 2% above the trip threshold		14	20	26	µs
Output Undervoltage Protection Threshold	With respect to error comparator threshold		65	70	75	%
Output Undervoltage Protection Blanking Time	From EN signal going high		1	2.2	3.5	ms
TRIP Source Current	VTRIP=1V		9	10	11	µA
VTRIP setting range	VTRIP		0.2	---	1.6	V
Current-Limit Threshold (Positive Direction)	VTRIP=1.6V		180	200	220	mV
	VTRIP=0.2V		17	25	33	
Current-Limit Threshold (Negative Direction)	VTRIP=1.6V		-220	-200	-180	mV
	VTRIP=0.2V		-33	-25	-15	
Current Comparator Offset	LX- (VTRIP/8)		-10	---	10	mV
Current-Limit Threshold (Zero Crossing)	GND - LX, Skip mode		-5	0	6	mV

Electrical Characteristics (continued)

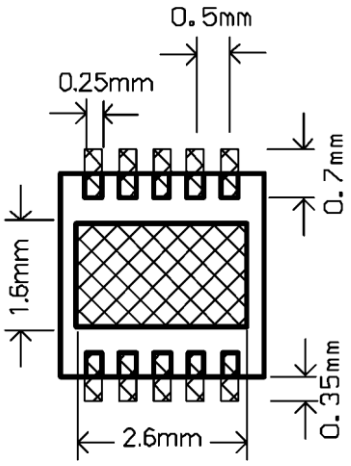
(VIN=15V, V_{CC}=5V, EN= V_{CC}, T_A=25°C)

The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
PGOOD Trip Threshold	Measure at FB with respect to error comparator threshold, rising edge.	-10	-7	-5.5	%
PGOOD Hysteresis	Falling edge	---	32	---	mV
PGOOD Output Low Voltage	ISINK=2.5mA	---	---	0.2	V
PGOOD Propagation Delay		160	240	400	μs
Thermal Shutdown Threshold	Hysteresis=17°C	---	147	---	°C
V_{CC} Undervoltage Lockout Threshold	Rising edge, hysteresis = 300mV,PWM disabled below this level	3.9	4.2	4.5	V
DH Gate-Driver On-Resistance (Pull-Up)	BST - LX forced to 5V Source 50mA	---	1.5	3	Ω
DH Gate-Driver On-Resistance (Pull-Down)	BST - LX forced to 5V Sink 50mA	---	0.7	1.8	Ω
DL Gate-Driver On-Resistance (Pull-Up)	DL, high state Source 50mA	---	1.0	2.2	Ω
DL Gate-Driver On-Resistance (Pull-Down)	DL, low state Sink 50mA	---	0.5	1.2	Ω
Dead Time	DL rising	---	17	---	ns
	DH rising	---	22	---	
BST Switch Forward Voltage	Forwarding Current=10mA	0.2	0.35	0.4	V
EN Input High Voltage	Enable	1.8	---	VCC	V
EN Input Low Voltage	Disable	---	---	0.5	
EN Input Current	VEN=5V	---	---	1.0	μA
RF Input Threshold	set forced-PWM mode	1.8	---	---	V
	Set Skip mode	---	---	0.5	

Minimum Footprint PCB Layout Section

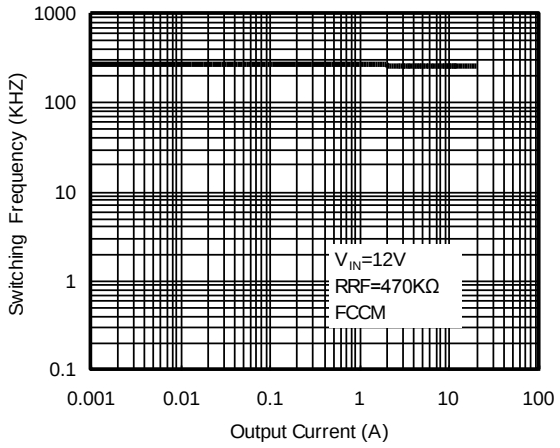
TDFN3X3-10



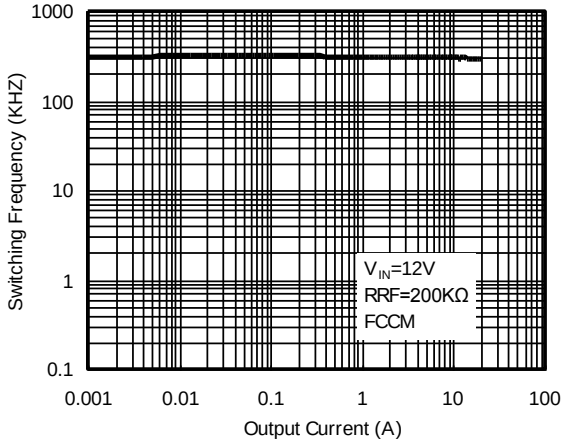
Typical Performance Characteristics

T_A=25°C, unless otherwise noted.

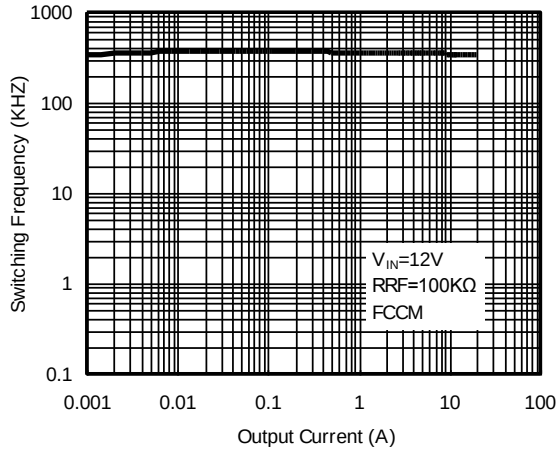
Switching Frequency vs Output Current



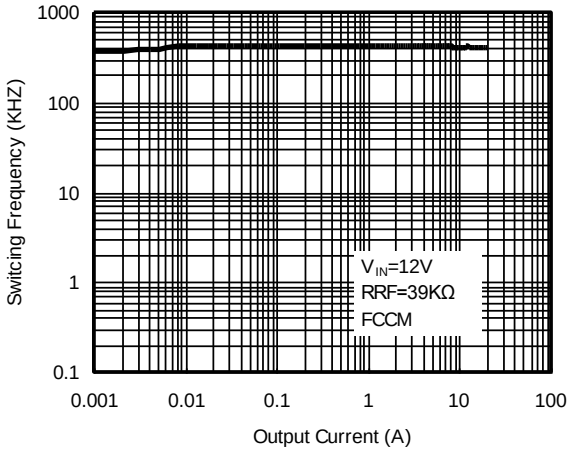
Switching Frequency vs Output Current



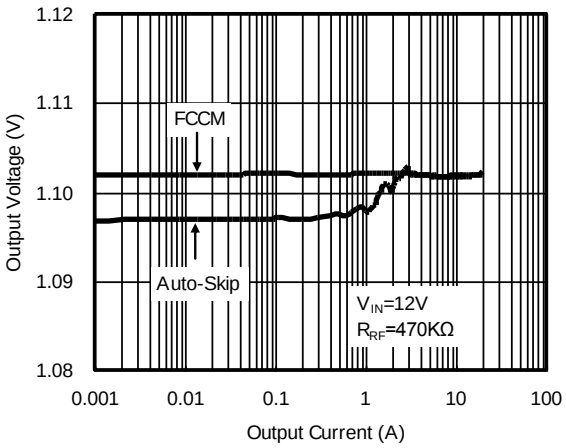
Switching Frequency vs Output Current



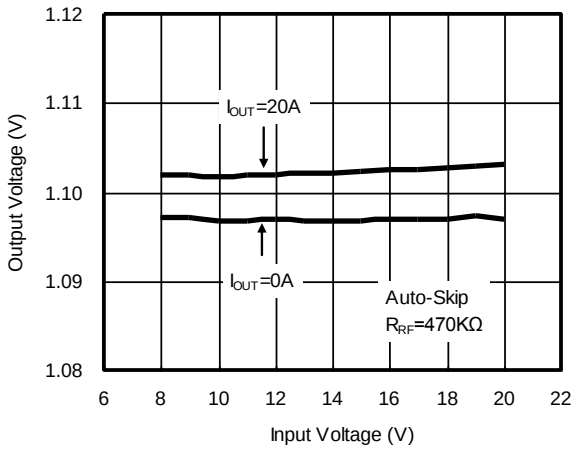
Switching Frequency vs Output Current



Output Voltage vs Output Current

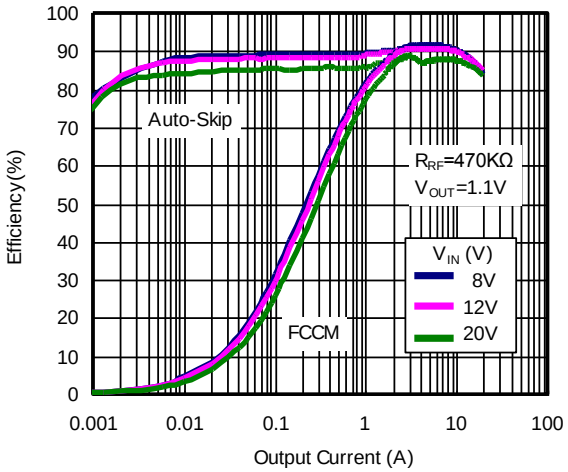


Output Voltage vs Input Voltage

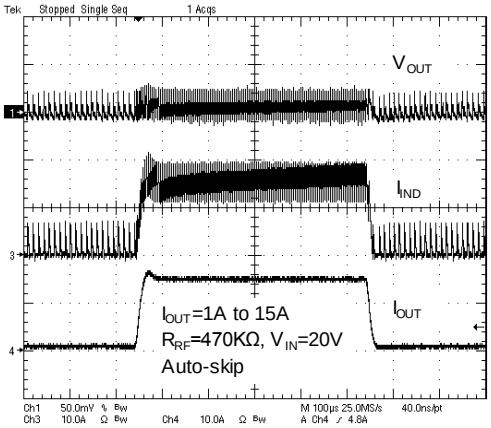


Typical Performance Characteristics (continued)

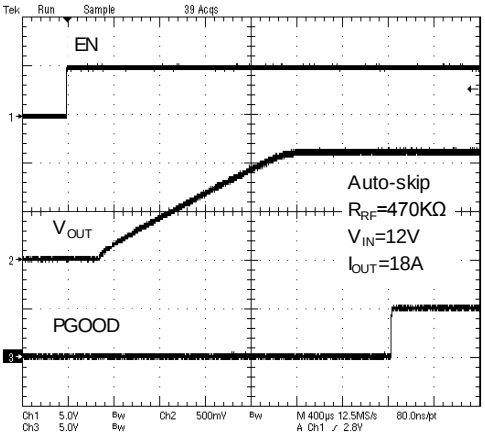
Efficiency vs Output Current



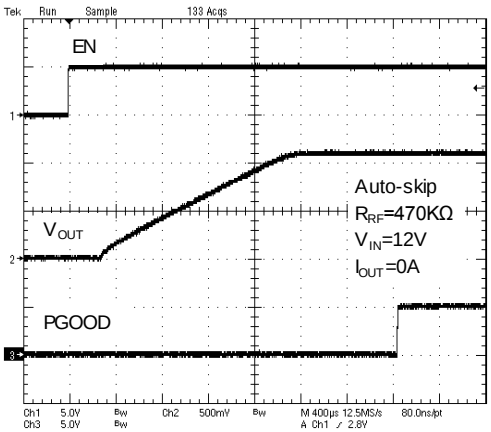
Load Transient Response



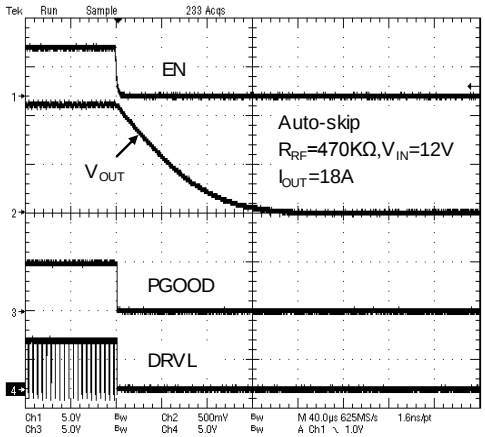
Soft Start Waveform



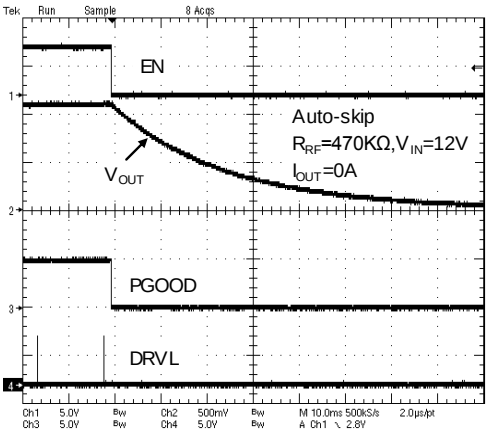
Soft Start Waveform



Shutdown Waveform



Shutdown Waveform



Pin Description

PIN	NAME	FUNCTION
1	PGOOD	Power-Good Open-Drain Output. PGOOD is low when the output voltage is more than 10% below the normal regulation point or during soft-start. PGOOD is high impedance when the output is in regulation and the soft-start circuit has terminated.
2	TRIP	Current-Limit Threshold Adjustment. Connect a resistor from TRIP to GND to set current limit threshold VOCL=VTRIP/8 (0.2V<VTRIP<1.6V)
3	EN	Enable Input. Drive EN pin to GND to force the G5318 into shutdown. A rising edge on EN clears the fault latch.
4	FB	Feedback Input. Connect FB to a resistor divider for an adjustable output.
5	RF	On-Time Selection-Control Input. Connect to GND with 39kΩ to 470kΩ resistor, R_{RF} to select the switching frequency as the Table 2. The switching frequency setting is detected and stored into internal registers during startup. RF pin also controls the pulse-skipping mode and force PWM mode selection: Connect to GND with resistor : pulse-skipping mode Connect to PGOOD with resistor : force PWM mode after PGOOD becomes high
6	DL	Low-Side Gate-Driver Output. Swings from GND to VCC.
7	VCC	5V Supply Input. Connect to the system supply voltage, +4.5V to +6.5V, Bypass to GND with a 1μF (min) ceramic capacitor.
8	LX	External Inductor Connection. Connect LX to the switched side of the inductor. LX serves as the lower supply rail for the DH high-side gate driver. LX is also the positive input to the current-limit comparator.
9	DH	High-Side Gate Driver Output. Swings from LX to BST.
10	BST	Boost Flying-Capacitor Connection. Connect to an external capacitor according to the Standard Application Circuit. Internally connected to VCC by bootstrap switch.
11	GND	Ground (Thermal PAD)

Block Diagram

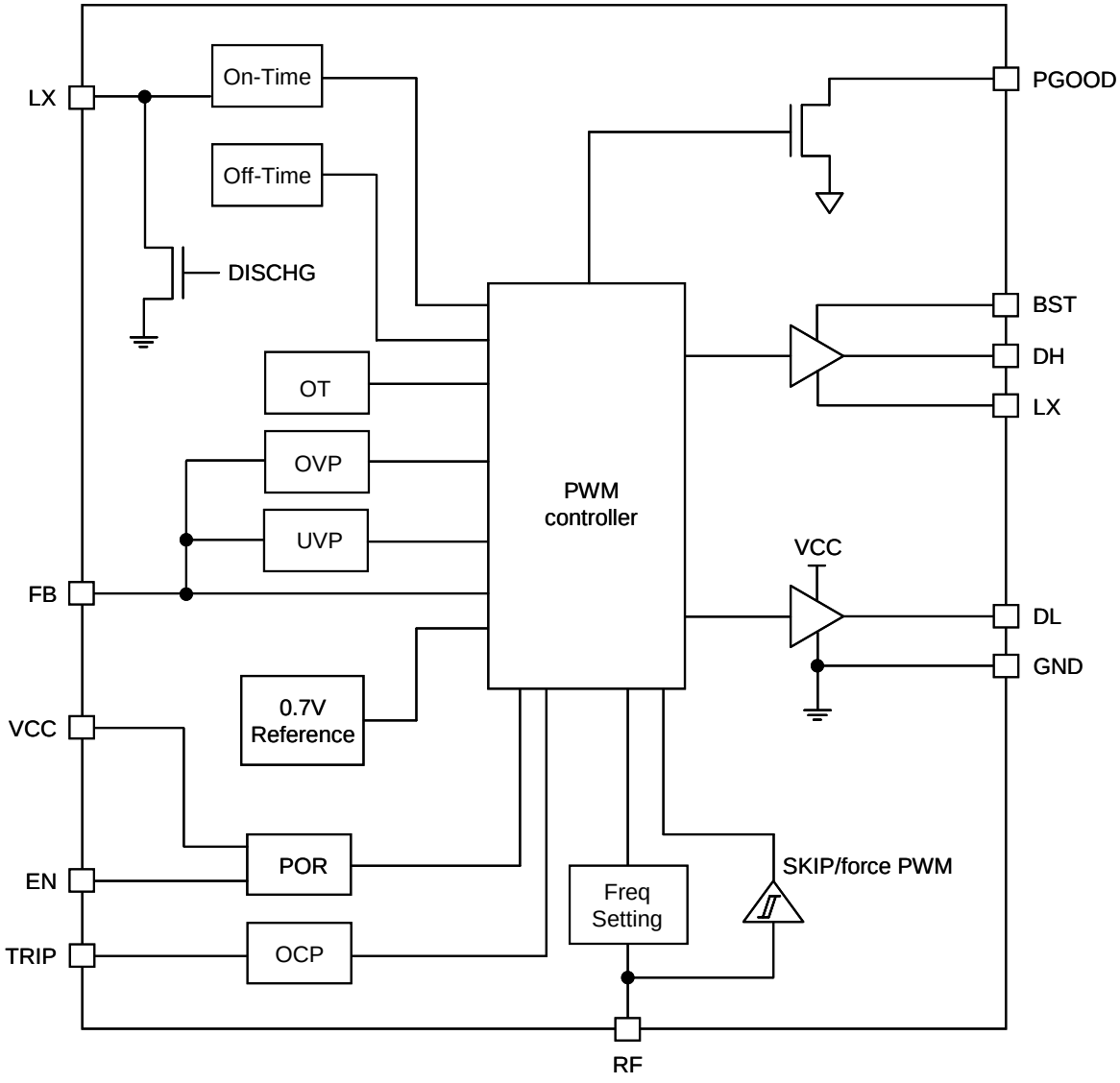


Fig. 1 Block Diagram of G5318

Application Information

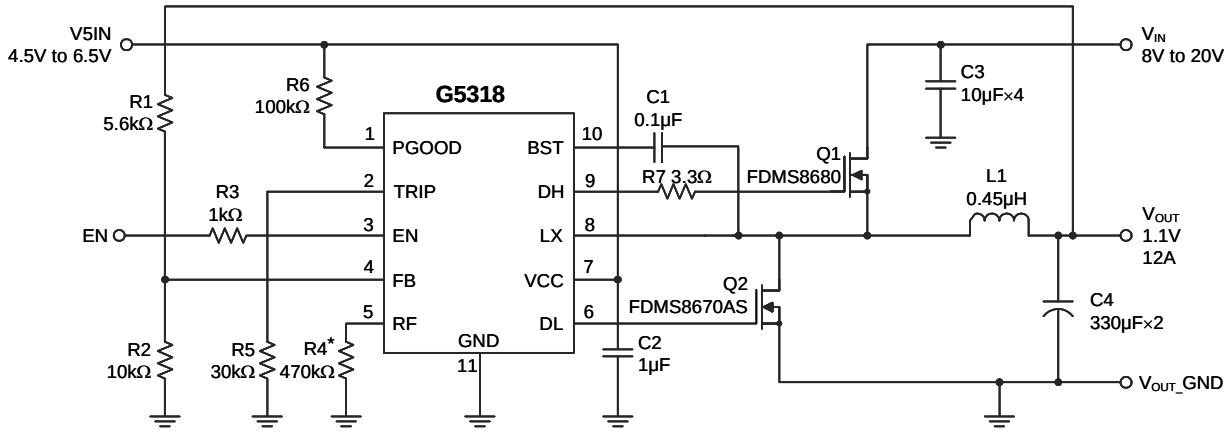
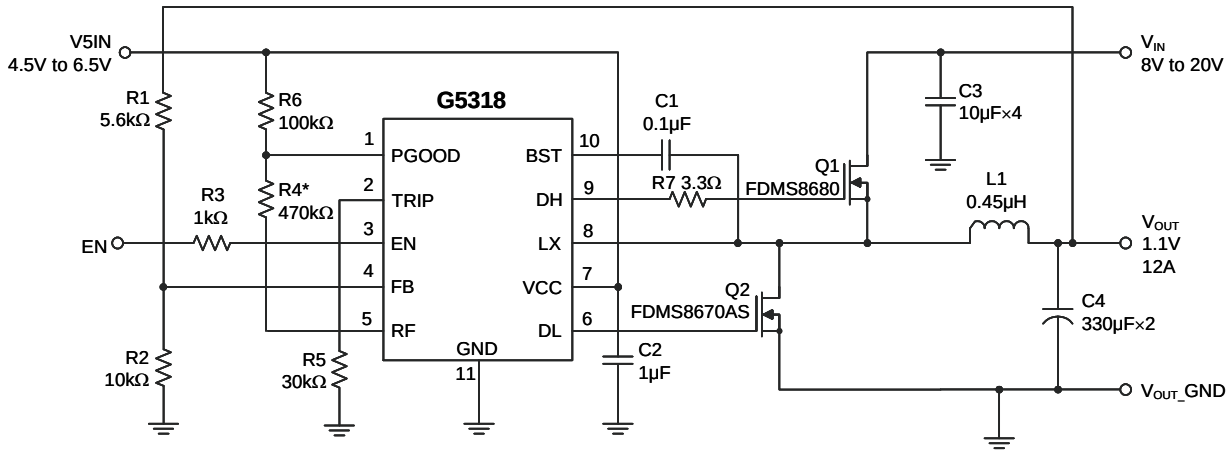


Fig. 2.1 1.1V/12A Auto-Skip Mode



*: See Table 2 for Resistor and Switching Frequency.

Fig. 2.2 1.1V/12A Forced Continuous Conduction Mode

Table 1. Component Selection for Standard Application:

SYMBOL	SPECIFICATION	MANUFACTURER	PART NUMBER
C3	10μF, 25V	Taiyo Yuden	TMK325BJ106MM
Q1	30V, 25A, 8.5mΩ		FDMS8680
Q2	30V, 42A, 3.5mΩ		FDMS8670AS
L1	0.45μH, 25A, 1.1mΩ	Panasonic	ETQP4LR45XFC
C4	330μF, 2V, 12mΩ	Panasonic	EEFCX0D331XR

Detailed Description

G5318 is a step down controller and targeted to the low-voltage supply of notebook computers. A Quasi-PWM control is adapted in G5318. It is a constant-on-time PWM control with input feed-forward while maintaining a relatively constant switching frequency. It advantages in the fast load-transient response compared with conventional constant-on-time PWM control. The Figure 1 shows the Block Diagram of G5318.

5V bias Supply (VCC)

G5318 required an external 5V bias supply for the PWM circuit and gate-drivers. In the notebook computer, there is a high efficiency 5V system supply and eliminate the cost of external LDO. If no 5V supply existed in the system, it can be generated 5V by LDO such like G920.

Constant-on-time PMW Control with Input Feed-Forward

The Quasi-PWM control algorithm can be described briefly: the high-side switch on-time is determined by a one-shot whose period is inversely proportional to input voltage and directly proportional to output voltage. Another on-shot determines the minimum off-time. The on-time one-shot can be triggered if the error comparator is low, the low side switch current is below the current-limit threshold, and the minimum off-time one-shot has timed out.

Switching Frequency Selection

G5318 allows to select the switching frequency. There are four preset values by a resistor connected to RF pin as shown in Table 2. The setting is detected and stored into internal registers during startup. Leaving the resistance open sets the switching frequency to the lowest value, 290kHz. But it is recommended to apply one of the resistance on the table in any application.

Table 2a Resistor and Switching Frequency (V_{IN}=12V)

Resistance (R_{RF})	Switching Frequency
470kΩ	290kHz
200kΩ	340kHz
100kΩ	380kHz
39kΩ	430kHz

Table 2b Resistor and Switching Frequency (V_{IN}=5V)

Resistance (R_{RF})	Switching Frequency
470kΩ	240kHz
200kΩ	290kHz
100kΩ	330kHz
39kΩ	400kHz

Pulse-Skipping Mode and Forced-PWM Mode

In Pulse-Skipping Mode (RF pin pulled down to GND by a resistor), an automatic switchover to PFM takes place at light load. It turns off the low side switch when the inductor current crosses to zero. This scheme will improve the light-load efficiency. The disadvantage of Pulse-Skipping Mode is the noisy and asynchronous switching waveform at light load. It is not suitable to power the audio and noise-sensitive system.

In Forced-PWM Mode (RF pin tied to high to PGOOD by a resistor), disable the zero-crossing detector of inductor current. The inductor current can reverse at light loads to main the duty ratio of PWM loop. The gate-drive waveform of low side is the complement of the gate-drive waveform of high side. The advantage of Forced-PWM Mode is to keep an almost constant switching frequency. It is suitable to power the audio system with reducing the audio band noise. It improves the load-transient response and provides the sink-current capability. The trade-off is the efficiency cost at light load.

Current Limit

G5318 uses the on-state resistance of low side MOSFET as a current-sensing resistor. If the current–sense voltage (GND-LX) is above the current-limit threshold, the PWM is not allowed to initiate a new cycle. The actual peak current is the current-limit threshold adding one inductor current ripple. So it depends on the on-resistance of MOSFET, Inductor value, and battery voltage. No external current-sensing resistor is necessary in the output current path. A TRIP pin could be used to adjust the current-limit threshold. The R_{TRIP} resistor between TRIP pin and GND pin sets the threshold. It is connected to a 10μA current source within G5318 which has 4700ppm/°C temperature slope to compensate the temperature dependency of the $R_{DS(ON)}$. The equation for the current limit threshold is as follows:

$$I_{LIMIT} = \frac{R_{TRIP}}{8 \times R_{DS(ON)}} \times 10^{-5} \text{ (A)}$$

The negative current-limit threshold in force PWM mode is set as the same absolute value as positive current-limit threshold but with negative polarity (GND-LX).

Gate Drivers

In the low duty factor application, like notebook computer, it exists large difference of input voltage and output voltage. Therefore, large low-side MOSFET and moderate-size high-side MOSFET are needed for high efficiency. The DH and DL drivers are optimized for driving high-side and low-side MOSFETs. A non-overlap control circuit is needed to avoid the DH and DL turning on simultaneously. The DL driver with a 0.5Ω pull low transistor helps prevent the DL from being coupled to high during the fast rising-time of the LX node, due to the drain to gate capacitive coupling of low-side synchronous-rectifier MOSFET. A resistor in series with the BST is recommended that will reduce the EMI-producing efficiency loss by increasing the turn-on time of the high-side MOSFET.

POR, UVLO, and Soft-Start

Power-on reset (POR) occurs when VCC rises above approximately 2V. It reset the fault latch and soft-start counter. When VCC is below 3.9V, undervolatge lockout (UVLO) inhibits switching and forces DL to high. An internal soft-start controls to ramp up the output voltage smoothly regardless of load current within 1.5ms.

Power-Good Indicator

The Output voltage is always monitored for undervoltage by the PGOOD comparator. The PGOOD is open-drain type signal. In shutdown and soft-start period, PGOOD is kept low. After the soft-start timer has timed out, the PGOOD is released if the output voltage is within 10% of normal value.

Fault Protection

G5318 provides undervoltage protection, overvoltage protection, and thermal protection.

The undervoltage protection (UVP) function is like foldback current limit function. If the output voltage is under 70% of normal value 1.5ms after shutdown released, the undervoltage protection function is activated. The PWM is latched off and would not restart until VCC power is cycled or EN is toggled.

The overvoltage protection (OVP) function activates when the output voltage is 20% above the set voltage. The low-side MOSFET turn on 100% and the high-side MOSFET turn off. This rapidly discharges the output capacitor and decreases the output voltage. The SMPS is latched off and would not restart until VCC power is cycled or EN is toggled.

The thermal protection (OT) function activates when die temperature exceeds the threshold value (typically: 147°C) the SMPS is shut down. This is non-latch protection.

Adjustable-Output Feedback

Connecting the FB pin to a resistor divider between OUT to GND to adjust the output voltage between 0.7V to 2.6V.

Chose R2=10kΩ and solve the R1 with the equation:

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right)$$

where V_{FB} = 0.7V norminal.

Test Mode

A test mode is provided for system developing stage. It can disable all the OVP and UVP features, and clear the fault latch if it has been set. Force the EN pin above VCC by external sourcing current, G5318 enters a no-fault test mode. (No more than 0.6V above VCC is allowable)

Application Information

Inductor Selection

The inductor value is determined as follows:

$$L = \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN} \times f \times \Delta I_{LPP}}$$

Where ΔI_{LPP} is defined as inductor ripple current.

The inductor ripple current also impacts transient-response performance, especially at low V_{IN}- V_{OUT} differentials. Low inductor values allow the inductor current to slew faster, replenishing charge removed from the output filter capacitors by a sudden load step.

Maintaining the ratio of the inductor ripple current to the designed maximum load current within a 20% to 50% range is prudent.

Current Limit setting

The minimum current-limit threshold must be high enough to support the maximum load current. The valley of the inductor current occurs at $I_{LOAD(MAX)}$ minus half of the inductor current ripple.

I_{LIMIT} equals minimum current-limit threshold voltage divided by the $R_{DS(ON)}$of Q2. Use the worst-case maximum value for $R_{DS(ON)}$ from the MOSFET Q2 data sheet, and add some margin for the rise in $R_{DS(ON)}$ with temperature. A good general rule is to allow 0.5% additional resistance for each °C of temperature rise.

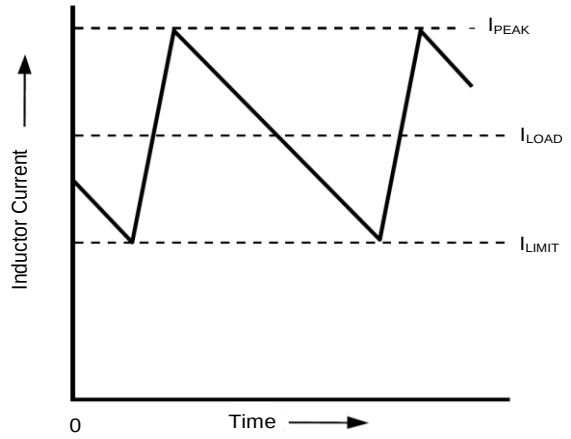


Fig. 3 Current Limit Setting

Output Capacitor Selection

The output filter capacitor must have low enough effective series resistance (ESR) to meet output ripple and load-transient requirements, yet have high enough ESR to satisfy stability requirements. Also, the capacitance must be high enough to absorb the inductor energy going from a full-load to no-load condition without tripping the overvoltage protection circuit.

In CPU V_{CORE} converters and other applications where the output is subject to violent load transients, the output capacitor's size depends on how much ESR is needed to prevent the output from dipping too low under a load transient.

In non-CPU applications, the output capacitor's size depends on how much ESR is needed to maintain an acceptable level of output voltage ripple:

$$R_{ESR} \leq \frac{V_{OUTPP}}{\Delta I_{LPP}}$$

Output Capacitor Stability considerations

Stability is determined by the value of the ESR zero relative to the switching frequency. The point of instability is given by the following equation:

$$f_{ESR} = \frac{f}{\pi}$$

Where f = switching frequency

$$f_{ESR} = \frac{1}{2 \times \pi \times ESR \times C_{OUT}}$$

For a typical 300kHz application, the ESR zero frequency must be well below 95kHz, preferably below 50kHz.

Don't put high-value ceramic capacitors directly across the feedback sense point without taking precautions to ensure stability. Large ceramic capacitors can have a high ESR zero frequency and cause erratic, unstable operation. However, it's easy to add enough series resistance by placing the capacitors a couple of inches downstream from the feedback sense point, which should be as close as possible to the inductor.

Unstable operation manifests itself in two related but distinctly different ways: double-pulsing and fast-feedback loop instability.

Double-pulsing occurs due to noise on the output or due to the ESR is too low to without enough voltage ramp in the output voltage signal. This "fools" the error comparator into triggering a new cycle immediately after the 400ns minimum off-time period has expired. Double-pulsing is more annoying than harmful, resulting in nothing worse than increased output ripple. However, it can indicate the possible presence of loop instability, which is caused by insufficient ESR. Loop instability can result in oscillations at the output after line or load perturbations that can trip the overvoltage protection latch or cause the output voltage to fall below the tolerance limit. The easiest method for checking stability is to apply a very fast zero-to-max load transient and carefully observe the output voltage ripple envelope for over-shoot and ringing. It can help to simultaneously monitor the inductor current with a current probe. Don't allow more than one cycle of ringing after the initial step-response under- or overshoot.

Input Capacitor Selection

The input capacitor must meet the ripple current requirement (I_{RMS}) imposed by the switching currents. Nontantalum chemistries (ceramic, aluminum, or OS-CON) are preferred due to their resistance to power-up surge currents.

For optimal circuit reliability, choose a capacitor that has less than 10°C temperature rise at the peak ripple current.

$$I_{RMS} = I_{LOAD}\left(\frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}\right)$$

Power MOSFET Selection

Most of the following MOSFET guidelines focus on the challenge of obtaining high load-current capability (>5A) when using high-voltage (>20V) AC adapters. Low-current applications usually require less attention. For maximum efficiency, choose a high-side MOSFET (Q1) that has conduction losses equal to the switching losses at the optimum battery voltage (15V). Check to ensure that the conduction losses at minimum input voltage don't exceed the package thermal limits or

violate the overall thermal budget. Check to ensure that conduction losses plus switching losses at the maximum input voltage don't exceed the package ratings or violate the overall thermal budget.

Choose a low-side MOSFET (Q2) that has the lowest possible $R_{DS(ON)}$, comes in a moderate to small pack-age (i.e., SO-8), and is reasonably priced. Ensure that G5318 DL gate driver can drive Q2 ; in other words, check that the gate isn't pulled up by the high-side switch turn on, due to parasitic drain-to-gate capacitance, causing cross-conduction problems. Switching losses aren't an issue for the low-side MOSFET, since it's a zero-voltage switched device when used in the buck topology.

MOSFET Power Dissipation

Worst-case conduction losses occur at the duty factor extremes. For the high-side MOSFET, the worst-case power dissipation due to resistance occurs at minimum battery voltage:

$$PD(Q1\ Resistive) = \left(\frac{V_{OUT}}{V_{IN(MIN)}}\right) \times I_{LOAD}^2 \times R_{DS(ON)}$$

Generally, a small high-side MOSFET is desired to reduce switching losses as high input voltages. However, the $R_{DS(ON)}$ required to stay within package power-dissipation limits often limits how small the MOSFET can be. Again, the optimum occurs when the switching (AC) losses equal the conduction ($R_{DS(ON)}$) losses. High-side switching losses don't usually become an issue until the input is greater than approximately 15V.Switching losses in the high-side MOSFET can become an insidious heat problem when maximum AC adapter voltages are applied, due to the squared term in the CV^2F switching loss equation. If the chosen high-side MOSFET for adequate $R_{DS(ON)}$ at low battery voltages becomes extra-ordinarily hot when subjected to $V_{IN(MAX)}$, the choice of MOSFET must be reconsidered. Calculating the power dissipation in Q1 due to switching losses is difficult, since it must allow for difficult-to-quantify factors that influence the turn-on and turn-off times. These factors include the internal gate resistance, gate charge, threshold voltage, source inductance, and PC board layout characteristics. The following switching loss calculation provides only a very rough estimate and is no substitute for breadboard evaluation, preferably including a sanity check using a thermocouple mounted on Q1.

$$PD(Q1\ Switching) = \frac{C_{RSS} \times V_{in}^2 \times f \times I_{LOAD}}{I_{GATE}}$$

Where C_{RSS} is the reverse transfer capacitance of Q1 and I_{GATE} is the peak gate-drive source/sink current (1A typical). For the low-side MOSFET, Q2, the worst-case power dissipation always occurs at maximum battery voltage:

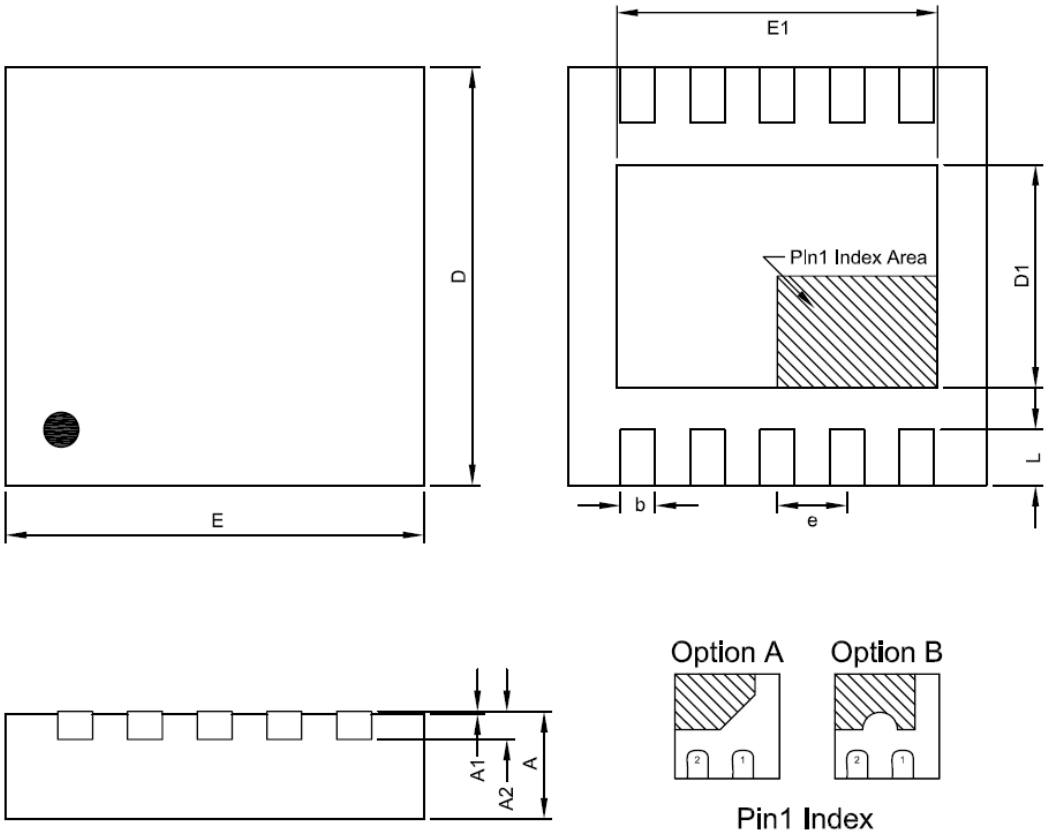
$$PD(Q2) = \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right) \times I_{LOAD}^2 \times R_{DS(ON)}$$

The absolute worst case for MOSFET power dissipation occurs under heavy overloads that are greater than $I_{LOAD(MAX)}$ but are not quite high enough to exceed the current limit and cause the fault latch to trip. To protect against this possibility, the circuit "overdesign" is necessary to tolerate $I_{LOAD} = I_{LIMIT(HIGH)} + (\Delta I_{LPP} / 2)$, where $I_{LIMIT(HIGH)}$ is the maximum valley current allowed by the current-limit circuit, including threshold tolerance and on-resistance variation. This means that the MOSFETs must be very well heatsinked. If short-circuit protection without overload protection is enough, a normal I_{LOAD} value can be used for calculating component stresses.

Layout Considerations

- Connect GND Pin (Thermal PAD) to ground of bypass VCC, and FB path.
- Connect ground of power component Low-side MOSFET source, anode of C_{IN}, and C_{OUT} to system ground by a plane.
- All sensitive analog traces such as FB should be placed away from high-voltage switching node such as LX, BST, DH, and DL nodes to avoid coupling.

Package Information

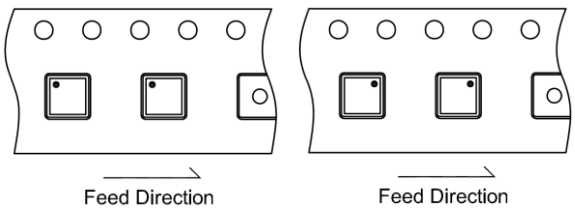


TDFN3X3-10 Package

Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.0276	0.0295	0.0315
A1	0.00	- - -	0.05	0.0000	- - -	0.0020
A2	0.20 REF			0.0079 REF		
D	2.95	3.00	3.05	0.1161	0.1181	0.1201
E	2.95	3.00	3.05	0.1161	0.1181	0.1201
D1	1.50	1.60	1.75	0.0591	0.0630	0.0689
E1	2.20	2.60	2.70	0.0866	0.1024	0.1063
b	0.18	0.25	0.30	0.0071	0.0098	0.0118
e	0.50 BSC			0.0197 BSC		
L	0.30	0.40	0.50	0.0118	0.0157	0.0197

Taping Specification

G5318RE1U **G5318RE1D**



PACKAGE	Q'TY/BY REEL
TDFN3X3-10	3,000 ea