High Efficiency 6A Synchronous Buck Converter

Features

- **Ultra-High Efficiency**
- **Integrated 20mΩ at VCC=5V N-Channel MOSFET for Low Side**
- **Integrated 20mΩ at VCC=5V N-Channel MOSFET for High Side**
- **No Current-Sense Resistor (Lossless I_{LIMIT})**
- **Quasi-PWM with 100ns Load-Step Response**
- **1% VOUT Accuracy Over Line and Load**
- **Programmable Switching Frequency**
- **Adjustable Output Range from 0.8V**
- **4.5V to 28V Adapter or Battery Input Range**
- **Integrated Boost Switch**
- **OVP & UVP**
- **Over Temperature Protection (non-latch)**
- **Adjustable Soft-Start**
- **Power-Good Indicator**

General Description

G5335A is a 6A, synchronous DC/DC buck converter with integrated 20mΩ N-channel high-side MOSFET and 20mΩ N-channel low-side MOSFET. It uses constant on-time control scheme to handle wide input/output voltage ratios with ease and provides 100ns "instant-on" response to load transients while maintaining a relatively constant switching frequency. The G5335A achieves high efficiency at a reduced cost by eliminating the current-sense resistor found in traditional current-mode PWMs. Single-stage buck conversion allows these devices to directly step down high-voltage batteries for the highest possible efficiency. The G5335A is intended for the power supply of Notebook Computer, or other low-voltage supplies as low as 0.8V. The G5335A is available in QFN4X4-23 package.

Applications

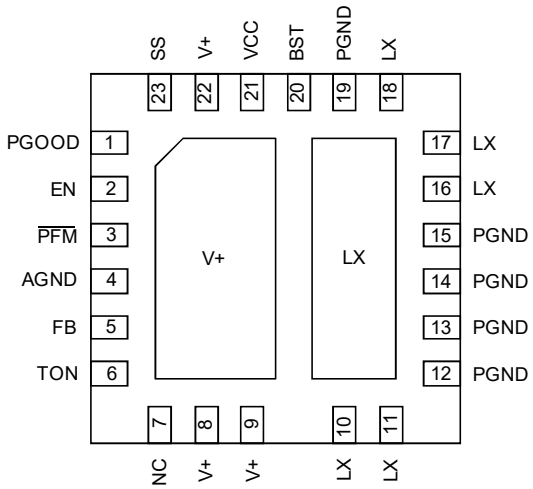
- **Notebook Computers**
- **I/O Supply**
- **Chipset/RAM Supply as Low as 0.8V**
- **Networking Power Supply**

Ordering Information

ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE (Green)
G5335AQT1U	5335A	-40°C to +85°C	QFN4X4-23

Note: QT: QFN4X4-23
1: Bonding Code
U : Tape & Reel
Green: Lead Free / Halogen Free

Pin Configuration



G5335A QFN4X4-23

Absolute Maximum Ratings

V+, TON to AGND . . . . . -0.3V to 30V
VCC to AGND . . . . . -0.3V to 6V
EN, FB, PGOOD, $\overline{PFM}$ to AGND . . . . . -0.3V to 6V
BST to PGND . . . . . -0.3V to 35V
LX to BST. . . . . -6V to 0.3V
LX to PGND . . . . . -0.3V to 30V
<30ns . . . . . -6V to 35V
V+ to LX <30ns. . ... -6V to 35V
Thermal Resistance of Junction to Ambient, (θ_{JA})
QFN4X4-23 . . . . . 25°C/W

Thermal Resistance of Junction to Ambient, (θ_{JC})
QFN4X4-23 . . . . . 4.5°C/W
Junction Temperature . . . . . .150°C
Storage Temperature . . . . . -65°C to 150°C
Reflow Temperature (soldering, 10sec) . . . . . 260°C
ESD (HBM) 2KV
ESD (MM) 200V

Electrical Characteristics

(VIN=15V, VCC=5V, EN=5V, T_A=25°C)

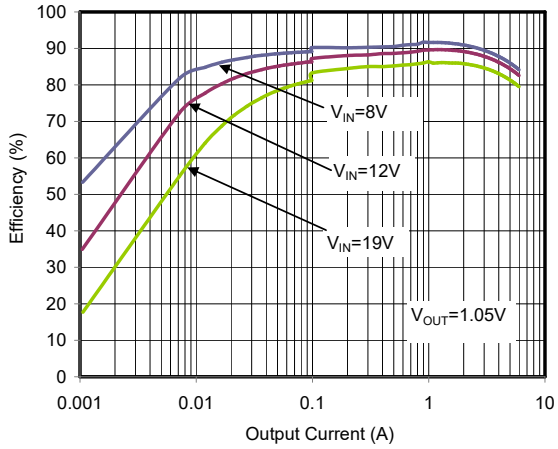
The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V+ Input Voltage Range	V+	4.5	---	28	V
VCC Input Voltage Range	VCC	4.5	5	5.5	V
Error Comparator Threshold (DC Output Voltage Accuracy)	VFB	0.792	0.8	0.808	V
SS Source Current	SS=0V	9	11	13	μA
On Time	VIN=12V, VOUT=1.05V, R_{TON} = 100kΩ, nominal	200	250	300	ns
Minimum On Time	VOUT=0.1V, R_{TON} = 100kΩ	---	80	---	ns
Minimum Off Time	FB=0.7V	---	400	---	ns
Quiescent Supply Current (VCC)	FB forced above the regulation point	---	80	---	μA
Shutdown Current (VCC+V+)		---	1	---	μA
Output Shutdown Discharge Resistance	EN=AGND	---	27	---	Ω
Overvoltage Trip Threshold	With respect to error comparator threshold	15	20	25	%
Overvoltage Fault Propagation Delay	FB forced 2% above the trip threshold	10	35	50	μs
Output Undervoltage Protection Threshold	With respect to error comparator threshold	60	70	80	%
Output Undervoltage Protection Blanking Time	From EN signal going high; Css=10nF	---	3.3	---	ms
Current-Limit Threshold	IVCC=5V	6.5	---	---	A
PGOOD Trip Threshold	Measure at FB with respect to error comparator threshold, falling edge	-14	-10	-7.5	%
PGOOD Output Low Voltage	ISINK=1mA	---	---	0.5	V
PGOOD Propagation Delay	From EN signal going high; Css=10nF	---	3.3	---	ms
Thermal Shutdown Threshold	Hysteresis=15°C	---	150	---	°C
VCC Undervoltage Lockout Threshold	Falling edge, hysteresis = 300mV,PWM disabled below this level	---	3.7	---	V
High Side Switch Resistance	BST - LX forced to 5V, VCC=5V	---	20	24	mΩ
Low Side Switch Resistance	VCC=5V	---	20	24	mΩ
BST Switch Forward Voltage	Forwarding Current=10mA	0.2	0.35	0.4	V
Logic Input High Voltage	EN, $\overline{PFM}$	1.65	---	---	V
Logic Input Low Voltage	EN, $\overline{PFM}$	---	---	0.5	V

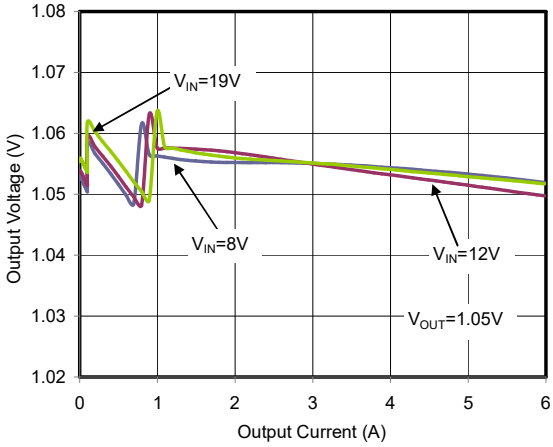
Typical Performance Characteristics

Condition as Application Circuit, V_{IN}=12V, V_{OUT}=1.05V, T_A=25°C, unless otherwise noted.
C_{OUT}=Ceramic 22µF*5

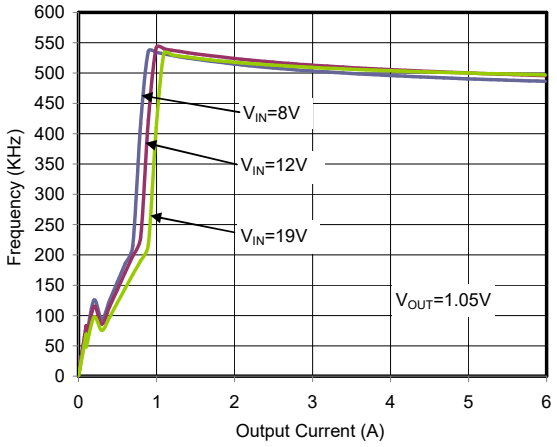
Efficiency vs. Load Current (V_{OUT}=1.05V)



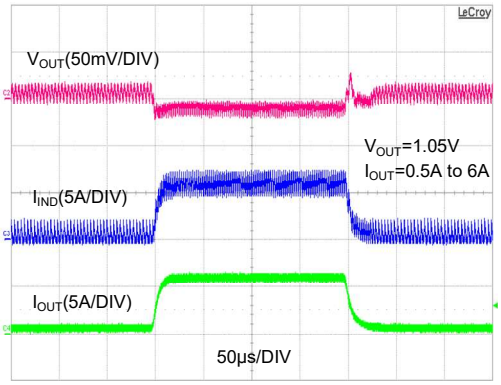
Output Voltage vs. Load Current (V_{OUT}=1.05V)



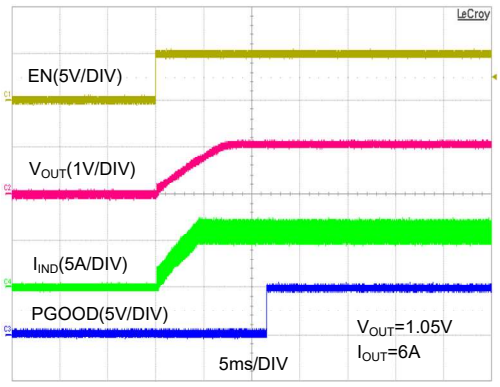
Switching Frequency vs. Load Current (V_{OUT}=1.05V)



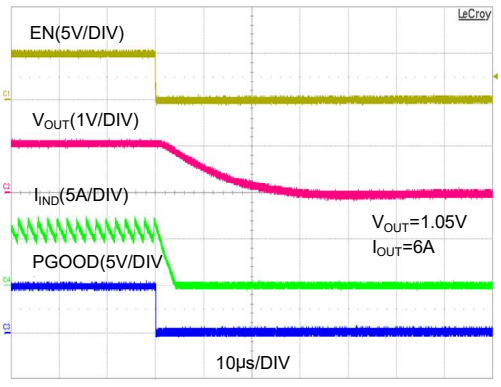
Load Transient Response (V_{OUT}=1.05V)



Soft-start Waveforms



Soft-stop Waveforms



Pin Description

PIN	NAME	FUNCTION
1	PGOOD	Power-Good Open-Drain Output. PGOOD is low when the output voltage is more than 10% below the normal regulation point or during soft-start. PGOOD is high impedance when the output is in regulation and the soft-start circuit has terminated.
2	EN	Shutdown Input. Drive EN to GND to force the G5335A into shutdown. A rising edge on EN clears the fault latch.
3	$\overline{PFM}$	PFM Selection Pin. Connect to VCC for forced PWM mode, connect to GND for PFM mode
4	AGND	Analog Ground
5	FB	Feedback Input. Connect FB to a resistor divider from OUT for an adjustable output.
6	TON	On-Time Selection-Control Input. Connect to V+ with a resistor, R_{TON}.
7	NC	No connection
8,9,22	V+	Power Supply Input. V+ is used to set the PWM one-shot Timing. Bypass to GND with a 4.7μF (min) Capacitor.
10,11,16,17,18	LX	External Inductor Connection. Connect LX to the switched side of the inductor. LX serves as the lower supply rail for the DH high-side gate driver. LX is also the positive input to the current-limit comparator.
12,13,14,15,19	PGND	Power Ground. Source node of low side power MOSFET.
20	BST	Boost Flying-Capacitor Connection. Connect to an external capacitor according to the Standard Application Circuit. See *MOSFET Gate Drivers (DH, DL)* section.
21	VCC	Analog Supply Input and Supply for Internal circuits. Bypass to AGND with a 4.7μF (min) ceramic capacitor.
23	SS	Soft_start Time Setting Pin. Connect a capacitor between SS to AGND to set the soft –start time

Application Information

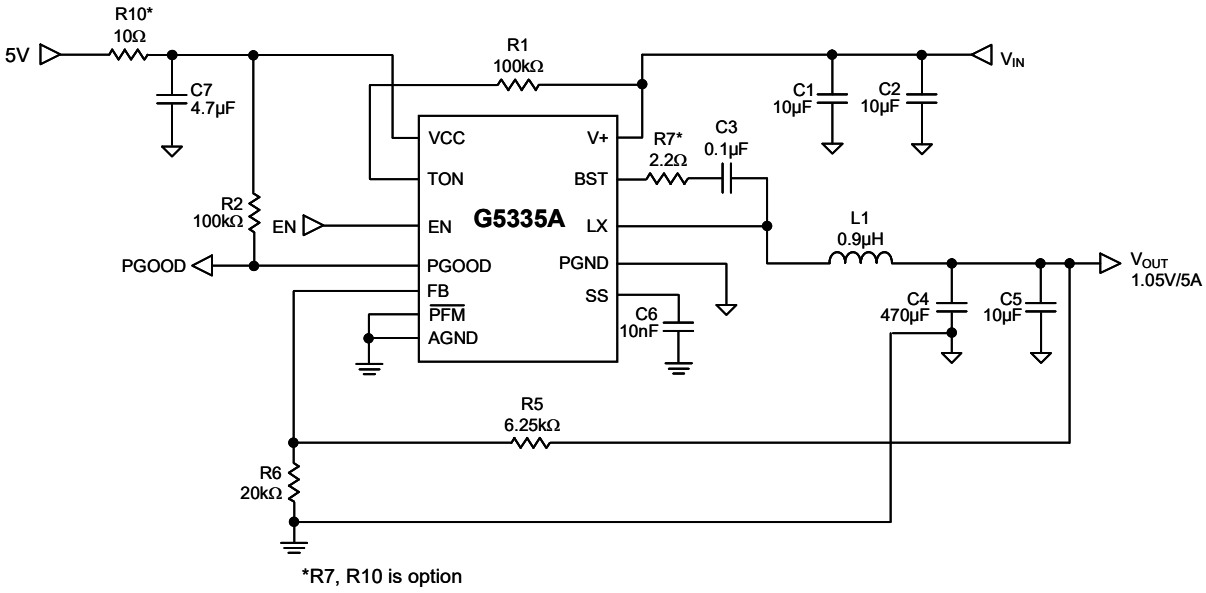


Fig. 1-A Standard Application Circuit

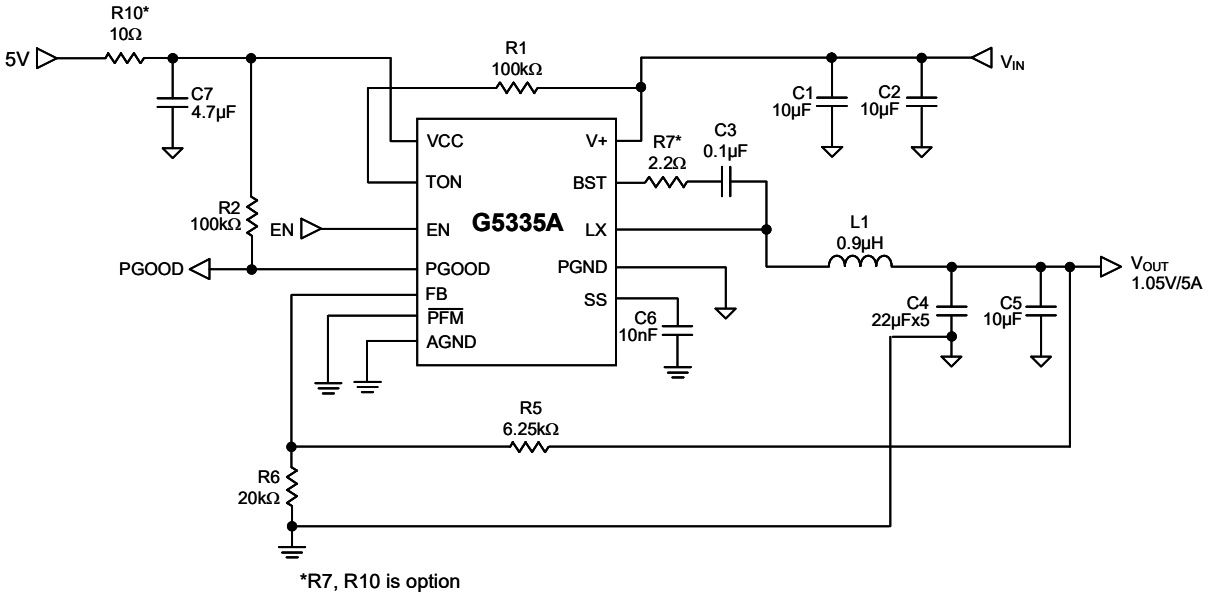


Fig. 1-B Application Circuit with MLCC Type Output Capacitor

Block Diagram

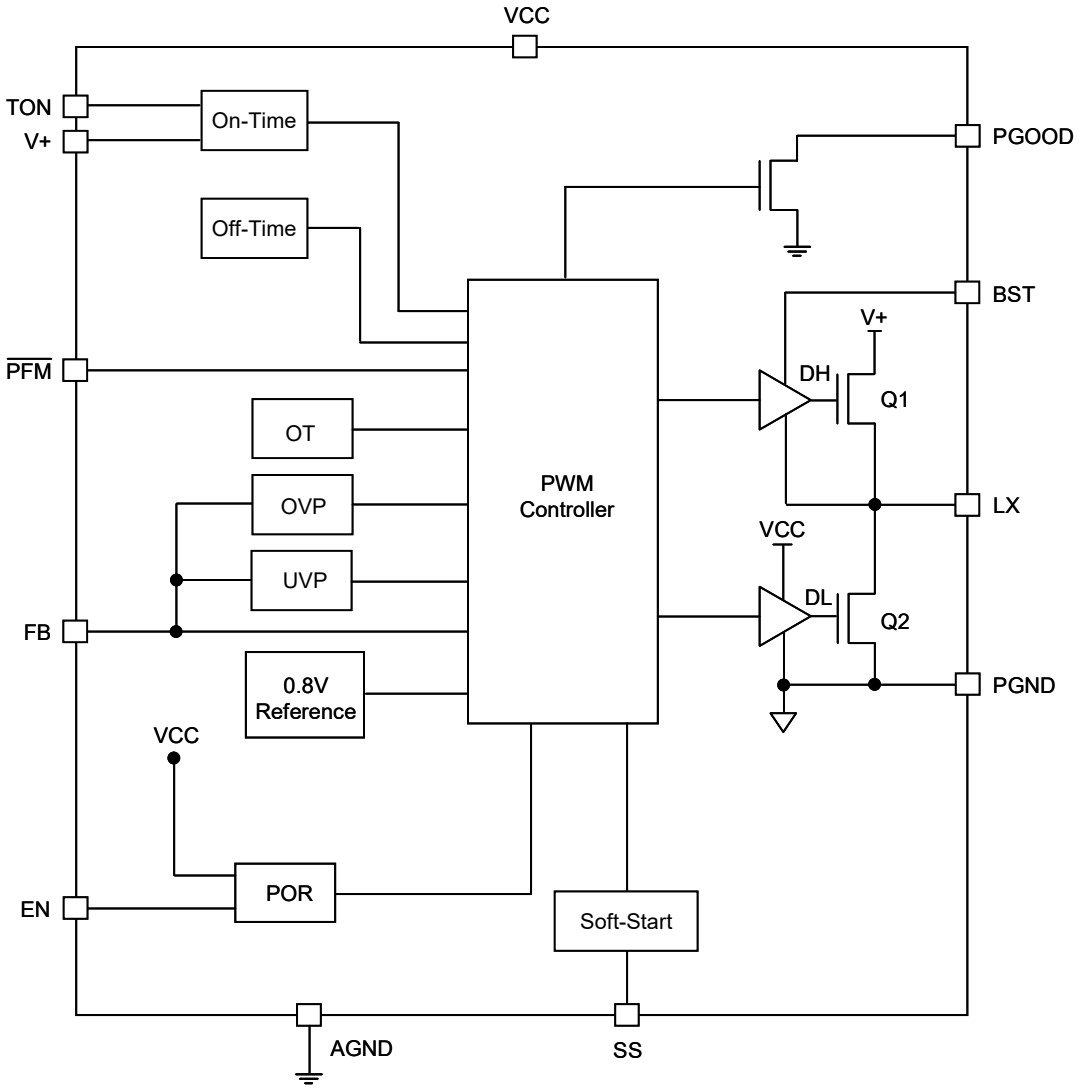


Fig. 2 Block Diagram of G5335A

Table 1. Component Selection for Standard Application (Fig. 1) :

SYMBOL	SPECIFICATION	MANUFACTURER	PART NUMBER
C1, C2	10μF, 25V	Taiyo Yuden	TMK316BJ106KL
L1	0.9μH	SUMIDA	OR9MC-95
C4	470μF, 2.5V, 15mΩ	KEMET	T520V477M2R5A(1)E015

Detailed Description

G5335A is a 6A, synchronous buck converter. A Quasi-PWM control is adapted in G5335A. It is a constant-on-time PWM control with input feed-forward while maintaining a relatively constant switching frequency. It advantages in the fast load-transient response compared with conventional constant-on-time PWM control. The Figure 2 shows the Block Diagram of G5335A.

5V Bias Supply (VCC)

G5335A required a 5V bias supply for the internal PWM circuit and gate-drivers. In the NB computer, there is a high efficiency 5V system supply and eliminate the cost of external LDO. Bypass VCC to GND with 4.7μF(min) capacitor and close to the device.

Constant-on-time PMW Control with Input Feed-Forward

The Quasi-PWM control algorithm can be described briefly: the high-side switch on-time is determined by a one-shot whose period is inversely proportional to input voltage and directly proportional to output voltage. Another on-shot determines the minimum off-time. The on-time one-shot can be triggered if the error comparator is low, the low side switch current is below the current-limit threshold, and the minimum off-time one-shot has timed out.

On-Time Selection

G5335A allows to program the on-time. The on time is determined as below

$$T_{ON} = \frac{R_{TON}}{V_{IN}} \times 2.63 \times 10^{-11}$$

It results in a nearly constant switching frequency R_{TON} is a resistor connected from V_{IN} to the TON pin.

Pulse-Skipping Mode and Forced PWM Mode

Connect $\overline{PFM}$ to ground, G5335A operates in Pulse-Skipping Mode. An automatic switchover to PFM takes place at light load. It turns off the low side switch when the inductor current crosses to zero. This scheme will improve the light-load efficiency. Connect $\overline{PFM}$ to VCC, G5335A operates in forced PWM mode. The fixed frequency PWM mode reduces the RF interference in sensitive application.

Current Limit

G5335A uses the on-state resistance of low side MOSFET as a current-sensing resistor. If the current–sense voltage (PGND-LX) is above the current-limit threshold, the PWM is not allowed to initiate a new cycle. The actual peak current is the current-limit threshold adding one inductor current ripple. So it depends on the on-resistance of MOSFET, Inductor value, and battery voltage. No external current-sensing resistor is necessary in the output current path. The current-limit threshold is set as 6.5A.

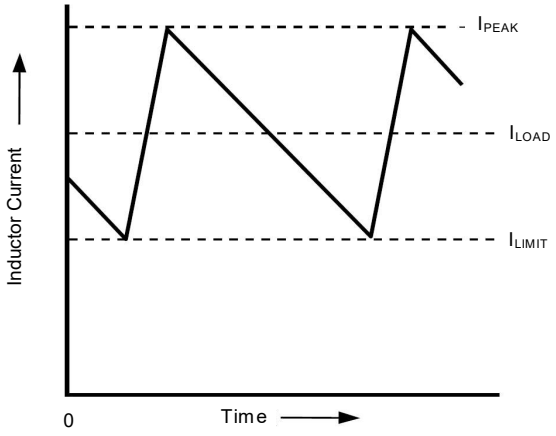


Fig. 3 Current Limit Setting

Gate Drivers

In the low duty factor application, it exists large difference of input voltage and output voltage. Therefore, large low-side MOSFET and moderate-size high-side MOSFET are needed for high efficiency. The DH and DL drivers are optimized for driving high-side and low-side MOSFETs. A non-overlap control circuit is needed to avoid the DH and DL turning on simultaneously. The DL driver with a 0.5Ω pull low transistor helps prevent the DL from being coupled to high during the fast rising-time of the LX node, due to the drain to gate capacitive coupling of low-side synchronous-rectifier MOSFET. A resistor in series with the BST is recommended that will reduce the EMI-producing efficiency loss by increasing the turn-on time of the high-side MOSFET.

POR, UVLO, and Soft-Start

Power-on reset (POR) occurs when VCC rises above approximately 2V. It reset the fault latch and soft-start counter. When VCC is below 3.7V, undervoltage lockout (UVLO) inhibits switching and forces DL to high. An internal soft-start timer ramps up the current limit threshold to 100% of current limit setting within soft-start time. The soft-start time could be calculated as below:

$$T_{SS}(\mu s) = 106 \times C_{SS}(nF) \times 11 / I_{SS}(\mu A)$$

Power-Good Indicator

The Output voltage is always monitored for undervoltage by the PGOOD comparator. The PGOOD is open-drain type signal. In shutdown and soft-start period, PGOOD is kept low. After the soft-start timer has timed out, the PGOOD is released if the output voltage is within 10% of normal value. The PGOOD delay time could be calculated as below:

$$T_D(\mu s) = 330 \times C_{SS}(nF) \times 11 / I_{SS}(\mu A)$$

Fault Protection

G5335A provides undervoltage protection, overvoltage protection, and overtemperature protection.

The undervoltage protection (UVP) function is like foldback current limit function. If the output voltage is under 70% of normal value 3.3ms (Css=10nF) after shutdown released, the undervoltage protection function is activated. The PWM is latched off and would not restart until VCC power is cycled or EN is toggled.

The overvoltage protection (OVP) function activates when the output voltage is 20% above the set voltage. The low-side MOSFET turn on 100% and the high-side MOSFET turn off. This rapidly discharges the output capacitor and decreases the output voltage. The SMPS is latched off and would not restart until VCC power is cycled or EN is toggled.

The G5335A has an overtemperature protection (OTP) that occurs when the die temperature is above 150C. It will shutdown the PWM and force high-side and low-side gate drivers output low. It could be released when die cool down or VCC power is cycled or EN is toggled.

Adjustable-Output Feedback

Connecting the FB pin to a resistor divider between OUT to GND to adjust the output voltage from 0.8V. Chose R6=20kΩ and solve the R5 with the equation:

$$R5 = R6 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right)$$

where V_{FB} = 0.8V norminal.

Test Mode

A test mode is provided for system developing stage. It can disable all the OVP, UVP, and thermal shut-down features, and clear the fault latch if it has been set. Force the EN pin above VCC by external sourcing current, G5335A enters a no-fault test mode. (No more than 0.6V above VCC is allowable).

Application Information

Inductor Selection

The inductor value is determined as follows:

$$L = \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN} \times f \times \Delta I_{LPP}}$$

Where ΔI_{LPP} is defined as inductor ripple current.

The inductor ripple current also impacts transient-response performance, especially at low V_{IN}- V_{OUT} differentials. Low inductor values allow the inductor current to slew faster, replenishing charge removed from the output filter capacitors by a sudden load step.

Maintaining the ratio of the inductor ripple current to the designed maximum load current within a 20% to 50% range is prudent.

Output Capacitor Selection

The output filter capacitor must have low enough effective series resistance (ESR) to meet output ripple and load-transient requirements, yet have high enough ESR to satisfy stability requirements. Also, the capacitance must be high enough to absorb the inductor energy going from a full-load to no-load condition without tripping the overvoltage protection circuit.

The output filter capacitor could be used with MLCC type capacitor. It is recommended to use 22μF x 5 (minimum) as output capacitor.

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Input Capacitor Selection

The input capacitor must meet the ripple current requirement (I_{RMS}) imposed by the switching currents. Nontantalum chemistries (ceramic, aluminum, or OS-CON) are preferred due to their resistance to power-upsurge currents.

For optimal circuit reliability, choose a capacitor that has less than 10°C temperature rise at the peak ripple current.

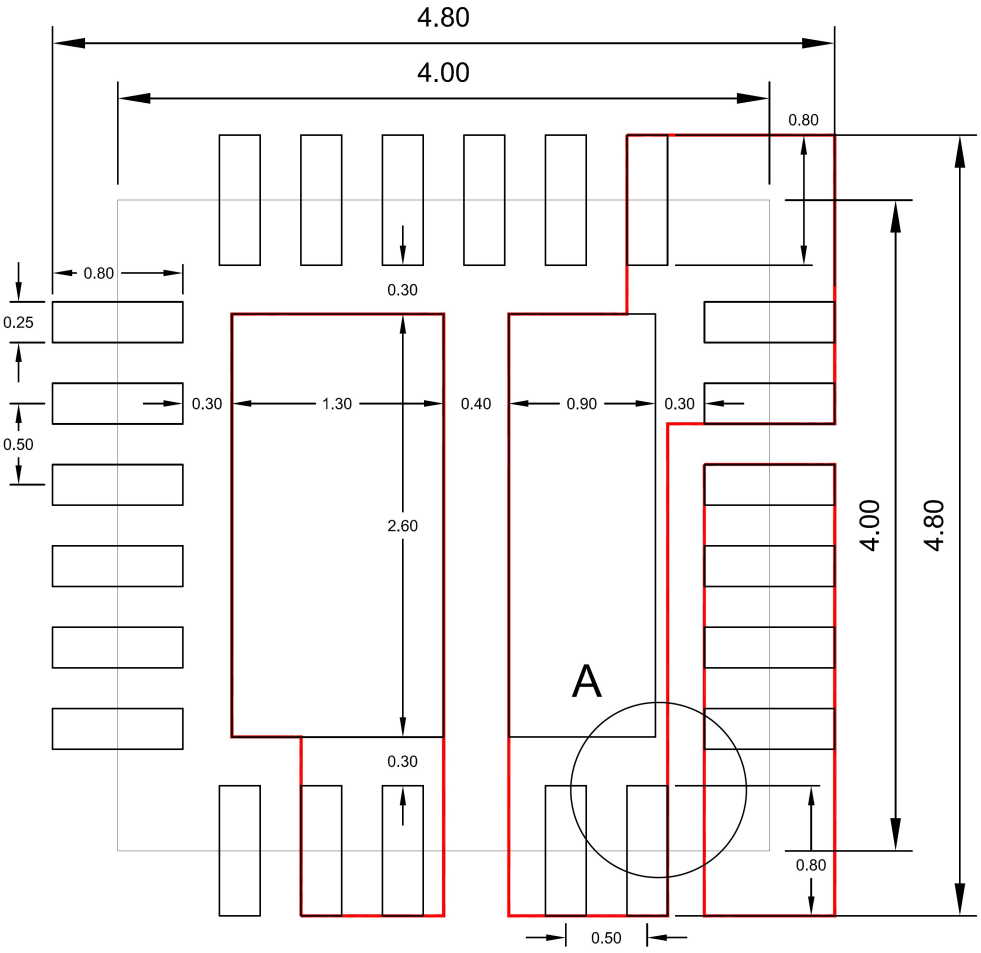
$$I_{RMS} = I_{LOAD}\left(\frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}\right)$$

Layout Considerations

- Connect AGND (Pin4) to ground of bypass VCC and FB path.
- Connect AGND and PGND together close to the IC and the negative terminal of C_{OUT}.
- Star connection PGND ground plane to system ground (normally, it's defined as ground of power supply or battery pack.).
- Connect PGND of power component Low-side MOSFET source, C_{IN}, and C_{OUT} to system ground by a plane.
- All sensitive analog traces such as OUT, and FB should be placed away from high-voltage switching node such as LX, BST nodes to avoid coupling.

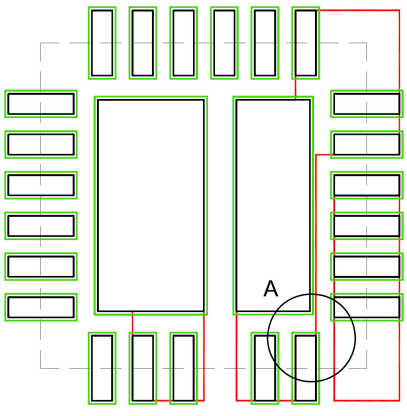
Minimum Footprint PCB Layout Section

QFN4X4-23

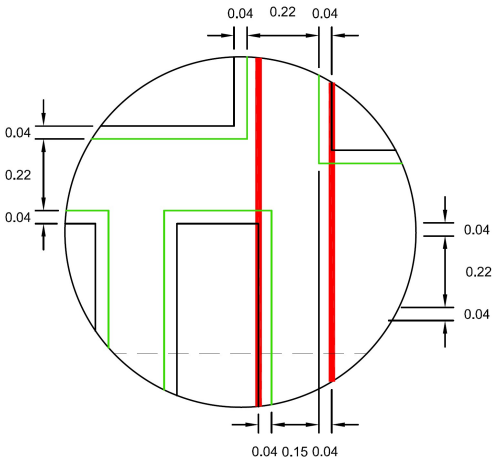


Top Layer

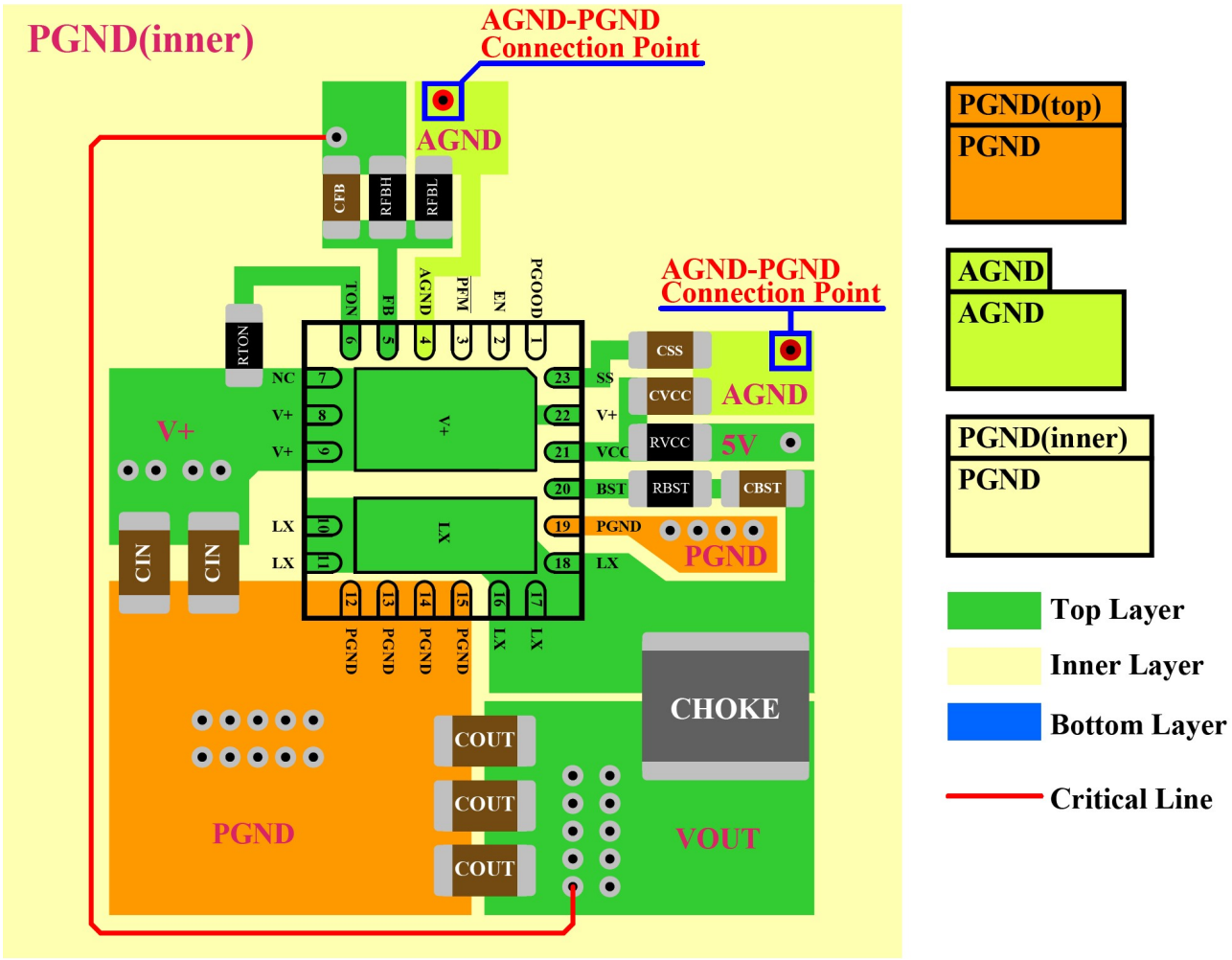
* Recommend Top Layer Thermal Pad Design Following Red Line for Better Characteristic.



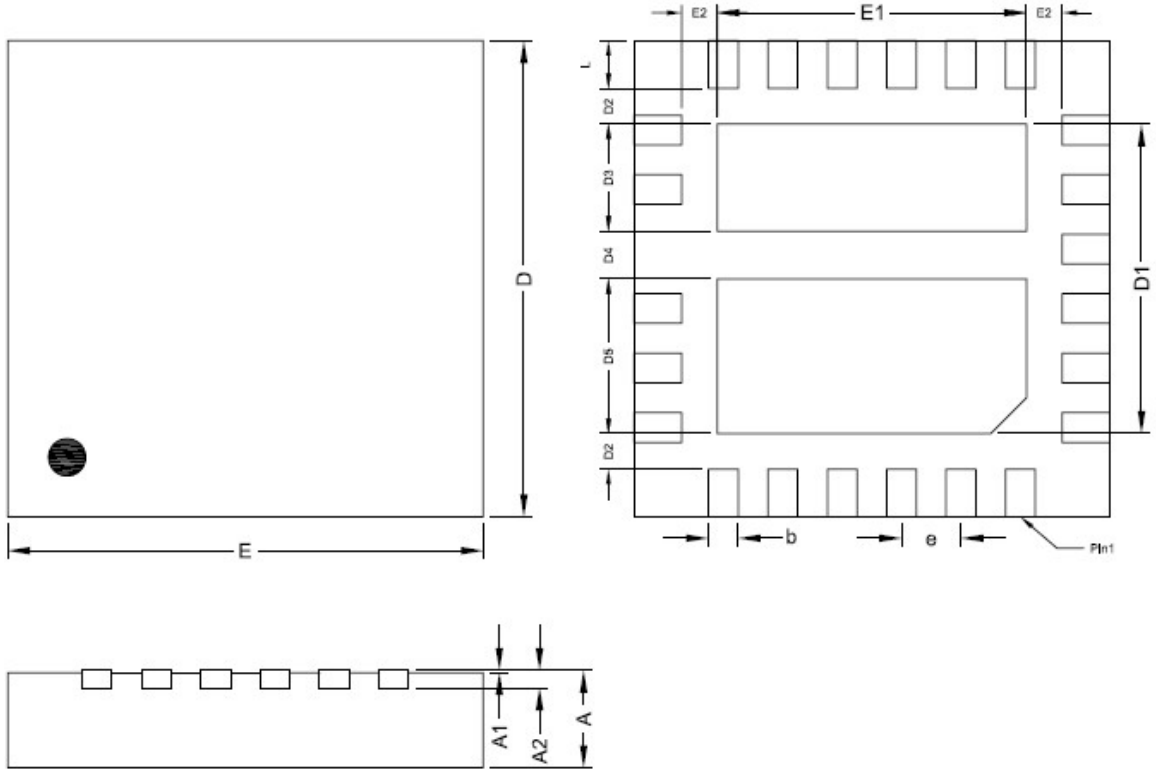
Top Layer with Solder Mask



Section A


PGND(inner)
AGND-PGND
Connection Point
AGND
CFB
RFBH
RFBL
TON
FB
AGND
PEM
EN
PGOOD
RTON
AGND-PGND
Connection Point
CSS
CVCC
AGND
RVCC
5V
CBST
RBST
NC
V+
V+
V+
SS
V+
VCC
BST
PGND
LX
PGND
LX
LX
CIN
CIN
PGND
PGND
PGND
PGND
LX
LX
CHOKE
COUT
COUT
COUT
PGND
VOUT
PGND(top)
PGND
AGND
AGND
PGND(inner)
PGND
Top Layer
Inner Layer
Bottom Layer
Critical Line

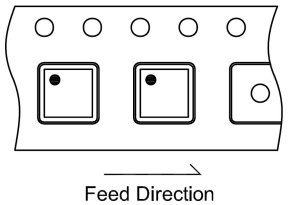
Package Information



QFN4X4-23 Package

Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0,70	0,80	0,90	0,0276	0,0315	0,0354
A1	0,00	---	0,05	0,0000	---	0,0020
A2		0,20 REF			0,0079 REF	
D	3,95	4,00	4,05	0,1555	0,1575	0,1594
E	3,95	4,00	4,05	0,1555	0,1575	0,1594
D1	2,50	2,60	2,70	0,0984	0,1023	0,1063
E1	2,50	2,60	2,70	0,0984	0,1023	0,1063
D2		0,30 BSC			0,0118 BSC	
E2		0.30 BSC			0.0118 BSC	
D3	0.85	0.90	0.95	0.0335	0.0354	0.0374
D4	0.35	0.40	0.45	0.0138	0.0157	0.0177
D5	1.25	1.30	1.35	0.0492	0.0512	0.0531
b	0.20	0.25	0.30	0.0079	0.0098	0.0118
e		0.50 BSC			0.0197 BSC	
L	0.35	0.40	0.45	0.0138	0.0157	0.0177

Taping Specification



PACKAGE	Q'TY/BY REEL
QFN4X4-23	3,000 ea