High Efficiency 5A Synchronous Buck Converter

Features

- **Ultra-High Efficiency**
- **Low Quiescent Current of 30μA**
- **Integrated 30mΩ at V5V=5V N-Channel MOSFET for Low Side**
- **Integrated 30mΩ at V5V=5V N-Channel MOSFET for High Side**
- **No Current-Sense Resistor (Lossless I_{LIMIT})**
- **Quasi-PWM with 100ns Load-Step Response**
- **1% VOUT Accuracy Over Line and Load**
- **Programmable Switching Frequency**
- **Adjustable Output Range from 0.9V**
- **4.5V to 28V Adapter or Battery Input Range**
- **Integrated Boost Switch**
- **OVP & UVP**
- **Over Temperature Protection (non-latch)**
- **3.3ms Soft-Start**
- **Power-Good Indicator**
- **Fixed 5V, 10mA Linear Regulator**

General Description

G5383B is a 5A, synchronous DC/DC buck converter with integrated 30mΩ N-channel high-side MOSFET and 30mΩ N-channel low-side MOSFET. It uses constant on-time control scheme to handle wide input/output voltage ratios with ease and provides 100ns "instant-on" response to load transients while maintaining a relatively constant switching frequency. The G5383B achieves high efficiency at a reduced cost by eliminating the current-sense resistor found in traditional current-mode PWMs. Single-stage buck conversion allows these devices to directly step down high-voltage batteries for the highest possible efficiency. The built-in 5V LDO supports 10mA for internal circuits. The G5383B is intended for the power supply as low as 0.9V. The G5383B is available in QFN3X3-24 package.

Applications

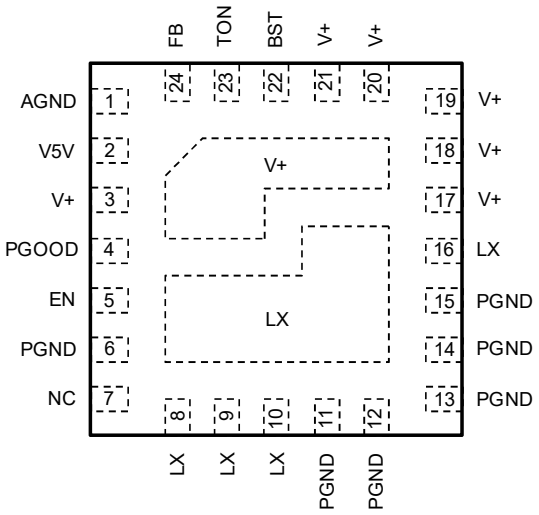
- **Networking Power Supply**
- **I/O Supply**

Ordering Information

ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE (Green)
G5383BQU1U	5383B	-40°C to +85°C	QFN3X3-24

Note: QU: QFN3X3-24
1: Bonding Code
U : Tape & Reel
Green : Lead Free / Halogen Free

Pin Configuration



G5383B QFN3X3-24

Absolute Maximum Ratings

V+ to AGND . . . . . -0.3V to 30V
V5V to AGND . . . . . -0.3V to 6V
EN, PGOOD to AGND . . . . . -0.3V to 6V
FB, TON to AGND . . . . . -0.3V to (V5V+0.3V)
BST to PGND . . . . . -0.3V to 35V
LX to BST . . . . . -6V to 0.3V
LX to PGND . . . . . -0.3V to 30V
<20ns . . . . . -6V to 35V
Thermal Resistance of Junction to Ambient, (θ_{JA})*
QFN3X3-24 . . . . . 28°C/W

Continuous Power Dissipation (T_A = +25°C)*
QFN3X3-24 . . . . . 4.25W
Thermal Resistance of Junction to Case, (θ_{JC}) *
QFN3X3-24 . . . . . 10°C/W
Junction Temperature . . . . . 150°C
Storage Temperature . . . . . -65°C to 150°C
Reflow Temperature (soldering, 10sec) . . . . . 260°C
ESD (HBM) 2KV
ESD (MM) 200V

*Please refer to EV Board PCB Layout Section.

Electrical Characteristics

(VIN=15V, V5V=5V, EN=5V, T_A=25°C)

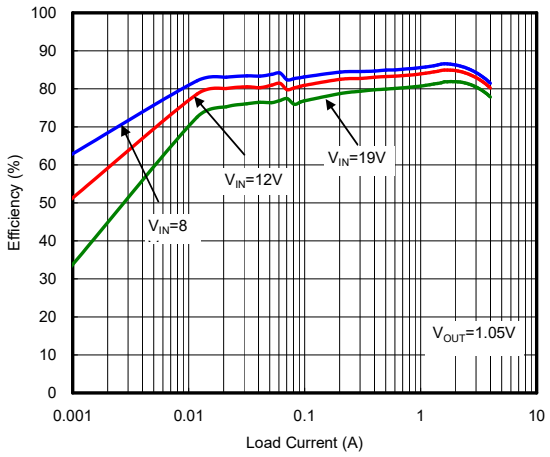
The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V+ Input Voltage Range	V+	4.5	---	28	V
LDO Output Voltage	V5V, V+ ≥ 6V	4.75	4.95	5.25	V
Error Comparator Threshold (DC Output Voltage Accuracy)	FB	0.891	0.9	0.909	V
Soft-Start Ramp Time	Rising edge of EN to 95% output voltage	---	3.3	---	ms
TON Operating Current	R_{TON} = 1000kΩ, V+ = 15V	---	15	---	μA
On Time	VLX=12V, VOUT=1.05V, R_{TON} = 240kΩ, nominal	---	310	---	ns
Minimum On Time	FB=0.1V, R_{TON} = 240kΩ	---	80	---	ns
Minimum Off Time	FB=0.7V, LX=-0.1V	---	400	---	ns
Quiescent Supply Current (V+)	FB forced above the regulation point	---	30	---	μA
Shutdown Current (V+)		---	1	---	μA
Output Shutdown Discharge Resistance	EN=AGND	---	50	---	Ω
Overvoltage Trip Threshold	With respect to error comparator threshold	15	20	26	%
Overvoltage Fault Propagation Delay	FB forced 2% above the trip threshold	10	25	50	μs
Output Undervoltage Protection Threshold	With respect to error comparator threshold	60	70	80	%
Output Undervoltage Protection Blanking Time	From EN signal going high	---	5.5	---	ms
Current-Limit Threshold (Positive Direction)		5	6	8	A
Current-Limit Threshold (Zero Crossing)		---	0.1	---	A
PGOOD Trip Threshold	Measure at FB with respect to error comparator threshold, falling edge	-14	-10	-7.5	%
PGOOD Output Low Voltage	ISINK=1mA	---	---	0.2	V
PGOOD Propagation Delay		---	5	16	μs
Thermal Shutdown Threshold	Hysteresis=15°C	---	135	---	°C
V5V Undervoltage Lockout Threshold	Rising edge, hysteresis = 200mV, PWM disabled below this level	3.7	---	4.3	V
High Side Switch Resistance	BST - LX forced to 5V, V5V=5V	---	30	40	mΩ
Low Side Switch Resistance	V5V=5V	---	30	40	mΩ
BST Switch Forward Voltage	Forwarding Current=10mA	0.2	0.35	0.4	V
Logic Input High Voltage	EN	1.65	---	V5V	V
Logic Input Low Voltage	EN	---	---	0.8	V

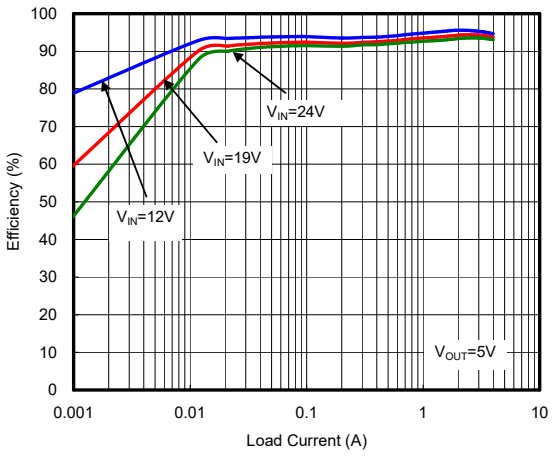
Typical Performance Characteristics

Condition as Application Circuit, V_{IN}=12V, V_{OUT}=1.05V, T_A=25°C, unless otherwise noted.

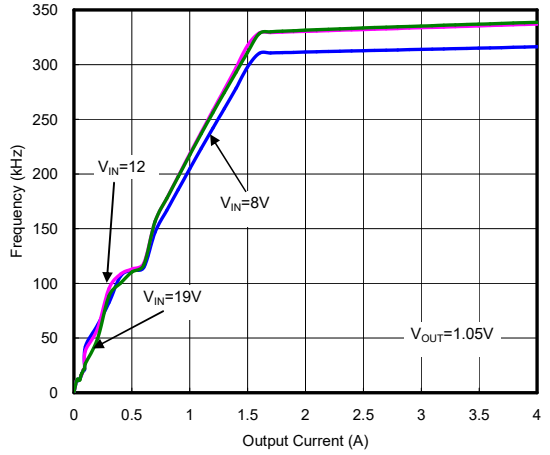
Efficiency vs. Load Current (V_{OUT}=1.05V)



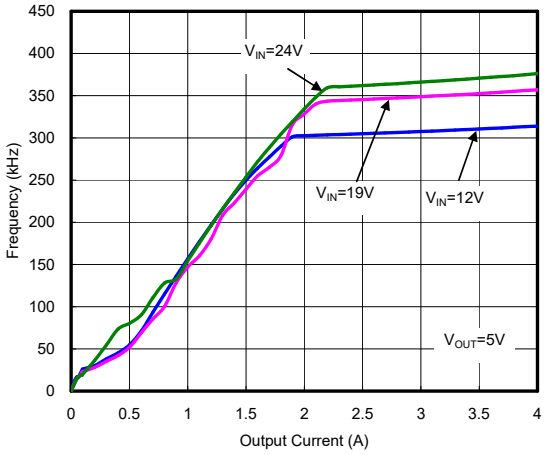
Efficiency vs. Load Current (V_{OUT}=5V)



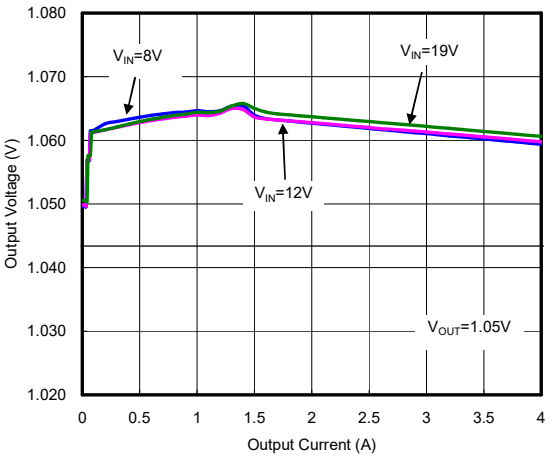
Switching Frequency vs. Load Current (V_{OUT}=1.05V)



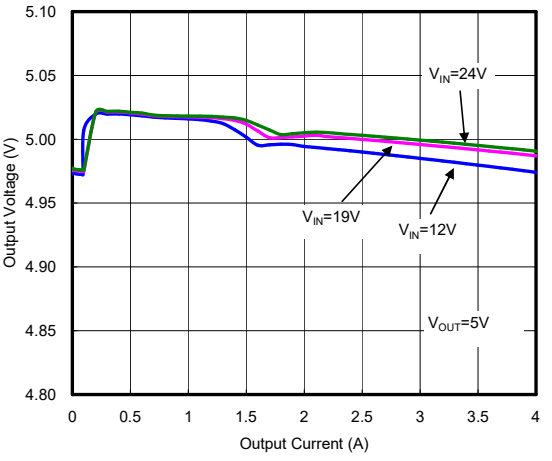
Switching Frequency vs. Load Current (V_{OUT}=5V)



Output Voltage vs. Load Current (V_{OUT}=1.05V)

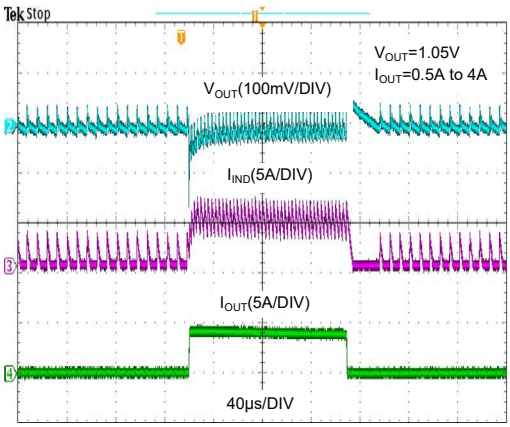


Output Voltage vs. Load Current (V_{OUT}=5V)

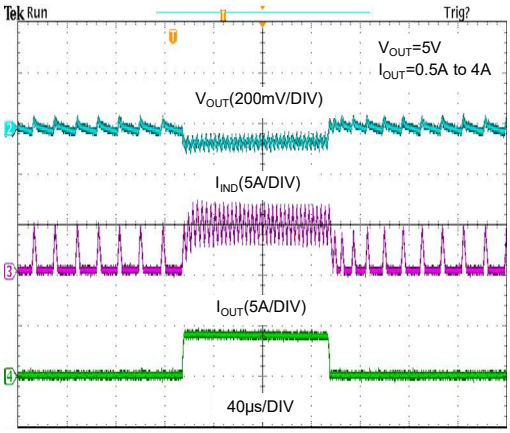


Typical Performance Characteristics (continued)

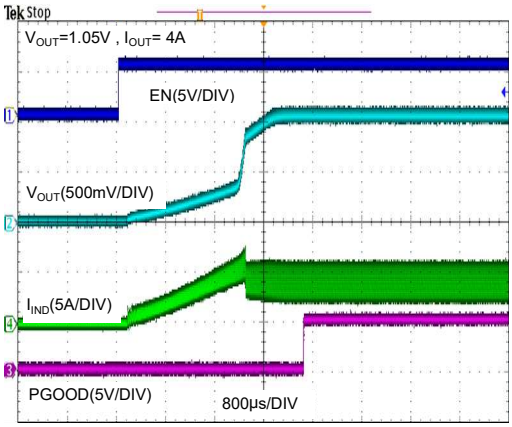
Load Transient Response (V_{OUT}=1.05V)



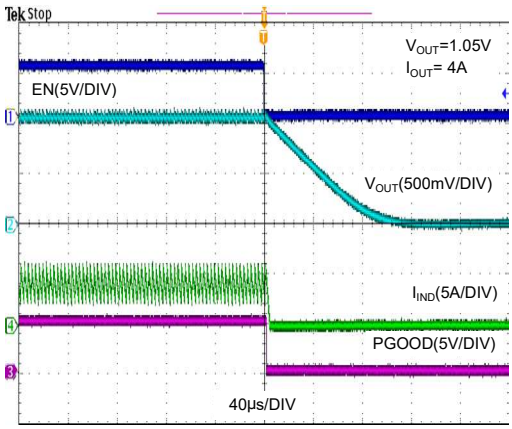
Load Transient Response (V_{OUT}=5V)



Soft-start Waveforms



Soft-stop Waveforms



Pin Description

PIN	NAME	FUNCTION
1	AGND	Analog Ground
2	V5V	5V Linear Regulator Output and Supply for DL Gate Driver. Bypass to GND with a 10μF (min) ceramic capacitor.
3,17,18,19,20,21	V+	Power Supply Input. V+ is used to set the PWM one-shot Timing. Bypass to GND with a 4.7μF (min) Capacitor.
4	PGOOD	Power-Good Open-Drain Output. PGOOD is low when the output voltage is more than 10% below the normal regulation point or during soft-start. PGOOD is high impedance when the output is in regulation and the soft-start circuit has terminated.
5	EN	Shutdown Input. Drive EN to GND to force the G5383B into shutdown. A rising edge on EN clears the fault latch.
6,11,12,13,14,15	PGND	Power Ground. Source node of low side driver and power MOSFET.
7	NC	No Connection
8,9,10,16	LX	External Inductor Connection. Connect LX to the switched side of the inductor. LX serves as the lower supply rail for the DH high-side gate driver. LX is also the positive input to the current-limit comparator.
22	BST	Boost Flying-Capacitor Connection. Connect to an external capacitor according to the Standard Application Circuit. See *MOSFET Gate Drivers (DH, DL)* section.
23	TON	On-Time Selection-Control Input. Connect to LX with a resistor, R_{TON}.
24	FB	Feedback Input. Connect FB to a resistor divider from OUT for an adjustable output.

Application Information

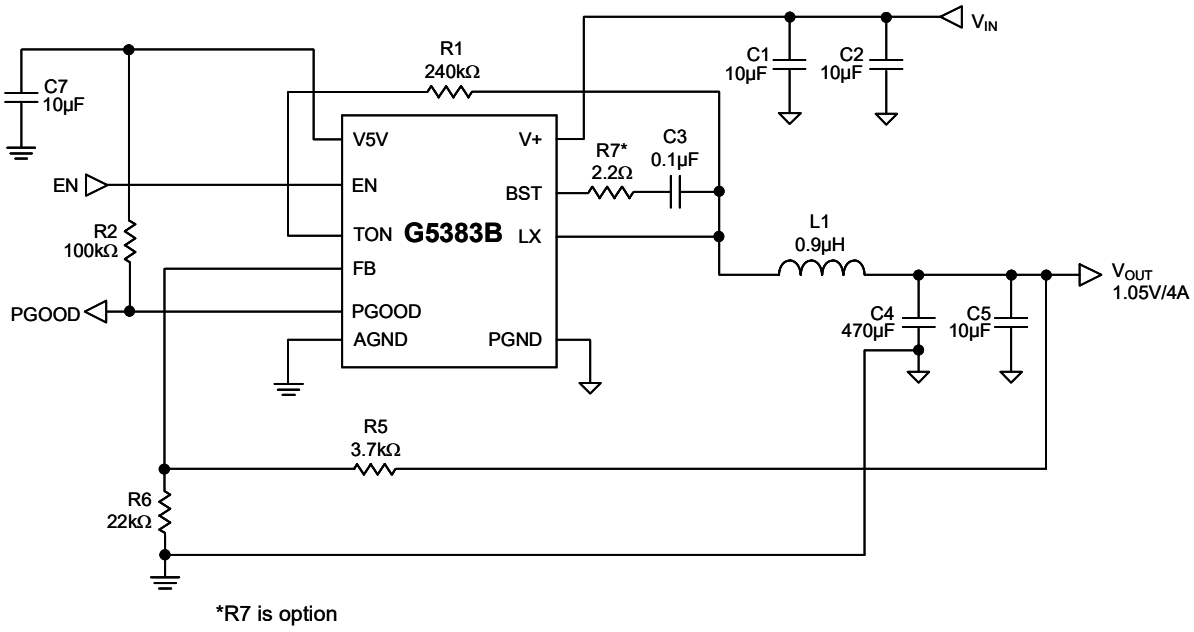


Fig. 1-A Standard Application Circuit

Application Information (continued)

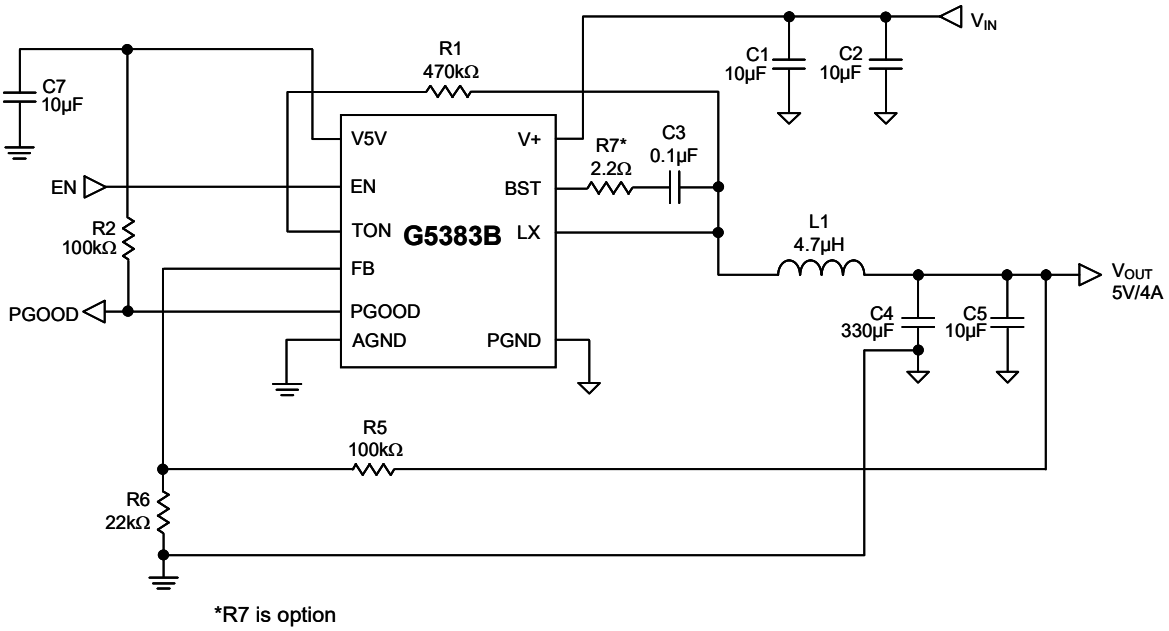


Fig. 1-B 5V Output Application Circuit

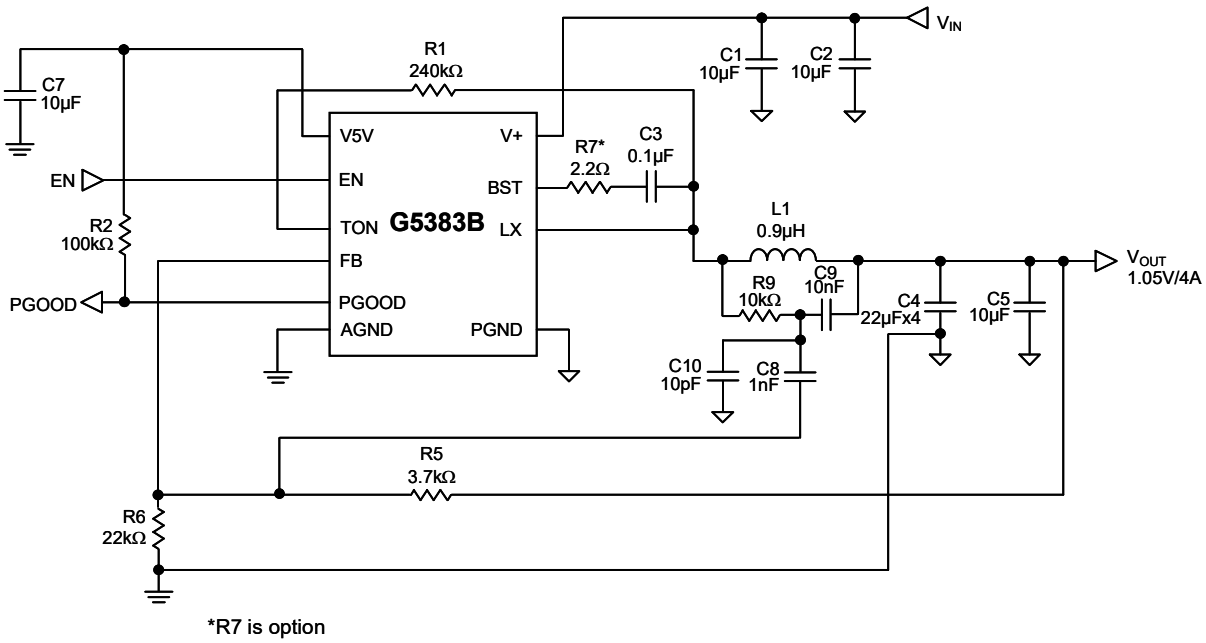


Fig. 1-C Application Circuit with MLCC Type Output Capacitor

Block Diagram

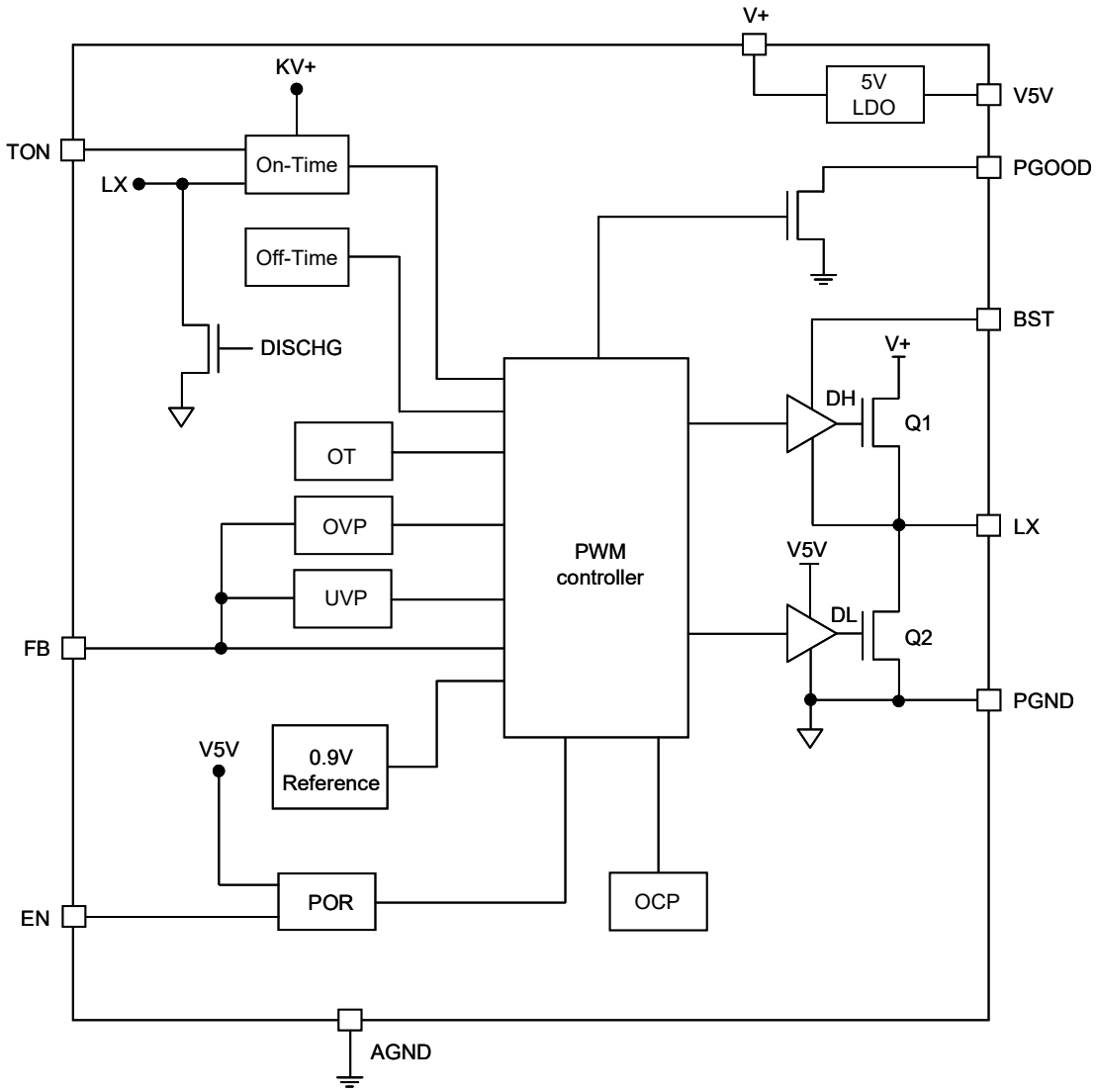


Fig. 2 Block Diagram of G5383B

Table 1. Component Selection for Standard Application (Fig. 1) :

SYMBOL	SPECIFICATION	MANUFACTURER	PART NUMBER
C1, C2	10μF, 25V	Taiyo Yuden	TMK316BJ106KL
L1	0.9μH	SUMIDA	OR9MC-95
C4	470μF, 2.5V, 15mΩ	KEMET	T520V477M2R5A(1)E015

Detailed Description

G5383B is a 5A, synchronous buck converter with a fixed 5V LDO. A Quasi-PWM control is adapted in G5383B. It is a constant-on-time PWM control with input feed-forward while maintaining a relatively constant switching frequency. It advantages in the fast load-transient response compared with conventional constant-on-time PWM control. The Figure 2 shows the Block Diagram of G5383B.

5V Linear Regulator

G5383B contains a linear regulator with fixed 5V output (V5V). LDO supports up to 10mA for external load and supports a 5V bias supply for the internal PWM circuit and gate-drivers. Bypass LDO output to GND with 10μF(min) Capacitor and close to the device.

Constant-on-time PMW Control with Input Feed-Forward

The Quasi-PWM control algorithm can be described briefly: the high-side switch on-time is determined by a one-shot whose period is inversely proportional to input voltage and directly proportional to output voltage. Another on-shot determines the minimum off-time. The on-time one-shot can be triggered if the error comparator is low, the low side switch current is below the current-limit threshold, and the minimum off-time one-shot has timed out.

Switching Frequency Selection

G5383B allows to program the switching frequency. The switching frequency is determined as below Figure 3.

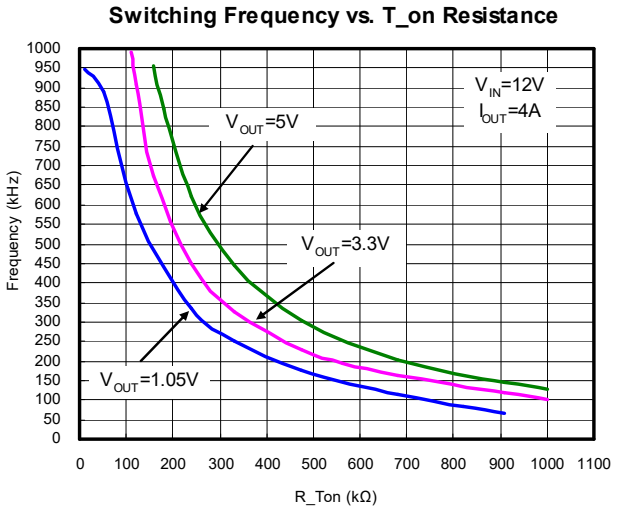


Figure 3

It results in a nearly constant switching frequency by R_{TON} that is a resistor connected from LX to the TON pin.

Pulse-Skipping Mode

In Pulse-Skipping Mode, an automatic switchover to PFM takes place at light load. It turns off the low side switch when the inductor current crosses to zero. This scheme will improve the light-load efficiency.

Gate Drivers

In the low duty factor application, it exists large difference of input voltage and output voltage. Therefore, large low-side MOSFET and moderate-size high-side MOSFET are needed for high efficiency. The DH and DL drivers are optimized for driving high-side and low-side MOSFETs. A non-overlap control circuit is needed to avoid the DH and DL turning on simultaneously. The DL driver with a 0.5Ω pull low transistor helps prevent the DL from being coupled to high during the fast rising-time of the LX node, due to the drain to gate capacitive coupling of low-side synchronous-rectifier MOSFET. A resistor in series with the BST is recommended that will reduce the EMI-producing efficiency loss by increasing the turn-on time of the high-side MOSFET

POR, UVLO, and Soft-Start

Power-on reset (POR) occurs when V5V rises above approximately 2V. It reset the fault latch and soft-start counter. When V5V is below 4.2V, undervoltage lockout (UVLO) inhibits switching and forces DL to high. An internal soft-start timer ramps up the current limit threshold to 100% of current limit setting within 3.3ms.

Power-Good Indicator

The Output voltage is always monitored for undervoltage by the PGOOD comparator. The PGOOD is open-drain type signal. In shutdown and soft-start period, PGOOD is kept low. After the soft-start timer has timed out, the PGOOD is released if the output voltage is within 10% of normal value.

Fault Protection

G5383B provides undervoltage protection, overvoltage protection, and overtemperature protection.

The undervoltage protection (UVP) function is like foldback current limit function. If the output voltage is under 70% of normal value 3.5ms after shutdown released, the undervoltage protection function is activated. The PWM is latched off and would not restart until V5V power is cycled or EN is toggled.

The overvoltage protection (OVP) function activates when the output voltage is 20% above the set voltage. The low-side MOSFET turn on 100% and the high-side MOSFET turn off. This rapidly discharges the output capacitor and decreases the output voltage. The SMPS is latched off and would not restart until V5V power is cycled or EN is toggled.

The G5383B has an overtemperature protection (OTP) that occurs when the die temperature is above 135C. It will shutdown the PWM and force high-side and low-side gate drivers output low. It could be released when die cool down or V5V power is cycled or EN is toggled.

Adjustable-Output Feedback

Connecting the FB pin to a resistor divider between OUT to AGND to adjust the output voltage from 0.9V.

Chose R6=10kΩ and solve the R5 with the equation:

$$R5 = R6 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right)$$

where V_{FB} = 0.9V norminal.

Test Mode

A test mode is provided for system developing stage. It can disable all the OVP, UVP, and thermal shutdown features, and clear the fault latch if it has been set. Force the EN pin above V5V by external sourcing current, G5383B enters a no-fault test mode. (No more than 0.6V above V5V is allowable)

Application Information

Inductor Selection

The inductor value is determined as follows:

$$L = \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN} \times f \times \Delta I_{LPP}}$$

Where ΔI_{LPP} is defined as inductor ripple current.

The inductor ripple current also impacts transient-response performance, especially at low V_{IN}- V_{OUT} differentials. Low inductor values allow the inductor current to slew faster, replenishing charge removed from the output filter capacitors by a sudden load step.

Maintaining the ratio of the inductor ripple current to the designed maximum load current within a 20% to 50% range is prudent.

Output Capacitor Selection

The output filter capacitor must have low enough effective series resistance (ESR) to meet output ripple and load-transient requirements, yet have high enough ESR to satisfy stability requirements. Also, the capacitance must be high enough to absorb the inductor energy going from a full-load to no-load condition without tripping the overvoltage protection circuit.

In CPU V_{CORE} converters and other applications where the output is subject to violent load transients, the output capacitor's size depends on how much ESR is needed to prevent the output from dipping too low under a load transient.

In non-CPU applications, the output capacitor's size depends on how much ESR is needed to maintain an acceptable level of output voltage ripple:

$$R_{ESR} \leq \frac{V_{OUTPP}}{\Delta I_{LPP}}$$

Output Capacitor Stability considerations

Stability is determined by the value of the ESR zero relative to the switching frequency. The point of instability is given by the following equation:

$$f_{ESR} = \frac{f}{\pi}$$

Where f = switching frequency

$$f_{ESR} = \frac{1}{2 \times \pi \times ESR \times C_{OUT}}$$

For a typical 300kHz application, the ESR zero frequency must be well below 95kHz, preferably below 50kHz. An OS-CON or POS CAP type capacitor, (ESR=10~20mΩ) is preferred. If use aluminum type capacitor, parallel a small ceramic capacitor is recommended.

Don't put high-value ceramic capacitors directly across the feedback sense point without taking precautions to ensure stability. Large ceramic capacitors can have a high ESR zero frequency and cause erratic, unstable operation. However, it's easy to add enough series resistance by placing the capacitors a couple of inches downstream from the feedback sense point, which should be as close as possible to the inductor.

Unstable operation manifests itself in two related but distinctly different ways: double-pulsing and fast-feedback loop instability.

Double-pulsing occurs due to noise on the output or due to the ESR is too low to without enough voltage ramp in the output voltage signal. This "fools" the error comparator into triggering a new cycle immediately after the 400ns minimum off-time period has expired. Double-pulsing is more annoying than harmful, resulting in nothing worse than increased output ripple. However, it can indicate the possible presence of loop instability, which is caused by insufficient ESR. Loop instability can result in oscillations at the output after line or load perturbations that can trip the overvoltage protection latch or cause the output voltage to fall below the tolerance limit. The easiest method for checking stability is to apply a very fast zero-to-max load transient and carefully observe the output voltage ripple envelope for over-shoot and ringing. It can help to simultaneously monitor the inductor current with a current probe. Don't allow more than one cycle of ringing after the initial step-response under- or over-shoot.

Input Capacitor Selection

The input capacitor must meet the ripple current requirement (I_{RMS}) imposed by the switching currents. Nontantalum chemistries (ceramic, aluminum, or OS-CON) are preferred due to their resistance to power-upsurge currents.

For optimal circuit reliability, choose a capacitor that has less than 10°C temperature rise at the peak ripple current.

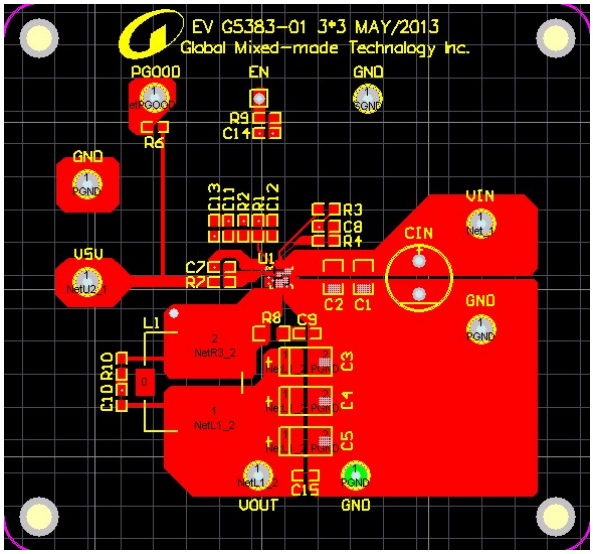
$$I_{RMS} = I_{LOAD}\left(\frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}\right)$$

Layout Considerations

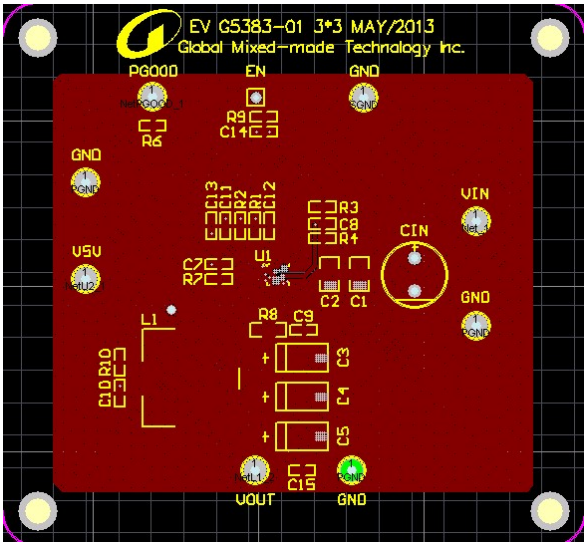
- Connect AGND (Pin1) to ground of bypass V5V and FB path.
- Connect AGND and PGND together close to the IC and the negative terminal of C_{OUT}.
- Star connection PGND ground plane to system ground (normally, it's defined as ground of power supply or battery pack.).
- Connect PGND of power component Low-side MOSFET source, C_{IN}, and C_{OUT} to system ground by a plane.
- All sensitive analog traces such as FB should be placed away from high-voltage switching node such as LX, BST nodes to avoid coupling.

EV Board PCB Layout Section

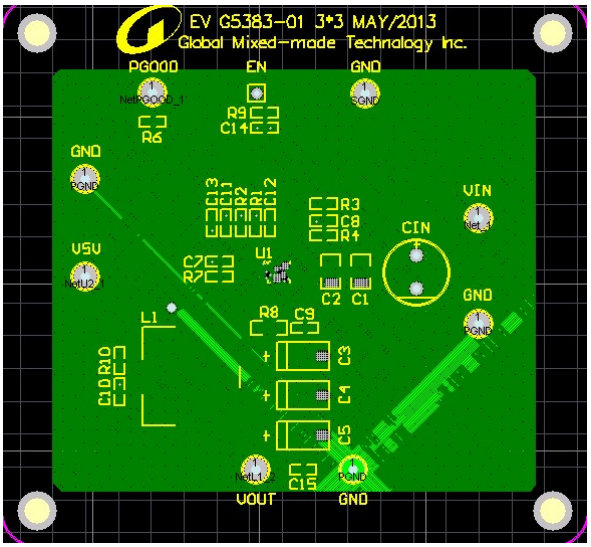
TOP Layer



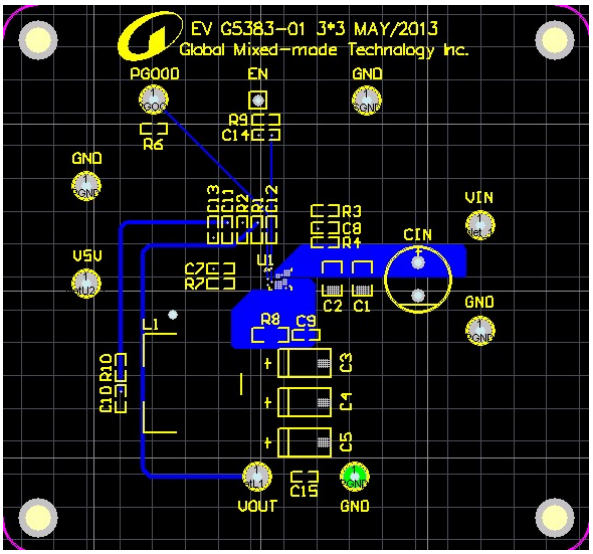
Mid1 Layer



Mid2 Layer

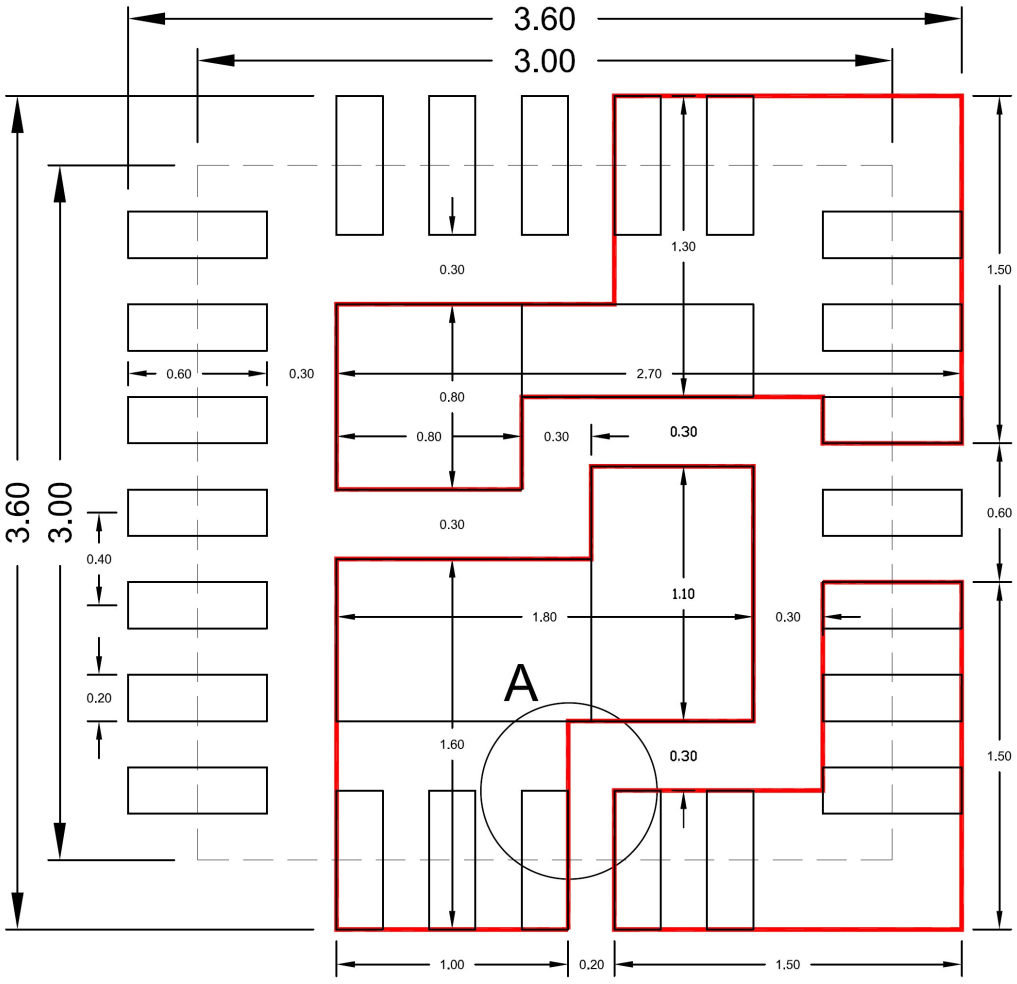


Bottom Layer



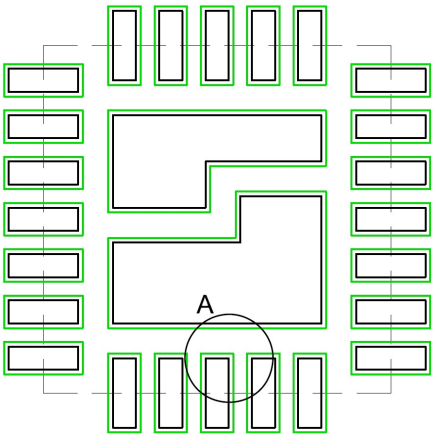
Minimum Footprint PCB Layout Section

QFN3X3-24

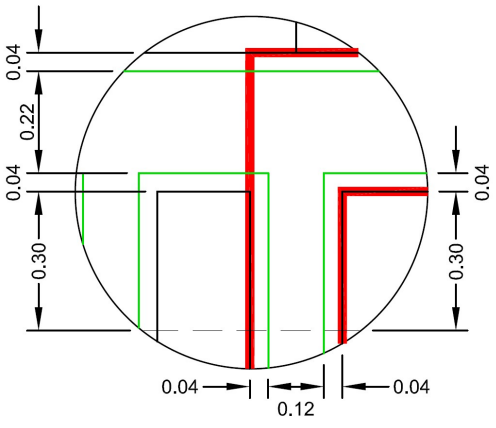


Top Layer

* Recommend Top Layer Thermal Pad Design Following Red Line for Better Characteristic.

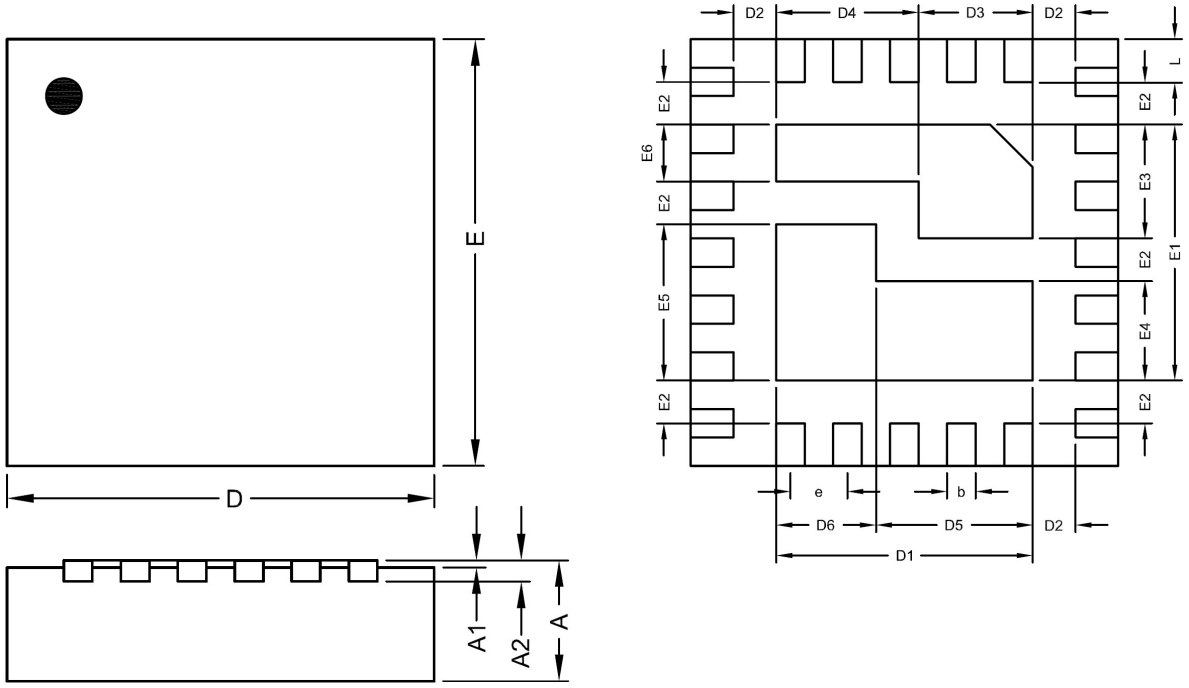


Top Layer with Solder Mask



Section A

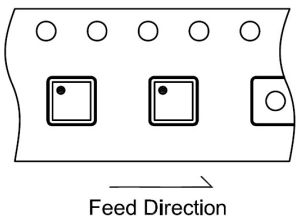
Package Information



QFN3X3-24 Package

Symble	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.80	0.90	0.0276	0.0315	0.0354
A1	0.00	- - -	0.05	0.0000	- - -	0.0020
A2		0.02 BSC			0.0079 BSC	
D	2.95	3.00	3.05	0.1161	0.1181	0.1201
E	2.95	3.00	3.05	0.1161	0.1181	0.1201
D1	1.70	1.80	1.90	0.0669	0.0709	0.0748
D2		0.30 BSC			0.0118 BSC	
D3	0.75	0.80	0.85	0.0295	0.0315	0.0335
D4	0.95	1.00	1.05	0.0374	0.0394	0.0413
D5	1.05	1.10	1.15	0.0413	0.0433	0.0453
D6	0.65	0.70	0.75	0.0256	0.0276	0.0295
E1	1.70	1.80	1.90	0.0669	0.0709	0.0748
E2		0.30 BSC			0.0118 BSC	
E3	0.75	0.80	0.85	0.0295	0.0315	0.0335
E4	0.65	0.70	0.75	0.0256	0.0276	0.0295
E5	1.05	1.10	1.15	0.0413	0.0433	0.0453
E6	0.35	0.40	0.45	0.0138	0.0157	0.0177
b	0.15	0.20	0.25	0.0059	0.0079	0.0098
e		0.40 BSC			0.0157 BSC	
L	0.25	0.30	0.35	0.0099	0.0118	0.0138

Taping Specification



PACKAGE	Q'TY/BY REEL
QFN3X3-24	3,000 ea