G5517

Integrated Power Solution for TFT-LCD

Features

- **2.5V to 5.5V Input Supply Range**
- **1.2MHz Current-Mode Step-Up Converter**
- **Built-In 18V, 3A 0.2Ω n-Channel MOSFET**
- **Charge Pumps for V_{GON} and V_{GOFF}**
- **High Voltage Switch with Adjustable Delay**
- **Thermal Overload Protection**
- **TQFN4X4-24 Package**

Applications

- **LCD Monitor Panels**
- **Notebook Computer Displays**
- **LCD TVs**

General Description

The G5517 includes a step-up converter, two charge pumps, and a high current operational amplifier for TFT LCD. Also included are a logic-controlled high-voltage switch with adjustable delay and an open drain output reset comparator.

The step-up DC/DC converter provides the regulated power supply for the panel source driver IC. The converter is a high performance current-mode regulator with operating frequency at 1.2MHz. It also provides fast transient response and high efficiency.

The charge pumps in G5517 regulate TFT gate-on and gate-off power supplies. The power-on sequence is controlled by the control logic. The blanking time for reset function is 163ms (typ.) from startup. The RSTIN begins to detect voltage below 1.25V afterward. For more detail information, please refer to the timing chart.

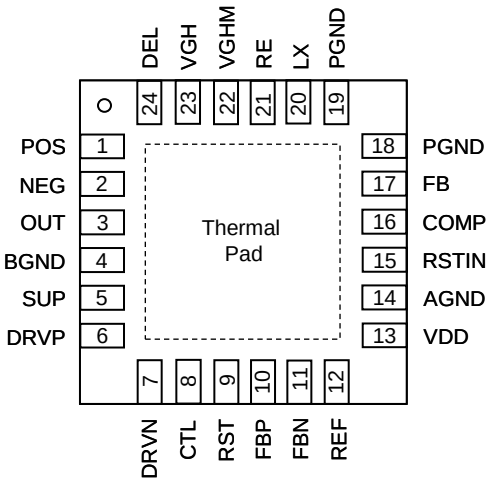
G5517 is available in TQFN4X4-24 package

Ordering Information

ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE (Green)
G5517R51U	5517	-40°C to 85°C	TQFN4X4-24

Note: R5: TQFN4X4-24
1: Bonding Code
U: Tape & Reel
Green : Lead Free / Halogen Free.

Pin Configuration



G5517 TQFN4X4-24

Note: Recommend connecting the Thermal Pad to the Ground for excellent power dissipation.

Absolute Maximum Ratings

VDD, RST to AGND . . . . . -0.3V to 7V
SUP, LX to GND . . . . . -0.3V to 20V
VGH to GND . . . . . -0.3V to 36V
VGHM to GND . . . . . .-0.3V to 36V
FB, FBP, FBN, DEL, RSTIN. . . . . -0.3V to V_{DD}+0.3V
POS, NEG . . . . . -0.3V to SUP+0.3V
COMP, REF . . . . . .-0.3V to V_{DD}+0.3V
DRVP, DRVN . . . . . .-0.3V to SUP+0.3V
Thermal Resistance Junction to Ambient, (θ_{JA})
TQFN4X4-24 . . . . . 89°C/W(1)
TQFN4X4-24 (1in^2) . . . . . 73°C/W(2)

Continuous Power Dissipation (T_A=25°C)
TQFN4X4-24 . . . . . .1.4W(1)
TQFN4X4-24(1in^2) . . . . . 1.7W(2)
Thermal Resistance Junction to Case, (θ_{JC})
TQFN4X4-24 . . . . . 13°C/W
Operating Temperature . . . . . -40°C to 85°C
Junction Temperature . . . . . 150°C
Storage Temperature . . . . . .-65°C to 150°C
Reflow Temperature (soldering, 10 sec) . . . . . .260°C

Note:
(1): Please refer to Minimum Footprint PCB Layout Section.
(2):Please refer to 1in^2 of 1oz PCB Layout Section.

Stress beyond those listed under “Absolute Maximum Rating” may cause permanent damage to the device.

Electrical Characteristics

VDD=3.3V, SUP=12V, T_A = 25°C.

The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VDD Input Voltage Range		2.5	---	5.5	V
SUP Input Voltage Range		6	---	18	V
VDD Under Voltage lockout	Falling	2.05	2.15	2.25	V
	Rising	2.15	2.25	2.35	
VDD Operating Current	V_{FB}=1.5V, not switching	---	0.4	0.8	mA
	V_{FB}=1.2V, switching	---	2.3	5	mA
SUP Operating Current	V_{POS}=5V	---	1.2	3.0	mA
Thermal Shutdown		---	150	---	°C
Reference Voltage					
Reference Voltage	I_{VREF}=100μA	1.238	1.25	1.262	V
Line Regulation	I_{VREF}=100μA VDD=2.5V~5.5V	---	2	5	mV
Load regulation	I_{VREF}=0~100μA	---	1	5	mV
Oscillator					
Oscillation Frequency		1.0	1.2	1.4	MHz
Maximum Duty Cycle		86	90	94	%
Soft Start & Fault Detect & DEL					
PWM Soft Start Time		---	10	---	ms
VG_{OFF} Soft Start Time		---	3.4	---	ms
VG_{ON} Soft Start Time		---	3.4	---	ms
Duration to Trigger Fault Condition		---	55	---	ms
FB Fault Protection Voltage		0.95	1.00	1.05	V
FBN Fault Protection Voltage		0.4	0.45	0.5	V
FBP Fault Protection Voltage		0.95	1.00	1.05	V
FB Under Voltage Protection		---	0.1	---	V
Error Amplifier (Boost Converter)					
Feedback Voltage		1.238	1.25	1.262	V
Input Bias Current	V_{FB}=1V to 1.5V	-40	0	40	nA
Feedback-Voltage Line Regulation	Unit Gain, V_{COMP}=1.25V, 2.3V<V_{DD}<5.5V	---	0.05	0.15	%/V
Transconductance	△ I=5μA	---	105	---	μA/V
Voltage Gain		---	1500	---	V/V

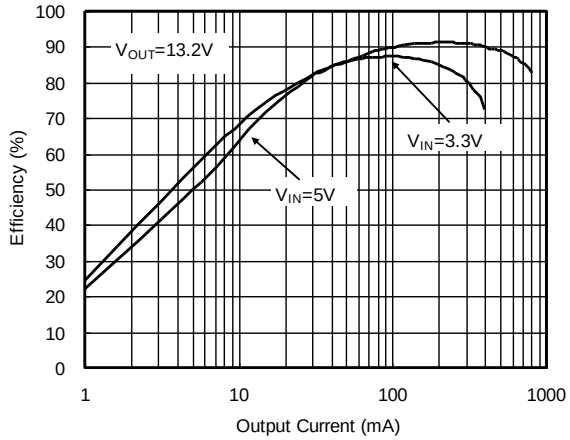
Electrical Characteristics (continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Switching NMOS					
Current Limit		2.5	3	---	A
On-Resistance		---	0.2	---	Ω
Leakage Current	V_{LX}=15V	---	0.01	20	μA
Charge Pump					
SUP Input Supply Range		6	---	18	V
SUP Over Voltage Protect		---	18	20	V
Charge Pump Frequency		500	600	700	kHz
FBN Threshold Voltage		235	250	265	mV
FBP Threshold Voltage		1.23	1.25	1.27	V
FBN Input Bias Current		-40	0	40	nA
FBP Input Bias Current		-40	0	40	nA
DRVN Switch Ron	R_{ONP2},R_{ONN2}	---	3	20	Ω
DRVP Switch Ron	R_{ONP3},R_{ONN3}	---	3	20	Ω
Reset Output					
RST Output Voltage	I_{RST}=1.2mA	---	---	0.2	V
RSTIN Threshold Voltage	Hys=50mV	---	1.25	---	V
RSTIN Input Current		-40	0	40	nA
RST Blanking Time		146	163	180	ms
Vcom Buffer					
Input Offset Voltage	V_{POS}=5V		2	15	mV
Input Bias Current	$V_{POS/NEG}$=5V	-40	0	40	nA
Output Swing	I_{OUT}=-200μA, V_{POS}=5V	---	5.03	5.06	V
	I_{OUT}=200μA, V_{POS}=5V	4.94	4.97	---	
Short Circuit Current	Measure I_{OUT}	---	±200	---	mA
Slew Rate	V_{POS}=2V to 8V, V_{POS}=8V to 2V, 20% to 80%	---	40	---	V/μs
Setting Time	V_{POS}=4.5V to 5.5V, 90%	---	5	---	μs
High Voltage Switch Controller					
DEL Source Current		4	5	6	μA
DEL Threshold Voltage		1.22	1.25	1.28	V
DEL Discharge R_{ON}		---	8	---	Ω
CTL Input Low Voltage		---	---	0.5	V
CTL Input High Voltage		2	---	---	V
CTL Input Bias Current	V_{CTL}=0 to V_{DD}	-40	0	40	nA
Propagation Delay CTL to VGHM	VGH=25V	---	100	---	ns
VGH to VGHM Switch Ron	V_{DEL}=1.5V, V_{CTL}=VDD	---	15	30	Ω
RE to VGHM Switch Ron	V_{DEL}=1.5V, V_{CTL}=GND	---	30	60	Ω
VGHM to AGND Switch Ron	V_{DEL}=1V	1.5	2.5	3.5	kΩ

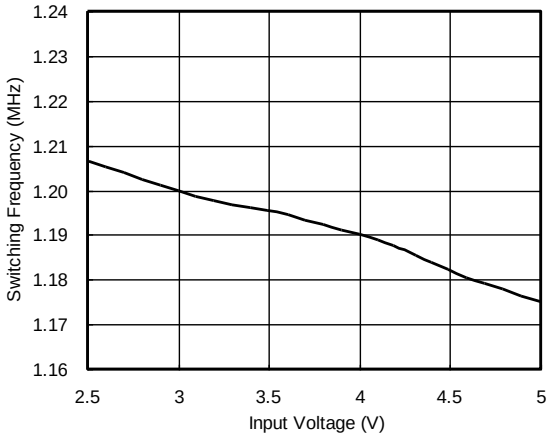
Typical Performance Characteristics

Circuit of Typical Application Circuit, T_A=25°C, unless otherwise noted.

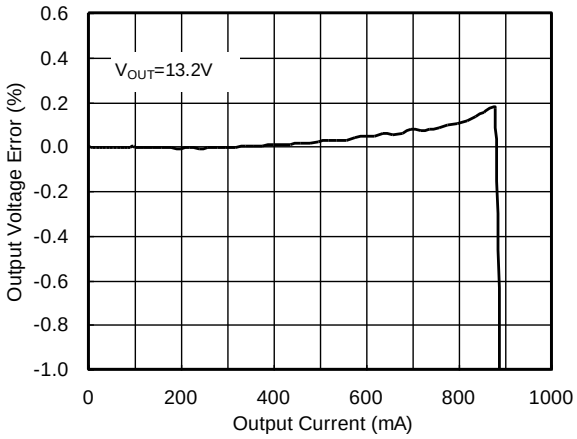
Boost Converter Efficiency vs. Output Current



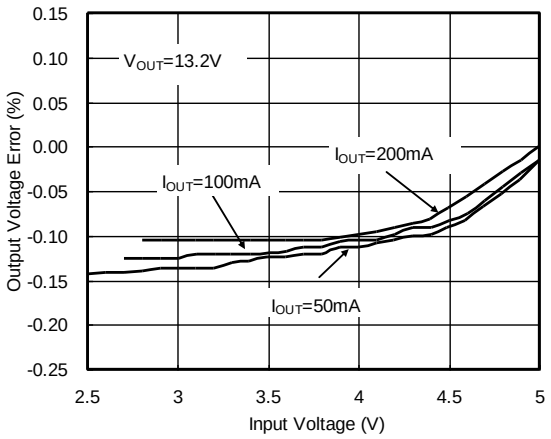
Boost Converter Switching Frequency vs. Input Voltage



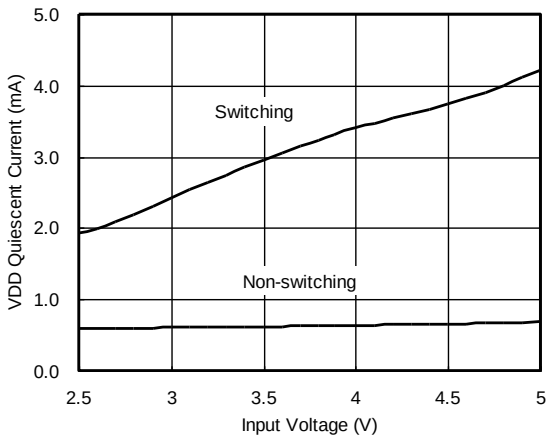
Boost Converter Output Voltage vs. Output Current



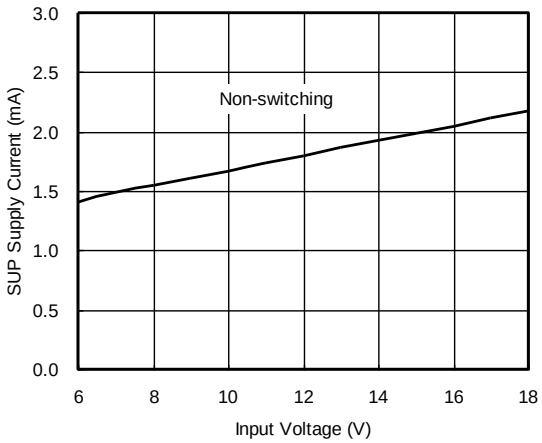
Boost Converter Output Voltage vs. Input Voltage



VDD Quiescent Current vs. Input Voltage

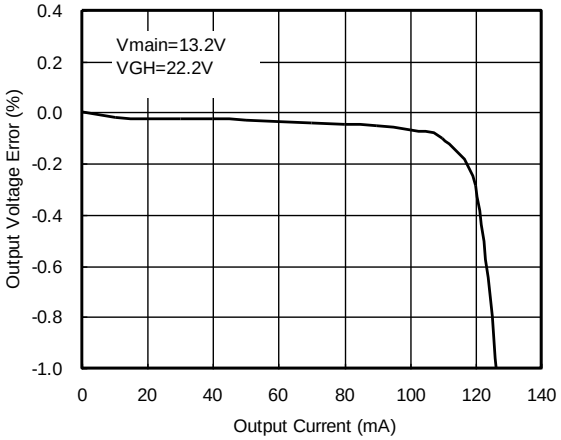


SUP Supply Current vs. Input Voltage

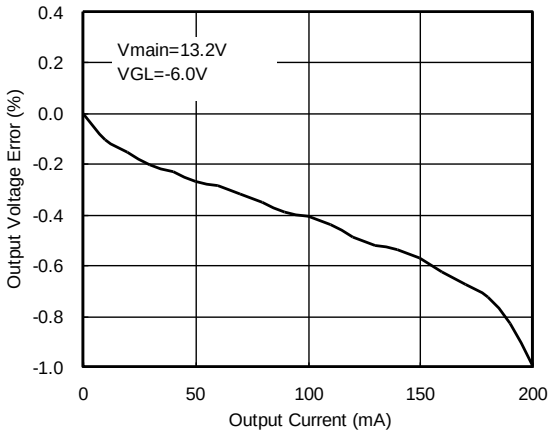


Typical Performance Characteristics (continued)

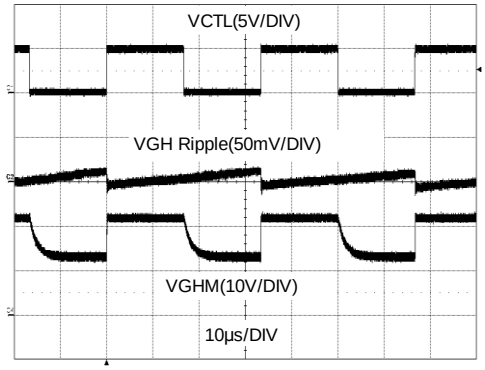
VGH Output Voltage vs. Output Current



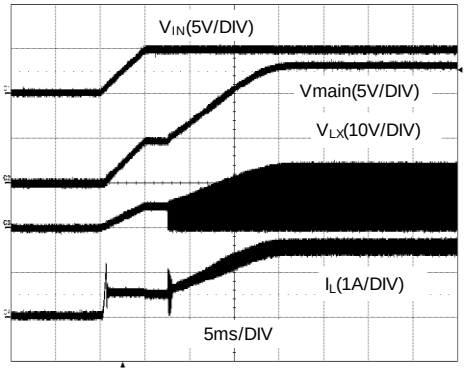
VGL Output Voltage vs. Output Current



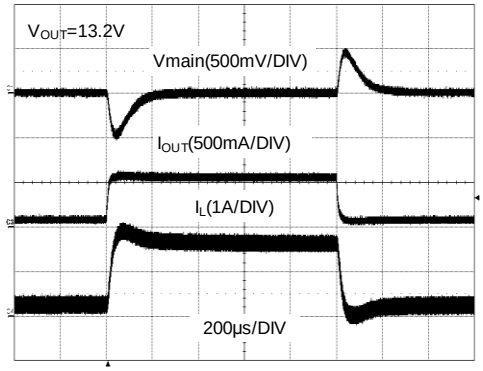
VGHM with VCTL



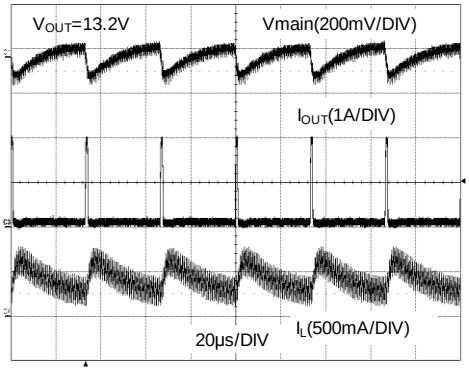
Boost Converter Start-up Waveforms (I_{OUT}=600mA)



Boost Converter Load Transient Response (I_{OUT}=100 to 600mA)

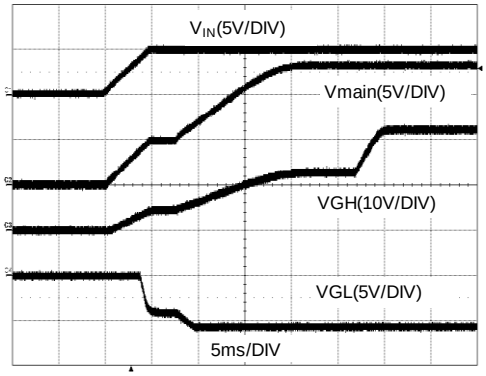


Boost Converter Pulsed Load Transient Response (I_{OUT}=100mA to 2.0A)

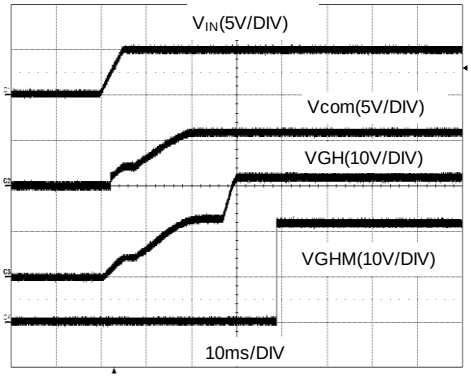


Typical Performance Characteristics (continued)

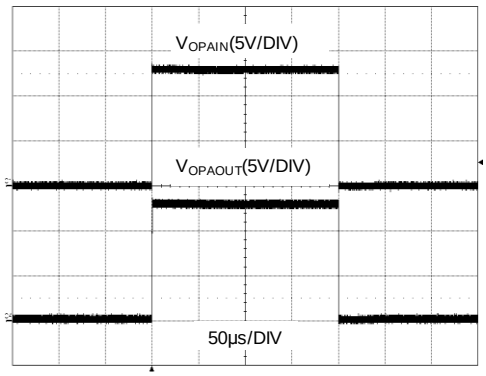
Power-on Sequence with VGH & VGL



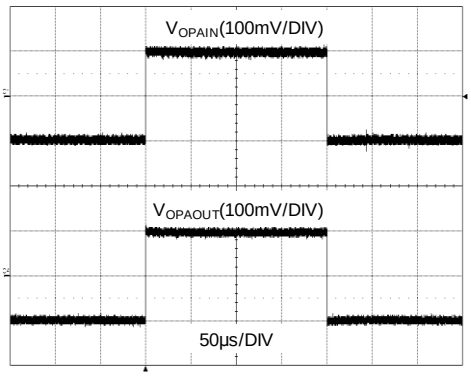
Power-on Sequence with Vcom & VGHM



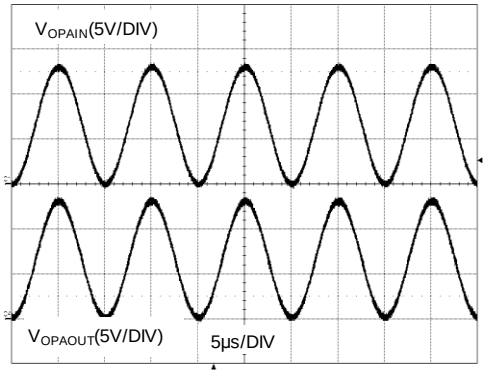
Operational-Amprifier Large Signal Step Response



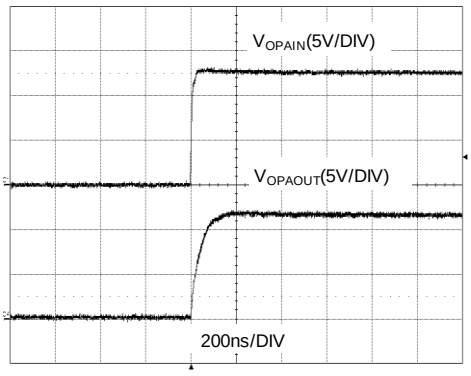
Operational-Amprifier Small Signal Step Response



Operational-Amprifier Rail to Rail Input/output

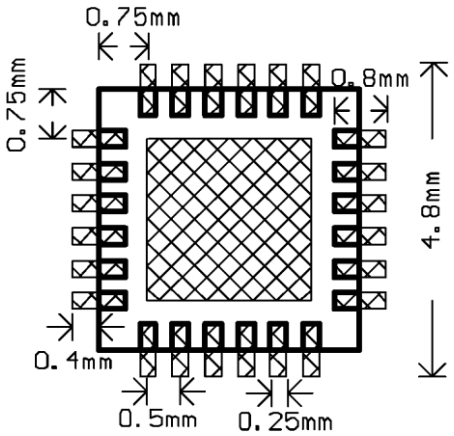


Operational-Amprifier Slew Rate



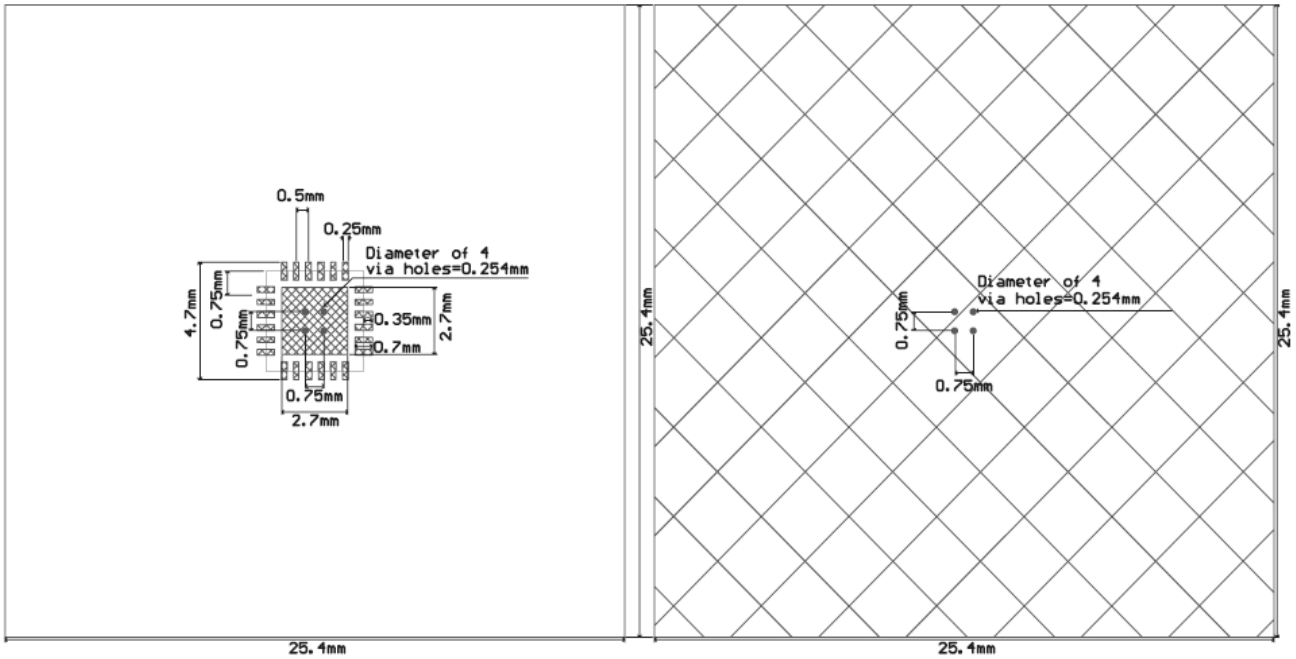
Minimum Footprint PCB Layout Section

TQFN4X4-24



1in^2 of 1oz PCB Layout Section

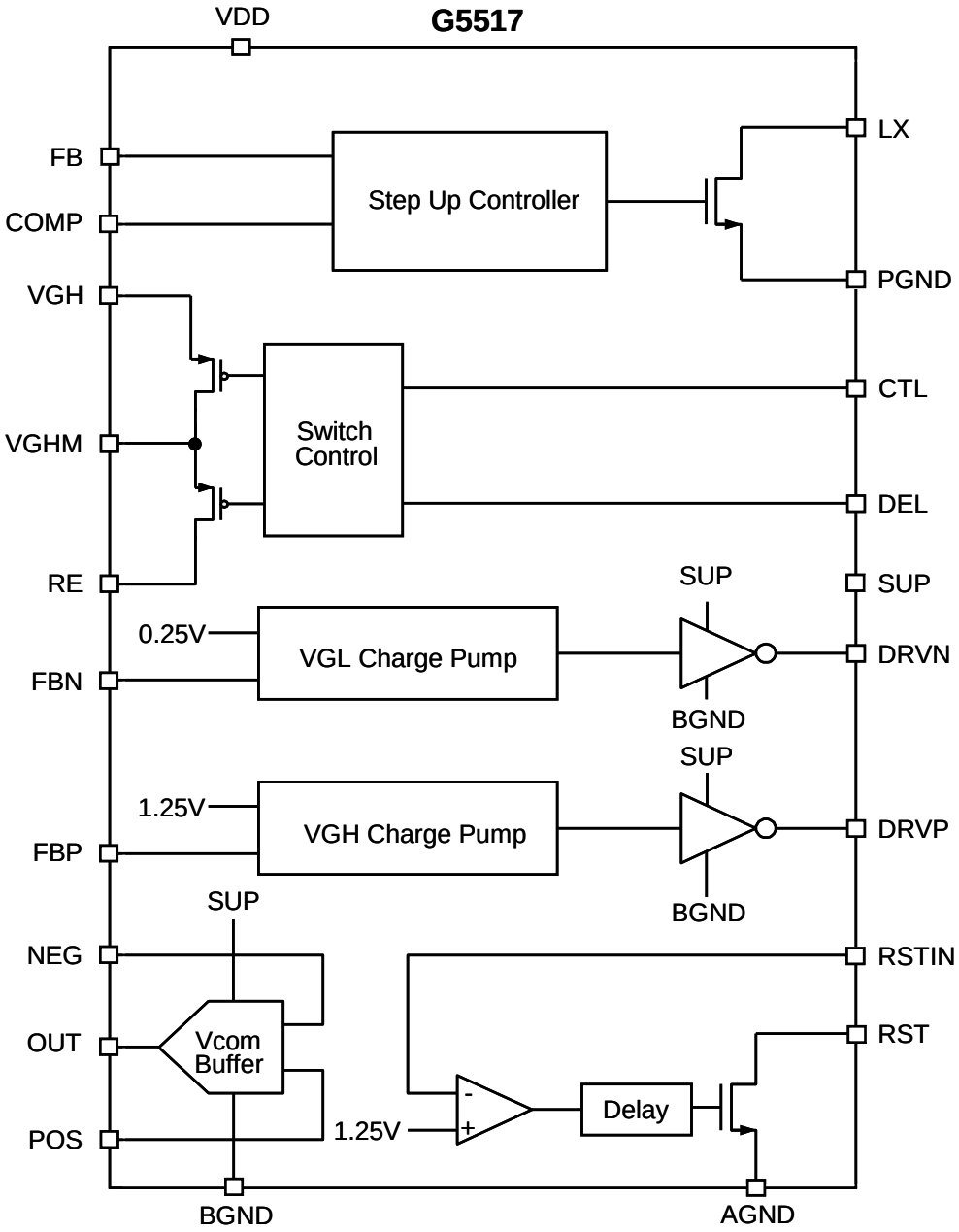
TQNF4X4-24



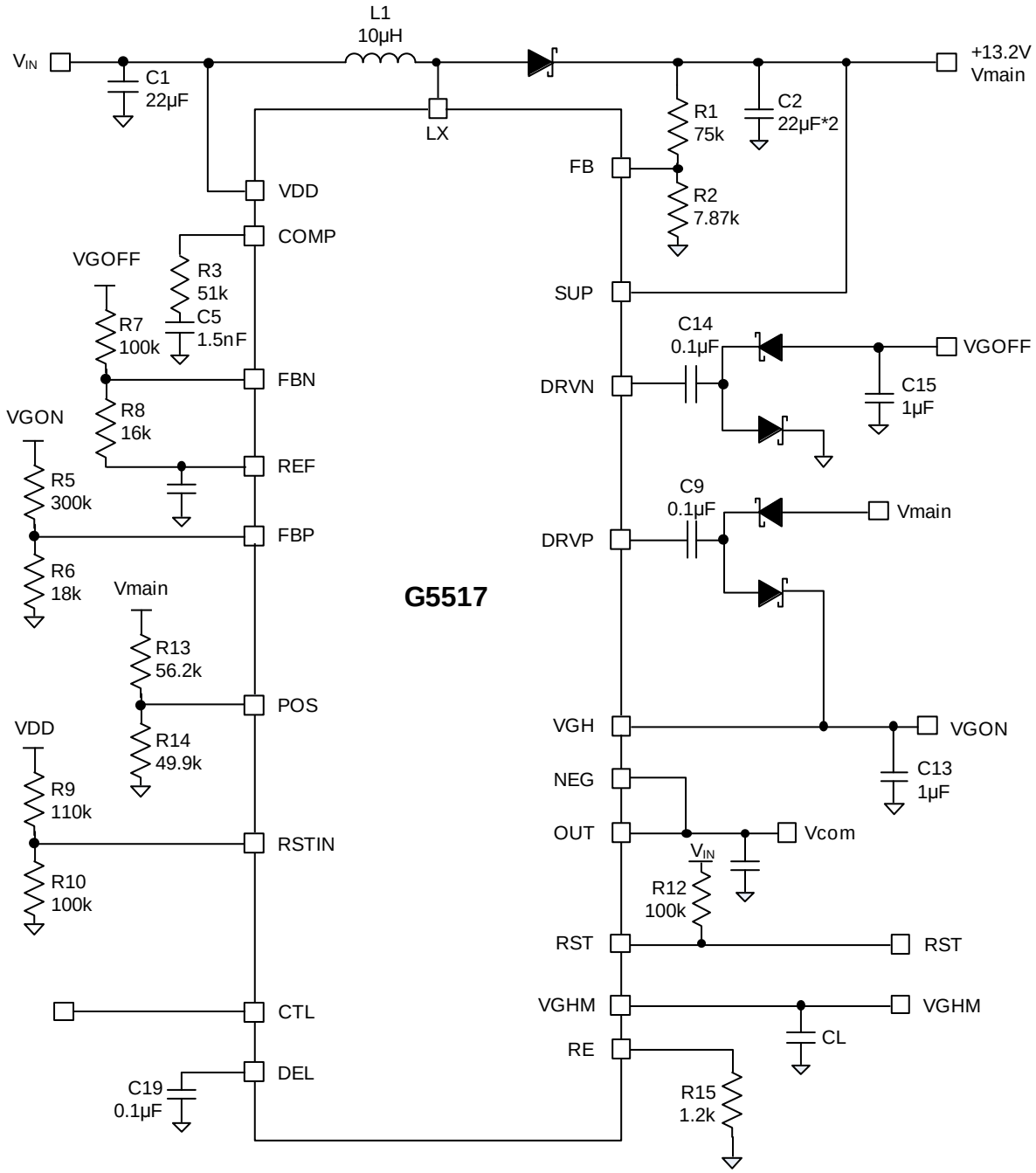
Pin Description

PIN	NAME	I/O	FUNCTION
1	POS	I	V_{COM} Buffer Positive Input
2	NEG	I	V_{COM} Buffer Negative Input
3	OUT	O	V_{COM} Buffer Output
4	BGND		V_{COM} Buffer Ground
5	SUP	I	V_{COM} Buffer and Charge Pump Power Supply
6	DRVP	O	Positive Charge Pump Output Pin
7	DRVN	O	Negative Charge Pump Output Pin
8	CTL	I	High Voltage Switch Control Pin
9	RST	O	Reset Signal Open Drain Output
10	FBP	I	Positive Charge Pump Feedback Pin
11	FBN	I	Negative Charge Pump Feedback Pin
12	REF	O	Reference Voltage
13	VDD	I	Main PWM Power Supply
14	AGND		Analog Ground
15	RSTIN	I	Reset Comparator Input
16	COMP	O	Main PWM Error Amplifier Output
17	FB	I	Main PWM Feedback Pin
18	PGND		LX MOS Ground
19	PGND		LX MOS Ground
20	LX		Main PWM Switching Pin
21	RE	O	Gate High Voltage Fall Time Setting Pin
22	VGHM	O	Switching Gate High Voltage for TFT
23	VGH		Gate High Voltage Input
24	DEL	I	VGH Delay Adjust Pin

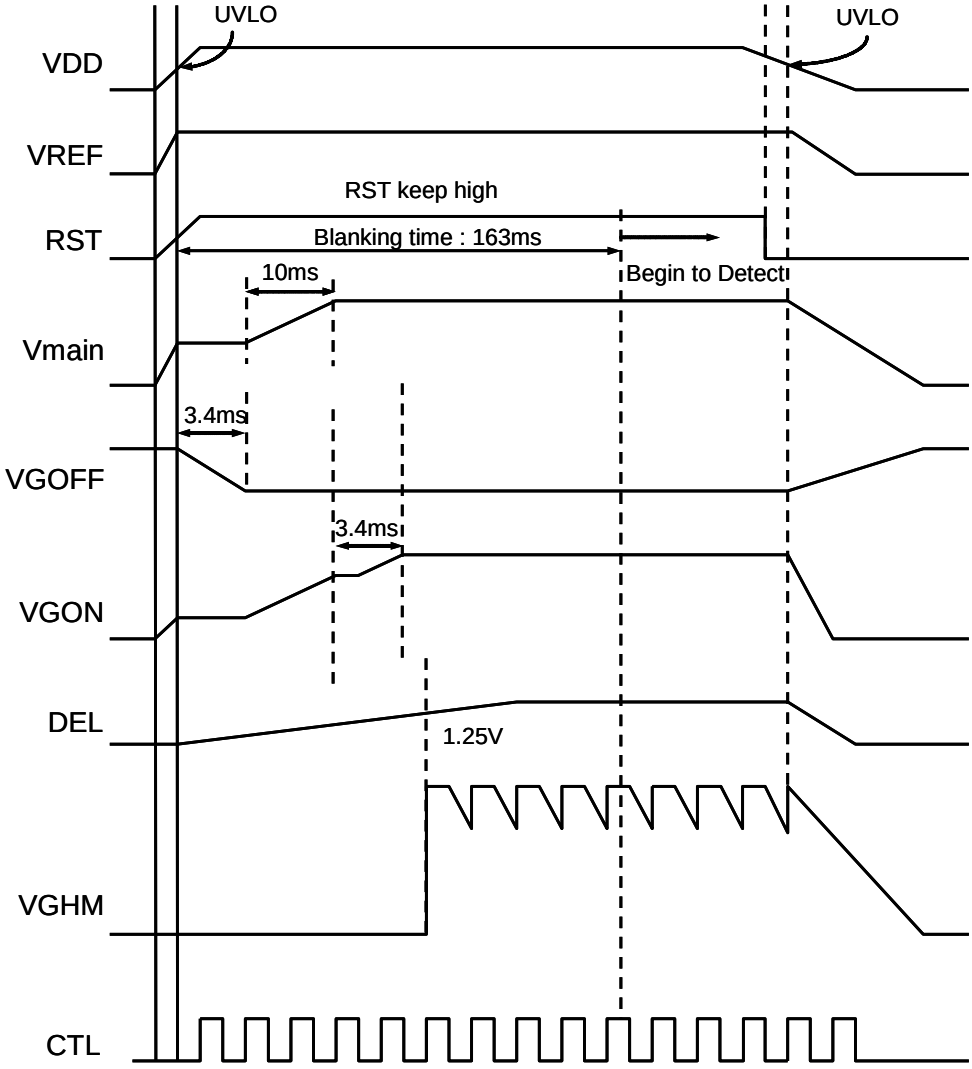
Block Diagram



Typical Application Circuit



Power on Power off Timing Chart



Application Information

The G5517 contains a high performance boost regulator to generate voltage for source driver supply, and gate-on, gate-off charge pumps for gate driver supply. It also includes of a high-current rail-to-rail operation amplifier for VCOM, a gate pulse modulator (GPM) and a voltage detector. For more detail description and the component selection are as follows.

Boost Regulator

The boost regulator is a high efficiency current-mode PWM architecture with 1.2MHz operation frequency. It performs fast transient responses to generate source driver supplies for TFT LCD display. The high operation frequency allows smaller components to minimize the thickness of LCD panel. To regulate the output voltage is to set resistive voltage-divider sensing at FB pin. The error amplifier varies the COMP voltage by sensing the FB pin to regulate the output voltage. For better stability, the slope compensation signal that combined with the current-sense signal will be compared with the COMP voltage to determine the current trip point and duty cycle.

Inductor Selection

A 4.7μH or 10μH inductor is recommended for small ripple applications. Small form factor and high efficiency are the major concerns for most G5517 applications. Inductor with low core losses and small DCR (cooper wire resistance) are good choice for G5517 applications.

To keep all current load conditions are in the continuous current mode (CCM), we can calculate the approximate inductor value by the following formula:

$$L > \frac{\eta_{TYP} \times (V_{OUT} - V_{IN}) \times V_{IN}^2}{2 \times f_{OSC} \times I_{OUT(MIN)} \times V_{OUT}^2}$$

Where $I_{OUT(MIN)}$ is the minimum loading current, and the expected efficiency (η_{TYP}) is taken from an appropriate curve in the Typical Performance Characteristics.

Capacitor Selection

The total output voltage ripple has two components: the capacitive ripple caused by the charging and discharging of the output capacitance, and the ohmic ripple due to the capacitor's equivalent series resistance (ESR):

$$V_{RIPPLE} = V_{RIPPLE(C)} + V_{RIPPLE(ESR)}$$

$$V_{RIPPLE(C)} \approx \frac{I_{OUT} \times (V_{OUT} - V_{IN})}{C_{OUT} \times f_{OSC} \times V_{OUT}}$$

$$V_{RIPPLE(ESR)} \approx I_{PEAK} \times R_{ESR(COUT)}$$

where I_{PEAK} is the peak inductor current. For ceramic capacitors, the output voltage ripple is typically dominated by $V_{RIPPLE(C)}$. The voltage rating and temperature characteristics of the output capacitor must also be considered.

Diode Selection

Schottky diodes, with their low forward voltage drop and fast reverse recovery, are the ideal choices for G5517 applications. The forward voltage drop of a Schottky diode represents the conduction losses in the diode, while the diode capacitance (CT or CD) represents the switching losses. For diode selection, both forward voltage drop and diode capacitance need to be considered. Schottky diodes with higher current ratings usually have lower forward voltage drop and larger diode capacitance, which can cause significant switching losses of the G5517. A Schottky diode rated at 2A is sufficient for most G5517 applications.

Output Voltage

The regulated output voltage is calculated by the following formula:

$$V_{OUT} = 1.25V \times \left(1 + \frac{R1}{R2}\right)$$

The recommended value for R2 should be up to 100kΩ without some sacrificing. Place the resistor-divider as close as possible to the chip can reduce noise sensitivity.

Loop Compensation

The voltage feedback loop can be compensated with an external compensation network consisted of R3, C5 as Typical Application Circuit. Choose R3 to set high frequency integrator gain for fast transient response and C5 to set the integrator zero to maintain loop stability. Follow the equations below to obtain better transient response and stable performance for those low-ESR output capacitor applications:

$$R3 = \frac{235 \times V_{IN} \times V_{OUT} \times C_{OUT}}{L \times I_{OUT(MAX)}}$$

$$C5 = \frac{V_{OUT} \times C_{OUT}}{10 \times I_{OUT(MAX)} \times R3}$$

Soft-Start

The G5517 provides internal soft-start function to minimize the inrush current. When power on, an internal constant current charges a built-in capacitor. The rising voltage rate on COMP pin will be limited during the charging period and the inductor peak current will also be limited at the same time. When power off, the built-in capacitor will be discharged for next soft start time.

Over Current Protection

The G5517 main boost converter has the function of peak current protection to limit peak inductor current. It prevents large current damaging the inductor and diode. During the ON-time, once the inductor current exceeds the current limit, the internal LX switch turns off immediately and shortens the duty cycle. Therefore, the output voltage drops if the over-current condition occurs. Actual current limit is always larger than the nominal value because of the internal circuit delay.

Over Temperature Protection

The G5517 main boost converter has thermal protection function to prevent the excessive power dissipation from overheating. When the junction temperature exceeds 150°C, it will shut down the device and require VDD power-on-reset (POR) to restart.

Under Voltage Protection

If the boost regulator feedback voltage (FB) or the charge pumps feedback voltage (FBP,FBN) exceed the fault-detection threshold, the G5517 activates an internal timer. If the fault condition continues for 55ms, the PWM will latch off and won't restart until VDD power is cycled. The under-voltage protection is disabled during the soft-start time.

Gate-High Regulator

The gate-high regulator is to provide the TFT-LCD gate on voltage. The charge pump can provide a programmable output voltage. To regulate the output voltage must set the resistive voltage-divider sensing at FBP pin. The error amplifier varies the difference voltage by sensing FBP pin to regulate the output voltage as the following equation:

$$V_{GH} = 1.25V \times \left(1 + \frac{R5}{R6}\right)$$

Besides, the Schottky diodes with a current rating should equal to or greater than two times of the average charge pump input current.

Gate-Off Regulator

The gate-off charge-pump regulator is typically used to generate the negative supply rail for the TFT LCD gate driver ICs. The error amplifier compares the FBN with internal voltage 0.25V to regulate the setting voltage.

The gate-off charge pump output voltage equation is as follows:

$$V_{GOFF} = 0.25V - \left(\frac{R7}{R8}\right)$$

Gate Pulse Modulator

The GPM is controlled by the frame signals from timing controller to modulate the Gate-On voltage, VGHM, which acts a flicker compensation circuit to reduce the coupling effect between gate lines and pixels. It also can delay the Gate-On voltage while power-on for achieving a correct power-on sequence for gate driver ICs. The delay time can be calculated as:

$$t_{D\_VGHM} = 1.25 \times \left(\frac{C19}{I_{DPM}}\right) = 250k \times C19$$

The falling time of the Gate-On voltage is programmable by external capacitor (C_L) and resistor (R15), The VGHM voltage in discharge condition can be calculated by follow formula:

$$VGHM = VGH \times \mathbf{exp}\left(\frac{-t}{(RM3 + R15) \times C_L}\right)$$

Where C_L is the parasitic capacitor of Panel, and t is VGHM discharge time.

Operational Amplifier

The function of the operational amplifier is to drive the LCD backplane VCOM. The operational amplifier features ±200mA output short circuit current, 40V/μs slew rate.

Voltage Detector

The voltage detector monitors the RSTIN voltage to generate a reset signal while RSTIN is lower than the detecting level and the detecting level is decided by an external resistor divider.

$$V_{DET} = V_{RSTIN} \times \left(1 + \frac{R9}{R10}\right) = 1.25V \times \left(1 + \frac{R9}{R10}\right)$$

$$V_{HYS} = 50mV \times \left(1 + \frac{R9}{R10}\right)$$

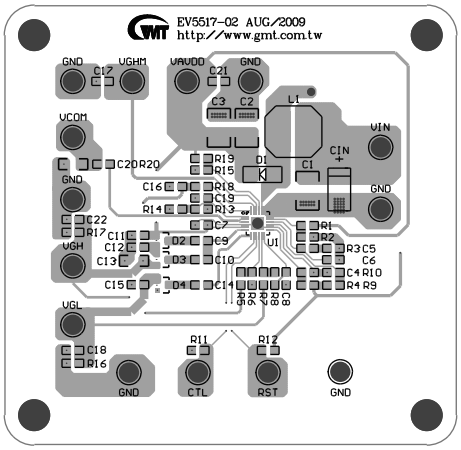
The controller would issue a blanking period about 163ms after VDD reaching UVLO threshold. During the blanking period, voltage detector would ignore the VDD drop and keep RST in high impedance. After the blanking period and if RSTIN goes below 1.25V, RST is pulled low indicating low RSTIN input. RST stays low until VDD falls below approximately 1V. Then RST cannot be held low any more and RST is pulled up by the external resister. For more detail timing information, please reference the Power-On Power-Off Timing Chart.

PCB Layout considerations:

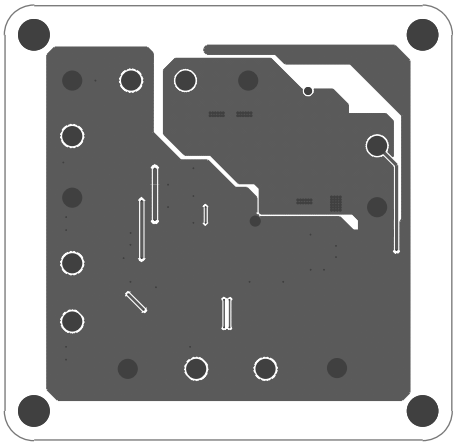
- The placement of the input bypass capacitor of VDD pin must be as close as possible to the G5517 to reduce the input ripple voltage and noise coupling. The trace that connects input voltage and the IC's VDD pin should be in front of the input power capacitor. The ground of input bypass capacitor must connect to the IC's AGND pin shortly.
- All feedback resistors and compensation network should be connected to G5517 as close as possible, and the grounds of them should connect to the analog signal ground AGND. Each route of analog signal should keep away from the switching noise source such as the power loops of Boost converter and charge-pump converters.
- Power loops of the converters should be connected with the shortest and widest traces as possible. The long and narrow trace increases the ESR and ESL, and that will induce more effective noise at high frequency easily.
- Separate the power ground and analog signal ground into different planes to prevent the interference, and connect these two parts at the GND connector after the power output capacitor.

EV5517 PCB Layout

Top Overlayer & Top Layer

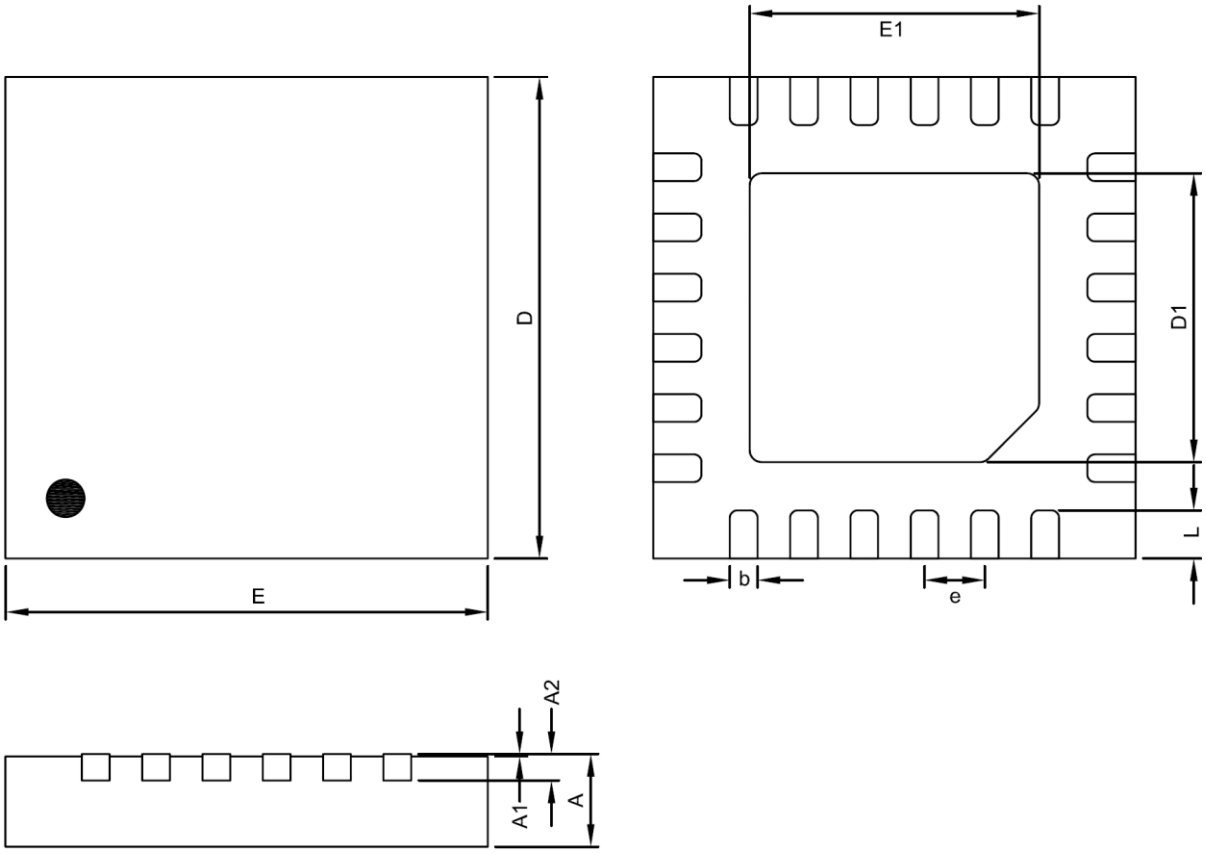


Bottom Layer



EV5517-02 PCB	Information
Board Material	FR4
Size	85mm×83mm
Board Thickness	1.6mm
Layers	2
Copper Thickness	2 oz.

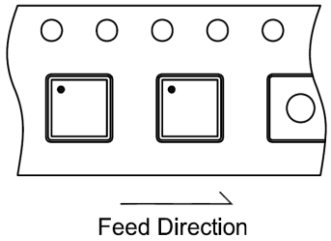
Package Information



TQFN4X4-24 Package

Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.0276	0.0295	0.0315
A1	0.00	- - -	0.05	0.0000	- - -	0.0020
A2	0.20 REF			0.0079 REF		
D	3.95	4.00	4.05	0.1555	0.1575	0.1594
E	3.95	4.00	4.05	0.1555	0.1575	0.1594
D1	2.50	2.70	2.85	0.0984	0.1063	0.1122
E1	2.50	2.70	2.85	0.0984	0.1063	0.1122
b	0.18	0.23	0.30	0.0071	0.0091	0.0118
e	0.50 BSC			0.0197 BSC		
L	0.35	0.40	0.45	0.0118	0.0138	0.0177

Taping Specification



PACKAGE	Q'TY/REEL
TQFN4X4-24	3,000 ea