Complete DDR Memory Solution Synchronous Buck PWM Controller, 1.5A LDO, Buffered Reference

Features

●Synchronous Buck Controller (VDDQ)

- **Ultra-High Efficiency**
- **No Current-Sense Resistor (Lossless I_{LIMIT})**
- **Quasi-PWM with 100ns Load-Step Response**
- **Adjustable Output Range from 0.675V to 3.6V for 1.8V(DDR2) /1.5V(DDR3) /1.35V(DDR3L) /1.2V(LPDDR3) /1.2V(DDR4)**
- **2V to 28V Battery Input Range**
- **Programmable Switching Frequency**
- **OVP & UVP of VDDQ Output**
- **Drives Large Synchronous-Rectifier FETs**
- **Power-Good Indicator**

●1.5A LDO (VTT), Buffered Reference (VTTREF)

- **Support DDR2 (0.9 VTT) and DDR3 (0.75 VTT) and DDR4 (0.6 VTT) Requirements**
- **VLDOIN Voltage Range: 1.2V to 3.6V**
- **Requires Only 20µF Ceramic VTT Output Capacitance**
- **Supports High-Z in S3 and Soft-Off in S4/S5**
- **Integrated Divider Tracks 1/2 VDDQSNS for Both VTT and VTTREF**
- **Remote Sensing (VTTSNS)**
- **±20mV Accuracy for VTT and VTTREF**
- **VTT Discharge Mode :**
  Non-tracking-discharge Mode (G5619)
  Tracking-discharge Mode (G5619A)
- **10mA Buffered Reference (VTTREF)**
- **Built-In Soft-Start to Reduce the VLDOIN Surging Current**
- **Over Current Protection of VTT Output**
- **Thermal Shutdown Protection**

Applications

- **Notebook Computers**
- **CPU Core Supply**
- **Chipset/RAM Supply as Low as 0.675V**

General Description

The G5619/G5619A is intended for DDR2/DDR3/ DDR3L/LPDDR3/DDR4 memory systems. It integrates a synchronous buck PWM controller with a 1.5A sink-source linear regulator and buffered reference.

The PWM controller uses constant on-time control scheme to handle wide input/output voltage ratios with ease and provides 100ns “instant-on” response to load transients while maintaining a relatively constant switching frequency. The G5619/G5619A achieves high efficiency at a reduced cost by eliminating the current-sense resistor found in traditional current-mode PWMs. Efficiency is further enhanced by an ability to drive very large synchronous rectifier MOSFETs. Single-stage buck conversion allows these devices to directly step down high-voltage batteries for the highest possible efficiency.

The 1.5A sink/source tracking termination regulator is specifically designed for low-cost/ low-external component count systems. The regulator contains a high speed operational amplifier that provides fast load transient response with only 20µF (2x10µF) of ceramic output capacitance. The G5619/G5619A supports remote sensing functions and all features required to power the VTT bus termination according to the JEDEC specification. In addition, the G5619/G5619A includes integrated sleep-state controls placing VTT in High-Z in S3 (suspend to RAM) and soft-off for VTT and VTTREF in S4/S5 (Shutdown).

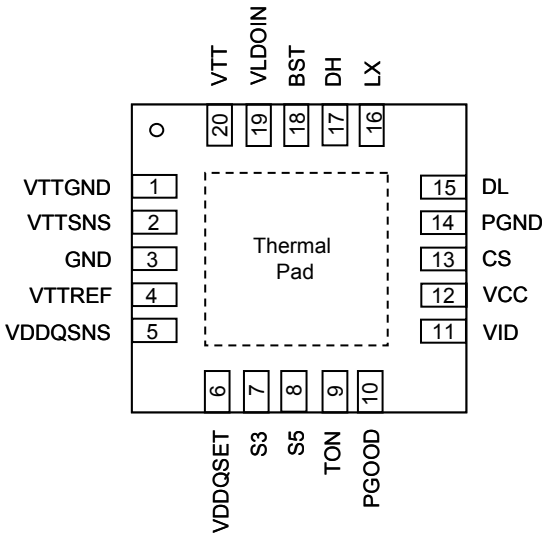
The G5619/G5619A provides OVP, UVP, over current and thermal shutdown protection functions and is available in a 20-pin 3X3 TQFN package.

Ordering Information

ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE (Green)
G5619RZ1U	5619	-40°C to +85°C	TQFN3X3-20
G5619ARZ1U	5619A	-40°C to +85°C	TQFN3X3-20

Note: RZ: TQFN3X3-20
1: Bonding Code
U : Tape & Reel
Green : Lead Free / Halogen Free.

Pin Configuration



G5619/G5619A TQFN3X3-20

Note: Recommend connecting the Thermal Pad to the Ground for excellent power dissipation.

Absolute Maximum Ratings

VCC, VLDOIN to GND . . . . . .-0.3V to 6V
PGOOD to GND . . . . . -0.3V to 6V
TON to GND . . . . . -0.3V to 30V
VTT, VDDQSET, VDDQSNS, VTTSNS, VTTREF, S3, S5, VID to GND. . . . . -0.3V to 6V
DL to GND . . . . . .-0.3V to (VPP+0.3V)
BST to GND . . . . . .-0.3V to 36V
DH to LX . . . . . .-0.3V to 6V
LX to BST . . . . . .-6V to 0.3V
LX to PGND . . . . . .-0.3V to 30V
<20ns . . . . . -6V to 36V

Thermal Resistance Junction to Ambient, (θ_{JA})*
TQFN3X3-20 . . . . . .76°C/W
Continuous Power Dissipation (T_A=25°C)*
TQFN3X3-20 . . . . . .1.6W
Thermal Resistance Junction to Case, (θ_{JC})
TQFN3X3-20 . . . . . .15°C/W
Junction Temperature . . . . . 150°C
Storage Temperature . . . . . -65°C to 150°C
Reflow Temperature (soldering, 10sec) . . . . . 260°C

* : Please refer to 1in^2 of 1oz PCB Layout Section.

Electrical Characteristics

(V+=15V, VCC=5V, VLDOIN=VDDQSNS=1.5V, T_A=25°C)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Synchronous Buck PWM Controller					
Input Voltage Range	Battery Voltage, V+	2	---	24	V
	VCC	4.5	---	5.5	
Error Comparator Threshold (DC Output Voltage Accuracy)	VID=0V, VDDQSET = VDDQ	0.7425	0.75	0.7575	V
	VID=5V, VDDQSET = VDDQ	0.668	0.675	0.682	
Load Regulation Error	ILOAD = 0 to 3A	---	10	---	mV
Line Regulation Error	VCC = 4.5V to 5.5V, V+ = 4.5V to 24V	---	5	---	mV
Quiescent Supply Current 1 (V_{CC1})	V_{S3}=5V, V_{S5}=5V, VDDQSET forced above the regulation point in adjust mode	---	500	---	µA
Quiescent Supply Current 2 (V_{CC2})	V_{S3}=0V, V_{S5}=5V, VDDQSET forced above the regulation point in adjust mode	---	80	---	µA
Shutdown Current 3 (V_{CC3})	V_{S3}=0V, V_{S5}=0V	---	0.1	10	µA
Minimum ON Time		---	100	---	ns
Minimum OFF Time		---	350	---	ns
Operation ON Time	R_{TON}=620kΩ, V_{DDQSNS}=1.5V	270	338	406	ns
Overvoltage Trip Threshold	With respect to error comparator threshold; 5% hysteresis	12	15	20	%
Overvoltage Fault Propagation Delay	VDDQSET forced 2% above the trip threshold in adjust mode	---	30	---	µs
Output Undervoltage Protection Threshold		400	440	500	mV
Output Undervoltage Protection Blanking Time	From VDDQ enable	---	4	---	ms
Current-Limit Threshold Setting Range	PGND – LX	30	---	200	mV
CS Pin Source Current		4.5	5	5.5	µA
Over Current Comparator Offset	PGND – LX	-10	---	10	mV
Current-Limit Threshold (Zero Crossing)	PGND – LX	---	3	---	mV

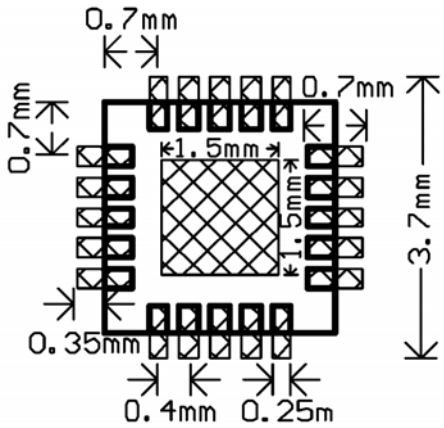
Electrical Characteristics (continued)

(V+=15V, VCC=5V, VLDOIN=VDDQSNS=1.5V, T_A=25°C)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
PGOOD Trip Threshold	Measure at VDDQSET with respect to error comparator threshold, falling edge	-12	-10	-7	%
PGOOD Propagation Delay		---	5.2	---	µs
PGOOD Output Low Voltage	ISINK=1mA	---	---	0.4	V
V_{CC} Undervoltage Lockout Threshold	Rising edge, hysteresis =120mV,PWM disabled below this level	3.9	4.2	4.5	V
DH Gate-Driver On-Resistance	BST - LX forced to 5V	---	1.5	5	Ω
DL Gate-Driver On-Resistance (Pull-Up)	DL, high state	---	1.5	5	Ω
DL Gate-Driver On-Resistance (Pull-Low)	DL, low state	---	0.5	1.7	Ω
DH Gate-Driver Source/Sink Current	DH forced to 2.5V, BST - LX forced to 5V	---	1	---	A
DL Gate-Driver Source Current	DL forced to 2.5V	---	1	---	A
DL Gate-Driver Sink Current	DL forced to 2.5V	---	3	---	A
Dead Time	DL rising	---	18	---	nS
	DH rising	---	14	---	
BST Diode Forward Voltage	Force 10mA current	0.2	0.3	0.4	V
1.5A LDO, Buffered Reference					
Supply current, VLDOIN	no load, V_{S5}=5V, V_{S3} =5V	---	0.03	2	mA
Standby current, VLDOIN	no load, V_{S5}=5V, V_{S3} =0V	---	0.1	10	µA
Shutdown current, VLDOIN	no load, V_{S5}=0V, V_{S3} =0V	---	0.1	1	µA
VDDQSNS input Impedance	V_{S5}=5V, V_{S3} =5V	---	30	---	kΩ
VDDQ Shutdown Discharge Resistance	V_{S5}=0V	---	15	---	Ω
VTTSNS input current	V_{S5}=5V, V_{S3} =5V	---	0.3	1	µA
VTT output voltage		0.9/0.75/0.675/0.6			V
VTT Output Voltage Load Regulation (VTTREF-VTT)	I_{VTT}=0	-20	---	20	mV
	$\|I_{VTT}\|$<1A	-30	---	30	
	$\|I_{VTT}\|$<1.2A	-40	---	40	
VTT Source Current limit	VTT=VDDQSNS/2 *0.95, VTTOK=high	1.6	2.8	---	A
	VTT=0	1	1.5	---	
VTT Sink Current limit	VTT=VDDQSNS/2 *1.05, VTTOK=high	1.6	2.8	---	A
	VTT=VDDQSNS	1	1.5	---	
VTT leakage current in S3 mode	V_{S3}=0V,V_{S5}=5V	-10	---	10	µA
VTT Discharge Current	V_{S5}=0V, V_{S3} =0V, VDDQSNS=0, VTT=0.5V	10	20	---	mA
VTTREF Output Voltage	$\|I_{VTTREF}\|$<10mA, $V_{VDDQSNS}$=1.8V	0.882	---	0.918	V
	$\|I_{VTTREF}\|$<10mA, $V_{VDDQSNS}$ =1.5V	0.735	---	0.765	
	$\|I_{VTTREF}\|$<10mA, $V_{VDDQSNS}$ =1.35V	0.668	---	0.682	
	$\|I_{VTTREF}\|$<10mA, $V_{VDDQSNS}$ =1.2V	0.588	---	0.612	
VTTREF Source Current	$V_{VDDQSNS}$=1.5V, V_{VTTREF}=0	---	-30	---	mA
VTTREF Sink Current	$V_{VDDQSNS}$= V_{VTTREF} =1.5V	---	70	---	mA
High Level Input Voltage	S3 , S5	1.6	---	---	V
Low Level Input Voltage	S3 , S5	---	---	1	V
Logic input Leakage Current	S3 , S5	-1	---	1	µA
VID Input Threshold Voltage	High Level	0.75	---	---	V
	Low Level	---	---	0.3	
VTTSNS Leakage Current	V_{S5}=5V, V_{S3} =0V	-1	---	1	µA
Thermal Shutdown		---	150	---	°C
Thermal Shutdown Hystersis		---	18	---	°C

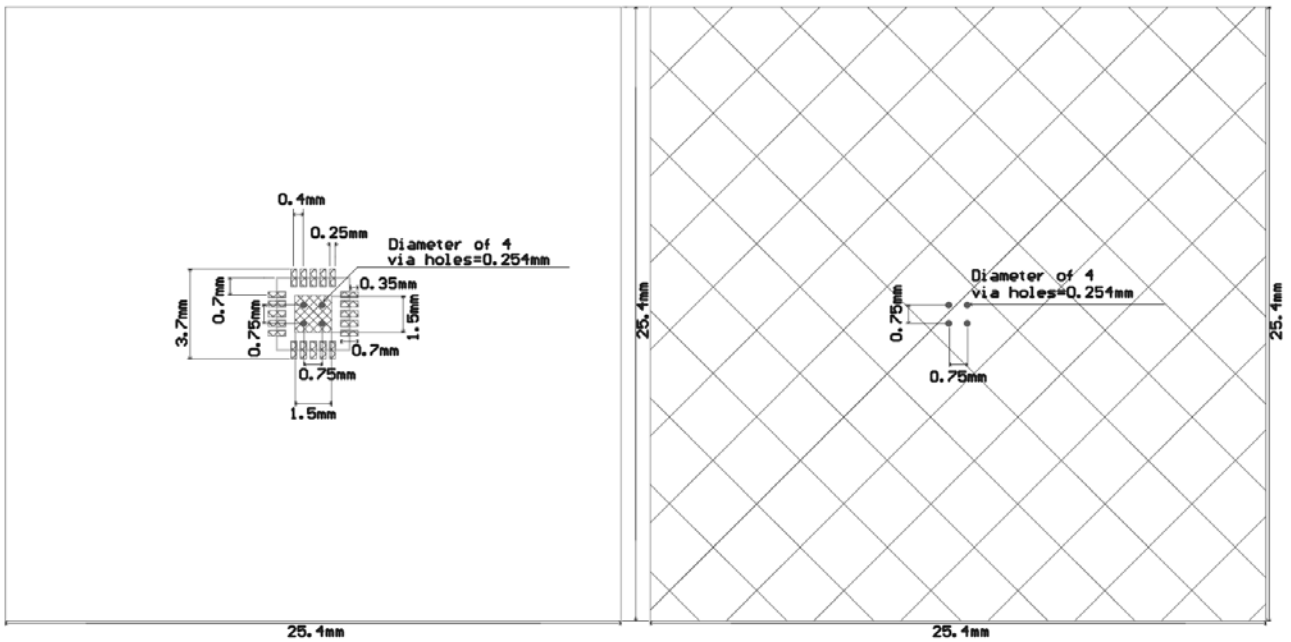
Minimum Footprint PCB Layout Section

TQFN3X3-20



1in^2 of 1oz PCB Layout Section

TQNF3X3-20



Pin Description

PIN	NAME	FUNCTION
1	VTTGND	Power Ground Output For The VTT Output
2	VTTSNS	Voltage Sense Input for the VTT LDO
3	GND	Ground
4	VTTREF	Buffered Reference Output, equal to VDDQSNS/2
5	VDDQSNS	VDDQ sense input
6	VDDQSET	Feedback Input.
7	S3	Active Low Suspend to RAM Mode Control Pin, VTT is turned off and left Hi-Z
8	S5	Active Low Shutdown Pin. VTT and VTTREF are turned off and discharged to Ground.
9	TON	Set the On-time through a pull-up resistor connecting to V_{IN}.
10	PGOOD	Power-Good Open-Drain Output. PGOOD is low when the output voltage is more than 10% below the normal regulation point or during soft-start. PGOOD is high impedance when the output is in regulation and the soft-start circuit has terminated.
11	VID	Internal Reference Setting. VID=0V, Reference=0.75V; VID=5V, Reference=0.675V
12	VCC	Supply Input for Analog Supply and the DL Gate Drive. Connect to the system supply voltage, +4.5V to +5.5V. Bypass to GND with a 1µF (min) ceramic capacitor.
13	CS	Current Limit Threshold Setting Input. Connect a resistor to GND
14	PGND	Power Ground for DL driver
15	DL	Low-Side Gate-Driver Output. Swings from PGND to VPP.
16	LX	External Inductor Connection. Connect LX to the switched side of the inductor. LX serves as the lower supply rail for the DH high-side gate driver. LX is also the positive input to the current-limit comparator.
17	DH	High-Side Gate Driver Output. Swings from LX to BST.
18	BST	Boost Flying-Capacitor Connection.
19	VLDOIN	Power Supply for the VTT and VTTREF output stage
20	VTT	Output Voltage for connection to termination resistors, equal to VDDQSNS/2

Application Information

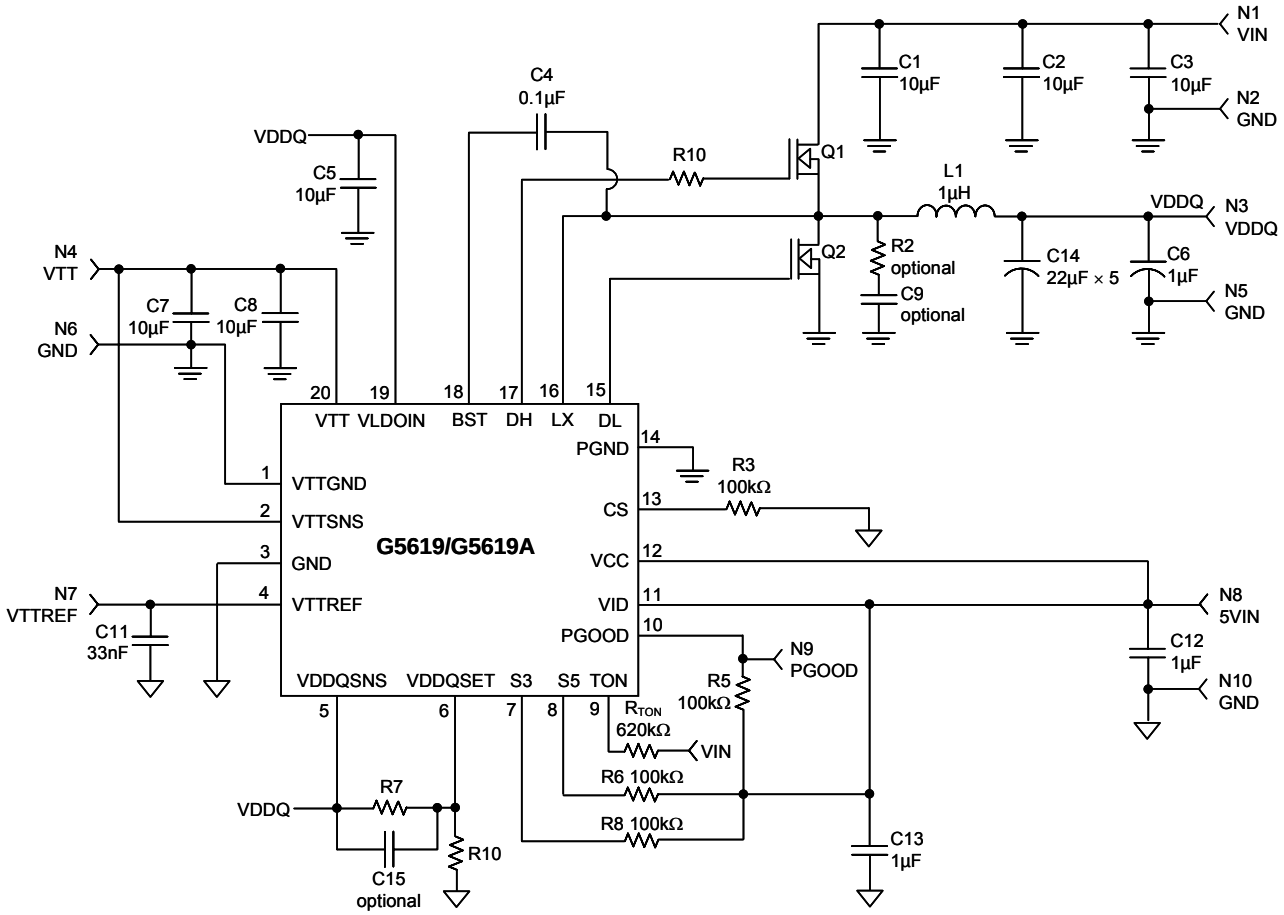


Table 1. Component Selection for standard application:

SYMBOL	SPECIFICATION	MANUFACTURER	PART NUMBER
U1	DC-DC regulator with DDR memory power supplies	GMT	G5619/G5619ARZ1U
C1,C2,C3	10µF, 25V	TAIYO YUDEN	TMK316BJ106ML
C14	22µF, 6.3V		
Q1	30V, 13.5mΩ	AOS	AO4474
Q2	30V, 5.6mΩ	AOS	AO4456
L1	1µH, 2.5mΩ	SUMIDA	CDEP125
C5,C7,C8	10µF, 6.3V	TAIYO YUDEN	JMK316BJ106KD

Block Diagram

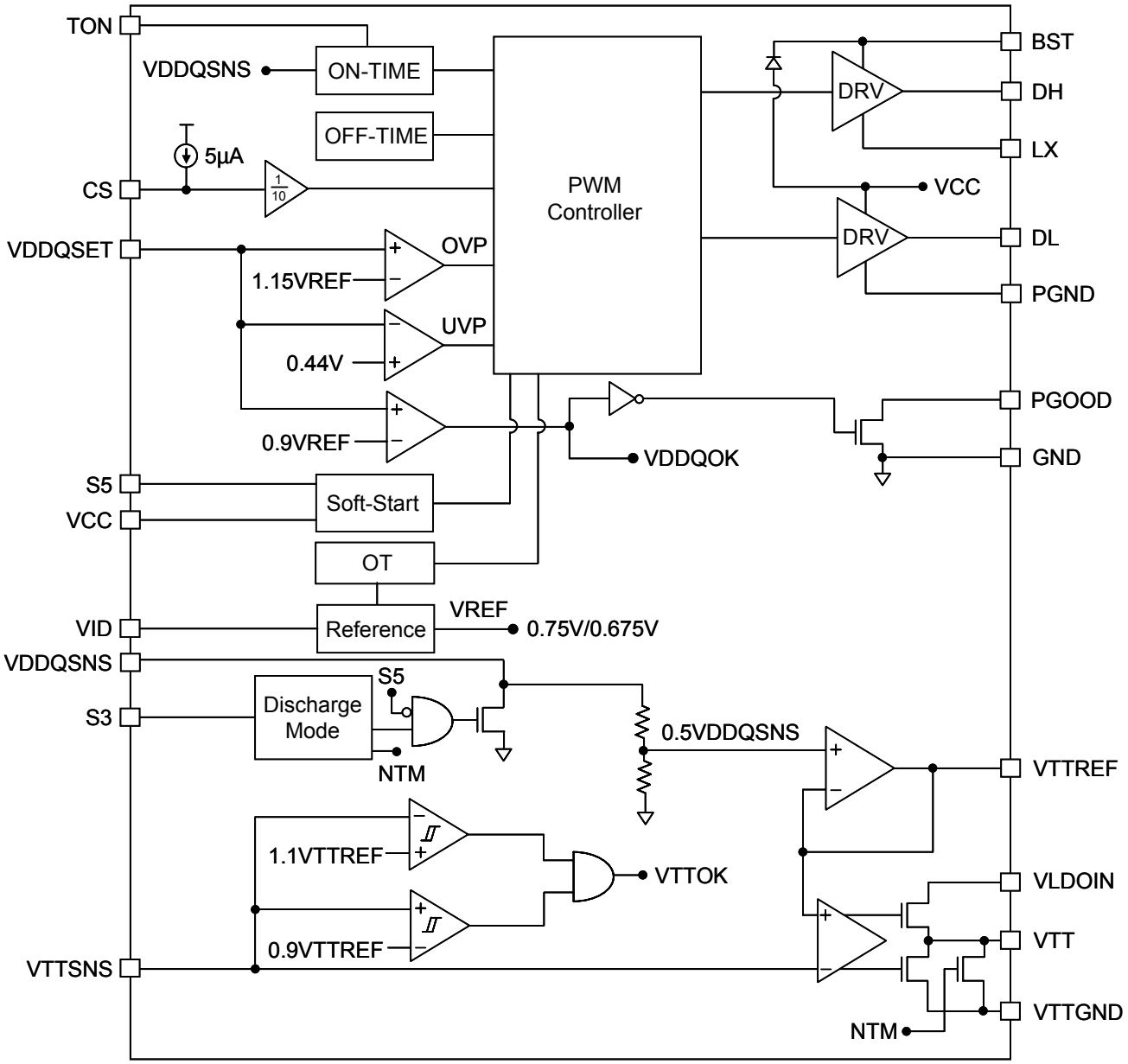


Figure 1 Block Diagram

Detailed Description

G5619/G5619A provides a step down controller and targeted to the low-voltage supply of notebook computers. A Quasi-PWM control is adapted in G5619/G5619A. It is a constant-on-time PWM control with input feed-forward while maintaining a relatively constant switching frequency. It advantages in the fast load-transient response compared with conventional constant-on-time PWM control. Figure 1 shows the Block Diagram.

5V bias Supply (VCC)

G5619/G5619A required an external 5V bias supply for the PWM circuit, LDO, buffered reference and gate-drivers. In the notebook computer, there is a high efficiency 5V system supply and eliminate the cost of external LDO. If no 5V supply existed in the system, it can be generated 5V by LDO such like G920.

Constant-on-time PMW Control with Input Feed-Forward

The Quasi-PWM control algorithm can be described briefly: the high-side switch on-time is determined by a one-shot whose period is inversely proportional to input voltage and directly proportional to output voltage. Another on-shot determines the minimum off-time. The on-time one-shot can be triggered if the error comparator is low, the low side switch current is below the current-limit threshold, and the minimum off-time one-shot has timed out.

On-Time Selection

G5619/G5619A allows to program the on-time. The on time is determined as below

$$T_{ON} = \frac{R_{TON} \times V_{OUT}}{(V_{IN} - 1)} \times 4.0 \times 10^{-12}$$

It results in a nearly constant switching frequency R_{TON} is a resistor connected from V_{IN} to the TON pin. Due to the high impedance of this resistor, 1nF ceramic capacitor is recommended to bypass TON pin to ground.

Current Limit

G5619/G5619A uses the on-state resistance of low side MOSFET as a current-sensing resistor. If the current sense voltage (PGND-LX) is above the current-limit threshold, the PWM is not allowed to initiate a new cycle. The actual peak current is the current-limit threshold adding one inductor current ripple. So it depends on the on-resistance of MOSFET, Inductor value, and battery voltage. No external current sensing resistor is necessary in the output current path. A CS pin could be used to adjust the current-limit threshold. There is a source current from CS pin. Connect a resistor from CS to GND for current-limit threshold setting. The equation for current limit threshold is as follows:

$$I_{LIMIT} = \frac{1}{10} \times \frac{R_{CS}}{R_{DS(ON)}} \times 5\mu A$$

Gate Drivers

In the low duty factor application, like notebook computer, it exists large difference of input voltage and output voltage. Therefore, large low-side MOSFET and moderate-size high-side MOSFET are needed for high efficiency. The DH and DL drivers are optimized for driving high-side and low-side MOSFETs. A non-overlap control circuit is needed to avoid the DH and DL turning on simultaneously. The DL driver with a 0.5Ω pull low transistor helps prevent the DL from being coupled to high during the fast rising-time of the LX node, due to the drain to gate capacitive coupling of low-side synchronous-rectifier MOSFET. A resistor in series with the BST is recommended that will reduce the EMI-producing efficiency loss by increasing the turn-on time of the high-side MOSFET.

POR, UVLO, and Soft-Start of VDDQ

Power-on reset (POR) occurs when VCC rises above approximately 2V. It reset the fault latch and soft-start. When VCC is below 4.2V, undervoltage lockout (UVLO) inhibits switching and forces DL to high.

Power-Good Indicator

The Output voltage is always monitored for undervoltage by the PGOOD comparator. The PGOOD is open-drain type signal. In shutdown and soft-start period, PGOOD is kept low. After the soft-start timer has timed out, the PGOOD is released if the output voltage is within 10% of normal value.

Fault Protection

G5619/G5619A provides undervoltage protection, overvoltage protection, and thermal protection.

The undervoltage protection (UVP) function is like foldback current limit function. If the output voltage is under 440mV more than 4ms after shutdown released, the undervoltage protection function is activated. The PWM is latched off and would not restart until VCC power is cycled or enable signal is toggled.

The overvoltage protection (OVP) function activates when the output voltage is 15% above the set voltage. The low-side MOSFET turn off. This rapidly discharges the output capacitor and decrease the output voltage. The PWM is latched off and would not restart until VCC power is cycled or enable signal is toggled.

The thermal protection (OT) function activates when die temperature exceeds the threshold value (typically: 150°C) the SMPS is shut down. This is non-latch protection.

VDDQ-Output Voltage Setting

Connect the VDDQSET pin to a resistor divider between VDDQSNS and GND to adjust the output voltage between 0.675V to 3.6V.

Chose R10=10kΩ and solve the R7 with the equation:

$$R7 = R10 \times \left(\frac{V_{VDDQ}}{V_{REF}} - 1 \right)$$

where V_{REF} = 0.75V if VID=0V

V_{REF} = 0.675V if VID=5V

VTT SINK/SOURCE Regulator

The G5619/G5619A provides a 1.5A sink/source tracking termination regulator designed specially for low-cost, low external components system where space is at premium such as notebook PC applications. The G5619/G5619A integrates high performance low−dropout linear regulator (LDO) that is capable of sourcing and sinking current up to 1.5A. This VTT linear regulator is implemented with ultimately fast response feedback loop so that small ceramic capacitors are enough to keep tracking to the VTTREF within ±20mV at all conditions including fast load transient. To achieve tight regulation with minimum effect of trace resistance, a remote sensing terminal, VTTSNS, should be connected to the positive node of VTT output capacitor as a separate trace from the high current line from VTT.

VTTREF Regulator

The VTTREF block consists of an on-chip 1/2 divider, LPF and buffer. This regulator can source/sink current up to 10mA. Bypass VTTREF to GND using a 0.1μF ceramic capacitor to ensure stable operation.

Power on Sequence

To operate safely, the G5619/G5619A must keep VCC voltage higher than VLDOIN, VDDQSNS, S3 and S5 pins' voltage .This condition is due to the internal parasitic diodes between VCC to other pins by ESD issue. If the VCC voltage is lower than the other pins voltage, the G5619/G5619A will consume extra current through the parasitic diodes during the power-on period.

VTT Soft-Start

The soft-start function of the VTT is achieved via a current clamp, allowing the output capacitors to be charged with low and constant current that gives linear ramp up of the output voltage. The current limit threshold is changed in two stages using an internal VTTOK signal. When VTT is outside the VTTOK threshold, the current limit level is 1.5A. When VTT rises above (VTTREF - 10%) or falls below (VTTREF + 10%) the current limit level switches to 2.8A. The thresholds are typically VTTREF 10% (from outside regulation to inside) and 15% (when it falls outside). The soft-start function is completely symmetrical and it works not only from GND to VTTREF voltage, but also from VDDQSNS to VTTREF voltage. Note that the VTT output is in a high impedance state during the S3 state (S3 = low, S5 = high) and its voltage can be up to VDDQSNS voltage depending on the external condition. Note that VTT does not start under a full load condition.

S3, S5 Control and Soft-Off

The S3 and S5 terminals should be connected to SLP_S3 and SLP_S5 signals respectively. VDDQ, VTTREF and VTT are turned on at normal state (S3 = high, S5 = high). VDDQ, VTTREF are kept alive while VTT is turned off and left high impedance in standby state (S3 = low, S5 = high). VDDQ, VTT and VTTREF outputs are turned off and discharged to the ground through internal MOSFETs during shutdown state (S5 = low), the detail discharge function is described in Discharge Mode Selection section. The control function is showed on the Table 2.

Table 2. S3 and S5 Control Table

STATE	S3	S5	VTT	VTTREF
Normal	Hi	Hi	VTTREF	VDDQSNS/2
Standby	Lo	Hi	OFF (High-Z)	VDDQSNS/2
Shutdown	Lo	Lo	0V (Discharge)	0V (Discharge)

Discharge Mode

G5619/G5619A discharges VDDQ, VTTREF and VTT outputs during S3 and S5 are both low. G5619 is set as no-tracking-discharge mode. G5619A is set as tracking-discharge mode.

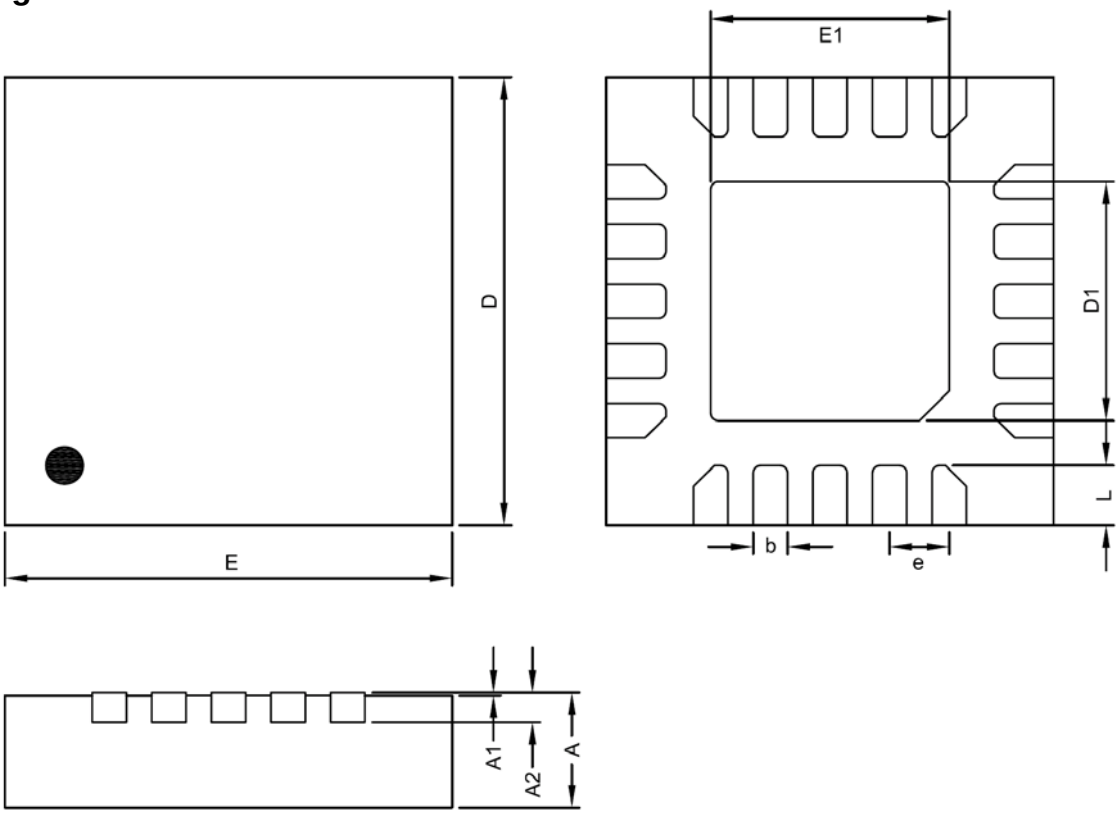
In non-tracking-discharge mode, G5619 discharges outputs using internal MOSFETs which are connected to VDDQSNS and VTT. The current capability of these MOSFETs is limited to discharge slowly.

In tracking-discharge mode, G5619A discharges outputs through the internal VTT regulator transistors and VTT output tracks half of VDDQ voltage during this discharge. Note that VDDQ discharge current flows via VLDOIN to VTTGND. VLDOIN must be connected to VDDQ output in this mode in tracking-discharge mode. The internal LDO can handle up to 1.5A and discharge quickly.

VTT Current Protection

The LDO has a constant overcurrent limit (OCL) at 2.8A. This trip point is reduced to 1.5A before the output voltage comes within 10% of the target voltage or goes outside of 15% of the target voltage.

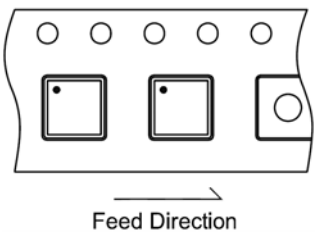
Package Information



TQFN3X3-20 Package

Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.0276	0.0295	0.0315
A1	0.00	---	0.05	0.0000	---	0.0020
A2	0.20 REF			0.0079 REF		
D	2.95	3.00	3.05	0.1161	0.1181	0.1201
E	2.95	3.00	3.05	0.1161	0.1181	0.1201
D1	1.45	1.60	1.75	0.0571	0.0630	0.0689
E1	1.45	1.60	1.75	0.0571	0.0630	0.0689
b	0.15	0.20	0.25	0.0059	0.0079	0.0098
e	0.40 BSC			0.0157 BSC		
L	0.35	0.40	0.45	0.0138	0.0157	0.0177

Taping Specification



PACKAGE	Q'TY/BY REEL
TQFN3X3-20	3,000 ea