G5853

Mobile Phone Power Management System

Features

- **2.8V ~ 5.5V Input Voltage Operation.**
- **95% Efficient DC/DC Converter**
- **Built-in 11-ch synchronous buck converters, 18-ch LDOs, and 1-ch low quiescent current LDO for RTC**
- **Bucks and LDOs can be set to lower quiescent current at low load**
- **Low Power consumption (Shutdown) < 20μA.**
- **Buck1/2/3/4 Supports DVS Function, 25mV/step.**
- **Built-In Power ON/OFF Sequence for PMIC**
- **Built-In Short Circuit Protection (SCP), Under Voltage Protection (UVP), and cycle-by cycle current limit for DC/DC Converters.**
- **18-channel LDOs are Programmable to Voltage Options by I^2C**
- **32kHz Real Time Clock**
- **1-Channel 32kHz Digital CLK Output Buffer**
- **Built-In Thermal Shutdown Function.**
- **Built-In VCC OVP Function**
- **Built-In Power Key Function**
- **WLCSP10X10-84 (0.4mm pitch).**

General Description

The G5853 provide a complete power supply solution for handsets or data card. It contains 11 dc/dc converters and 18 LDOs to power each critical blocks of mobile phone, and is optimized for maximum battery life, featuring a low ground current when in standby mode operation. All channels DC/DC converters operate at the frequency of 1.5MHz or 3.0MHz to optimize size, cost, and efficiency. All Synchronous converters operate at pulse skipping mode at light load. The G5853 features a I^2C compatible interface.

The G5853 is available in WLCSP package.

Applications

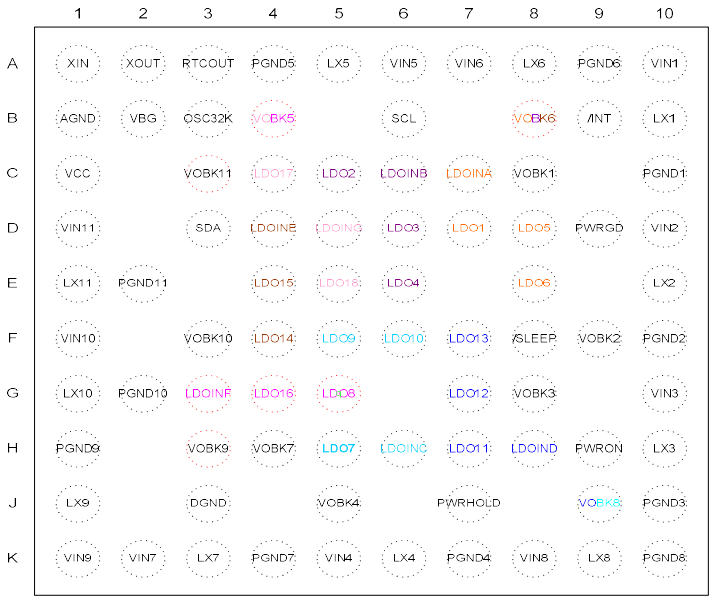
- **Mobile Handsets**
- **Smart Phone**
- **Basic Phone and High-end Phone**
- **Data Card Module**

Ordering Information

ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE (Green)
G5853J51U	5853	-40°C~+85°C	WLCSP10X10-84

Note: J5: WLCSP10X10-84
1: Bonding code
U: Tape & Reel
Green : Lead Free / Halogen Free

Pin Configuration



Top View
WLCSP 10X10-84

Absolute Maximum Ratings

OSC32K . . . . . -0.3V to (VOBK7+0.3) V
All other pins relative to GND . . . . . .-0.3V to 6.3V
Thermal Resistance Junction to Ambient, (θ_{JA})
WLCSP10X10-84 . . . . . 23°C/W
Continuous Power Dissipation (T_A=25°C)
WLCSP10X10-84 . . . . . 5.8W
Operating Ambient Temperature . . . . . -40°C to 85°C
Storage Temperature Range. . . . . -55°C to +150°C
Reflow Temperature (soldering, 10 sec) . . . . . 260°C
ESD (HBM) 2KV

1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Device is ESD sensitive. Handling precaution recommended. The Human Body model is a 100pF capacitor discharged through a 1.5KΩ resistor into each pin.
3. The package is placed on a 6-layer PCB. Please refer the “Board Layout”.

Electrical characteristics

(VCC=VINx =LDOINx=3.7V, T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
GENERAL						
VCC Operating Voltage for PMIC	V_{VCC_PMU}		2.8	---	5.5	V
VCC Over Voltage threshold	V_{VCC_OVLO}	VCC rising	5.8	6.0	---	V
VCC UVLO threshold	V_{VCC_UVLO}	VCC falling, VCCUV=3’b010	2.45	2.5	2.55	V
VCC UVLO Hysteresis	V_{UVLO_HYS}		150	200	250	mV
VCC DDLO threshold	V_{VCC_DDLO}	VCC falling	---	1.85	---	V
VCC Stand-by Supply Current	I_{VCC1}	All Power Units Enter Active Mode,	---	4	6	mA
	I_{VCC2}	All Power Units Enter ECO Mode,	---	250	300	μA
VCC Shutdown Supply Current	I_{VCC_SDN}	All Power Units off except RTC	---	5	10	μA
Control Signal						
Logic-Input Threshold	V_{TH}	High threshold	1.4	---	---	V
(PWRON,PWRHOLD,/SLEEP)	V_{TL}	Low threshold	---	---	0.5	V
Internal pull high resistance (PWRON,/SLEEP)	R_H	Pull high to VCC	---	200	---	kΩ
Internal pull low resistance (PWRHOLD)	R_L	Pull low to GND	---	200	---	kΩ
Open-Drain Output Low Voltage (/INT, PWRGD)	V_{ODLOW}	I_{SINK}=5mA, V_{VCC}=3.7V	---	---	100	mV
Open-Drain Output Leakage Current (/INT,PWRGD)	I_{LK_OD}	V_{OD}=5V	---	---	1	μA
PWRGD Delay Time	T_{DLY_PWRGD}		45	64	83	mS
PWRON long long-pressed delay time	$T_{dPWRONLLP}$	TIME_LLP[1:0]=11	7	10	13	Sec
PWRON long-pressed delay time	$T_{dPWRONLP}$	TIME_LP[1:0]=00	0.7	1	1.3	Sec
PWRON de-bouncing delay time	$T_{dbPWRONF}$	TIME_IT[1:0]=01	2.1	3	3.9	Sec
Protection						
UVP Protection Fault Delay	T_{D_Fault}	DCDC1~DCDC11	128	---	---	mS
Thermal Shutdown Detect	T_{SD}		---	150	---	°C
Thermal Shutdown Hysteresis	ΔT_{SD}		---	20	---	°C

Electrical Characteristics (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
2A Buck Converter (DCDC1,DCDC3,DCDC8)						
Quiescent Current	I_{QDC_ACT}	Active Mode, not include I_{VIN}	---	30	40	μA
	I_{QDC_ECO}	ECO Mode, not include I_{VIN}	---	5	9	μA
Soft-Start Internal	t_{SS_DC}		---	1	---	mS
VOUT regulation voltage accuracy	%VO1		-1.5	---	1.5	%
Switching frequency	f_{SW1p5M}	In CCM, DCDC-1/3, VO≤0.65V	1.25	1.5	1.75	MHz
	f_{SW3M}	In CCM, DCDC-1/3, VO>0.65V	2.5	3	3.5	MHz
	f_{SW3M}	In CCM, DCDC-8	2.5	3	3.5	MHz
Maximum Duty Cycle	D_{max1}		---	100	---	%
VIN Leakage Current	I_{VIN_LK}	V_{LX}=0V, V_{IN} =5.0V	---	---	1	μA
LX Leakage Current	I_{LX_LK}	V_{LX}=5.0V	---	---	1	μA
Switch ON Resistance	R_{ON1_P}	DCDC-1/3	---	65	---	mΩ
	R_{ON1_N}	DCDC-1/3	---	25	---	mΩ
	R_{ON8_P}	DCDC-8	---	90	---	mΩ
	R_{ON8_N}	DCDC-8	---	60	---	mΩ
Peak Current Limit	I_{LIM_DC1}		3.0	3.5	---	A
Under Voltage Protection Threshold	ΔV_{UVP_DC1}	ΔV_{UVP_CH1}=$VOUT_{SET}$-$VOUT_{UVP}$ (DCDC-1/3)	---	125	---	mV
	$\%V_{UVP\_DC8}$	Ratio=V_{UVP}/V_{OUT},DCDC8	---	90	---	%
Maximum Continuous Output Current	I_{O1_MAX}	V_{IN}=3.8V	---	---	2	A
Efficiency	η1	Io=Io_max, V_{IN} =3.8V, Vo=1.0V	---	80	---	%
	η3	Io=Io_max, V_{IN} =3.8V, Vo=0.75V	---	75	---	%
	η8	Io=Io_max, V_{IN} =3.8V, Vo=1.5V	---	83	---	%
PSM to PWM Output Current Threshold	I_{TH1}	L=0.47μH, Vo=1V, V_{IN} =3.8V	---	300	---	mA
	I_{TH8}	L=0.47μH, Vo=1.5V, V_{IN} =3.8V	---	350	---	mA
Discharge Resistance	R_{DISCH_DC1}	VCC=3.8V	---	50	---	Ω

Electrical Characteristics (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
3A Buck Converter (DCDC2,DCDC4,DCDC5,DCDC6,DCDC7)						
Quiescent Current	I_{QDC_ACT}	Active Mode, not include I_{VIN}	---	30	40	μA
	I_{QDC_ECO}	ECO Mode, not include I_{VIN}	---	5	9	μA
Soft-Start Internal	t_{SS_DC}		---	1	---	mS
VOUT regulation voltage accuracy	%VO2		-1.5	---	1.5	%
Switching frequency	f_{SW1p5M}	In CCM, DCDC-2/4, VO≤0.65V	1.25	1.5	1.75	MHz
	f_{SW3M}	In CCM, DCDC-2/4, VO>0.65V	2.5	3	3.5	MHz
	f_{SW3M}	In CCM, DCDC-5/6/7	2.5	3	3.5	MHz
Maximum Duty Cycle	D_{max2}		---	100	---	%
VIN Leakage Current	I_{VIN_LK}	V_{LX}=0V, V_{IN} =5.0V	---	---	1	μA
LX Leakage Current	I_{LX_LK}	V_{LX}=5.0V	---	---	1	μA
Switch ON Resistance	R_{ON2_P}	DCDC-2/4/5/6/7	---	65	---	mΩ
	R_{ON2_N}	DCDC-2/4/5/7	---	25	---	mΩ
	R_{ON6_N}	DCDC-6	---	60	---	mΩ
Peak Current Limit	I_{LIM_DC2}		4.0	4.5	---	A
Under Voltage Protection Threshold	ΔV_{UVP_DC2}	ΔV_{UVP_CH2}=$VOUT_{SET}$-$VOUT_{UVP}$ (DCDC-2/4/5)	---	125	---	mV
	$\%V_{UVP\_DC6}$	Ratio=V_{UVP}/V_{OUT},DCDC6	---	75	---	%
	$\%V_{UVP\_DC7}$	Ratio=V_{UVP}/V_{OUT},DCDC7	---	90	---	%
Maximum Continuous Output Current	I_{O2_MAX}	V_{IN} =3.8V	---	---	3	A
Efficiency (DCDC-2)	η2	Io=Io_max, V_{IN} =3.8V, Vo=1.0V	---	77	---	%
Efficiency (DCDC-4)	η4	Io=Io_max, V_{IN} =3.8V, Vo=0.75V	---	70	---	%
Efficiency (DCDC-5)	η5	Io=Io_max, V_{IN} =3.8V, Vo=1.2V	---	80	---	%
Efficiency (DCDC-6)	η6	Io=Io_max, V_{IN} =3.8V, Vo=3.2V	---	89	---	%
Efficiency (DCDC-7)	η7	Io=Io_max, V_{IN} =3.8V, Vo=1.8V	---	85	---	%
PSM to PWM Output Current Threshold	I_{TH2}	L=0.47μH, Vo=1.0V, V_{IN} =3.8V	---	300	---	mA
	I_{TH5}	L=0.47μH, Vo=1.2V, V_{IN} =3.8V	---	320	---	mA
	I_{TH6}	L=0.47μH, Vo=3.2V, V_{IN} =3.8V	---	130	---	mA
	I_{TH7}	L=0.47μH, Vo=1.8V, V_{IN}=3.8V	---	350	---	mA
Discharge Resistance	R_{DISCH_DC2}	VCC=3.8V	---	50	---	Ω

Electrical Characteristics (continued)

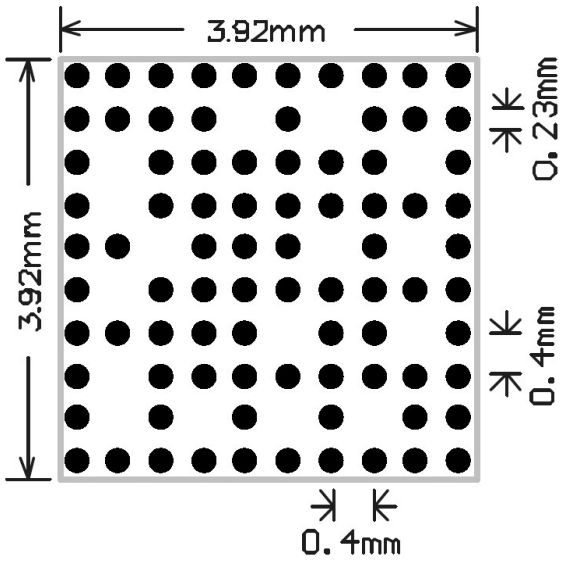
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
1A Buck Converter (DCDC9,DCDC10,DCDC11)						
Quiescent Current	I_{QDC_ACT}	Active Mode, not include I_{VIN}	---	30	40	μA
	I_{QDC_ECO}	ECO Mode, not include I_{VIN}	---	5	9	μA
Soft-Start Internal	t_{SS_DC}		---	1	---	mS
VOUT regulation voltage accuracy	%VO9		-1.5	---	1.5	%
Switching frequency	f_{SW1p5M}	In CCM, DCDC-10, VO≤0.65V	1.25	1.5	1.75	MHz
	f_{SW3M}	In CCM, DCDC-10, VO>0.65V	2.5	3	3.5	MHz
	f_{SW3M}	In CCM, DCDC-9/11	2.5	3	3.5	MHz
Maximum Duty Cycle	D_{max9}		---	100	---	%
VIN Leakage Current	I_{VIN_LK}	V_{LX}=0V, V_{IN} =5.0V	---	---	1	μA
LX Leakage Current	I_{LX_LK}	V_{LX}=5.0V	---	---	1	μA
Switch ON Resistance	R_{ON9_P}		---	130	---	mΩ
	R_{ON9_N}		---	110	---	mΩ
Peak Current Limit	I_{LIM_DC9}		2	2.5	---	A
Under Voltage Protection Threshold	ΔV_{UVP_DC9}	ΔV_{UVP_CH2}=$VOUT_{SET}$-$VOUT_{UVP}$ (DCDC-9/10)	---	125	---	mV
	$\%V_{UVP\_DC11}$	Ratio=V_{UVP}/V_{OUT}, DCDC11	---	90	---	%
Maximum Continuous Output Current	I_{O9_MAX}	V_{IN} =3.8V	---	---	1	A
Efficiency (DCDC-9)	η9	Io=Io_max, V_{IN} =3.8V, Vo=1.15V	---	80	---	%
Efficiency (DCDC-10)	η10	Io=Io_max, V_{IN} =3.8V, Vo=0.6V	---	75	---	%
Efficiency (DCDC-11)	η11	Io=Io_max, V_{IN} =3.8V, Vo=1.5V	---	90	---	%
PSM to PWM Output Current Threshold	I_{TH2}	L=1μH, Vo=1.2V, V_{IN} =3.8V	---	165	---	mA
	I_{TH5}	L=1μH, Vo=1.1V, V_{IN} =3.8V	---	160	---	mA
	I_{TH6}	L=1μH, Vo=1.5V, V_{IN} =3.8V	---	150	---	mA
Discharge Resistance	R_{DISCH_DC9}	VCC=3.8V	---	50	---	Ω
LDO						
Input voltage range	V_{LDOIN}	LDO7,8,9,10,11,12,13,16,17,18	1.1	---	2.5	V
		LDO1,2,3,4,5,6,14,15	2.4	---	5.0	V
Soft-Start Internal	SS_{LDO}		---	1	---	mS
Output Voltage accuracy	$\%V_{LDO}$	Io=100mA,	-1.5	---	1.5	%
Continuous output current	I_{O_ECO}	ECO mode, LDOx	---	---	5	mA
	I_{O1_NRM}	Normal Mode, LDO1,2,5,6	---	---	300	mA
	I_{O3_NRM}	Normal Mode, other LDOs	---	---	500	mA
	I_{O15_NRM}	Normal Mode, LDO15,17,18	---	---	750	mA
	I_{O16_NRM}	Normal Mode, LDO16	---	---	1000	mA
LDO Input Current	I_{LDOIN}	Io=0mA, Normal mode	---	---	32	μA
	I_{LDOINB_ECO}	Io=0mA, ECO mode	---	---	8	μA
Dropout Voltage	V_{DOLDO}	Io= I_{OX_NRM}, Normal mode	---	200	300	mV
	V_{DOLLDO}	Io=50mA, Normal mode	---	35	70	mV
Output current limit	I_{LIMLDO}	LDOIN>LDO+1.0V, , Normal mode	I_{OX_NRM} +50	I_{OX_NRM} +100	---	mA
LDO Load Regulation	%LD	LDOIN>LDO+1.0V, Normal mode Io=1mA ~ (I_{OX_NRM} -100mA)	---	---	1	%
Short Circuit Protection threshold	$\%V_{SCPLDO}$	Ratio=V_{SCP}/V_{OUT}	---	12.5	---	%
Ripple Rejection	PSRR	f=10Hz~3kHz, Io=100mA	70	75	---	dB
Output Noise Voltage	V_{NRMS}	f=10Hz~100kHz, Normal mode	---	45	---	μVrms
ECO exit time	T_{d_ECO}	Minimum wait time to draw full current after leaving ECO mode	---	---	50	μS
Discharge Resistance	R_{DISCH_LDO}	VCC=3.8V	---	50	---	Ω

Electrical characteristics (continued)

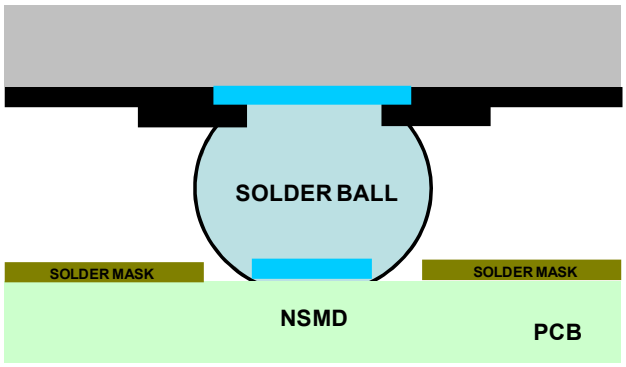
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
RTCLDO						
Input voltage range	V_{VINRTC}	VCC	2.5	---	5.5	V
Standby current	I_{Q1_RTC}	V_{VCC}=3.7v	---	5	8	μA
Output voltage	V_{RTCO}	Io=0.1mA, VORTC=2'b10	---	3.0	---	V
Dropout Voltage	V_{DO1_RTC}	Io=50mA, VORTC=2'b10	---	---	800	mV
	V_{DO2_RTC}	Io=10mA, VORTC=2'b10	---	---	150	mV
Maximum Output Current		V_{VCC}=4.2v, RTCOUT=95%*V_{SET}	60	---	200	mA
32.768kHz Real Time Clock						
RTC Supply Current	I_{Q_RTC}	RTCOUT=3.0V	---	1	---	μA
OSC32K Duty Cycle	D_{OSC_32K}		40	---	60	%
OSC32K Output high voltage	V_{OH_OSC}	Follow DCDC7 output voltage	---	VOBK7	---	V
OSC32K Output Sink Current	I_{SINK_OSC}	OSC32K=0.4V, VOBK7=1.8V, VCC=3.3V~4.2V	---	1	---	mA
OSC32K Output Source Current	I_{SOURCE_OSC}	OSC32K =VOBK7-0.4V, VCC=3.3V~4.2V	---	1	---	mA
OSC32K startup delay time	T_{DLY_X32K}	Delay from DCDC7 power ready	---	100	---	mS
SMBus Interface						
Logic Input High Voltage	V_{IH}	SCL, SDA	1.4	---	---	V
Logic Input Low Voltage	V_{IL}	SCL, SDA	---	---	0.5	V
Logic Input Current		Logic inputs forced to VCC or GND	-2	---	2	μA
SMBus Input Capacitance		SCL, SDA	---	5	---	pF
SMBus Clock Frequency	f_{SCL}	Fast mode	---	---	400	kHz
		High-speed mode, load 400pF max	---	---	1.7	MHz
		High-speed mode, load 100pF max	---	---	3.4	MHz
SCL Clock Low Time	t_{LOW}	Fast mode	1.3	---	---	μS
SCL Clock High Time	t_{HIGH}	Fast mode	0.6	---	---	μS
SDA Setup Time	$t_{SU:DAT}$	Fast mode	100	---	---	nS
SDA Hold Time	$t_{HD:DAT}$	Fast mode	0.03	---	0.9	μS
Bus-Free Time from START and STOP	t_{BUF}	Fast mode	1.3	---	---	μS
Hold Time Repeated START Condition	$t_{HD:STA}$	Fast mode	0.6	---	---	μS
Setup Time Repeated START Condition	$t_{SU:STA}$	Fast mode	0.6	---	---	μS
Setup Time for STOP Condition	$t_{SU:STO}$	Fast mode	0.6	---	---	μS
Rise Time of SCL/SDA signals	t_r	10% to 90% points	20	---	300	nS
Fall Time of SCL/SDA signals	t_f	90% to 10% points	20	---	300	nS

Minimum Footprint PCB Layout Section

WLCSP10X10-84



1. NSMD Structure
2. Pad size = 228.6um (9mils)
3. Solder mask open =330.2um (2mils + 9mils + 2mils)



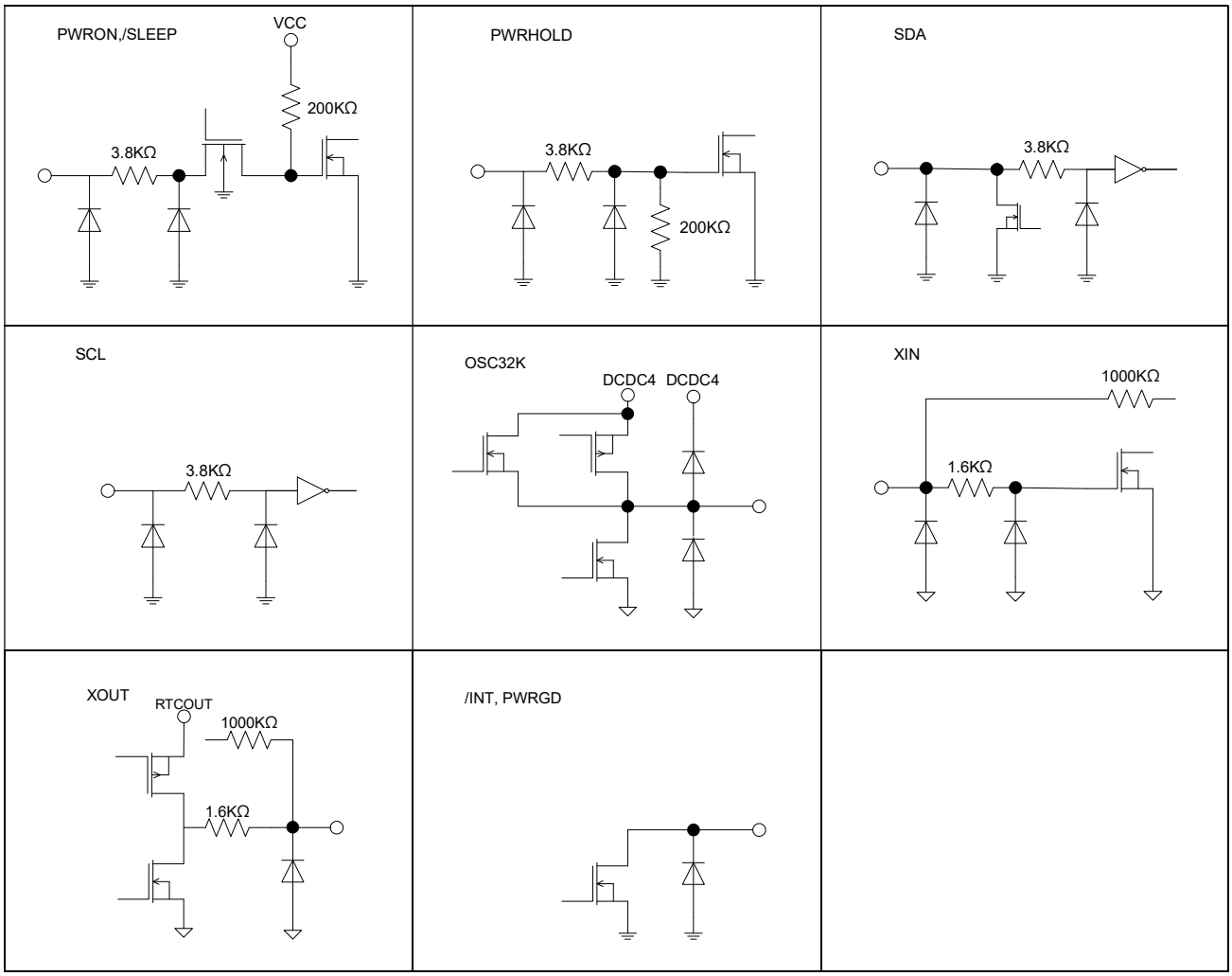
Pin Description

Pin	NAME	TYPE	Function
A10	VIN1	P	Power Input of DCDC1 Buck Converter.
B10	LX1	DO	Inductor switch node of DCDC1 Buck Converter.
C10	PGND1	G	Power ground of DCDC1 Buck Converter
C8	VOBK1	AI	Sensing Input of DCDC1 Buck Converter's output voltage.
D10	VIN2	P	Power Input of DCDC2 Buck Converter.
E10	LX2	DO	Inductor switch node of DCDC2 Buck Converter.
F10	PGND2	G	Power ground of DCDC2 Buck Converter
F9	VOBK2	AI	Sensing Input of DCDC2 Buck Converter's output voltage.
G10	VIN3	P	Power Input of DCDC3 Buck Converter.
H10	LX3	DO	Inductor switch node of DCDC3 Buck Converter.
J10	PGND3	G	Power ground of DCDC3 Buck Converter
G8	VOBK3	AI	Sensing Input of DCDC3 Buck Converter's output voltage
K5	VIN4	P	Power Input of DCDC4 Buck Converter.
K6	LX4	DO	Inductor switch node of DCDC4 Buck Converter.
K7	PGND4	G	Power ground of DCDC4 Buck Converter
J5	VOBK4	AI	Sensing Input of DCDC4 Buck Converter's output voltage
A6	VIN5	P	Power Input of DCDC5 Buck Converter.
A5	LX5	DO	Inductor switch node of DCDC5 Buck Converter.
A4	PGND5	G	Power ground of DCDC5 Buck Converter
B4	VOBK5	AI	Sensing Input of DCDC5 Buck Converter's output voltage
A7	VIN6	P	Power Input of DCDC6 Buck Converter.
A8	LX6	DO	Inductor switch node of DCDC6 Buck Converter.
A9	PGND6	G	Power ground of DCDC6 Buck Converter
B8	VOBK6	AI	Sensing Input of DCDC5 Buck Converter's output voltage.
K2	VIN7	P	Power Input of DCDC7 Buck Converter.
K3	LX7	DO	Inductor switch node of DCDC7 Buck Converter.
K4	PGND7	G	Power ground of DCDC7 Buck Converter
H4	VOBK7	AI	Sensing Input of DCDC7 Buck Converter's output voltage
K8	VIN8	P	Power Input of DCDC8 Buck Converter.
K9	LX8	DO	Inductor switch node of DCDC8 Buck Converter.
K10	PGND8	G	Power ground of DCDC8 Buck Converter
J9	VOBK8	AI	Sensing Input of DCDC8 Buck Converter's output voltage
K1	VIN9	P	Power Input of DCDC9 Buck Converter.
J1	LX9	DO	Inductor switch node of DCDC9 Buck Converter.
H1	PGND9	G	Power ground of DCDC9 Buck Converter
H3	VOBK9	AI	Sensing Input of DCDC9 Buck Converter's output voltage
F1	VIN10	P	Power Input of DCDC10 Buck Converter.
G1	LX10	DO	Inductor switch node of DCDC10 Buck Converter.
G2	PGND10	G	Power ground of DCDC10 Buck Converter
F3	VOBK10	AI	Sensing Input of DCDC10 Buck Converter's output voltage
D1	VIN11	P	Power Input of DCDC11 Buck Converter.
E1	LX11	DO	Inductor switch node of DCDC11 Buck Converter.
E2	PGND11	G	Power ground of DCDC11 Buck Converter
C3	VOBK11	AI	Sensing Input of DCDC11 Buck Converter's output voltage
C7	LDOINA	P	Power Input of LDO1, LDO5, and LDO6.
C6	LDOINB	P	Power Input of LDO2, LDO3, and LDO4.
H6	LDOINC	P	Power Input of LDO7, LDO9, and LDO10.
H8	LDOIND	P	Power Input of LDO11, LDO12, and LDO13.
D4	LDOINE	P	Power Input of LDO14, and LDO15.
G3	LDOINF	P	Power Input of LDO8, and LDO16.
D5	LDOING	P	Power Input of LDO17, and LDO18.

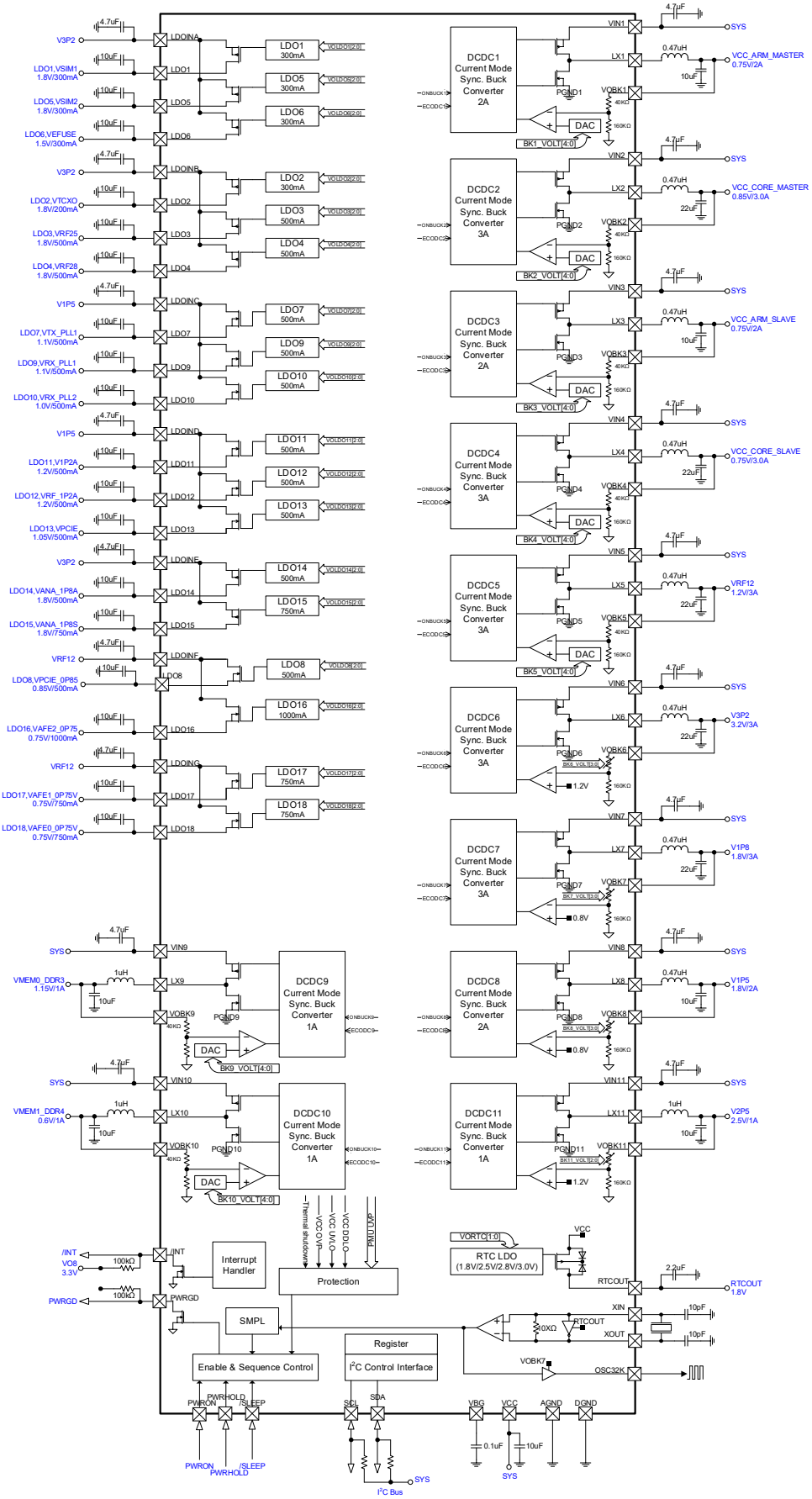
Pin Description (continued)

Pin	NAME	TYPE	Function
D7	LDO1	AO	LDO Output of LDO1.
C5	LDO2	AO	LDO Output of LDO2.
D6	LDO3	AO	LDO Output of LDO3.
E6	LDO4	AO	LDO Output of LDO4.
D8	LDO5	AO	LDO Output of LDO5.
E8	LDO6	AO	LDO Output of LDO6.
H5	LDO7	AO	LDO Output of LDO7.
G5	LDO8	AO	LDO Output of LDO8.
F5	LDO9	AO	LDO Output of LDO9.
F6	LDO10	AO	LDO Output of LDO10.
H7	LDO11	AO	LDO Output of LDO11.
G7	LDO12	AO	LDO Output of LDO12.
F7	LDO13	AO	LDO Output of LDO13.
F4	LDO14	AO	LDO Output of LDO14.
E4	LDO15	AO	LDO Output of LDO15.
G4	LDO16	AO	LDO Output of LDO16.
C4	LDO17	AO	LDO Output of LDO17.
E5	LDO18	AO	LDO Output of LDO18.
A3	RTCOUT	AO	LDO Output of RTC LDO. Bypass this pin to ground with a 2.2μF ceramic capacitor.
A1	XIN	AI	Crystal Oscillator Input
A2	XOUT	IO	Crystal Oscillator Output
B3	OSC32K	DO	32.768kHz clock output
H9	PWRON	DI	Power on/off key, internal pull high to VCC. Active-low.
J7	PWRHOLD	DI	Power on/off signal from Microprocessor, internal pull low to AGND. Active-high.
F8	/SLEEP	DI	SLEEP mode control pin. internal pull high to VCC. Active-low.
D9	PWRGD	DO	Indicator of PMU power on/off with open drain output.
B9	/INT	DO	Interrupt Indicator with open drain output.
B6	SCL	DI	Clock Input PIN of I^2C interface.
D3	SDA	IO	Data Input PIN of I^2C interface.
C1	VCC	P	IC Power Supply Input pin. Bypass with a 10uF or greater ceramic capacitor.
B1	AGND	G	Chip analog ground
J3	DGND	G	Chip digital ground
B2	VBG	AO	1.21V Reference Voltage Output. Bypass this pin to ground with a 0.1μF ceramic capacitor.
A: Analog Pin, D: Digital Pin, I: Input Pin, O: Output Pin, P: Power Pin, G: Ground Pin			

Equivalent Circuits of Inputs and Outputs



Block Diagram & Application circuit



I²C Interface

G5853 I²C slave address=7'b0010010. The write or read bit stream (N≥1) is shown below:

Driven by Master

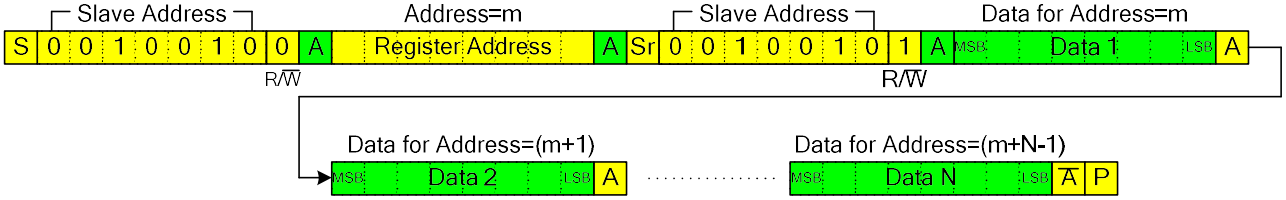
Driven by G5853

S Start

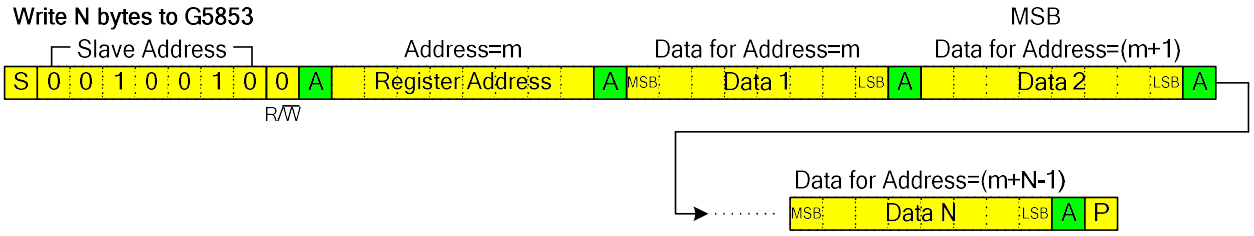
P Stop

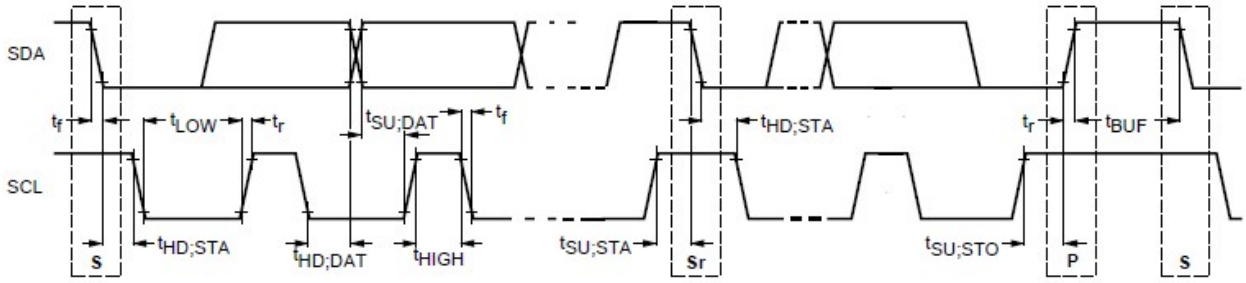
Sr Repeat Start

Read N bytes from G5853



Write N bytes to G5853





I²C Register Map

ADDR.	FUNCTION	RESET VALUE	7	6	5	4	3	2	1	0
0x00 (R)	INTR_A	0x00	PWRON	PWRON _LLP	PWRON_LP	PWRON_IT	PWRHOLD	---	---	SMPL
0x01 (R)	INTR_B	0x00	PWRGD	---	---	THERMAL5	THERMAL4	THERMAL3	THERMAL2	THERMAL1
0x02 (R)	INTR_C	0x00	FAULT_BK8	FAULT_BK7	FAULT_BK6	FAULT_BK5	FAULT_BK4	FAULT_BK3	FAULT_BK2	FAULT_BK1
0x03 (R)	INTR_D	0x00	---	---	---	---	---	FAULT _BK11	FAULT _BK10	FAULT_BK9
0x04 (R)	INTR_E	0x00	FAULT _LDO8	FAULT _LDO7	FAULT _LDO6	FAULT _LDO5	FAULT _LDO4	FAULT _LDO3	FAULT _LDO2	FAULT _LDO1
0x05 (R)	INTR_F	0x00	FAULT _LDO16	FAULT _LDO15	FAULT _LDO14	FAULT _LDO13	FAULT _LDO12	FAULT _LDO11	FAULT _LDO10	FAULT _LDO9
0x06 (R)	INTR_G	0x00	---	---	---	---	---	---	FAULT _LDO18	FAULT _LDO17
0x07 (R/W)	INTR_MASK_A	0xFD	MASK _PWRON	MASK_LLP	MASK_LP	MASK_IT	MASK _PWRHOLD	---	---	MASK _SMPL
0x08 (R/W)	INTR_MASK_B	0x9F	MASK _PWRGD	---	---	MASK _TH5	MASK _TH4	MASK _TH3	MASK _TH2	MASK _TH1
0x09 (R/W)	INTR_MASK_C	0xFF	MASK _BK8	MASK _BK7	MASK _BK6	MASK _BK5	MASK _BK4	MASK _BK3	MASK _BK2	MASK _BK1
0x0A (R/W)	INTR_MASK_D	0xFF	---	---	---	---	---	MASK _BK11	MASK _BK10	MASK _BK9
0x0B (R/W	INTR_MASK_E	0xFF	MASK _LDO8	MASK _LDO7	MASK _LDO6	MASK _LDO5	MASK _LDO4	MASK _LDO3	MASK _LDO2	MASK _LDO1
0x0C (R/W))	INTR_MASK_F	0xFF	MASK _LDO16	MASK _LDO15	MASK _LDO14	MASK _LDO13	MASK _LDO12	MASK _LDO11	MASK _LDO10	MASK _LDO9
0x0D (R/W)	INTR_MASK_G	0xF3	---	---	---	---	---	---	MASK _LDO18	MASK _LDO17
0x0E (R)	STATUS_A	0x00	FAULT_BK8	FAULT_BK7	FAULT_BK6	FAULT_BK5	FAULT_BK4	FAULT_BK3	FAULT_BK2	FAULT_BK1
0x0F (R)	STATUS_B	0x00	---	---	---	---	---	FAULT _BK11	FAULT _BK10	FAULT_BK9
0x10 (R)	STATUS_C	0x00	FAULT _LDO8	FAULT _LDO7	FAULT _LDO6	FAULT _LDO5	FAULT _LDO4	FAULT _LDO3	FAULT _LDO2	FAULT _LDO1
0x11 (R)	STATUS_D	0x00	FAULT _LDO16	FAULT _LDO15	FAULT _LDO14	FAULT _LDO13	FAULT _LDO12	FAULT _LDO11	FAULT _LDO10	FAULT _LDO9
0x12 (R)	STATUS_E	0x00	---	---	---	---	---	---	FAULT _LDO18	FAULT _LDO17
0x20 (R/W)	BUCK1_VOLT	0x04	---	---	---	BK1_VOLT[4:0]				
0x21 (R/W)	BUCK2_VOLT	0x08	---	---	---	BK2_VOLT[4:0]				
0x22 (R/W)	BUCK3_VOLT	0x08	---	---	---	BK3_VOLT[4:0]				
0x23 (R/W)	BUCK4_VOLT	0x08	---	---	---	BK4_VOLT[4:0]				
0x24 (R/W)	BUCK5_VOLT	0x12	---	---	---	BK5_VOLT[4:0]				
0x25 (R/W)	BUCK6_BUCK7 _VOLT	0xDB	BK7_VOLT[3:0]				BK6_VOLT[3:0]			
0x26 (R/W)	BUCK8_BUCK11 _VOLT	0x4D		BK11_VOLT[2:0]			BK8_VOLT[3:0]			
0x27 (R/W)	BUCK9_VOLT	0x10	---	---	---	BK9_VOLT[4:0]				
0x28 (R/W)	BUCK10_VOLT	0x02	---	---	---	BK10_VOLT[4:0]				
0x29 (R/W)	BUCK1_SLPVOLT	0x04	---	---	---	BK1_SLPVOLT[4:0]				
0x2A (R/W)	BUCK2_SLPVOLT	0x08	---	---	---	BK2_SLPVOLT[4:0]				
0x2B (R/W)	BUCK3_SLPVOLT	0x08	---	---	---	BK3_SLPVOLT[4:0]				
0x2C (R/W)	BUCK4_SLPVOLT	0x08	---	---	---	BK4_SLPVOLT[4:0]				
0x2D (R/W)	BUCK5_SLPVOLT	0x12	---	---	---	BK5_SLPVOLT[4:0]				
0x2E (R/W)	BUCK6_BUCK7 _SLPVOLT	0xDB	BK7_SLPVOLT[3:0]				BK6_SLPVOLT[3:0]			
0x2F (R/W)	BUCK8_BUCK11 _SLPVOLT	0x4D	---	BK11_SLPVOLT[2:0]			BK8_SLPVOLT[3:0]			
0x30 (R/W)	BUCK9_SLPVOLT	0x10	---	---	---	BK9_SLPVOLT[4:0]				
0x31 (R/W)	BUCK10_SLPVOLT	0x02	---	---	---	BK10_SLPVOLT[4:0]				

I²C Register Map (continued)

ADDR.	FUNCTION	RESET VALUE	7	6	5	4	3	2	1	0
0x32 (R/W)	BUCK_MODE CONTROL	0x23	BK2_NRMMODE[1:0]		BK2_SLPMODE[1:0]		BK1_NRMMODE[1:0]		BK1_SLPMODE[1:0]	
0x33 (R/W)	BUCK_MODE CONTROL	0x22	BK4_NRMMODE[1:0]		BK4_SLPMODE[1:0]		BK3_NRMMODE[1:0]		BK3_SLPMODE[1:0]	
0x34 (R/W)	BUCK_MODE CONTROL	0x23	BK6_NRMMODE[1:0]		BK6_SLPMODE[1:0]		BK5_NRMMODE[1:0]		BK5_SLPMODE[1:0]	
0x35 (R/W)	BUCK_MODE CONTROL	0x22	BK8_NRMMODE[1:0]		BK8_SLPMODE[1:0]		BK7_NRMMODE[1:0]		BK7_SLPMODE[1:0]	
0x36 (R/W)	BUCK_MODE CONTROL	0x22	BK10_NRMMODE[1:0]		BK10_SLPMODE[1:0]		BK9_NRMMODE[1:0]		BK9_SLPMODE[1:0]	
0x37 (R/W)	BUCK_MODE CONTROL	0x02	---	---	---	---	BK11_NRMMODE[1:0]		BK11_SLPMODE[1:0]	
0x40 (R/W)	LDO1/2_VOLT	0x33	---	LDO2_VOLT[2:0]			---	LDO1_VOLT[2:0]		
0x41 (R/W)	LDO3/4_VOLT	0x33	---	LDO4_VOLT[2:0]			---	LDO3_VOLT[2:0]		
0x42 (R/W)	LDO5/6_VOLT	0x23	---	LDO6_VOLT[2:0]			---	LDO5_VOLT[2:0]		
0x43 (R/W)	LDO7/8_VOLT	0x31	---	LDO8_VOLT[2:0]			---	LDO7_VOLT[2:0]		
0x44 (R/W)	LDO9/10_VOLT	0x11	---	LDO10_VOLT[2:0]			---	LDO9_VOLT[2:0]		
0x45 (R/W)	LDO11/12_VOLT	0x33	---	LDO12_VOLT[2:0]			---	LDO11_VOLT[2:0]		
0x46 (R/W)	LDO13/14_VOLT	0x32	---	LDO14_VOLT[2:0]			---	LDO13_VOLT[2:0]		
0x47 (R/W)	LDO15/16_VOLT	0x23	---	LDO16_VOLT[2:0]			---	LDO15_VOLT[2:0]		
0x48 (R/W)	LDO17/18_VOLT	0x22	---	LDO18_VOLT[2:0]			---	LDO17_VOLT[2:0]		
0x49 (R/W)	LDO1/2_SLPVOLT	0x33	---	LDO2_SLPVOLT[2:0]			---	LDO1_SLPVOLT[2:0]		
0x4A (R/W)	LDO3/4_SLPVOLT	0x33	---	LDO4_SLPVOLT[2:0]			---	LDO3_SLPVOLT[2:0]		
0x4B (R/W)	LDO5/6_SLPVOLT	0x23	---	LDO6_SLPVOLT[2:0]			---	LDO5_SLPVOLT[2:0]		
0x4C (R/W)	LDO7/8_SLPVOLT	0x31	---	LDO8_SLPVOLT[2:0]			---	LDO7_SLPVOLT[2:0]		
0x4D (R/W)	LDO9/10_SLPVOLT	0x11	---	LDO10_SLPVOLT[2:0]			---	LDO9_SLPVOLT[2:0]		
0x4E (R/W)	LDO11/12_SLPVOLT	0x33	---	LDO12_SLPVOLT[2:0]			---	LDO11_SLPVOLT[2:0]		
0x4F (R/W)	LDO13/14_SLPVOLT	0x32	---	LDO14_SLPVOLT[2:0]			---	LDO13_SLPVOLT[2:0]		
0x50 (R/W)	LDO15/16_SLPVOLT	0x23	---	LDO16_SLPVOLT[2:0]			---	LDO15_SLPVOLT[2:0]		
0x51 (R/W)	LDO17/18_SLPVOLT	0x22	---	LDO18_SLPVOLT[2:0]			---	LDO17_SLPVOLT[2:0]		
0x52 (R/W)	LDO_MODE CONTROL	0xFE	LDO4_SLPMODE[1:0]		LDO3_SLPMODE[1:0]		LDO2_SLPMODE[1:0]		LDO1_SLPMODE[1:0]	
0x53 (R/W)	LDO_MODE CONTROL	0xFF	LDO8_SLPMODE[1:0]		LDO7_SLPMODE[1:0]		LDO6_SLPMODE[1:0]		LDO5_SLPMODE[1:0]	
0x54 (R/W)	LDO_MODE CONTROL	0xEF	LDO12_SLPMODE[1:0]		LDO11_SLPMODE[1:0]		LDO10_SLPMODE[1:0]		LDO9_SLPMODE[1:0]	
0x55 (R/W)	LDO_MODE CONTROL	0xBF	LDO16_SLPMODE[1:0]		LDO15_SLPMODE[1:0]		LDO14_SLPMODE[1:0]		LDO13_SLPMODE[1:0]	
0x56 (R/W)	LDO_MODE CONTROL	0x0F	---	---	---	---	LDO18_SLPMODE[1:0]		LDO17_SLPMODE[1:0]	
0x60 (R/W)	BUCK_ENABLE CONTROL	0xFF	ONBUCK8	ONBUCK7	ONBUCK6	ONBUCK5	ONBUCK4	ONBUCK3	ONBUCK2	ONBUCK1
0x61 (R/W)	BUCK_ENABLE CONTROL	0x07	---	---	---	---	---	ONBUCK11	ONBUCK10	ONBUCK9
0x62 (R/W)	LDO_ENABLE CONTROL	0xDE	ONLDO8	ONLDO7	ONLDO6	ONLDO5	ONLDO4	ONLDO3	ONLDO2	ONLDO1
0x63 (R/W)	LDO_ENABLE CONTROL	0xFF	ONLDO16	ONLDO15	ONLDO14	ONLDO13	ONLDO12	ONLDO11	ONLDO10	ONLDO9
0x64 (R/W)	LDO_ENABLE CONTROL	0x03	---	---	---	---	---	---	ONLDO18	ONLDO17
0x65 (R/W)	BUCK_ENABLE DISCHARGE	0xFF	ENDISCHG_BK8	ENDISCHG_BK7	ENDISCHG_BK6	ENDISCHG_BK5	ENDISCHG_BK4	ENDISCHG_BK3	ENDISCHG_BK2	ENDISCHG_BK1
0x66 (R/W)	BUCK_ENABLE DISCHARGE	0x07	---	---	---	---	---	ENDISCHG_BK11	ENDISCHG_BK10	ENDISCHG_BK9
0x67 (R/W)	LDO_ENABLE DISCHARGE	0xFF	ENDISCHG_LDO8	ENDISCHG_LDO7	ENDISCHG_LDO6	ENDISCHG_LDO5	ENDISCHG_LDO4	ENDISCHG_LDO3	ENDISCHG_LDO2	ENDISCHG_LDO1
0x68 (R/W)	LDO_ENABLE DISCHARGE	0xFF	ENDISCHG_LDO16	ENDISCHG_LDO15	ENDISCHG_LDO14	ENDISCHG_LDO13	ENDISCHG_LDO12	ENDISCHG_LDO11	ENDISCHG_LDO10	ENDISCHG_LDO9
0x69 (R/W)	LDO_ENABLE DISCHARGE	0x03	---	---	---	---	---	---	ENDISCHG_LDO18	ENDISCHG_LDO17

I²C Register Map (continued)

ADDR.	FUNCTION	RESET VALUE	7	6	5	4	3	2	1	0
0x70 (R/W)	SYS Control	0x00	SOFTON	SLEEP	---	---	VORTC[1:0]		---	RST_FAULT
0x71 (R/W)	PWRKEY CONTROL	0x71	---	EN_LLP	TIME_LLP[1:0]		TIME_LP[1:0]		TIME_IT[1:0]	
0x72 (R/W)	VCC_UV CONTROL	0x32	---	EN_SMPL	SMPL_SEL[1:0]		---	VCCUV[2:0]		
0x73 (R/W)	TDLY_X32K CONTROL	0x0E	TIMER_X32K[7:0]							
0xE0 (R)	VERSION	0x44	CHIP_ID[3:0]				VERSION[3:0]			
0xFA (R/W)	GMT TEST	0x00	---	---	---	TM[4:0]				

I²C Register Reset Conditions

ADDR.	Register Function	Rest Condition
0x00~0x06	Interrupt Registers	VCC<V_{VCC_DDLO}, or the power-off reset pulse. Also reset by reading them
0x0E~0x12	Power Rails Fault Status	VCC< V_{VCC_DDLO} or 0x50[0] is written to 1
0x65~0x69	Power Rails Enable Discharge Registers	RTCOUT<1.3V, or the power-on leading pulse
0x70[3:2]	RTC LDO Voltage Registers	VCC< V_{VCC_DDLO}
0x71	Power-key IT/LP/LLP Registers	VCC< V_{VCC_DDLO}, or the power-on leading pulse
0x72[2:0]	VCC UV Registers	RTCOUT<1.3V
0x72[6:4]	VCC SMPL Registers	RTCOUT<1.3V, or power-off reset pulse when VCC> V_{VCC_UVLO}
Other Registers		VCC< V_{VCC_DDLO}, or the power-off reset pulse.

I²C Register Function Table

Address: 0x00
Description: Interrupt of PWRON and PWRHOLD pin status.

Bits	b7	b6	b5	b4	b3	b2	b1	b0
Meaning	PWRON	PWRON_LLP	PWRON_LP	PWRON_IT	PWRHOLD	---	---	SMPL
Default	0	0	0	0	0	---	---	0
Read/Write	R	R	R	R	R	---	---	R

Bits	Name	Description
b7	PWRON	1: PWRON pin state has changed since last read.
b6	PWRON_LLP	1: PWRON has been held low with duration longer than $T_{dPWRONLLP}$ since last read.
b5	PWRON_LP	1: PWRON has been held low with duration longer than $T_{dPWRONLP}$ since last read.
b4	PWRON_IT	1: PWRON has been held low with duration longer than $T_{dbPWRONF}$ since last read.
b3	PWRHOLD	1: PWRHOLD state has changed since last read.
b2	---	
b1	---	
b0	SMPL	1: sudden momentary power loss condition occurs since last read.

Address: 0x01
Description: Interrupt of PWRGD pin and die temperature.

Bits	b7	b6	b5	b4	b3	b2	b1	b0
Meaning	PWRGD	---	---	THERMAL5	THERMAL4	THERMAL3	THERMAL2	THERMAL1
Default	0	---	---	0	0	0	0	0
Read/Write	R	---	---	R	R	R	R	R

Bits	Name	Description
b7	PWRGD	1: PWRGD pin state has changed since last read.
b6	---	
b5	---	
b4	THERMAL5	1: PMIC Die Temperature> 150°C
b3	THERMAL4	1: 150°C >PMIC Die Temperature> 130°C
b2	THERMAL3	1: 130°C >PMIC Die Temperature> 110°C
b1	THERMAL2	1: 110°C >PMIC Die Temperature> 90°C
b0	THERMAL1	1: PMIC Die Temperature<90°C

Address: 0x02
Description: Interrupt of Buck Converters' fault condition.

Bits	b7	b6	b5	b4	b3	b2	b1	b0
Meaning	FAULT_BK8	FAULT_BK7	FAULT_BK6	FAULT_BK5	FAULT_BK4	FAULT_BK3	FAULT_BK2	FAULT_BK1
Default	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

Bits	Name	Description
b7	FAULT_BK7	1: Output UVP of Buck8
b6	FAULT_BK7	1: Output UVP of Buck7
b5	FAULT_BK6	1: Output UVP of Buck6
b4	FAULT_BK5	1: Output UVP of Buck5
b3	FAULT_BK4	1: Output UVP of Buck4
b2	FAULT_BK3	1: Output UVP of Buck3
b1	FAULT_BK2	1: Output UVP of Buck2
b0	FAULT_BK1	1: Output UVP of Buck1

Address: 0x03
Description: Interrupt of Buck Converters' fault condition.

Bits	b7	b6	b5	b4	b3	b2	b1	b0
Meaning	---	---	---	---	---	FAULT_BK11	FAULT_BK10	FAULT_BK9
Default	---	---	---	---	---	0	0	0
Read/Write	---	---	---	---	---	R	R	R

Bits	Name	Description
b7	---	
b6	---	
b5	---	
b4	---	
b3	---	
b2	FAULT_BK11	1: Output UVP of Buck3
b1	FAULT_BK10	1: Output UVP of Buck2
b0	FAULT_BK9	1: Output UVP of Buck1

Address: 0x04
Description: Interrupt of LDOs' fault condition. LDO1~LDO8

Bits	b7	b6	b5	b4	b3	b2	b1	b0
Meaning	FAULT_LDO8	FAULT_LDO7	FAULT_LDO6	FAULT_LDO5	FAULT_LDO4	FAULT_LDO3	FAULT_LDO2	FAULT_LDO1
Default	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

Bits	Name	Description
b7	FAULT_LDO8	1: Output SCP of LDO8
b6	FAULT_LDO7	1: Output SCP of LDO7
b5	FAULT_LDO6	1: Output SCP of LDO6
b4	FAULT_LDO5	1: Output SCP of LDO5
b3	FAULT_LDO4	1: Output SCP of LDO4
b2	FAULT_LDO3	1: Output SCP of LDO3
b1	FAULT_LDO2	1: Output SCP of LDO2
b0	FAULT_LDO1	1: Output SCP of LDO1

Address: 0x05
Description: Interrupt of LDOs' fault condition. LDO9~LDO16

Bits	b7	b6	b5	b4	b3	b2	b1	b0
Meaning	FAULT_LDO16	FAULT_LDO15	FAULT_LDO14	FAULT_LDO13	FAULT_LDO12	FAULT_LDO11	FAULT_LDO10	FAULT_LDO9
Default	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

Bits	Name	Description
b7	FAULT_LDO16	1: Output SCP of LDO16
b6	FAULT_LDO15	1: Output SCP of LDO15
b5	FAULT_LDO14	1: Output SCP of LDO14
b4	FAULT_LDO13	1: Output SCP of LDO13
b3	FAULT_LDO12	1: Output SCP of LDO12
b2	FAULT_LDO11	1: Output SCP of LDO11
b1	FAULT_LDO10	1: Output SCP of LDO10
b0	FAULT_LDO9	1: Output SCP of LDO9

Address: 0x06
Description: Interrupt of LDOs' fault condition. LDO17~LDO18

Bits	b7	b6	b5	b4	b3	b2	b1	b0
Meaning	---	---	---	---	---	---	FAULT_LDO18	FAULT_LDO17
Default	---	---	---	---	---	---	0	0
Read/Write	---	---	---	---	---	---	R	R

Bits	Name	Description
b7	---	
b6	---	
b5	---	
b4	---	
b3	---	
b2	---	
b1	FAULT_LDO18	1: Output SCP of LDO18
b0	FAULT_LDO17	1: Output SCP of LDO17

Address: 0x07
Description: Interrupt mask of PMIC PWRON and PWRHOLD pin status.

Bits	b7	b6	b5	b4	b3	b2	b1	b0
Meaning	MASK_PWRON	MASK_LLP	MASK_LP	MASK_IT	MASK_PWRHOLD	---	---	---
Default	1	1	1	1	1	---	---	---
Read/Write	R/W	R/W	R/W	R/W	R/W	---	---	---

Bits	Name	Description
b7	MASK_PWRON	0: interrupt active.1: interrupt masked.
b6	MASK_LLP	
b5	MASK_LP	
b4	MASK_IT	
b3	MASK_PWRHOLD	
b2	---	
b1	---	
b0	MASK_SMPL	0: interrupt active.1: interrupt masked.

Address: 0x08
Description: Interrupt mask of die temperature.

Bits	b7	b6	b5	b4	b3	b2	b1	b0
Meaning	MASK_PWRGD	---	---	MASK_TH5	MASK_TH4	MASK_TH3	MASK_TH2	MASK_TH1
Default	1	---	---	1	1	1	1	1
Read/Write	R/W	---	---	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
b7	MASK_PWRGD	0: interrupt active.1: interrupt masked.
b6	---	
b5	---	
b4	MASK_TH5	
b3	MASK_TH4	
b2	MASK_TH3	
b1	MASK_TH2	
b0	MASK_TH1	

Address: 0x09
Description: Interrupt mask of Buck Converters' fault condition.

Bits	b7	b6	b5	b4	b3	b2	b1	b0
Meaning	MASK_BK8	MASK_BK7	MASK_BK6	MASK_BK5	MASK_BK4	MASK_BK3	MASK_BK2	MASK_BK1
Default	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
b7	MASK_BK8	0: interrupt active.1: interrupt masked.
b6	MASK_BK7	
b5	MASK_BK6	
b4	MASK_BK5	
b3	MASK_BK4	
b2	MASK_BK3	
b1	MASK_BK2	
b0	MASK_BK1	

Address: 0x0A
Description: Interrupt mask of Buck Converters' fault condition.

Bits	b7	b6	b5	b4	b3	b2	b1	b0
Meaning	---	---	---	---	---	MASK_BK11	MASK_BK10	MASK_BK9
Default	---	---	---	---	---	1	1	1
Read/Write	---	---	---	---	---	R/W	R/W	R/W

Bits	Name	Description
b7	---	
b6	---	
b5	---	
b4	---	
b3	---	
b2	MASK_BK11	0: interrupt active.1: interrupt masked.
b1	MASK_BK10	
b0	MASK_BK9	

Address: 0x0B
Description: Interrupt mask of LDOs' fault condition.

Bits	b7	b6	b5	b4	b3	b2	b1	b0
Meaning	MASK_LDO8	MASK_LDO7	MASK_LDO6	MASK_LDO5	MASK_LDO4	MASK_LDO3	MASK_LDO2	MASK_LDO1
Default	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
b7	MASK_LDO8	0: interrupt active.1: interrupt masked.
b6	MASK_LDO7	
b5	MASK_LDO6	
b4	MASK_LDO5	
b3	MASK_LDO4	
b2	MASK_LDO3	
b1	MASK_LDO2	
b0	MASK_LDO1	

Address: 0x0C
Description: Interrupt mask of LDOs' fault condition.

Bits	b7	b6	b5	b4	b3	b2	b1	b0
Meaning	MASK_LDO16	MASK_LDO15	MASK_LDO14	MASK_LDO13	MASK_LDO12	MASK_LDO11	MASK_LDO10	MASK_LDO9
Default	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
b7	MASK_LDO16	0: interrupt active.1: interrupt masked.
b6	MASK_LDO15	
b5	MASK_LDO14	
b4	MASK_LDO13	
b3	MASK_LDO12	
b2	MASK_LDO11	
b1	MASK_LDO10	
b0	MASK_LDO9	

Address: 0x0D
Description: Interrupt mask of LDOs' fault condition.

Bits	b7	b6	b5	b4	b3	b2	b1	b0
Meaning	---	---	---	---	---	---	MASK_LDO18	MASK_LDO17
Default	---	---	---	---	---	---	1	1
Read/Write	---	---	---	---	---	---	R/W	R/W

Bits	Name	Description
b7	---	
b6	---	
b5	---	
b4	---	
b3	---	
b2	---	
b1	MASK_LDO18	0: interrupt active.1: interrupt masked.
b0	MASK_LDO17	

Address: 0x0E
Description: Status of Buck Converters' fault condition.

Bits	b7	b6	b5	b4	b3	b2	b1	b0
Meaning	FAULT_BK8	FAULT_BK7	FAULT_BK6	FAULT_BK5	FAULT_BK4	FAULT_BK3	FAULT_BK2	FAULT_BK1
Default	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

Bits	Name	Description
b7	FAULT_BK7	1: Output UVP of Buck8
b6	FAULT_BK7	1: Output UVP of Buck7
b5	FAULT_BK6	1: Output UVP of Buck6
b4	FAULT_BK5	1: Output UVP of Buck5
b3	FAULT_BK4	1: Output UVP of Buck4
b2	FAULT_BK3	1: Output UVP of Buck3
b1	FAULT_BK2	1: Output UVP of Buck2
b0	FAULT_BK1	1: Output UVP of Buck1

Address: 0x0F
Description: Status of Buck Converters' fault condition.

Bits	b7	b6	b5	b4	b3	b2	b1	b0
Meaning	---	---	---	---	---	FAULT_BK11	FAULT_BK10	FAULT_BK9
Default	---	---	---	---	---	0	0	0
Read/Write	---	---	---	---	---	R	R	R

Bits	Name	Description
b7	---	
b6	---	
b5	---	
b4	---	
b3	---	
b2	FAULT_BK11	1: Output UVP of Buck3
b1	FAULT_BK10	1: Output UVP of Buck2
b0	FAULT_BK9	1: Output UVP of Buck1

Address: 0x10
Description: Status of LDOs' fault condition.

Bits	b7	b6	b5	b4	b3	b2	b1	b0
Meaning	FAULT_LDO8	FAULT_LDO7	FAULT_LDO6	FAULT_LDO5	FAULT_LDO4	FAULT_LDO3	FAULT_LDO2	FAULT_LDO1
Default	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

Bits	Name	Description
b7	FAULT_LDO8	1: Output SCP of LDO8
b6	FAULT_LDO7	1: Output SCP of LDO7
b5	FAULT_LDO6	1: Output SCP of LDO6
b4	FAULT_LDO5	1: Output SCP of LDO5
b3	FAULT_LDO4	1: Output SCP of LDO4
b2	FAULT_LDO3	1: Output SCP of LDO3
b1	FAULT_LDO2	1: Output SCP of LDO2
b0	FAULT_LDO1	1: Output SCP of LDO1

Address: 0x11
Description: Status of LDOs' fault condition.

Bits	b7	b6	b5	b4	b3	b2	b1	b0
Meaning	FAULT_LDO16	FAULT_LDO15	FAULT_LDO14	FAULT_LDO13	FAULT_LDO12	FAULT_LDO11	FAULT_LDO10	FAULT_LDO9
Default	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

Bits	Name	Description
b7	FAULT_LDO16	1: Output SCP of LDO16
b6	FAULT_LDO15	1: Output SCP of LDO15
b5	FAULT_LDO14	1: Output SCP of LDO14
b4	FAULT_LDO13	1: Output SCP of LDO13
b3	FAULT_LDO12	1: Output SCP of LDO12
b2	FAULT_LDO11	1: Output SCP of LDO11
b1	FAULT_LDO10	1: Output SCP of LDO10
b0	FAULT_LDO9	1: Output SCP of LDO9

Address: 0x12
Description: Status of LDOs' fault condition.

Bits	b7	b6	b5	b4	b3	b2	b1	b0
Meaning	---	---	---	---	---	---	FAULT_LDO18	FAULT_LDO17
Default	---	---	---	---	---	---	0	0
Read/Write	---	---	---	---	---	---	R	R

Bits	Name	Description
b7	---	
b6	---	
b5	---	
b4	---	
b3	---	
b2	---	
b1	FAULT_LDO18	1: Output SCP of LDO18
b0	FAULT_LDO17	1: Output SCP of LDO17

Address: 0x20/0x29
Description: Buck1 output voltage in normal/sleep mode

Bits	b7	b6	b5	b4	b3	b2	b1	b0
Meaning	---	---	---	BK1_VOLT[4]	BK1_VOLT[3]	BK1_VOLT[2]	BK1_VOLT[1]	BK1_VOLT[0]
Default	---	---	---	0	0	1	0	0
Read/Write	---	---	---	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
b7	---	
b6	---	
b5	---	
b4	BK1_VOLT[4]	V_{OUT}= BK1_VOLT[4:0] x 25mV + 0.65V, V_{OUT} Range: 0.65V~1.425V
b3	BK1_VOLT[3]	
b2	BK1_VOLT[2]	
b1	BK1_VOLT[1]	
b0	BK1_VOLT[0]	

Address: 0x21/0x2A
Description: Buck2 output voltage in normal/sleep mode

Bits	b7	b6	b5	b4	b3	b2	b1	b0
Meaning	---	---	---	BK2_VOLT[4]	BK2_VOLT[3]	BK2_VOLT[2]	BK2_VOLT[1]	BK2_VOLT[0]
Default	---	---	---	0	1	0	0	0
Read/Write	---	---	---	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
b7	---	
b6	---	
b5	---	
b4	BK2_VOLT[4]	V_{OUT}= BK2_VOLT[4:0] x 25mV + 0.65V, V_{OUT} Range: 0.65V~1.425V
b3	BK2_VOLT[3]	
b2	BK2_VOLT[2]	
b1	BK2_VOLT[1]	
b0	BK2_VOLT[0]	

Address: 0x22/0x2B
Description: Buck3 output voltage in normal/sleep mode

Bits	b7	b6	b5	b4	b3	b2	b1	b0
Meaning	---	---	---	BK3_VOLT[4]	BK3_VOLT[3]	BK3_VOLT[2]	BK3_VOLT[1]	BK3_VOLT[0]
Default	---	---	---	0	1	0	0	0
Read/Write	---	---	---	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
b7	---	
b6	---	
b5	---	
b4	BK3_VOLT[4]	V_{OUT}= BK3_VOLT[4:0] x25mV + 0.55V, V_{OUT} Range: 0.55V~1.325V
b3	BK3_VOLT[3]	
b2	BK3_VOLT[2]	
b1	BK3_VOLT[1]	
b0	BK3_VOLT[0]	

Address: 0x23/0x2C
Description: Buck4 output voltage in normal/sleep mode

Bits	b7	b6	b5	b4	b3	b2	b1	b0
Meaning	---	---	---	BK4_VOLT[4]	BK4_VOLT[3]	BK4_VOLT[2]	BK4_VOLT[1]	BK4_VOLT[0]
Default	---	---	---	0	1	0	0	0
Read/Write	---	---	---	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
b7	---	
b6	---	
b5	---	
b4	BK4_VOLT[4]	V_{OUT}= BK4_VOLT[4:0] x25mV + 0.55V, V_{OUT} Range: 0.55V~1.325V
b3	BK4_VOLT[3]	
b2	BK4_VOLT[2]	
b1	BK4_VOLT[1]	
b0	BK4_VOLT[0]	

Address: 0x24/0x2D
Description: Buck5 output voltage in normal/sleep mode

Bits	b7	b6	b5	b4	b3	b2	b1	b0
Meaning	---	---	---	BK5_VOLT[4]	BK5_VOLT[3]	BK5_VOLT[2]	BK5_VOLT[1]	BK5_VOLT[0]
Default	---	---	---	1	0	0	1	0
Read/Write	---	---	---	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
b7	---	
b6	---	
b5	---	
b4	BK5_VOLT[4]	V_{OUT}= BK5_VOLT[4:0] x 25mV + 0.75V, V_{OUT} Range: 0.75V~1.525V
b3	BK5_VOLT[3]	
b2	BK5_VOLT[2]	
b1	BK5_VOLT[1]	
b0	BK5_VOLT[0]	

Address: 0x25/0x2E
Description: Buck6 and Buck7 output voltage in normal/sleep mode

Bits	b7	b6	b5	b4	b3	b2	b1	b0
Meaning	BK7_VOLT[3]	BK7_VOLT[2]	BK7_VOLT[1]	BK7_VOLT[0]	BK6_VOLT[3]	BK6_VOLT[2]	BK6_VOLT[1]	BK6_VOLT[0]
Default	1	1	0	1	1	0	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
b7	BK7_VOLT[3]	0000:1.00V, 0001:1.05V, 0010:1.10V, 0011:1.15V, 0100:1.20V, 0101:1.25V, 0110:1.30V, 0111:1.35V, 1000:1.40V, 1001:1.45V, 1010:1.50V, 1011:1.70V, 1100:1.75V, 1101:1.80V, 1110:1.85V, 1111:1.90V,
b6	BK7_VOLT[2]	
b5	BK7_VOLT[1]	
b4	BK7_VOLT[0]	
b3	BK6_VOLT[3]	V_{OUT}= BK6_VOLT[3:0] x 50mV + 2.65V, V_{OUT} Range: 2.65V~3.4V
b2	BK6_VOLT[2]	
b1	BK6_VOLT[1]	
b0	BK6_VOLT[0]	

Address: 0x26/0x2F
Description: Buck8 and Buck11 output voltage in normal/sleep mode

Bits	b7	b6	b5	b4	b3	b2	b1	b0
Meaning	---	BK11_VOLT[2]	BK11_VOLT[1]	BK11_VOLT[0]	BK8_VOLT[3]	BK8_VOLT[2]	BK8_VOLT[1]	BK8_VOLT[0]
Default	---	1	0	0	1	1	0	1
Read/Write	---	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
b7	---	
b6	BK11_VOLT[2]	000:2.1V, 001:2.2V, 010:2.3V, 011:2.4V, 100:2.5V, 101:2.6V, 110:2.7V, 111:2.8V,
b5	BK11_VOLT[1]	
b4	BK11_VOLT[0]	
b3	BK8_VOLT[3]	0000:1.00V, 0001:1.05V, 0010:1.10V, 0011:1.15V, 0100:1.20V, 0101:1.25V, 0110:1.30V, 0111:1.35V, 1000:1.40V, 1001:1.45V, 1010:1.50V, 1011:1.70V, 1100:1.75V, 1101:1.80V, 1110:1.85V, 1111:1.90V,
b2	BK8_VOLT[2]	
b1	BK8_VOLT[1]	
b0	BK8_VOLT[0]	

Address: 0x27/0x30
Description: Buck9 output voltage in normal/sleep mode

Bits	b7	b6	b5	b4	b3	b2	b1	b0
Meaning	---	---	---	BK9_VOLT[4]	BK9_VOLT[3]	BK9_VOLT[2]	BK9_VOLT[1]	BK9_VOLT[0]
Default	---	---	---	1	0	0	0	0
Read/Write	---	---	---	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
b7	---	
b6	---	
b5	---	
b4	BK9_VOLT[4]	V_{OUT}= BK9_VOLT[4:0] x 25mV + 0.75V, V_{OUT} Range: 0.75V~1.525V
b3	BK9_VOLT[3]	
b2	BK9_VOLT[2]	
b1	BK9_VOLT[1]	
b0	BK9_VOLT[0]	

Address: 0x28/0x31
Description: Buck10 output voltage in normal/sleep mode

Bits	b7	b6	b5	b4	b3	b2	b1	b0
Meaning	---	---	---	BK10_VOLT[4]	BK10_VOLT[3]	BK10_VOLT[2]	BK10_VOLT[1]	BK10_VOLT[0]
Default	---	---	---	0	0	0	1	0
Read/Write	---	---	---	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
b7	---	
b6	---	
b5	---	
b4	BK10_VOLT[4]	V_{OUT}= BK10_VOLT[4:0] x25mV + 0.55V, V_{OUT} Range: 0.55V~1.325V
b3	BK10_VOLT[3]	
b2	BK10_VOLT[2]	
b1	BK10_VOLT[1]	
b0	BK10_VOLT[0]	

Address: 0x32
Description: Buck1and Buck2 operation mode in normal/sleep mode

Bits	b7	b6	b5	b4	b3	b2	b1	b0
Meaning	BK2_NRMMODE[1]	BK2_NRMMODE[0]	BK2_SLPMODE[1]	BK2_SLPMODE[0]	BK1_NRMMODE[1]	BK1_NRMMODE[0]	BK1_SLPMODE[1]	BK1_SLPMODE[0]
Default	0	0	1	0	0	0	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
b7	BK2_NRMMODE[1]	00/01: auto PWM/PSM with ECO, 10: forced PWM, 11: auto PWM/PSM w/o ECO
b6	BK2_NRMMODE[0]	
b5	BK2_SLPMODE[1]	00: auto PWM/PSM w/o ECO, VOUT is configured by BK2_VOLT[4:0], 01:auto PWM/PSM with ECO, VOUT is configured by BK2_VOLT[4:0]
b4	BK2_SLPMODE[0]	10: auto PWM/PSM with ECO, VOUT is configured by BK2_SLPVOLT[4:0], 11:OFF
b3	BK1_NRMMODE[1]	00/01: auto PWM/PSM with ECO, 10: forced PWM, 11: auto PWM/PSM w/o ECO
b2	BK1_NRMMODE[0]	
b1	BK1_SLPMODE[1]	00: auto PWM/PSM w/o ECO, VOUT is configured by BK1_VOLT[4:0], 01:auto PWM/PSM with ECO, VOUT is configured by BK1_VOLT[4:0]
b0	BK1_SLPMODE[0]	10: auto PWM/PSM with ECO, VOUT is configured by BK1_SLPVOLT[4:0], 11:OFF

Address: 0x33
Description: Buck3 and Buck4 operation mode in normal/sleep mode

Bits	b7	b6	b5	b4	b3	b2	b1	b0
Meaning	BK4_NRMMODE[1]	BK4_NRMMODE[0]	BK4_SLPMODE[1]	BK4_SLPMODE[0]	BK3_NRMMODE[1]	BK3_NRMMODE[0]	BK3_SLPMODE[1]	BK3_SLPMODE[0]
Default	0	0	1	0	0	0	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
b7	BK4_NRMMODE[1]	00/01: auto PWM/PSM with ECO, 10: forced PWM, 11: auto PWM/PSM w/o ECO
b6	BK4_NRMMODE[0]	
b5	BK4_SLPMODE[1]	00: auto PWM/PSM w/o ECO, VOUT is configured by BK4_VOLT[4:0], 01:auto PWM/PSM with ECO, VOUT is configured by BK4_VOLT[4:0]
b4	BK4_SLPMODE[0]	10: auto PWM/PSM with ECO, VOUT is configured by BK4_SLPVOLT[4:0], 11:OFF
b3	BK3_NRMMODE[1]	00/01: auto PWM/PSM with ECO, 10: forced PWM, 11: auto PWM/PSM w/o ECO
b2	BK3_NRMMODE[0]	
b1	BK3_SLPMODE[1]	00: auto PWM/PSM w/o ECO, VOUT is configured by BK3_VOLT[4:0], 01:auto PWM/PSM with ECO, VOUT is configured by BK3_VOLT[4:0]
b0	BK3_SLPMODE[0]	10: auto PWM/PSM with ECO, VOUT is configured by BK3_SLPVOLT[4:0], 11:OFF

Address: 0x34
Description: Buck5 and Buck6 operation mode in normal/sleep mode

Bits	b7	b6	b5	b4	b3	b2	b1	b0
Meaning	BK6_NRMMODE[1]	BK6_NRMMODE[0]	BK6_SLPMODE[1]	BK6_SLPMODE[0]	BK5_NRMMODE[1]	BK5_NRMMODE[0]	BK5_SLPMODE[1]	BK5_SLPMODE[0]
Default	0	0	1	0	0	0	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
b7	BK6_NRMMODE[1]	00/01: auto PWM/PSM with ECO, 10: forced PWM, 11: auto PWM/PSM w/o ECO
b6	BK6_NRMMODE[0]	
b5	BK6_SLPMODE[1]	00: auto PWM/PSM w/o ECO, VOUT is configured by BK6_VOLT[3:0], 01:auto PWM/PSM with ECO, VOUT is configured by BK6_VOLT[3:0]
b4	BK6_SLPMODE[0]	10: auto PWM/PSM with ECO, VOUT is configured by BK6_SLPVOLT[3:0], 11:OFF
b3	BK5_NRMMODE[1]	00/01: auto PWM/PSM with ECO, 10: forced PWM, 11: auto PWM/PSM w/o ECO
b2	BK5_NRMMODE[0]	
b1	BK5_SLPMODE[1]	00: auto PWM/PSM w/o ECO, VOUT is configured by BK5_VOLT[4:0], 01:auto PWM/PSM with ECO, VOUT is configured by BK5_VOLT[4:0]
b0	BK5_SLPMODE[0]	10: auto PWM/PSM with ECO, VOUT is configured by BK5_SLPVOLT[4:0], 11:OFF

Address: 0x35
Description: Buck7 and Buck8 operation mode in normal/sleep mode

Bits	b7	b6	b5	b4	b3	b2	b1	b0
Meaning	BK8_NRMMODE[1]	BK8_NRMMODE[0]	BK8_SLPMODE[1]	BK8_SLPMODE[0]	BK7_NRMMODE[1]	BK7_NRMMODE[0]	BK7_SLPMODE[1]	BK7_SLPMODE[0]
Default	0	0	1	0	0	0	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
b7	BK8_NRMMODE[1]	00/01: auto PWM/PSM with ECO, 10: forced PWM, 11: auto PWM/PSM w/o ECO
b6	BK8_NRMMODE[0]	
b5	BK8_SLPMODE[1]	00: auto PWM/PSM w/o ECO, VOUT is configured by BK8_VOLT[3:0], 01:auto PWM/PSM with ECO, VOUT is configured by BK8_VOLT[3:0]
b4	BK8_SLPMODE[0]	10: auto PWM/PSM with ECO, VOUT is configured by BK8_SLPVOLT[3:0], 11:OFF
b3	BK7_NRMMODE[1]	00/01: auto PWM/PSM with ECO, 10: forced PWM, 11: auto PWM/PSM w/o ECO
b2	BK7_NRMMODE[0]	
b1	BK7_SLPMODE[1]	00: auto PWM/PSM w/o ECO, VOUT is configured by BK7_VOLT[3:0], 01:auto PWM/PSM with ECO, VOUT is configured by BK7_VOLT[3:0]
b0	BK7_SLPMODE[0]	10: auto PWM/PSM with ECO, VOUT is configured by BK7_SLPVOLT[3:0], 11:OFF

Address: 0x36
Description: Buck9 and Buck10 operation mode in normal/sleep mode

Bits	b7	b6	b5	b4	b3	b2	b1	b0
Meaning	BK10_NRMMODE[1]	BK10_NRMMODE[0]	BK10_SLPMODE[1]	BK10_SLPMODE[0]	BK9_NRMMODE[1]	BK9_NRMMODE[0]	BK9_SLPMODE[1]	BK9_SLPMODE[0]
Default	0	0	1	0	0	0	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
b7	BK10_NRMMODE[1]	00/01: auto PWM/PSM with ECO, 10: forced PWM, 11: auto PWM/PSM w/o ECO
b6	BK10_NRMMODE[0]	
b5	BK10_SLPMODE[1]	00: auto PWM/PSM w/o ECO, VOUT is configured by BK10_VOLT[4:0], 01:auto PWM/PSM with ECO, VOUT is configured by BK10_VOLT[4:0]
b4	BK10_SLPMODE[0]	10: auto PWM/PSM with ECO, VOUT is configured by BK10_SLPVOLT[4:0], 11:OFF
b3	BK9_NRMMODE[1]	00/01: auto PWM/PSM with ECO, 10: forced PWM, 11: auto PWM/PSM w/o ECO
b2	BK9_NRMMODE[0]	
b1	BK9_SLPMODE[1]	00: auto PWM/PSM w/o ECO, VOUT is configured by BK9_VOLT[4:0], 01:auto PWM/PSM with ECO, VOUT is configured by BK9_VOLT[4:0]
b0	BK9_SLPMODE[0]	10: auto PWM/PSM with ECO, VOUT is configured by BK9_SLPVOLT[4:0], 11:OFF

Address: 0x37
Description: Buck11 operation mode in normal/sleep mode

Bits	b7	b6	b5	b4	b3	b2	b1	b0
Meaning	---	---	---	---	BK11_NRMMODE[1]	BK11_NRMMODE[0]	BK11_SLPMODE[1]	BK11_SLPMODE[0]
Default	---	---	---	---	0	0	1	0
Read/Write	---	---	---	---	R/W	R/W	R/W	R/W

Bits	Name	Description
b7	---	
b6	---	
b5	---	
b4	---	
b3	BK11_NRMMODE[1]	00/01: auto PWM/PSM with ECO, 10: forced PWM, 11: auto PWM/PSM w/o ECO
b2	BK11_NRMMODE[0]	
b1	BK11_SLPMODE[1]	00: auto PWM/PSM w/o ECO, VOUT is configured by BK11_VOLT[2:0], 01:auto PWM/PSM with ECO, VOUT is configured by BK11_VOLT[2:0]
b0	BK11_SLPMODE[0]	10: auto PWM/PSM with ECO, VOUT is configured by BK11_SLPVOLT[2:0], 11:OFF

Address: 0x40/0x49
Description: LDO1 and LDO2 output voltage in normal/sleep mode

Bits	b7	b6	b5	b4	b3	b2	b1	b0
Meaning	---	LDO2_VOLT[2]	LDO2_VOLT[1]	LDO2_VOLT[0]	---	LDO1_VOLT[2]	LDO1_VOLT[1]	LDO1_VOLT[0]
Default	---	0	1	1	---	0	1	1
Read/Write	---	R/W	R/W	R/W	---	R/W	R/W	R/W

Bits	Name	Description
b7	---	
b6	LDO2_VOLT[2]	Voltage Group-LA
b5	LDO2_VOLT[1]	000:1.0v, 001:1.2V, 010:1.5V, 011:1.8V, 100:2.5V, 101:2.8V, 110:3.0V, 111:3.3V,
b4	LDO2_VOLT[0]	
b3	---	
b2	LDO1_VOLT[2]	Voltage Group-LA
b1	LDO1_VOLT[1]	000:1.0V, 001:1.2V, 010:1.5V, 011:1.8V, 100:2.5V, 101:2.8V, 110:3.0V, 111:3.3V,
b0	LDO1_VOLT[0]	

Address: 0x41/0x4A
Description: LDO3 and LDO4 output voltage in normal/sleep mode

Bits	b7	b6	b5	b4	b3	b2	b1	b0
Meaning	---	LDO4_VOLT[2]	LDO4_VOLT[1]	LDO4_VOLT[0]	---	LDO3_VOLT[2]	LDO3_VOLT[1]	LDO3_VOLT[0]
Default	---	0	1	1	---	0	1	1
Read/Write	---	R/W	R/W	R/W	---	R/W	R/W	R/W

Bits	Name	Description
b7	---	
b6	LDO4_VOLT[2]	Voltage Group-LA
b5	LDO4_VOLT[1]	000:1.0V, 001:1.2V, 010:1.5V, 011:1.8V, 100:2.5V, 101:2.8VV, 110:3.0V, 111:3.3V,
b4	LDO4_VOLT[0]	
b3	---	
b2	LDO3_VOLT[2]	Voltage Group-LA
b1	LDO3_VOLT[1]	000:1.0V, 001:1.2V, 010:1.5V, 011:1.8V, 100:2.5V, 101:2.8V, 110:3.0V, 111:3.3V,
b0	LDO3_VOLT[0]	

Address: 0x42/0x4B
Description: LDO5 and LDO6 output voltage in normal/sleep mode

Bits	b7	b6	b5	b4	b3	b2	b1	b0
Meaning	---	LDO6_VOLT[2]	LDO6_VOLT[1]	LDO6_VOLT[0]	---	LDO5_VOLT[2]	LDO5_VOLT[1]	LDO5_VOLT[0]
Default	---	0	1	0	---	0	1	1
Read/Write	---	R/W	R/W	R/W	---	R/W	R/W	R/W

Bits	Name	Description
b7	---	
b6	LDO6_VOLT[2]	Voltage Group-LA
b5	LDO6_VOLT[1]	000:1.0V, 001:1.2V, 010:1.5V, 011:1.8V, 100:2.5V, 101:2.8V, 110:3.0V, 111:3.3V,
b4	LDO6_VOLT[0]	
b3	---	
b2	LDO5_VOLT[2]	Voltage Group-LA
b1	LDO5_VOLT[1]	000:1.0V, 001:1.2V, 010:1.5V, 011:1.8V, 100:2.5V, 101:2.8V, 110:3.0V, 111:3.3V,
b0	LDO5_VOLT[0]	

Address: 0x43/0x4C
Description: LDO7 and LDO8 output voltage in normal/sleep mode

Bits	b7	b6	b5	b4	b3	b2	b1	b0
Meaning	---	LDO8_VOLT[2]	LDO8_VOLT[1]	LDO8_VOLT[0]	---	LDO7_VOLT[2]	LDO7_VOLT[1]	LDO7_VOLT[0]
Default	---	0	1	1	---	0	0	1
Read/Write	---	R/W	R/W	R/W	---	R/W	R/W	R/W

Bits	Name	Description
b7	---	
b6	LDO8_VOLT[2]	Voltage Group-LD
b5	LDO8_VOLT[1]	000:0.65V, 001:0.7V, 010:0.75V, 011:0.85V, 100:0.9V, 101:0.95V, 110:1.0V, 111:1.05V,
b4	LDO8_VOLT[0]	
b3	---	
b2	LDO7_VOLT[2]	Voltage Group-LB
b1	LDO7_VOLT[1]	000:1.0V, 001:1.1V, 010:1.15V, 011:1.2V, 100:1.25V, 101:1.3V, 110:1.35V, 111:1.4V,
b0	LDO7_VOLT[0]	

Address: 0x44/0x4D
Description: LDO9 and LDO10 output voltage in normal/sleep mode

Bits	b7	b6	b5	b4	b3	b2	b1	b0
Meaning	---	LDO10_VOLT[2]	LDO10_VOLT[1]	LDO10_VOLT[0]	---	LDO9_VOLT[2]	LDO9_VOLT[1]	LDO9_VOLT[0]
Default	---	0	0	1	---	0	0	1
Read/Write	---	R/W	R/W	R/W	---	R/W	R/W	R/W

Bits	Name	Description
b7	---	
b6	LDO10_VOLT[2]	Voltage Group-LC 000:0.9V, 001:1.0V, 010:1.05V, 011:1.1V, 100:1.15V, 101:1.2V, 110:1.25V, 111:1.3V,
b5	LDO10_VOLT[1]	
b4	LDO10_VOLT[0]	
b3	---	
b2	LDO9_VOLT[2]	Voltage Group-LB 000:1.0V, 001:1.1V, 010:1.15V, 011:1.2V, 100:1.25V, 101:1.3V, 110:1.35V, 111:1.4V,
b1	LDO9_VOLT[1]	
b0	LDO9_VOLT[0]	

Address: 0x45/0x4E
Description: LDO11 and LDO12 output voltage in normal/sleep mode

Bits	b7	b6	b5	b4	b3	b2	b1	b0
Meaning	---	LDO12_VOLT[2]	LDO12_VOLT[1]	LDO12_VOLT[0]	---	LDO11_VOLT[2]	LDO11_VOLT[1]	LDO11_VOLT[0]
Default	---	0	1	1	---	0	1	1
Read/Write	---	R/W	R/W	R/W	---	R/W	R/W	R/W

Bits	Name	Description
b7	---	
b6	LDO12_VOLT[2]	Voltage Group-LB 000:1.0V, 001:1.1V, 010:1.15V, 011:1.2V, 100:1.25V, 101:1.3V, 110:1.35V, 111:1.4V,
b5	LDO12_VOLT[1]	
b4	LDO12_VOLT[0]	
b3	---	
b2	LDO11_VOLT[2]	Voltage Group-LB 000:1.0V, 001:1.1V, 010:1.15V, 011:1.2V, 100:1.25V, 101:1.3V, 110:1.35V, 111:1.4V,
b1	LDO11_VOLT[1]	
b0	LDO11_VOLT[0]	

Address: 0x46/0x4F
Description: LDO13 and LDO14 output voltage in normal/sleep mode

Bits	b7	b6	b5	b4	b3	b2	b1	b0
Meaning	---	LDO14_VOLT[2]	LDO14_VOLT[1]	LDO14_VOLT[0]	---	LDO13_VOLT[2]	LDO13_VOLT[1]	LDO13_VOLT[0]
Default	---	0	1	1	---	0	1	0
Read/Write	---	R/W	R/W	R/W	---	R/W	R/W	R/W

Bits	Name	Description
b7	---	
b6	LDO14_VOLT[2]	Voltage Group-LA 000:1.0V, 001:1.2V, 010:1.5V, 011:1.8V, 100:2.5V, 101:2.8V, 110:3.0V, 111:3.3V,
b5	LDO14_VOLT[1]	
b4	LDO14_VOLT[0]	
b3	---	
b2	LDO13_VOLT[2]	Voltage Group-LC 000:0.9V, 001:1.0V, 010:1.05V, 011:1.1V, 100:1.15V, 101:1.2V, 110:1.25V, 111:1.3V,
b1	LDO13_VOLT[1]	
b0	LDO13_VOLT[0]	

Address: 0x47/0x50
Description: LDO15 and LDO16 output voltage in normal/sleep mode

Bits	b7	b6	b5	b4	b3	b2	b1	b0
Meaning	---	LDO16_VOLT[2]	LDO16_VOLT[1]	LDO16_VOLT[0]	---	LDO15_VOLT[2]	LDO15_VOLT[1]	LDO15_VOLT[0]
Default	---	0	1	0	---	0	1	1
Read/Write	---	R/W	R/W	R/W	---	R/W	R/W	R/W

Bits	Name	Description
b7	---	
b6	LDO16_VOLT[2]	Voltage Group-LD 000:0.65V, 001:0.7V, 010:0.75V, 011:0.85V, 100:0.9V, 101:0.95V, 110:1.0V, 111:1.05V,
b5	LDO16_VOLT[1]	
b4	LDO16_VOLT[0]	
b3	---	
b2	LDO15_VOLT[2]	Voltage Group-LA 000:1.0V, 001:1.2V, 010:1.5V, 011:1.8V, 100:2.5V, 101:2.8V, 110:3.0V, 111:3.3V,
b1	LDO15_VOLT[1]	
b0	LDO15_VOLT[0]	

Address: 0x48/0x51
Description: LDO17 and LDO18 output voltage in normal/sleep mode

Bits	b7	b6	b5	b4	b3	b2	b1	b0
Meaning	---	LDO18_VOLT[2]	LDO18_VOLT[1]	LDO18_VOLT[0]	---	LDO17_VOLT[2]	LDO17_VOLT[1]	LDO17_VOLT[0]
Default	---	0	1	0	---	0	1	0
Read/Write	---	R/W	R/W	R/W	---	R/W	R/W	R/W

Bits	Name	Description
b7	---	
b6	LDO18_VOLT[2]	Voltage Group-LD 000:0.65V, 001:0.7V, 010:0.75V, 011:0.85V, 100:0.9V, 101:0.95V, 110:1.0V, 111:1.05V,
b5	LDO18_VOLT[1]	
b4	LDO18_VOLT[0]	
b3	---	
b2	LDO17_VOLT[2]	Voltage Group-LD 000:0.65V, 001:0.7V, 010:0.75V, 011:0.85V, 100:0.9V, 101:0.95V, 110:1.0V, 111:1.05V,
b1	LDO17_VOLT[1]	
b0	LDO17_VOLT[0]	

Address: 0x52
Description: LDO1,LDO2,LDO3,and LDO4 operation mode in sleep mode

Bits	b7	b6	b5	b4	b3	b2	b1	b0
Meaning	LDO4_SLPMODE[1]	LDO4_SLPMODE[0]	LDO3_SLPMODE[1]	LDO3_SLPMODE[0]	LDO2_SLPMODE[1]	LDO2_SLPMODE[0]	LDO1_SLPMODE[1]	LDO1_SLPMODE[0]
Default	1	1	1	1	1	1	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
b7	LDO4_SLPMODE[1]	00: w/o ECO, VOUT is configured by LDOx_VOLT[n:0], 01:with ECO, VOUT is configured by LDOx_VOLT[n:0] 10: with ECO, VOUT is configured by LDOx_SLPVOLT[n:0], 11:OFF
b6	LDO4_SLPMODE[0]	
b5	LDO3_SLPMODE[1]	
b4	LDO3_SLPMODE[0]	
b3	LDO2_SLPMODE[1]	
b2	LDO2_SLPMODE[0]	
b1	LDO1_SLPMODE[1]	
b0	LDO1_SLPMODE[0]	

Address: 0x53
Description: LDO5,LDO6,LDO7,and LDO8 operation mode in sleep mode

Bits	b7	b6	b5	b4	b3	b2	b1	b0
Meaning	LDO8_SLPMODE[1]	LDO8_SLPMODE[0]	LDO7_SLPMODE[1]	LDO7_SLPMODE[0]	LDO6_SLPMODE[1]	LDO6_SLPMODE[0]	LDO5_SLPMODE[1]	LDO5_SLPMODE[0]
Default	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
b7	LDO8_SLPMODE[1]	00: w/o ECO, VOUT is configured by LDOx_VOLT[n:0], 01:with ECO, VOUT is configured by LDOx_VOLT[n:0] 10: with ECO, VOUT is configured by LDOx_SLPVOLT[n:0], 11:OFF
b6	LDO8_SLPMODE[0]	
b5	LDO7_SLPMODE[1]	
b4	LDO7_SLPMODE[0]	
b3	LDO6_SLPMODE[1]	
b2	LDO6_SLPMODE[0]	
b1	LDO5_SLPMODE[1]	
b0	LDO5_SLPMODE[0]	

Address: 0x54
Description: LDO9,LDO10,LDO11,and LDO12 operation mode in sleep mode

Bits	b7	b6	b5	b4	b3	b2	b1	b0
Meaning	LDO12_SLPMODE[1]	LDO12_SLPMODE[0]	LDO11_SLPMODE[1]	LDO11_SLPMODE[0]	LDO10_SLPMODE[1]	LDO10_SLPMODE[0]	LDO9_SLPMODE[1]	LDO9_SLPMODE[0]
Default	1	1	1	0	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
b7	LDO12_SLPMODE[1]	00: w/o ECO, VOUT is configured by LDOx_VOLT[n:0], 01:with ECO, VOUT is configured by LDOx_VOLT[n:0] 10: with ECO, VOUT is configured by LDOx_SLPVOLT[n:0], 11:OFF
b6	LDO12_SLPMODE[0]	
b5	LDO11_SLPMODE[1]	
b4	LDO11_SLPMODE[0]	
b3	LDO10_SLPMODE[1]	
b2	LDO10_SLPMODE[0]	
b1	LDO9_SLPMODE[1]	
b0	LDO9_SLPMODE[0]	

Address: 0x55
Description: LDO13,LDO14,LDO15,and LDO16 operation mode in sleep mode

Bits	b7	b6	b5	b4	b3	b2	b1	b0
Meaning	LDO16_SLPMODE[1]	LDO16_SLPMODE[0]	LDO15_SLPMODE[1]	LDO15_SLPMODE[0]	LDO14_SLPMODE[1]	LDO14_SLPMODE[0]	LDO13_SLPMODE[1]	LDO13_SLPMODE[0]
Default	1	0	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
b7	LDO16_SLPMODE[1]	00: w/o ECO, VOUT is configured by LDOx_VOLT[n:0], 01:with ECO, VOUT is configured by LDOx_VOLT[n:0] 10: with ECO, VOUT is configured by LDOx_SLPVOLT[n:0], 11:OFF
b6	LDO16_SLPMODE[0]	
b5	LDO15_SLPMODE[1]	
b4	LDO15_SLPMODE[0]	
b3	LDO14_SLPMODE[1]	
b2	LDO14_SLPMODE[0]	
b1	LDO13_SLPMODE[1]	
b0	LDO13_SLPMODE[0]	

Address: 0x56
Description: LDO17and LDO18 operation mode in sleep mode

Bits	b7	b6	b5	b4	b3	b2	b1	b0
Meaning	---	---	---	---	LDO18_SLPMODE[1]	LDO18_SLPMODE[0]	LDO17_SLPMODE[1]	LDO17_SLPMODE[0]
Default	---	---	---	---	1	1	1	1
Read/Write	---	---	---	---	R/W	R/W	R/W	R/W

Bits	Name	Description
b7	---	
b6	---	
b5	---	
b4	---	
b3	LDO18_SLPMODE[1]	00: w/o ECO, VOUT is configured by LDOx_VOLT[n:0], 01:with ECO, VOUT is configured by LDOx_VOLT[n:0] 10: with ECO, VOUT is configured by LDOx_SLPVOLT[n:0], 11:OFF
b2	LDO18_SLPMODE[0]	
b1	LDO17_SLPMODE[1]	
b0	LDO17_SLPMODE[0]	

Address: 0x60
Description: Buck1~Buck8 on/off control

Bits	b7	b6	b5	b4	b3	b2	b1	b0
Meaning	ONBUCK8	ONBUCK7	ONBUCK6	ONBUCK5	ONBUCK4	ONBUCK3	ONBUCK2	ONBUCK1
Default	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
b7	ONBUCK8	0:OFF, 1:ON
b6	ONBUCK7	
b5	ONBUCK6	
b4	ONBUCK5	
b3	ONBUCK4	
b2	ONBUCK3	
b1	ONBUCK2	
b0	ONBUCK1	

Address: 0x61
Description: Buck9~Buck11 on/off control

Bits	b7	b6	b5	b4	b3	b2	b1	b0
Meaning	---	---	---	---	---	ONBUCK11	ONBUCK10	ONBUCK9
Default	---	---	---	---	---	1	1	1
Read/Write	---	---	---	---	---	R/W	R/W	R/W

Bits	Name	Description
b7	---	
b6	---	
b5	---	
b4	---	
b3	---	
b2	ONBUCK11	0:OFF, 1:ON
b1	ONBUCK10	
b0	ONBUCK9	

Address: 0x62
Description: LDO1~LDO8 on/off control

Bits	b7	b6	b5	b4	b3	b2	b1	b0
Meaning	ONLDO8	ONLDO7	ONLDO6	ONLDO5	ONLDO4	ONLDO3	ONLDO2	ONLDO1
Default	1	1	0	1	1	1	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
b7	ONLDO8	0:OFF, 1:ON
b6	ONLDO7	
b5	ONLDO6	
b4	ONLDO5	
b3	ONLDO4	
b2	ONLDO3	
b1	ONLDO2	
b0	ONLDO1	

Address: 0x63
Description: LDO9~LDO16 on/off control

Bits	b7	b6	b5	b4	b3	b2	b1	b0
Meaning	ONLDO16	ONLDO15	ONLDO14	ONLDO13	ONLDO12	ONLDO11	ONLDO10	ONLDO9
Default	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
b7	ONLDO16	0:OFF, 1:ON
b6	ONLDO15	
b5	ONLDO14	
b4	ONLDO13	
b3	ONLDO12	
b2	ONLDO11	
b1	ONLDO10	
b0	ONLDO9	

Address: 0x64
Description: LDO17 and LDO18 on/off control

Bits	b7	b6	b5	b4	b3	b2	b1	b0
Meaning	---	---	---	---	---	---	ONLDO18	ONLDO17
Default	---	---	---	---	---	---	1	1
Read/Write	---	---	---	---	---	---	R/W	R/W

Bits	Name	Description
b7	---	
b6	---	
b5	---	
b4	---	
b3	---	
b2	---	
b1	ONLDO18	0:OFF, 1:ON
b0	ONLDO17	

Address: 0x65
Description: Buck1~Buck8 enable discharge control

Bits	b7	b6	b5	b4	b3	b2	b1	b0
Meaning	ENDISCHG_BK8	ENDISCHG_BK7	ENDISCHG_BK6	ENDISCHG_BK5	ENDISCHG_BK4	ENDISCHG_BK3	ENDISCHG_BK2	ENDISCHG_BK1
Default	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
b7	ENDISCHG_BK8	0: disable discharge function in shutdown mode. V_{OUT} is high impedance, 1: enable discharge function in shutdown mode
b6	ENDISCHG_BK7	
b5	ENDISCHG_BK6	
b4	ENDISCHG_BK5	
b3	ENDISCHG_BK4	
b2	ENDISCHG_BK3	
b1	ENDISCHG_BK2	
b0	ENDISCHG_BK1	

Address: 0x66
Description: Buck9~Buck11 enable discharge control

Bits	b7	b6	b5	b4	b3	b2	b1	b0
Meaning	---	---	---	---	---	ENDISCHG_BK11	ENDISCHG_BK10	ENDISCHG_BK9
Default	---	---	---	---	---	1	1	1
Read/Write	---	---	---	---	---	R/W	R/W	R/W

Bits	Name	Description
b7	---	
b6	---	
b5	---	
b4	---	
b3	---	
b2	ENDISCHG_BK11	0: disable discharge function in shutdown mode. V_{OUT} is high impedance, 1: enable discharge function in shutdown mode
b1	ENDISCHG_BK10	
b0	ENDISCHG_BK9	

Address: 0x67
Description: LDO1~LDO8 enable discharge control

Bits	b7	b6	b5	b4	b3	b2	b1	b0
Meaning	ENDISCHG_LDO8	ENDISCHG_LDO8	ENDISCHG_LDO6	ENDISCHG_LDO5	ENDISCHG_LDO4	ENDISCHG_LDO3	ENDISCHG_LDO2	ENDISCHG_LDO1
Default	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
b7	ENDISCHG_LDO8	0: disable discharge function in shutdown mode. V_{OUT} is high impedance, 1: enable discharge function in shutdown mode
b6	ENDISCHG_LDO7	
b5	ENDISCHG_LDO6	
b4	ENDISCHG_LDO5	
b3	ENDISCHG_LDO4	
b2	ENDISCHG_LDO3	
b1	ENDISCHG_LDO2	
b0	ENDISCHG_LDO1	

Address: 0x4F
Description: LDO9~LDO16 enable discharge control

Bits	b7	b6	b5	b4	b3	b2	b1	b0
Meaning	ENDISCHG_LDO16	ENDISCHG_LDO15	ENDISCHG_LDO14	ENDISCHG_LDO13	ENDISCHG_LDO12	ENDISCHG_LDO11	ENDISCHG_LDO10	ENDISCHG_LDO9
Default	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
b7	ENDISCHG_LDO16	0: disable discharge function in shutdown mode. V_{OUT} is high impedance, 1: enable discharge function in shutdown mode
b6	ENDISCHG_LDO15	
b5	ENDISCHG_LDO14	
b4	ENDISCHG_LDO13	
b3	ENDISCHG_LDO12	
b2	ENDISCHG_LDO11	
b1	ENDISCHG_LDO10	
b0	ENDISCHG_LDO9	

Address: 0x50
Description: LDO17 and LDO18 enable discharge control

Bits	b7	b6	b5	b4	b3	b2	b1	b0
Meaning	---	---	---	---	---	---	ENDISCHG_LDO18	ENDISCHG_LDO17
Default	---	---	---	---	---	---	1	1
Read/Write	---	---	---	---	---	---	R/W	R/W

Bits	Name	Description
b7	---	
b6	---	
b5	---	
b4	---	
b3	---	
b2	---	
b1	ENDISCHG_LDO18	0: disable discharge function in shutdown mode. V_{OUT} is high impedance, 1: enable discharge function in shutdown mode
b0	ENDISCHG_LDO17	

Address: 0x70
Description: System Control Register

Bits	b7	b6	b5	b4	b3	b2	b1	b0
Meaning	SOFTON	SLEEP	---	---	VORTC[1]	VORTC[0]	---	RST_FAULT
Default	0	0	---	---	0	0	---	0
Read/Write	R/W	R/W	---	---	R/W	R/W	---	R/W

Bits	Name	Description
b7	SOFTON	1: keep PMIC in normal operation mode after start-up.
b6	SLEEP	SLEEP, combined with the status of PWRHOLD pin and the SOFTON register, is used to control the operation status of PMIC SLEEP / PWRHOLD='Low' and SOFTON=0 / PMIC Status 0 / true / Shutdown mode 1 / true / Sleep mode X / false / Normal mode
b5	---	
b4	---	
b3	VORTC[1]	Set the RTC LDO output voltage 00:1.8V, 01:2.5V, 10:2.8V, 11:3.0V
b2	VORTC[0]	
b1	---	
b0	RST_FAULT	1: Reset status registers of PMIC fault conditions.

Address: 0x71
Description: PWRKEY Control Register

Bits	b7	b6	b5	b4	b3	b2	b1	b0
Meaning	---	EN_LLP	TIME_LLP[1]	TIME_LLP[0]	TIME_LP[1]	TIME_LP[0]	TIME_IT[1]	TIME_IT[0]
Default	---	1	1	1	0	0	0	1
Read/Write	---	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
b7	---	
b6	EN_LLP	0:disable PWRON long long-pressed, 1:enable /PWRON long long-pressed to shutdown PMIC
b5	TIME_LLP[1]	Configure PWRON long long-pressed delay time $T_{dPWRONLLP}$ 00:6Sec, 01:7Sec, 10:8Sec, 11:10Sec
b4	TIME_LLP[0]	
b3	TIME_LP[1]	Configure PWRON long-pressed delay time $T_{dPWRONLP}$ 00:1.0Sec, 01:1.5Sec, 10:2.0Sec, 11:2.5Sec
b2	TIME_LP[0]	
b1	TIME_IT[1]	Configure PWRON de-bouncing delay time $T_{dbPWRONF}$ 00:128mS, 01:3.0Sec, 10:3.5Sec, 11:4.0Sec
b0	TIME_IT[0]	

Address: 0x72
Description: VCC under-voltage Threshold Control

Bits	b7	b6	b5	b4	b3	b2	b1	b0
Meaning	---	EN_SMPL	SMPL_SEL[1]	SMPL_SEL[0]	---	VCCUV[2]	VCCUV[1]	VCCUV[0]
Default	---	0	1	1	---	0	1	0
Read/Write	---	R/W	R/W	R/W	---	R/W	R/W	R/W

Bits	Name	Description
b7	---	
b6	EN_SMPL	0:disable SMPL re-startup function, 1:enable SMPL re-startup function
b5	SMPL_SEL[1]	SMPL timeout duration 00:0.5Sec, 01:1.0Sec, 10:1.5Sec, 11:2Sec
b4	SMPL_SEL[0]	
b3	---	
b2	VCCUV[2]	UV=VCCUV[2:0] x 50mV + 2.4V, UV Range: 2.4V~2.75V
b1	VCCUV[1]	
b0	VCCUV[0]	

Address: 0x73
Description: TDLY_X32K Control Register

Bits	b7	b6	b5	b4	b3	b2	b1	b0
Meaning	TIMER_X32K[7]	TIMER_X32K[6]	TIMER_X32K[5]	TIMER_X32K[4]	TIMER_X32K[3]	TIMER_X32K[2]	TIMER_X32K[1]	TIMER_X32K[0]
Default	0	0	0	0	1	1	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
b7	TIMER_X32K[7]	Setting OSC_32K clock buffer delay Timer. T_{DLY_X32K}=TIMER_X32K[7:0]*8.2mS.
b6	TIMER_X32K[6]	
b5	TIMER_X32K[5]	
b4	TIMER_X32K[4]	
b3	TIMER_X32K[3]	
b2	TIMER_X32K[2]	
b1	TIMER_X32K[1]	
b0	TIMER_X32K[0]	

Address: 0xE0
Description: Chip Information

Bits	b7	b6	b5	b4	b3	b2	b1	b0
Meaning	CHIP_ID[3]	CHIP_ID[2]	CHIP_ID[1]	CHIP_ID[0]	VERSION[3]	VERSION[2]	VERSION[1]	VERSION[0]
Default	0	1	0	0	0	1	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits	Name	Description
b7	CHIP_ID[3]	CHIP_ID[3:0] is the identification code of G5853, code=4'b0100
b6	CHIP_ID[2]	
b5	CHIP_ID[1]	
b4	CHIP_ID[0]	
b3	VERSION[3]	VERSION[3:0] is the version code of G5853
b2	VERSION[2]	
b1	VERSION[1]	
b0	VERSION[0]	

Function Description

PMIC

The G5853 includes eleven DC/DC Converter, eighteen LDO regulators, and one RTC LDO to generate a multiple-output power-supply system.

No	Module Name	Topology	Default Voltage	Current Rating	Programmable Voltage	Power Pin / Power Domain	Default ON/OFF	SLEEP ON/OFF
1	BUCK1	1.5 or 3MHz/Syn. Buck	0.75V	2.0A	DVS:0.65V~1.425V	VIN1 / VSYS	ON	OFF
2	BUCK2	1.5 or 3MHz/Syn. Buck	0.85V	3.0A	DVS:0.65V~1.425V	VIN2 / VSYS	ON	ON
3	BUCK3	1.5 or 3MHz/Syn. Buck	0.75V	2.0A	DVS:0.55V~1.325V	VIN3 / VSYS	ON	ON
4	BUCK4	1.5 or 3MHz/Syn. Buck	0.75V	3.0A	DVS:0.55V~1. 325V	VIN4 / VSYS	ON	ON
5	BUCK5	3MHz/Syn. Buck	1.2V	3.0A	DVS:0.75V~1.525V	VIN5 / VSYS	ON	OFF
6	BUCK6	3MHz/Syn. Buck	3.2V	3.0A	2.65V~3.4V	VIN6 / VSYS	ON	ON
7	BUCK7	3MHz/Syn. Buck	1.8V	3.0A	1.0V~1.9V	VIN7 / VSYS	ON	ON
8	BUCK8	3MHz/Syn. Buck	1.8V	2.0A	1.0V~1.9V	VIN8 / VSYS	ON	ON
9	BUCK9	3MHz/Syn. Buck	1.15V	1.0A	DVS:0.75V~1.525V	VIN9 / VSYS	ON	ON
10	BUCK10	1.5 or 3MHz/Syn. Buck	0.6V	1.0A	DVS:0.55V~1. 325V	VIN10 / VSYS	ON	ON
11	BUCK11	3MHz/Syn. Buck	2.5V	1.0A	2.1V~2.8V	VIN11 / VSYS	ON	ON
12	LDO1	pMOS LDO	1.8V	300mA	Group-LA	LDOINA / DCDC6	OFF	ON
13	LDO2	pMOS LDO	1.8V	300mA	Group-LA	LDOINB / DCDC6	ON	OFF
14	LDO3	pMOS LDO	1.8V	500mA	Group-LA	LDOINB / DCDC6	ON	OFF
15	LDO4	pMOS LDO	1.8V	500mA	Group-LA	LDOINB / DCDC6	ON	OFF
16	LDO5	pMOS LDO	1.8V	300mA	Group-LA	LDOINA / DCDC6	ON	OFF
17	LDO6	pMOS LDO	1.5V	300mA	Group-LA	LDOINA / DCDC6	OFF	OFF
18	LDO7	nMOS LDO	1.1V	500mA	Group-LB	LDOINC / DCDC8	ON	OFF
19	LDO8	nMOS LDO	0.85V	500mA	Group- LD	LDOINF / DCDC5	ON	OFF
20	LDO9	nMOS LDO	1.1V	500mA	Group-LB	LDOINC / DCDC8	ON	OFF
21	LDO10	nMOS LDO	1.0V	500mA	Group-LC	LDOINC / DCDC8	ON	OFF
22	LDO11	nMOS LDO	1.2V	500mA	Group-LB	LDOIND / DCDC8	ON	ON
23	LDO12	nMOS LDO	1.2V	500mA	Group-LB	LDOIND / DCDC8	ON	OFF
24	LDO13	nMOS LDO	1.05V	500mA	Group-LC	LDOIND / DCDC8	ON	OFF
25	LDO14	pMOS LDO	1.8V	500mA	Group-LA	LDOINE / DCDC6	ON	OFF
26	LDO15	pMOS LDO	1.8V	750mA	Group-LA	LDOINE / DCDC6	ON	OFF
27	LDO16	nMOS LDO	0.75V	1000mA	Group-LD	LDOINF / DCDC5	ON	ON
28	LDO17	nMOS LDO	0.75V	750mA	Group- LD	LDOING / DCDC5	ON	OFF
29	LDO18	nMOS LDO	0.75V	750mA	Group- LD	LDOING / DCDC5	ON	OFF
30	RTCLDO	pMOS LDO	1.8V	50mA	1.8V/2.5V/2.8V/3.0V	VCC / VSYS	ON	ON

Group-LA: 1.0V/1.2V/1.5V/1.8V/2.5V/2.8V/3.0V/3.3V
Group-LB: 1.0V/1.1V/1.15V/1.2V/1.25V/1.3V/1.35V/1.4V
Group-LC: 0.9V/1.0V/1.05V/1.1V/1.15V/1.2V/1.25V/1.3V
Group-LD: 0.65V/0.7V/0.75V/0.85V/0.9V/0.95V/1.0V/1.05V

PMU Power ON/OFF Initiation

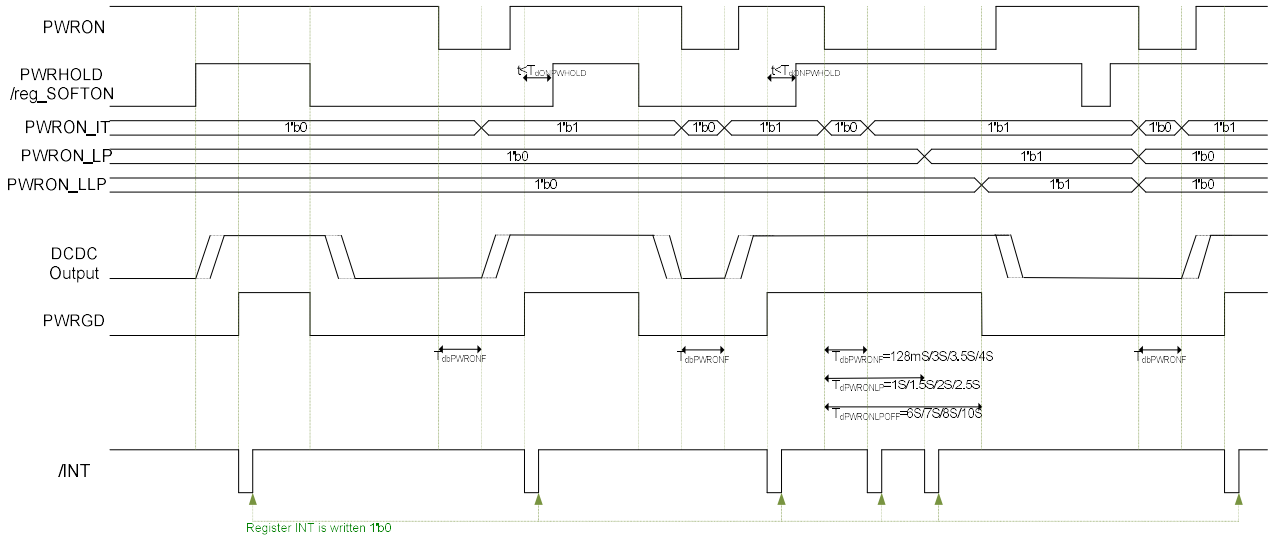
The following conditions are available to turn on the PMU of G5853:

- PWRON low-level pressed with duration longer than $T_{dbPWRONF}$
- Toggle PWRHOLD high-level or write 1 to register SOFTON (when PWRON_LPOFF=1'b0)

When the PMU start-up process is initiated by the PWRON low-level pressed, the microprocessor needs pull high PWRHOLD pin or write 1 to register SOFTON in 480mS delay from PWRGD rising edge. If no high-level signal is applied to PWRHOLD pin and register SOFTON is 0 after 480mS from PWRGD rising edge, the PMU starts the power-off process and enters shutdown mode.

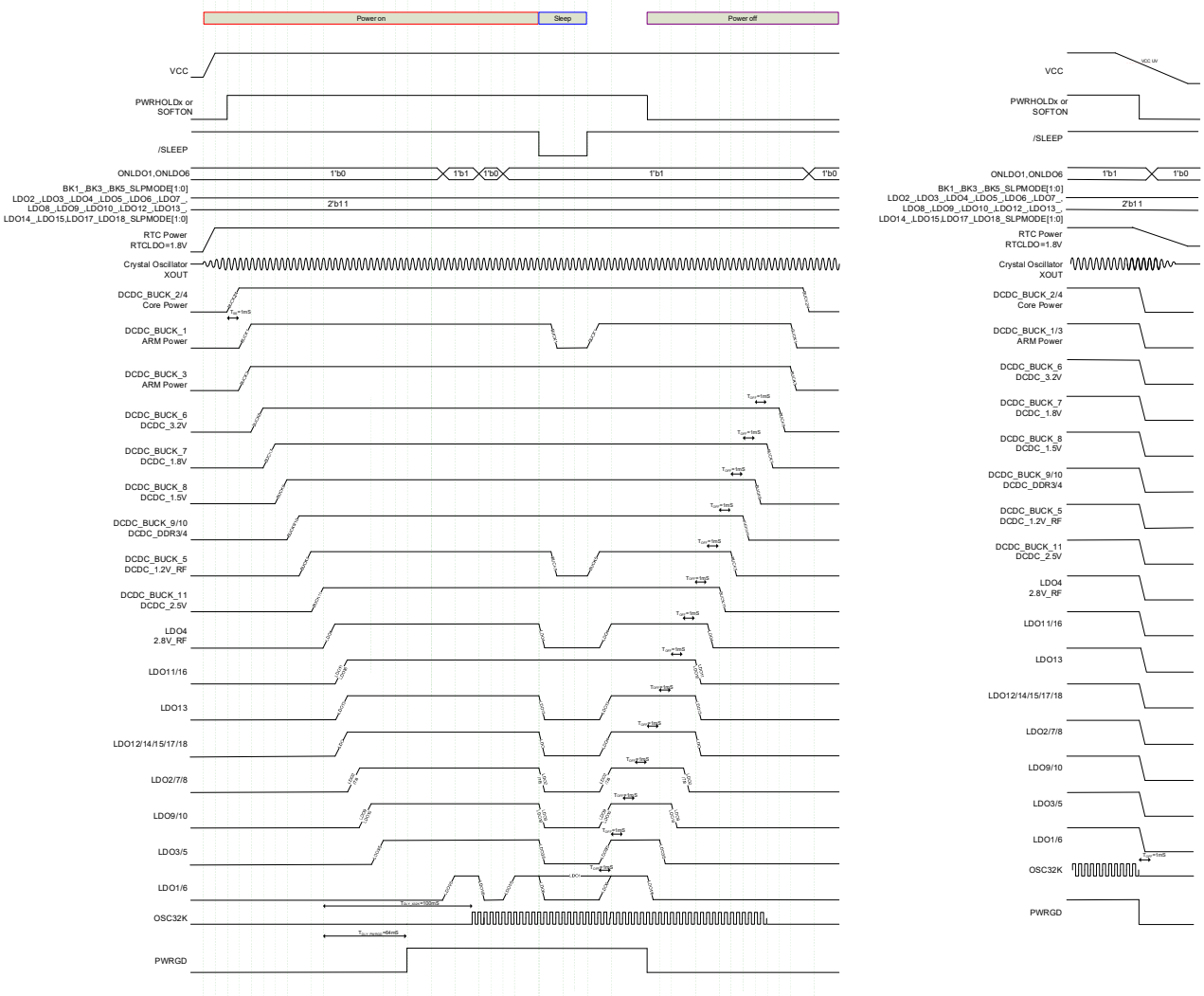
The following conditions are available to turn off the PMU of G5853:

- PWRON low-level pressed with duration longer than $T_{dPWRONLPOFF}$ (if EN_LLP=1'b1)
- Toggle PWRHOLD low-level and write 0 to register SOFTON after 480mS delay from the rising edge of PWRGD
- Output voltage UVP of DCDC converters occurs with duration longer than 128mS
- G5853 thermal shutdown occurs



PMIC Power ON/OFF Sequence

When the power on condition is met, these DC/DC converters, and LDOs start up in sequence except for LDO1, and LDO6. The open-drain output PWRGD is high with T_{DLY_PWRGD}(64mS typ.) from BUCK11 finishes power on. LDO1, and LDO6 can start up by writing 1 to register bit ONLDO after PWRGD is high. The 32kHz clock is enable at OSC_32K pin with T_{DLY_X32K}(100mS typ.) time delay configured by register TIMER_X32K.



PMIC Fault Protection

G5853 provides VCC over voltage protection, VCC under-voltage protection, thermal shutdown, power units' over-current protection, and short-circuit protection to achieve complete protection.

	Protection type	Threshold	Protection methods	Reset Method
Thermal	TSD	Junction Temp. >150°C	IC shutdown	Reset by the power- on/off initiation conditions
VCC	OVP	VCC>6.0V	IC shutdown	Reset by the power-on/off initiation conditions
	UVLO	VCC<2.5V	IC shutdown	Reset by VCC DDLO
	DDLO	VCC<1.8V	IC shutdown	Condition release
DCDC1 Buck	Current Limit	PMOS current>3.0A	PMOS Off, NMOS on	Automatic Reset at next cycle
	UVP	VOUT1< $VOUT_{SET}$-125mV	IC shutdown if period above 128ms	Reset by the power- on/off initiation conditions
DCDC2 Buck	Current Limit	PMOS current>4.0A	PMOS Off, NMOS on	Automatic Reset at next cycle
	UVP	VOUT2< $VOUT_{SET}$-125mV	IC shutdown if period above 128ms	Reset by the power- on/off initiation conditions
DCDC3 Buck	Current Limit	PMOS current>3A	PMOS Off, NMOS on	Automatic Reset at next cycle
	UVP	VOUT3< $VOUT_{SET}$-125mV	IC shutdown if period above 128ms	Reset by the power- on/off initiation conditions
DCDC4 Buck	Current Limit	PMOS current>4A	PMOS Off, NMOS on	Automatic Reset at next cycle
	UVP	VOUT4< $VOUT_{SET}$-125mV	IC shutdown if period above 128ms	Reset by the power- on/off initiation conditions
DCDC5 Buck	Current Limit	PMOS current>4A	PMOS Off, NMOS on	Automatic Reset at next cycle
	UVP	VOUT5< $VOUT_{SET}$-125mV	IC shutdown if period above 128ms	Reset by the power- on/off initiation conditions
DCDC6 Buck	Current Limit	PMOS current>4A	PMOS Off, NMOS on	Automatic Reset at next cycle
	UVP	VOUT6< 75%*$VOUT_{SET}$	IC shutdown if period above 128ms	Reset by the power- on/off initiation conditions
DCDC7 Buck	Current Limit	PMOS current>4A	PMOS Off, NMOS on	Automatic Reset at next cycle
	UVP	VOUT7< 90%*$VOUT_{SET}$	IC shutdown if period above 128ms	Reset by the power- on/off initiation conditions
DCDC8 Buck	Current Limit	PMOS current>3A	PMOS Off, NMOS on	Automatic Reset at next cycle
	UVP	VOUT8< 90%*$VOUT_{SET}$	IC shutdown if period above 128ms	Reset by the power- on/off initiation conditions
DCDC9,DCDC10 Buck	Current Limit	PMOS current>2A	PMOS Off, NMOS on	Automatic Reset at next cycle
	UVP	VOUT9< $VOUT_{SET}$-125mV	IC shutdown if period above 128ms	Reset by the power- on/off initiation conditions
DCDC11 Buck	Current Limit	PMOS current>2.0A	PMOS Off, NMOS on	Automatic Reset at next cycle
	UVP	VOUT11< 90%*$VOUT_{SET}$	IC shutdown if period above 128ms	Reset by the power- on/off initiation conditions
RTCLDO	Current Limit	PMOS current>60mA		PMOS current<60mA
LDO1~LDO18 LDO	Current Limit	PMOS current>I_{LIMLDO}		PMOS current< I_{LIMLDO}
	SCP	VOUTX<12.5%*$VOUTX_{SET}$	LDO shutdown	Reset by the power- on/off initiation conditions, I^2C ONLDO control

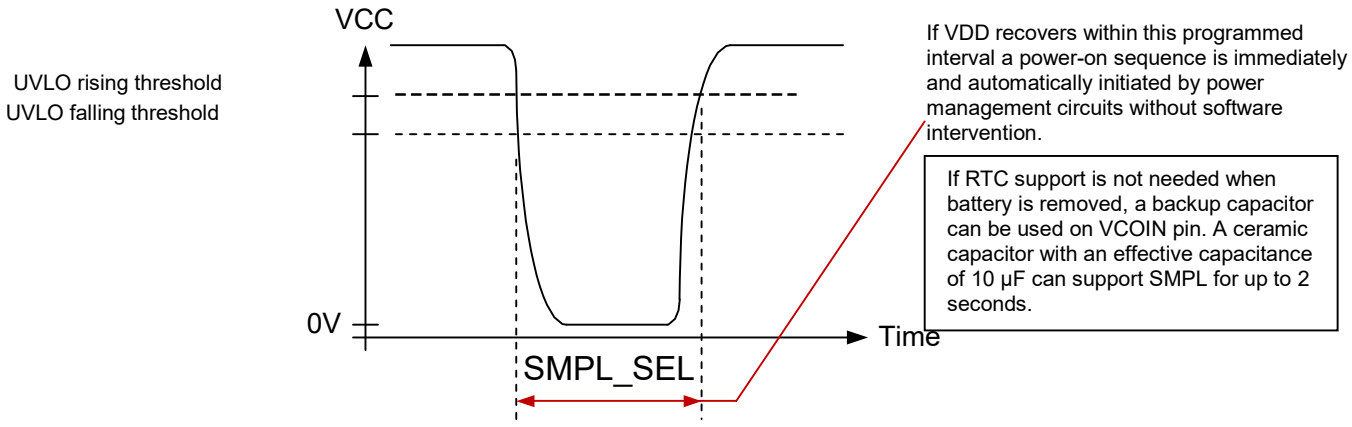
/INT, Interrupt Signal

The G5853 indicates interrupt signal to external processor by /INT open-drain output. /INT is toggled low when these conditions shown below happen. After /INT is toggled low in these conditions, /INT is toggled high after these interrupt registers are read through I^2C interface.

/INT Toggle Low	When PMIC turns on with event condition		During PMIC On	
	No Event	Event Occurred	Event Appear	Event Disappear
PWRON falling-edge de-bouncing (PWRON_IT)	NO	YES	YES	NO
PWRON long press (PWRON_LP)	NO	YES	YES	NO
PWRON long long press to turn off PMIC (PWRON_LLP)	NO	YES	YES	NO
Fault Condition of power units (FAULT_xx)	NO	YES	YES	NO
Chip Temperature (THERMALx)	NO	YES	YES	NO
Sudden Momentary Power Loss (SMPL)	NO	YES	YES	NO

Sudden Momentary Power Loss

If VCC drops out of range (< VCC_{UV} nominal), then it returns in-range within a programmable interval of between 0.5 and 2.0 seconds, and the recovery is executed.



PCB layout guidelines

Careful printed circuit layout is extremely important to avoid causing parasitical capacitance and line inductance. The following layout guidelines are recommended to achieve optimum performance.

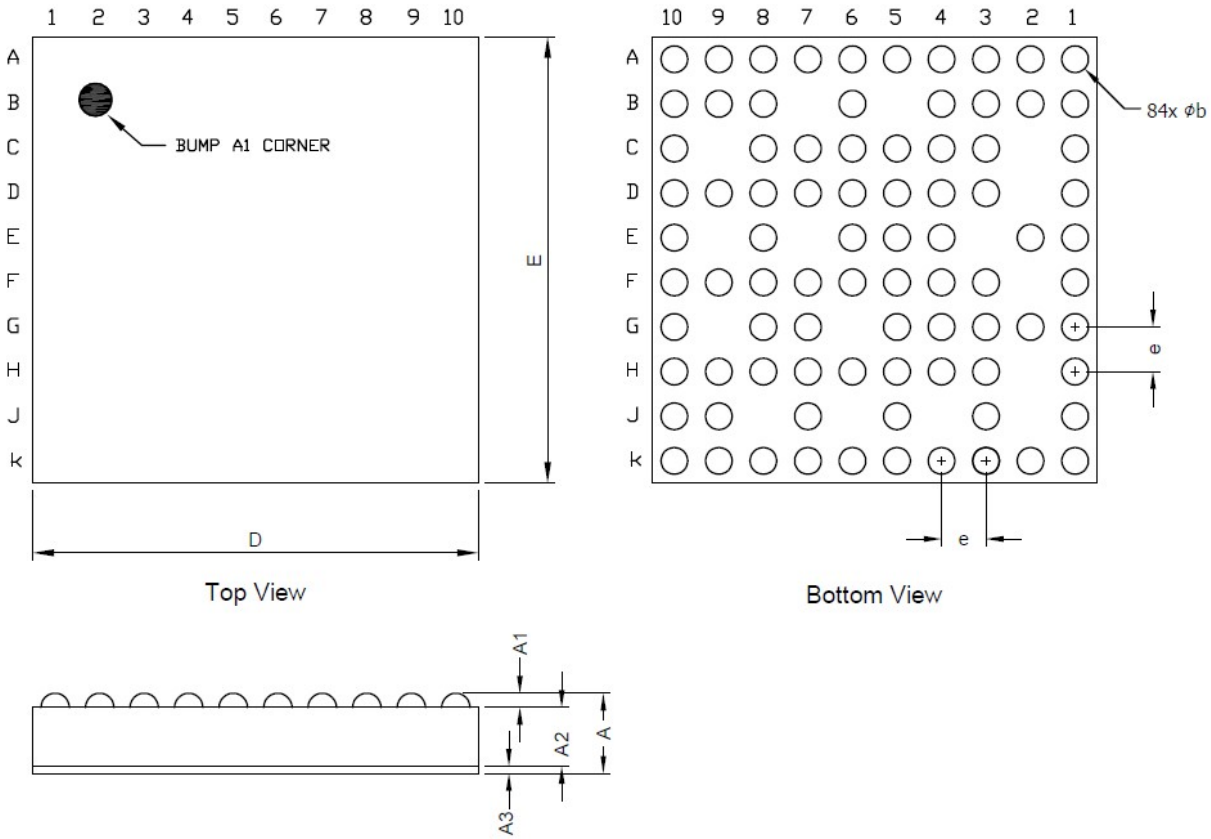
- Please the buck converter inductor close to the LX pin. Keep traces short, direct, and wide.
- Please ceramic bypass capacitors near the input/output pin.
- All feedback signals must first go through the regulator capacitors.
- Place the crystal and its components close to the oscillator side and the oscillator pins.
- Reduce the parasitic capacitance between XIN and XOUT signals by routing them as far apart as possible.
- Ensure that the ground plane under the oscillator and its components are of good quality.
- Avoid long connections to the crystal and to the load capacitor that create a large loop on the PCB.
- Do not route any digital-signal lines on the opposite side of the PCB under the crystal area.
- Keep other digital signal lines, especially clock lines and frequently switching signal lines, as far away from the crystal connections as possible. Crosstalk from digital signals may disturb the small-amplitude sine-shaped oscillator signal.

It is recommended to make use of the situation and add a ground guard ring around the crystal signals. And the section between crystal and the load capacitors is laid out symmetrically

Revision History

Ver	Eff_Date	Author	Change Description
0.1	2018/12/6	Angus	Original
0.2	2018/12/19	Angus	1. minimum footprint 2. package information
0.3	2019/1/2	Angus	1. change package to WLCSP 10x10-84b 2. update pin configuration 3. update minimum footprint PCB layout 4. update pin description 5. update package information
0.4	2019/1/8	Angus	1. change PSRR of LDO from 65dB to 75Db 2. rename pin ENLDO as /SLEEP 3. p.13:0x32,0x33,0x53,0x55,0x56,0x62,0x63 RESET value 4. p.29: LDO5 default OFF. LDO13 default ON. BUCK1,BUCK3 sleep OFF. LDO5 sleep ON. LDO13,LDO15,LDO17,LDO18 sleep OFF 5. p.31:PMIC on/off sequence

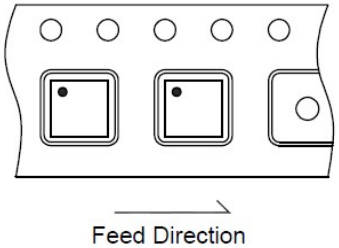
Package Information



WLCSP10X10-84 Package

Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.540	0.600	0.660	0.0213	0.0236	0.0260
A1	0.170	0.200	0.230	0.0067	0.0079	0.0091
A2	0.350	0.375	0.400	0.0138	0.0148	0.0157
A3	0.025 REF			0.0010 REF		
D	3.920	3.960	4.000	0.1543	0.1559	0.1575
E	3.920	3.960	4.000	0.1543	0.1559	0.1575
b	0.230	0.260	0.290	0.0091	0.0102	0.0114
e	0.400 BSC			0.0157 BSC		

Taping Specification



PACKAGE	Q'TY/REEL
WLCSP10X10-84	3,000 ea