High Voltage Synchronous Rectified Buck MOSFET Driver

Features

- **Drivers Two N-MOSFETS**
- **Adaptive Shoot-Through Protection**
- **0.5Ω On-Resistance, 4A sink Current Capability**
- **Supports High Switching Frequency**
- **Tri-State PWM Input for Power Stage Application**
- **Output Disable Function**
- **Integrated Boost Switch**
- **Low Bias Supply Current**
- **VCC POR Feature Integrated**

Applications

- **Core Voltage Supplies**
- **High Frequency Low Profile DC/DC Converter**
- **High Current Low Output Voltage DC/DC Converter**
- **High Input Voltage DC/DC Converters**

General Description

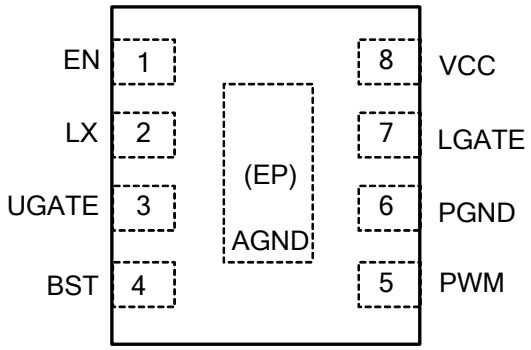
The G6090 is a high frequency, dual MOSFET driver specifically designed to drive two power N-MOSFETs in a synchronous–rectified buck converter topology. The drivers are capable of driving a 3nF load with a fast rising/falling time and a tiny propagation delay. The G6090 also embeds PWM tri-state mode that can turn OFF the UGATE and the LGATE for power state application. This device implements bootstrapping on the upper gates with only a single external capacitor The G6090 supports adaptive shoot though protection, under-voltage lockout (UVLO), and output disable the function in TDFN2X2-8 package.

Ordering Information

ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE (Green)
G6090RC1U	6090	-40°C~ +85°C	TDFN2X2-8

Note: RC: TDFN 2X2-8
1: Bonding Code
U: Tape & Reel
Green : Lead Free / Halogen Free

Pin Configuration



G6090 TDFN 2X2-8

Absolute Maximum Ratings

VCC to GND . . . . . -0.3V to 6V
EN, PWM to GND . . . . . -0.3V to 6V
BST to LX . . . . . -0.3V to 6V
BST to GND . . . . . -0.3V to 36V
LX to GND . . . . . -0.3V to 30V
< 20ns . . . . . -6V to 36V
UGATE to LX . . . . . -0.3V to 6V
LGATE to GND . . . . . -0.3V to 6V
Continuous Power Dissipation (T_A = +25°C)
TDFN2X2-8 . . . . . 1.6W

Thermal Resistance Junction to Ambient, (θ_{JA})
TDFN2X2-8. . . . . 78°C/W
Thermal Resistance Junction to Case, (θ_{JC})
TDFN2X2-8. . . . . 16°C/W
Junction Temperature . . . . . 150°C
Storage Temperature (T_S) . . . . . -55°C to +150°C
Reflow Temperature (soldering, 10sec) . . . . . 260°C
ESD(HBM) 2KV

Electrical characteristics

(VCC=5V, T_A=25°C)

The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified.

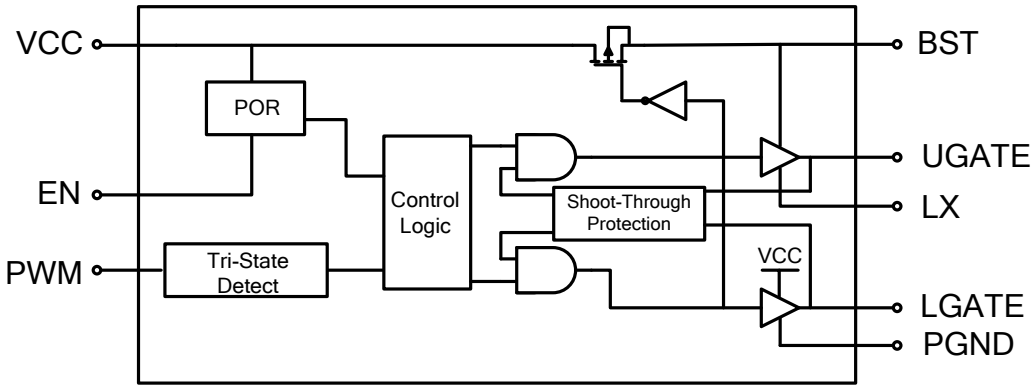
PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Quiescent Current		I_Q	PWM Pin Floating	---	80	---	μA
Shutdown Current		I_{SHDN}	V_{EN}=0V, PWM=0V, VCC=5V	---	0	5	μA
VCC Power On Reset (POR)		V_{PORH}	VCC POR Rising	---	4.2	4.5	V
		V_{PORL}	VCC POR Falling	3.5	3.84	---	V
		V_{PORHYS}	Hysteresis	---	360	---	mV
Internal Boost Switch On Resistance		R_{BST}	VCC to BST, 10mA.	---	---	80	Ω
PWM Input Current		I_{pwm}	V_{PWM}=5V	---	174	---	μA
			V_{PWM}=0V	---	-174	---	
PWM Tri-state Rising Threshold		V_{PWMH}	VCC=5V	3.5	---	---	V
PWM Tri-state Falling Threshold		V_{PWMH}	VCC=5V	---	---	1.3	V
EN Input Voltage	Logic-High	V_{ENH}	VCC=5V	1.4	---	---	V
	Logic-Low	V_{ENL}	VCC=5V	---	---	0.5	
UGATE Rising Time		t_{UGATEr}	VCC=5V, 3nF Load	---	8	---	ns
UGATE Falling Time		t_{UGATEf}	VCC=5V, 3nF Load	---	8	---	ns
LGATE Rising Time		t_{LGATEr}	VCC=5V, 3nF Load	---	8	---	ns
LGATE Falling Time		t_{LGATEf}	VCC=5V, 3nF Load	---	4	---	ns
UGATE Turn-Off Propagation Delay		t_{PDLU}	VCC=5V, Output Unloaded	---	35	---	ns
LGATE Turn-Off Propagation Delay		t_{PDLL}	VCC=5V, Output Unloaded	---	35	---	ns
UGATE Turn-On Propagation Delay		t_{PDHU}	VCC=5V, Output Unloaded	---	20	---	ns
LGATE Turn-On Propagation Delay		t_{PDHL}	VCC=5V, Output Unloaded	---	20	---	ns
UGATE/LGATE Tri-State Propagation Delay		t_{PTS}	VCC=5V, Output Unloaded	---	35	---	ns
UGATE Driver Source Resistance		R_{UATEsr}	100mA Source Current	---	1	---	Ω
UGATE Driver Sink Resistance		R_{UATEsk}	100mA Sink Current	---	1	---	Ω
LGATE Driver Source Resistance		R_{LATEsr}	100mA Source Current	---	1	---	Ω
LGATE Driver Sink Resistance		R_{LATEsk}	100mA Sink Current	---	0.5	---	Ω

Note
1. Please refer to EV Board PCB Layout Section

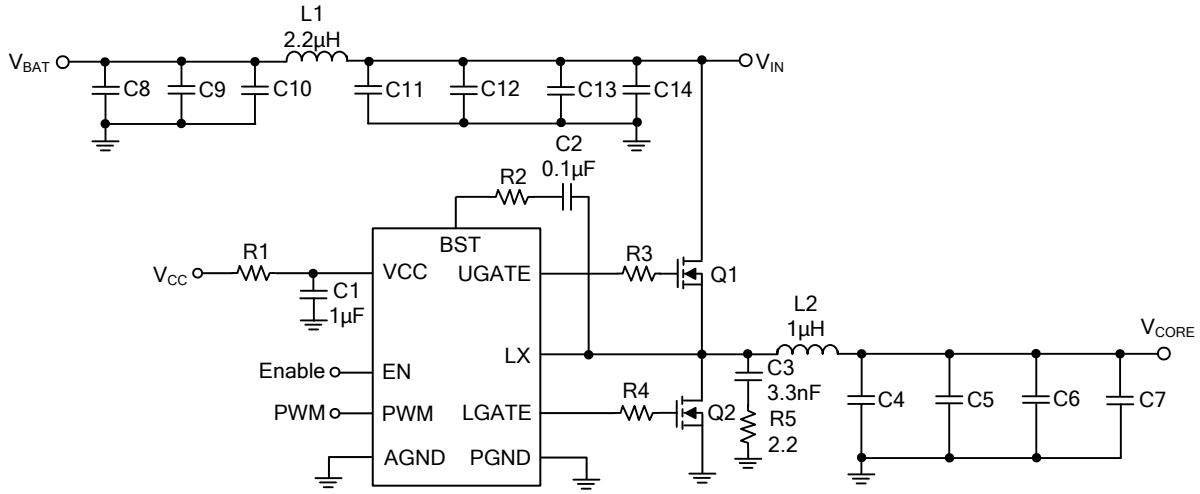
Pin Descriptions

PIN NUMBER	NAME	FUNCTION
1	EN	Enable Pin for MOSFET Driver
2	LX	Switch node connects to external Inductor and for high side MOSFET driver
3	UGATE	High Side Gate Driver
4	BST	Floating Bootstrap Supply Pin for high side MOSFET driver
5	PWM	Control Input for MOSFET Driver
6	PGND	Power Ground for MOSFET driver.
7	LGATE	Low Side Gate Driver
8	VCC	Input Supply Pin. Connect this pin to a 5V bias supply.
EP	AGND	Analog Ground.

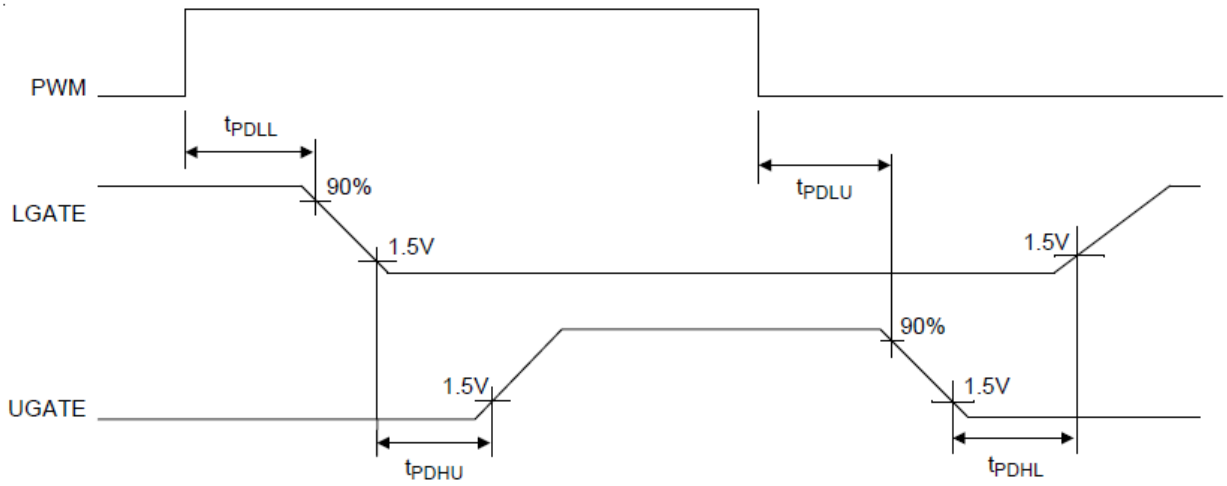
Block Diagram



Typical Application Circuit

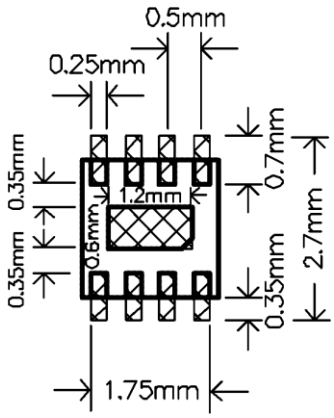


Timing Diagram



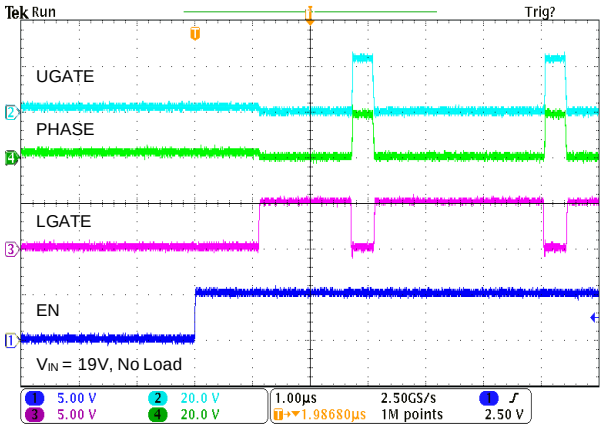
Minimum Footprint PCB Layout Section

TDFN2X2-8

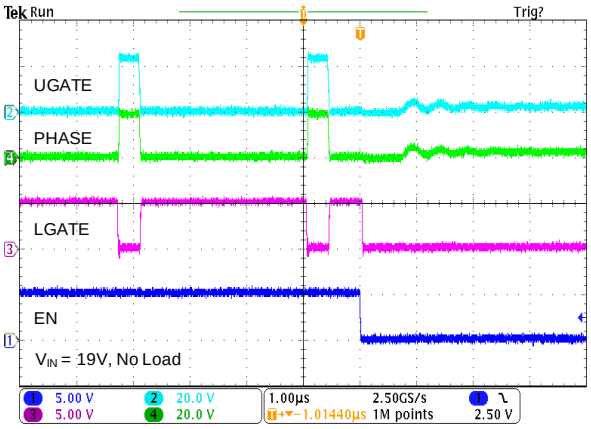


Typical Performance Characteristics

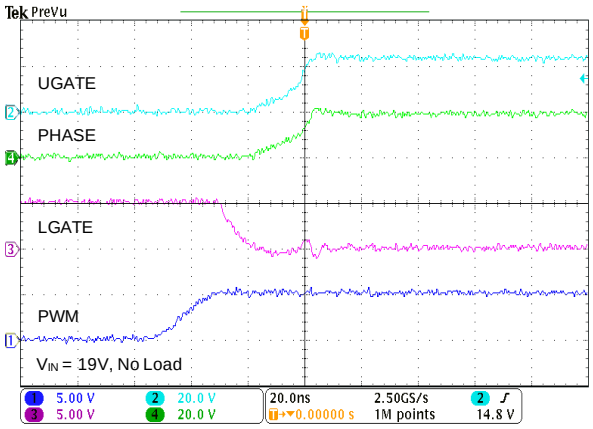
Driver Enable



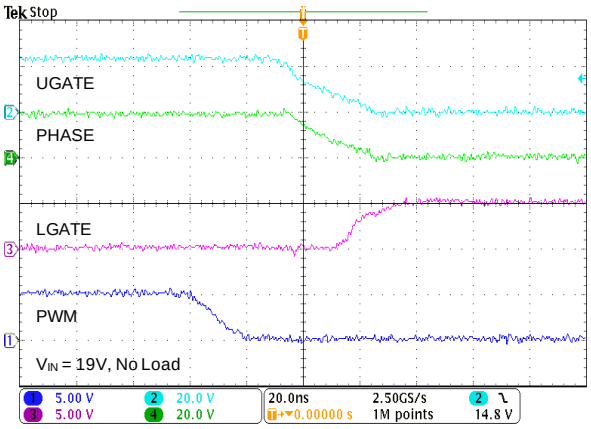
Driver Disable



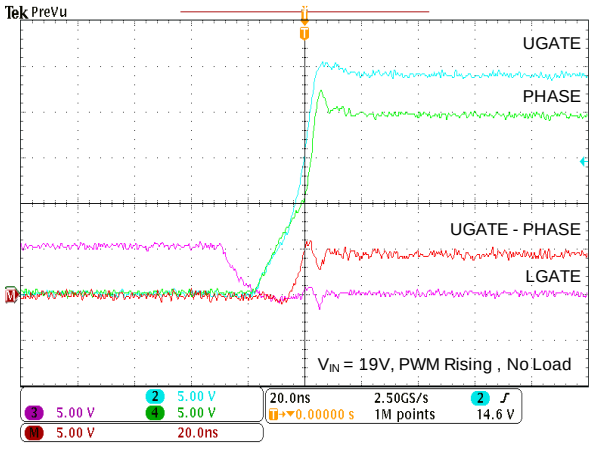
PWM Rising Edge



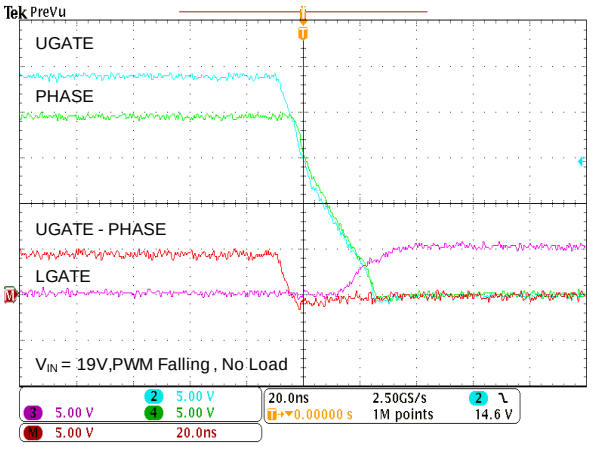
PWM Falling Edge



Dead Time

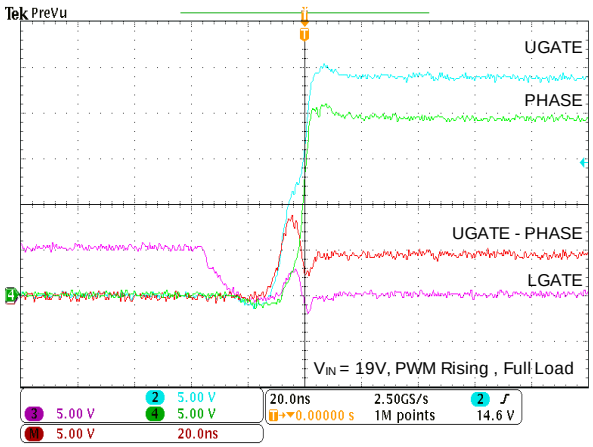


Dead Time

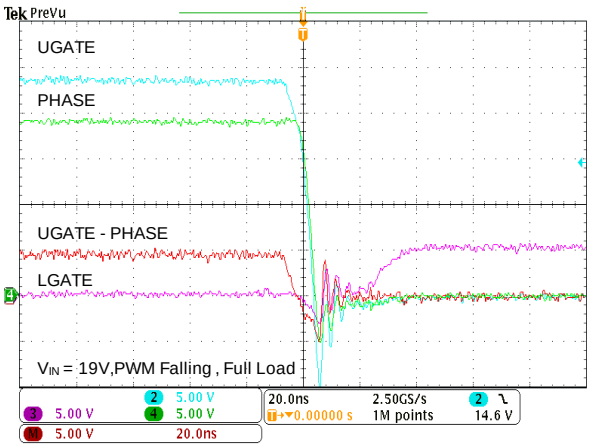


Typical Performance Characteristics

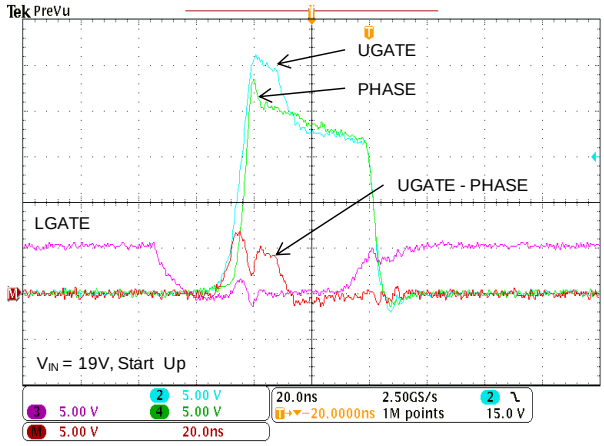
Dead Time



Dead Time



Short Pulse



Detailed Description

Supply Voltage and Power-On-Reset (POR)

The G6090 is designed to drive both high side and low side N-MOSFET of a synchronous buck converter through an externally input PWM control signal. The G6090 required a 5V bias supply for the internal PWM circuit and gate drivers. The POR circuit monitors the supply voltage at the VCC pin. When the VCC supply voltage exceeds the POR rising threshold voltage, the POR circuit enables the device. The POR circuit has a hysteresis and deglitch time so that it will ignore noise on the VCC pin. Bypass VCC to AGND with a 1uF MLCC and close to the device. When the POR asserted, Both UGATE and LGATE are controlled by the PWM input voltage. If the POR de-asserted, both UGATE and LGATE will be pulled to low.

Enable

Pulling the EN pin above 1.4V enables G6090, then PWM controls the UGATE and LGATE, and pulling EN pin below 0.5V will disable the driver outputs and keeps the UGATE and LGATE at low.

PWM

The PWM pin has three states with a non-overlap design. The non-overlap protection circuit ensures the LGATE can be pulled high after the difference voltage of the UGATE to the LX has gone below 1.5V for a propagation delay of t_{PDHL}, the same mechanism, the UGATE can be pulled high after the LAGTE has fallen below 1.5V for a propagation delay of t_{PDHU}. When the PWM pin is less than 1.5V, the UGATE goes low level and UGATE goes high level. When the PWM pin is higher than 3.7V, the UGATE goes high and the LGATE goes low. The G6090 is also compatible with Tri-State input. When the PWM output from the external PWM controller is in high impedance or not connected. The PWM voltage is approximately balancing in 2.5V. The G6090 enters in tri-state mode, the UGATE and the LGATE go low level. Refer to Table1 for PWM truth Table.

Table1 Truth Table

EN	PWM	UGATE	LGATE
0	X	0	0
1	Tri-state	0	0
1	0	0	1
1	1	1	0

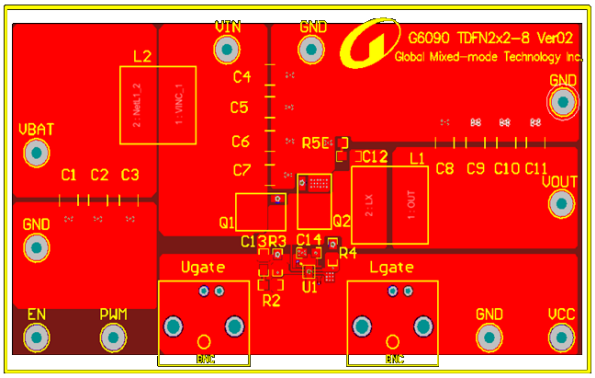
Where
“X” might be either 1 or 0.
“1” means logic high, and “0” means logic low.

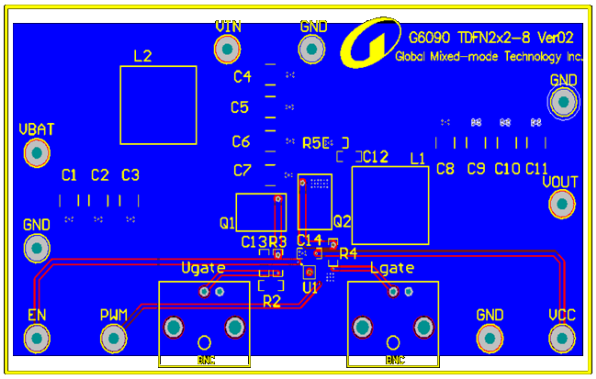
PCB Layout

Layout Considerations

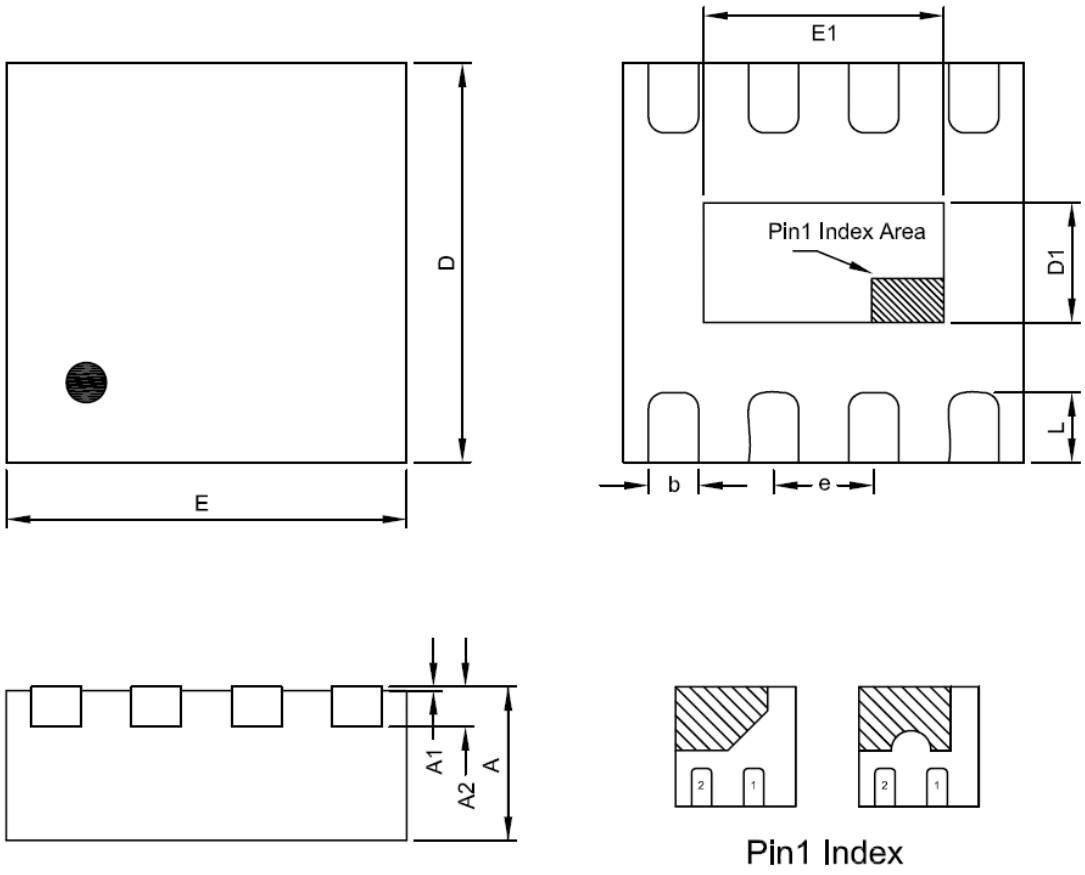
- The input capacitors of the converter should be placed close to the VIN pin, and the ground terminals of input capacitors and output capacitors should be closed PGND pin.
- Minimize copper trace connections that can inject noise into the system, the inductor should be placed as close as possible to the LX pin to minimize the noise coupling into other circuits.
- Short and wide copper trace for the UGATE pin to the gate of High-side MOSFET and LAGTE pin to the gate of Low-side MOSFET.
- Connect AGND and PGND together close to the IC and the negative terminal of COUT.
- Connect PGND of power component Low-side MOSFET source, CIN, and COUT to system ground by a polygon power plane.
- All sensitive analog traces such as VOUT should be placed away from high-voltage switching nodes such as LX, BST nodes to avoid coupling.

PCB Layout Guide





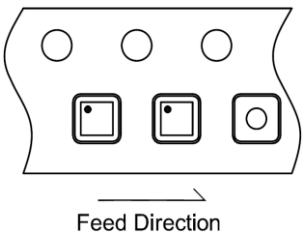
Package Information



TDFN2X2-8 Package

Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.0276	0.0295	0.0315
A1	0.00	- - -	0.05	0.0000	- - -	0.0020
A2	0.20 REF			0.0079 REF		
D	1.95	2.00	2.05	0.0768	0.0787	0.0807
E	1.95	2.00	2.05	0.0768	0.0787	0.0807
D1	0.55	0.65	0.75	0.0217	0.0256	0.0295
E1	1.15	1.25	1.35	0.0453	0.0492	0.0531
b	0.18	0.25	0.30	0.0071	0.0098	0.0118
e	0.50 BSC			0.0197 BSC		
L	0.30	0.35	0.40	0.0118	0.0138	0.0157

Taping Specification



PACKAGE	Q'TY/REEL
TDFN2X2-8	3,000 ea