G6201

Synchronous Buck PWM Controller with 2-Bit VID

Features

- **Input Range From 3.0V to 22V**
- **VCC Range From 4.5V to 5.5V**
- **Internal Soft-Start to Reduce Inrush Current**
- **2-Bit VID Selectable VOUT 0V/1.1V/1.65V/1.8V**
- **1% Reference Accuracy**
- **VOUT Slew Rate**
  - **G6201/A : +17mV/μs when VID counting up**
  - **G6201A : -17mV/μs when VID counting down**
  - **G6201 : Decay when VID counting down**
- **Selectable Switching Frequency**
- **Built-In PGOOD indicator**
- **Built-In ULVO(Under Voltage Lock Out)**
- **Built-In UVP(Under Voltage Protection), SCP (Short Circuit Protection), Cycle-By-Cycle current limit, and Thermal Shutdown**
- **TQFN3X3-20 package**

Applications

- **Tablets and Laptops**

General Description

The G6201 is a synchronous PWM controller with a 2-Bit VID selectable VOUT target for V_{CCIN_AUX} of Intel ICL and TGL platforms. It provides high efficiency, excellent transient response, and high DC output accuracy.

The G6201 supports output voltage selection function among 4 levels of 0V/1.1V/1.65V/1.8V by controlling VID1 & VID0 inputs. The G6201 achieves high efficiency at a reduced cost by eliminating the current-sense resistor of conventional current-mode PWM. Efficiency is further enhanced by an ability to drive very large synchronous rectifier MOSFETs. Single-stage buck conversion allows these devices to directly step down from a high-voltage input to a low-voltage output for the highest possible efficiency.

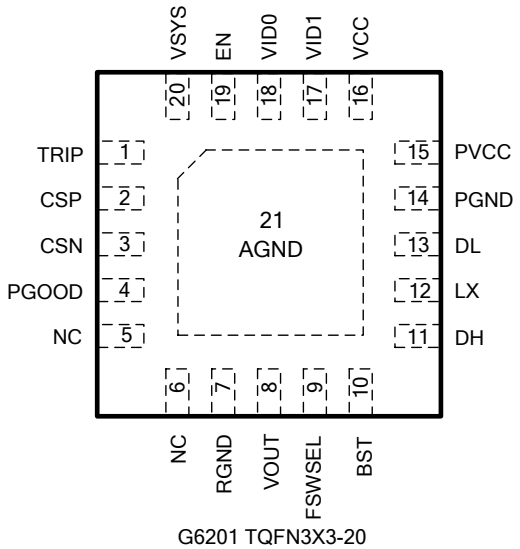
The G6201 provides UVLO, OVP, UVP, OTP, and current limit protection and is integrated into a TQFN3X3-20 package.

Ordering Information

ORDER NUMBER	MARKING	VOUT MODE	TEMP. RANGE	PACKAGE (Green)
G6201RZ1U	6201	Decay down	-40°C~+85°C	TQFN3X3-20
G6201ARZ1U	6201A	Slew down	-40°C~+85°C	TQFN3X3-20

Note: RZ:TQFN3X3-20
1: Bonding code
U: Tape & Reel
Green : Lead Free/ Halogen Free

Pin Configuration



G6201 TQFN3X3-20

Absolute Maximum Ratings

VSYS to GND . . . . . -0.3V to 29V
PVCC, VCC, EN, VIDx to GND . . . . . -0.3V to 6V
TRIP, FSWSEL, PGOOD to GND . . . . . -0.3V to 6V
BST, DH to LX . . . . . -0.3V to 6V
LX to GND . . . . . -0.3V to 29V
DL to GND . . . . . -0.3V to 6V
ESD (HBM) 2kV
ESD (MM) 200V

Operating Ambient Temperature . . . . -40°C to 85°C
Storage Temperature Range . . . . . -65°C to +165°C
Reflow Temperature (soldering, 10 sec). . . . . 260°C

Thermal Information

THERMAL METRIC		TQFN3X3-20	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance	59	°C/W
$R_{\theta JC\_top}$	Junction to case top thermal resistance	66	°C/W
$R_{\theta JB}$	Junction to board thermal resistance	27	°C/W
Ψ_{JT}	Junction to top characterization parameter	2	°C/W
Ψ_{JB}	Junction to board characterization parameter	27	°C/W
$R_{\theta JC\_bot}$	Junction to case bottom thermal resistance	5	°C/W

1. Package thermal metric is obtained using the method described in JEDEC specification JESD51-7, using a four-layer board.
2. The maximum power dissipation is $P_{D(MAX)} = \frac{(T_{JMAX} - T_A)}{R_{\theta JA}}$, Exceeding the maximum allowable power dissipation results in excessive die temperature, and the device will enter thermal shutdown.

Electrical characteristics

(VCC=5V, VSYS=19V, T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
GENERAL						
VCC Operating Voltage for PMIC	V_{CC}		4.5	5.0	5.5	V
VCC UVLO Threshold	V_{CC_UVLO}	VCC falling	3.7	3.9	4.1	V
VCC UVLO Hysteresis	$V_{CC\_UVLO\_HYS}$		---	200	---	mV
VCC Shutdown Current	I_{SD}	EN=0V	---	5	---	μA
VCC Supply Current	I_{VCC}	EN=5V, No switching, V_{OUT}=0V	---	300	550	μA
VSYS Operating Voltage	V_{SYS}		3	---	24	V
VSYS UVLO Threshold	V_{SYS_UVLO}	VSYS falling	---	2.7	---	V
VSYS UVLO Hysteresis	$V_{SYS\_UVLO\_HYS}$		---	200	---	mV
Control Signal						
Logic-Input High Threshold (EN/VID1/VID0)	V_{EN_H}	High threshold	1.0	---	---	V
Logic-Input Low Threshold (EN/VID1/VID0)	V_{EN_L}	Low threshold	---	---	0.4	V
FSWSEL	V_{FSWSEL_H}	Rising edge of 5V voltage rail	4.5	---	---	V
	V_{FSWSEL_HiZ}	Floating	1.0	1.3	1.6	V
	V_{FSWSEL_L}	Falling edge, 5V voltage rail	---	---	0.4	V

Note

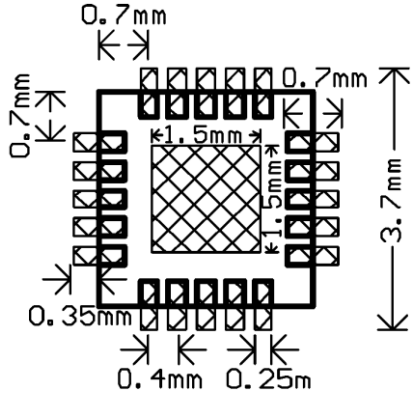
1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Device is ESD sensitive. Handling precaution recommended. The Human Body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.

Electrical characteristics (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Output Signal						
PGOOD Threshold	V_{PG_TH}	PGOOD Detect, Rising Edge	86	90	94	$\%V_{OUT}$
PGOOD Threshold Hysteresis	$V_{PG\_TH\_HYS}$		---	6	---	$\%V_{OUT}$
PGOOD Leakage Current		High state, V_{PGOOD} = 5.5V	---	---	1	μA
PGOOD Output Low Voltage	V_{POOG_LOW}	I_{PGOOD_LOW} = 10mA	---	---	0.3	V
PGOOD Available Time	t_{PG}	EN rising to PGOOD rising	---	1.5	2	ms
PWM Controller						
Output Voltage Soft-Start Internal	t_{SS_VDDQ}	VOUT voltage from 10% to 90%.	---	1	1.5	ms
Output Voltage	V_{OUT}	VID[1:0] = 11	1.782	1.8	1.818	V
		VID[1:0] = 10	1.6335	1.65	1.666	V
		VID[1:0] = 01	1.089	1.1	1.111	V
		VID[1:0] = 00	-0.01	0	0.01	V
Output Discharge Resistance	Rdis	EN=0V	---	50	---	Ω
Dynamic Voltage Scale Slew Rate			13	17	30	mV/μs
Switching Frequency	F_{SW}	FSWSEL = 5V	---	800	---	kHz
		FSWSEL = Floating	510	600	690	kHz
		FSWSEL = 0V	---	400	---	kHz
Minimum Off-Time	t_{OFF_MIN}		---	250	---	ns
Current Limit Setting Current	I_{TRIP}		5.4	6	6.6	μA
TRIP Voltage Range	V_{TRIP}		0	---	2.5	V
Current Comparator Offset		LX- (VTRIP/12)	-10	---	10	mV
Current Limit Temperature Coefficient			---	4700	---	ppm/°C
Zero Current Crossing Threshold	V_{LX_ZC}		-4	---	4	mV
Internal Boost Diode Resistance	R_{BOOT}	VCC to BST, I_{BOOT} = 10mA	---	40	80	Ω
DH Driver Source	R_{DH_SR}	BST – LX forced to 5V	---	2	4	Ω
DH Driver Sink	R_{DH_SK}	BST – LX forced to 5V	---	1	2	Ω
DL Driver Source	R_{DL_SR}	DL, High State	---	1.5	3	Ω
DL Driver Sink	R_{DL_SK}	DL, Low State	---	0.7	1.5	Ω
Dead Time	t_{d_LU}	From DL falling to DH rising	---	30	---	ns
	t_{d_UL}	From DH falling to DL rising	---	20	---	ns
Protection						
OVP Threshold	V_{OVP}		2.05	2.2	2.35	V
OVP Propagation Delay			---	5	---	μs
UVP Threshold	V_{UVP}		---	68	---	$\%V_{OUT}$
UVP Propagation Delay			---	2	---	μs
Thermal Shutdown Threshold	T_{SD}		---	160	---	°C

Minimum Footprint PCB Layout Section

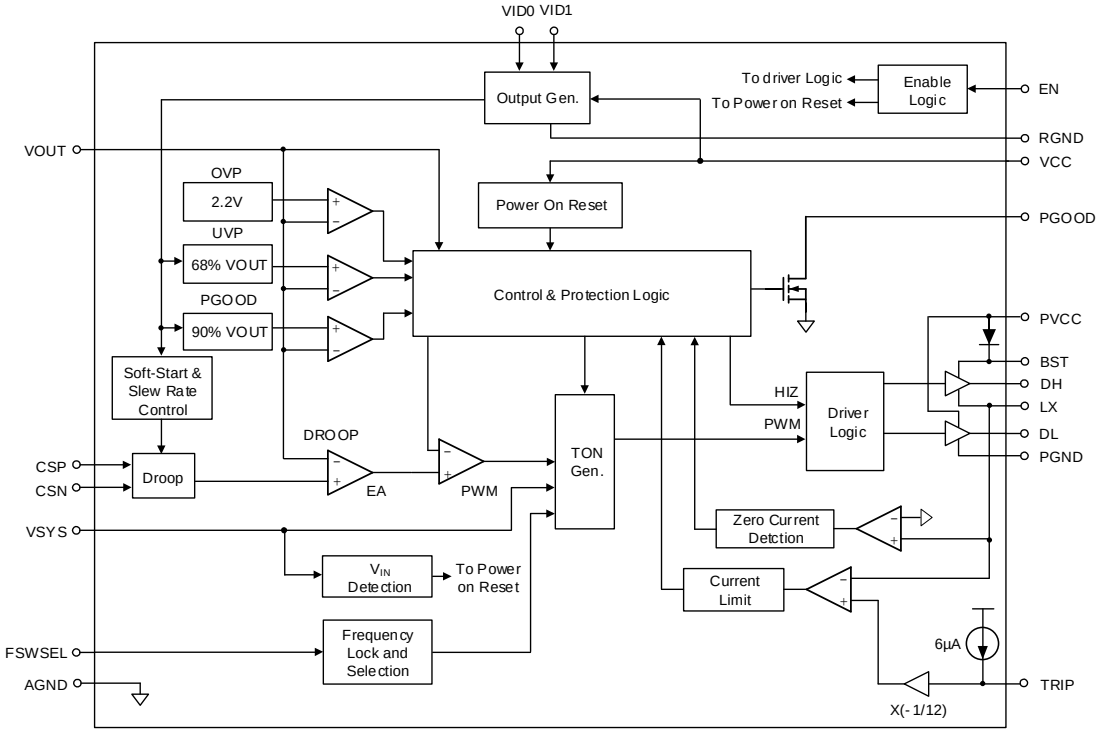
TQFN3X3-20



Pin Description

Pin	NAME	Function
1	TRIP	Current Limit Setting Current
2	CSP	Positive input pin of the current sense
3	CSN	Negative input pin of the current sense
4	PGOOD	Power Good Signal of VOUT
5	NC	No Connect
6	NC	No Connect
7	RGND	Remote sense GND, the negative node of the remote output voltage sense.
8	VOUT	Remote sense VOUT, the positive node of the remote output voltage sense.
9	FSWSEL	Switching frequency selectable pin
10	BST	Bootstrap Supply for the High-Side MOSFET.
11	DH	The High-Side Gate Drive Output.
12	LX	Switch node for Buck controller. Connect LX to the inductor and bootstrap capacitor. LX is connected to VIN when the High-Side MOSFET is on and to PGND when the LS-FET is on. Use wide and short PCB traces to make the connection. Keep sensitive traces away from LX.
13	DL	The Low-Side Gate Drive Output.
14	PGND	Power Ground for DL driver and low-side power MOSFET
15	PVCC	IC Power supply input pin. Connect a +4.5V to +5.5V Voltage Bypass to GND with a 1μF MLCC. It provides power for the Pre-gate driver.
16	VCC	IC power supply input pin. Connect a +4.5V to +5.5V Voltage Bypass to GND with a 1μF MLCC. It provides power for IC control algorithm.
17	VID1	VID1 Input. This pin is used to select VOUT voltage
18	VID0	VID0 Input. This pin is used to select VOUT voltage
19	EN	Enable
20	VSYS	Power Supply Input. VSYS is used to set the PWM one-shot Timing. Bypass to GND with an MLCC of 0.1μF.
EP	GND	Ground. The Exposed Pad must be soldered to a large PCB for maximum power dissipation.

Function Diagram



Block Diagram & Application circuit

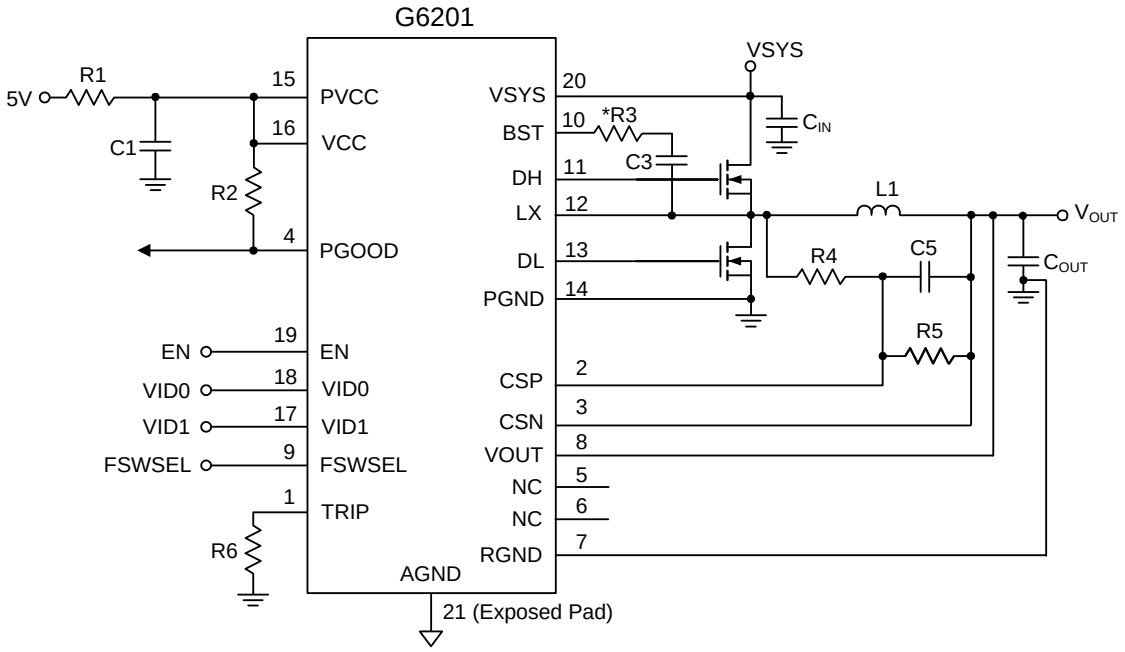


Figure 1

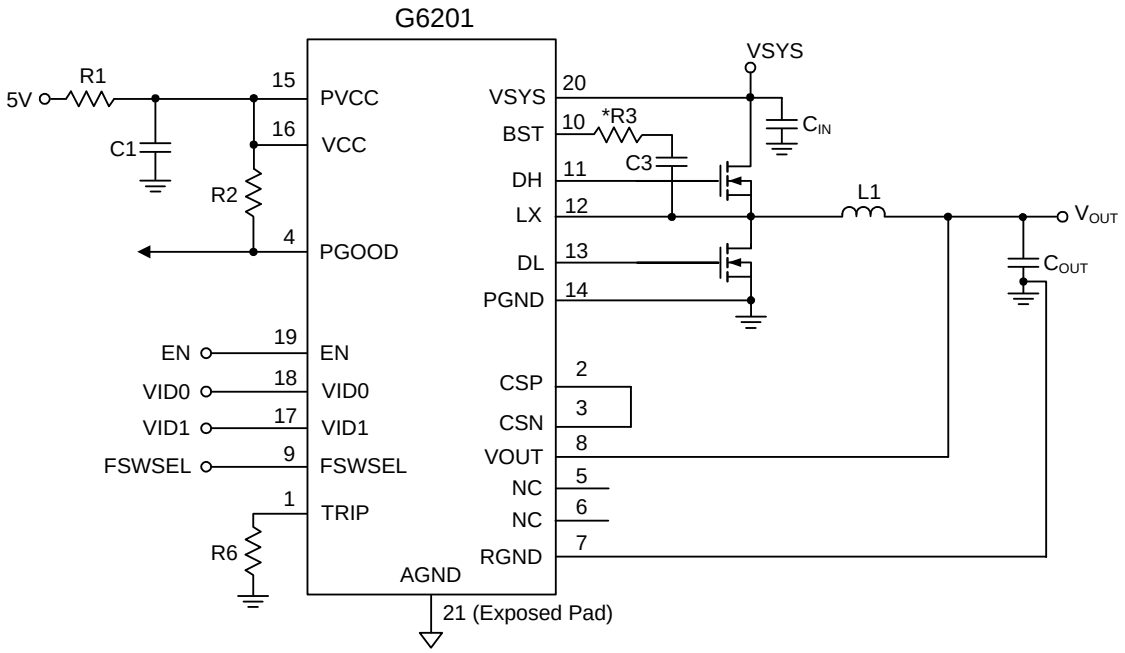


Figure 2

Operation and Application

G6201 is a high performance synchronous buck PWM controller, the control scheme is based on constant-on-time architecture, which measures real switching frequency from LX pin, and creates a virtual inductor current ramp in order to get good stability with using low-ESR multi-layer ceramic capacitors (MLCC). The buck controller has a full set of protection (OCP/UVP/OVP).

Enable

When the input voltage is greater than the under voltage lockout threshold, a logic-high (>1.2V) enables the G6201; a logic-low (<0.4V) or floating forces the IC into shutdown mode. When the device is disabled, there is a 50Ω resistive discharge path from the VOUT pin.

Inductor Selection

The inductor is required to supply constant current to the output load. A suitable inductor should consider inductance, required peak output current, physical size, and price. The lower inductance gains from reduced size, price and better the circuit's transient response. However, the lower inductance causes a larger inductor's ripple current and output ripple voltage. The higher inductance gets the opposition results as described in the previous. Volt-second balance determines a suitable inductor, the ΔI_L or called peak-to-peak inductor's ripple current in the range of 20% to 50% of the maximum I_{OUT} is usually used. (the maximum I_{OUT} is the same as Iccmax that can get from Intel's document). Set the maximum I_P below the maximum I_{OUT}. The inductance can be calculated with equations (1)~(2).To guarantee the required output current, saturation current rating and heat rating current of the selected inductor must exceed maximum I_P at the maximum I_{OUT}.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times F_{SW} \times \Delta I_L} \quad (1)$$

Once an inductance is chosen, the ripple current ΔI_L can be calculated to determine the required peak inductor current.

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times F_{SW} \times L} \quad (2)$$

$$I_P = I_{OUT} + \frac{\Delta I_L}{2} \quad (3)$$

$$I_V = I_{OUT} - \frac{\Delta I_L}{2} \quad (4)$$

$$V_{OUT} = D \times V_{IN} \text{ where } D = \frac{T_{ON}}{T_{SW}} = \frac{V_{OUT}}{V_{IN}} \quad (5)$$

Over Current Protection (OCP)

The G6201 OCP designed is implemented using a cycle-by-cycle inductor's "valley" current detected control circuit, Figure 3 The switch current is monitored by measuring the low-side voltage between the LX pin and GND. The voltage is proportional to the switching current and the on-resistance of the low-side MOSFET. During the period of high-side MOSFET turns on, the high-side switching current increases at a linear rate which is determined by V_{IN}, V_{OUT}, and inductance. And during low-side MOSFET turns on, the low-side switching current decreases linearly. The average value of the switching current is the I_{OUT} current. If the sensing voltage of the low side MOSFET is above the voltage proportional to the current limit, The G6201 keeps the low side MOSFET turning on until the sensing voltage falls below the voltage proportional to the current limit threshold and starts a new switching cycle. The G6201 current limit threshold can be set by a resistor (R_{TRIP}) between the TRIP pin and GND. Once the chip is enabled and VCC exceeds the UVLO threshold, an internal current source I_{TRIP} flows through R_{TRIP}. The voltage across TRIP is the current limit protection threshold V_{RTIP}. The threshold range of V_{TRIP} is from 50mV to 1V. R_{TRIP} can be determined using the following Equation (6)

$$R_{TRIP}(k\Omega) = \frac{R_{ON\_LS}(m\Omega) \times I_V(A) \times 12}{I_{TRIP}(uA)} \quad (6)$$

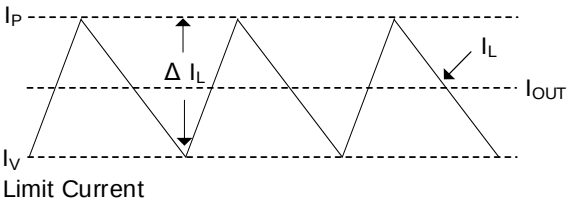


Figure 3 Cycle-By-Cycle Valley Current Detected Control

Where I_V represents desired inductor limit current (valley of inductor current) and I_{TRIP} is the limit setting current (6μA) with temperature coefficient of 4700ppm/°C to compensate the temperature dependency of the R_{ON_LS}.

Input Capacitor Selection

A Buck converter requires input decoupling capacitors because the high side MOSFET current of a buck converter is a discontinuous current when the high side MOSFET turns on and the low side MOSFET is off. The input power source is not easy to fully support the instant required current changes, thus the input capacitor supplies this instant changing current for the high side MOSFET and the inductor. By supplying the instant required current, the input capacitors maintain V_{IN} fairly steady. Generally, the V_{IN} ripple is caused by the phenomenon of the input capacitor discharged slightly during the high MOSFET on period and recharged during the low side MOSFET on period.

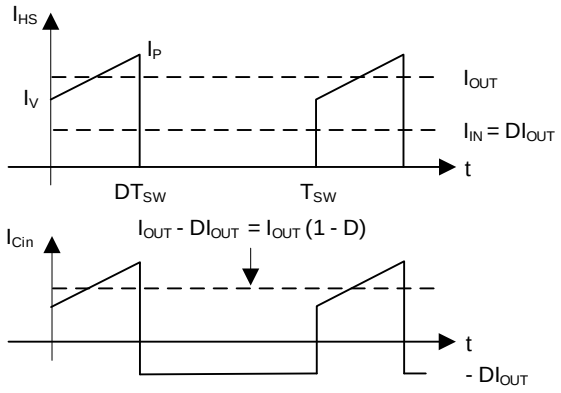


Figure 4 Root mean Square of I_{Cin}

High-quality MLCC, such as X5R or X7R, with capacitance greater than 20μF, is recommended for the input capacitor. The dielectric material of X5R and X7R behaves with less capacitance variation and fairly temperature stability. Voltage and current rating are also the key parameters to select a capacitor. Generally, selecting an input capacitor with a voltage rating 1.5 times greater than the maximum V_{IN} is a conservatively safe design. The input capacitor is used to supply the input RMS current, which can be approximately estimated using the following equations.

$$I_{Cin(rms)} = \sqrt{I_{HS(rms)}^2 - I_{IN}^2} = \sqrt{D(1\text{-}D) \times I_{OUT}^2 + \frac{\Delta I_L^2}{12}} \quad (7)$$

Assume, If the ΔI_L is small, it can be ignored

$$I_{Cin(rms)} = I_{OUT}\sqrt{D(1\text{-}D)} \quad (8)$$

The input capacitance also determines the V_{IN} ripple of the converter. The V_{IN} ripple can be approximately calculated by using the following equation:

$$\Delta V_{IN} = \frac{I_{OUT} \times D(1\text{-}D)}{C_{IN} \times F_{SW}} \quad (9)$$

Output Capacitor Selection

The output capacitor is required to maintain the V_{OUT} fairly steady. MLCC, POSCAP, KO–CAP, SP-Cap, or any lower ESR capacitors are recommended. V_{OUT} ripple voltage consists made up of the output capacitor's ESR and stored charge. These two ripple components are called ESR ripple and capacitive ripple. MLCC has extremely low ESR and relatively little capacitance, those components are similar in amplitude and have to be considered. The V_{OUT} ripple can be estimated using equation

$$V_{OUT\_Ripple(ESR)} = \Delta I_L \times ESR \quad (10)$$

$$V_{OUT\_Ripple(C)} = \frac{\Delta I_L}{8 \times C_{OUT} \times F_{SW}} \quad (11)$$

$$V_{OUT\_Ripple} = V_{OUT\_Ripple(ESR)} + V_{OUT\_Ripple(C)} \quad (12)$$

The $V_{OUT\_ripple(C)}$ phase legs behind from$\Delta\, i_c(t)$, the maximum and minimum of $V_{OUT\_ripple(C)}$ is justly at $\Delta\, i_c(t)$ = 0A. In some field applications, MLCC is fully instead of the low ESR capacitor, if the maximum V_{OUT_ripple} is at the middle of two LX pulses, the capacitive ripple dominates V_{OUT_ripple} in the case. V_{OUT_ripple} and $V_{OUT\_ripple(C)}$ are the same phase.

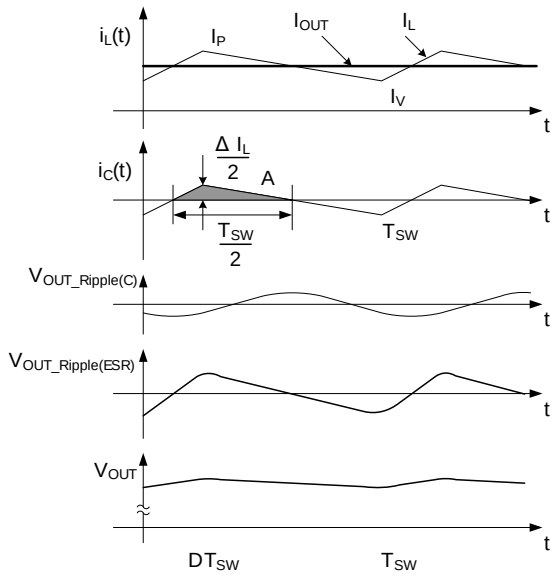


Figure 5 V_{OUT} Ripple Voltage

Gate Drivers(DH &DL)

In the low-duty factor application, like a notebook computer, there is a large difference between input and output voltage. Therefore, large low-side MOSFET and moderate-size high-side MOSFET are needed for high efficiency. The DH and DL drivers are optimized for driving high-side and low-side MOSFETs. A non-overlap control circuit is needed avoiding the DH and DL turning on simultaneously. The DL driver with a 0.7Ω pull low transistor helps prevent the DL from being coupled to high during the fast-rising time of the LX node, due to the drain to gate capacitive coupling of low-side synchronous-rectifier MOSFET. A resistor in series with the BST is recommended that will slow high-side MOSFET turn-on and then improve EMI ability.

V_{OUT} Overshoot and Undershoot Voltage

The V_{OUT} overshoot voltage usually occurs if there is a sudden and quick I_{OUT} from heavy load to light load. The inductor with a larger current keeps traveling the same direction, the only way for the inductor's current is to flow to the output capacitor (or releasing the stored energy of the inductor $LI^2/2$). This causes an enormous overshoot on the V_{OUT}, the overshoot voltage can be approximately calculated in the following equations, where VOS the overshoot voltage.

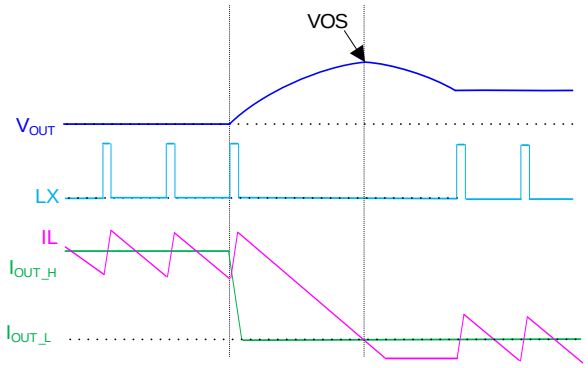


Figure 6 V_{OUT} Overshoot Voltage

$$VOS = \sqrt{\frac{L \times (I_{OUT\_H}^2 - I_{OUT\_L}^2)}{C_{OUT}} + V_{OUT}^2} \quad (13)$$

OR

$$VOS = \frac{L \times (I_{OUT\_H} - I_{OUT\_L})^2}{2 \times C_{OUT} \times V_{OUT}} + V_{OUT} \quad (14)$$

On the other hand, The V_{OUT} undershoot voltage is usually occurred by a heavy I_{OUT} is coming suddenly and quickly, the inductor's current is farthest small than the required I_{OUT}, the control logic uses the minimum Off-Time (t_{OFF_MIN}) operation to boost up the inductor's current pursuing the required I_{OUT}, However, it needs to take several LX pulses for inductor's current boosting to overtake I_{OUT}. In this duration, the output capacitor is discharging and supplying current for the suddenly and quickly heavy I_{OUT}. The undershoot voltage, VUS can be roughly estimated by the following equation (16). Where m is the number of LX pulses, choosing the closest an integer greater than or equal to a given number of the equation (15).

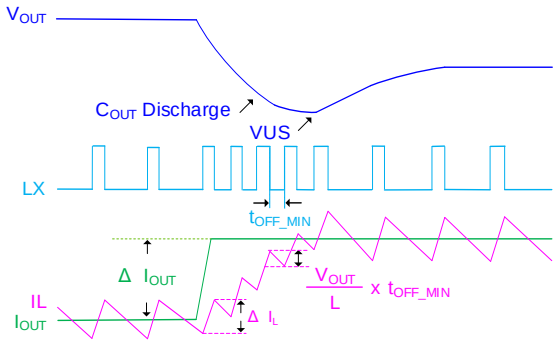


Figure 7 V_{OUT} undershoot Voltage

$$m = \text{Ceiling}\left(\frac{\Delta I_{OUT}}{\Delta I_L - \frac{V_{OUT}}{L} \times t_{OFF\_MIN}}\right) \quad (15)$$

$$VUS = V_{OUT} - \Delta I_{OUT}\left(ESR + \frac{(1+mD-D) \times T_{SW} + m \times t_{OFF\_MIN}}{2 \times C_{OUT}}\right) \quad (16)$$

Switching Frequency Setting

The G6201 provides 3 different levels of switching frequencies for flexible design. Table1 shows the voltage of FSWSEL for different switching frequencies.

Table 1 Switching Frequency

FSWSEL	Switching Frequency
> 4.5V	800 kHZ
Floating	600 kHz
< 0.4V	400 kHz

Output Voltage and 2-Bit VID Setting

The G6201 has embedded a 2-Bit VID for setting the output voltage which follows the Intel spec. Table 2 shows the VOUT voltage based on different 2-Bit VID setting. The VOUT also supports the dynamic voltage scale. VOUT will rise following a +17mV/μs slew rate when the 2-Bit VID binary counting up, and there are two methods for VOUT slewing down when the 2-Bit VID binary counting down, G6201A is slew rate controlled mode with VOUT falling rate of -17mV/μs and G6201 is Decay mode.

Table 2 VOUT Setting

VID1	VID0	VOUT
1	1	1.80
1	0	1.65
0	1	1.10
0	0	0

Load Line Droop Section

The G6201 also provides an external load line (droop) setting by a network shown in Figure 4. Due to the positive temperature coefficient of the copper wired inductor, temperature compensation is necessary for the lossless inductor current sense. For thermal compensation, an NTC Thermistor is used in the current sense network to compensate DCR variation via temperature changing. The DCR network equation is as follows.

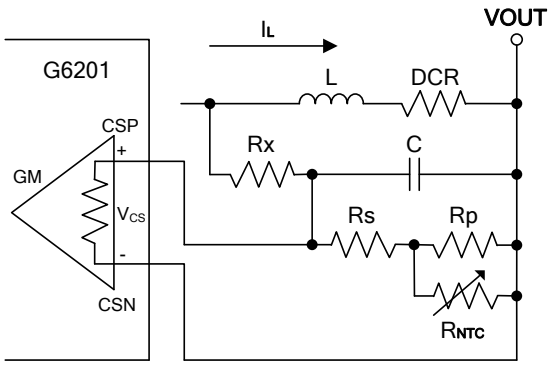


Figure 8 Cycle-By-Cycle Valley Current Detected Control

$$V_{CSP\text{-}CSN} = I_L \times DCR \times \frac{R_{EQ}}{R_X + R_{EQ}} \times \frac{1 + \frac{L}{DCR} S}{1 + \frac{R_X \times R_{EQ} \times C}{R_X + R_{EQ}} S} \quad (17)$$

$$R_{EQ} = R_S + \frac{R_P \times R_{NTC}}{C_P + R_{NTC}} \quad (18)$$

According to current sense network, the corresponding equation is represented as follows:

$$\text{If } \frac{L}{DCR} = \frac{R_X \times R_{EQ} \times C}{R_X + R_{EQ}} \quad (19)$$

$$V_{CSP\text{-}CSN} = I_L \times DCR \times \frac{R_{EQ}}{R_X + R_{EQ}} \quad (20)$$

If DCR network time constant matches inductor time constant, L/DCR, an expected transient waveform can be designed. The droop set equation as follows:

$$V_{DROOP} = (I_L \times DCR \times \frac{R_{EQ}}{R_X + R_{EQ}}) \times 8 \quad (21)$$

$$R_{DCLL} = \frac{V_{DROOP}}{I_L} = DCR \times \frac{R_{EQ}}{R_X + R_{EQ}} \times 8 \quad (22)$$

Where, 8 is an internal parameter of the G6201.
The V_{OUT} droop is equal to $V_{CSP\text{-}CSN}$ times 8.

PGOOD

The G6201 has an open drain and needs an external pull up resistor for the power good indicator. When VFB is high than 90% of regulated voltage, PGOOD will be pulled high by the external pull up resistor. If VFB drops lower than 84% of regulated voltage, PGOOD will be pulled low by the internal NMOS. Please keep PGOOD pull up voltage is lower than VCC.

Over Voltage Protection (OVP)

The G6201 built the V_{OUT} over voltage protection function. If the V_{OUT} becomes higher than 2.2V for 5us, the OVP comparator output goes high, and the V_{OUT} will be discharged and latched.

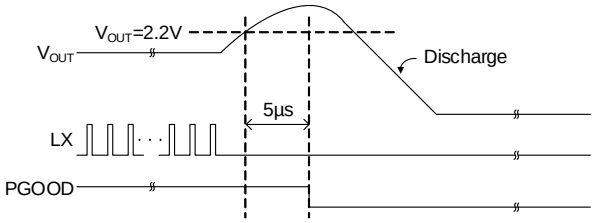


Figure 9 Over Voltage Protection

Under Voltage Protection (UVP)

The G6201 also built the V_{OUT} under voltage protection function. If the V_{OUT} becomes lower than 68%*V_{OUT} for 2us, the UVP comparator output goes high, and the V_{OUT} will be discharged and latched.

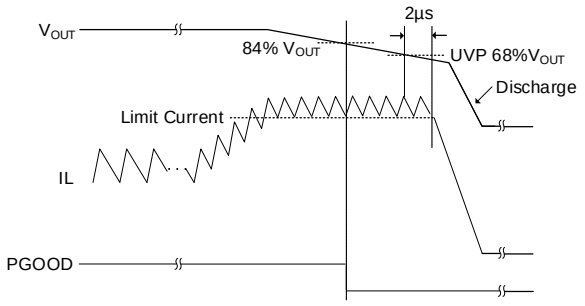


Figure 10 Under Voltage Protection

Over Temperature Protection (OTP)

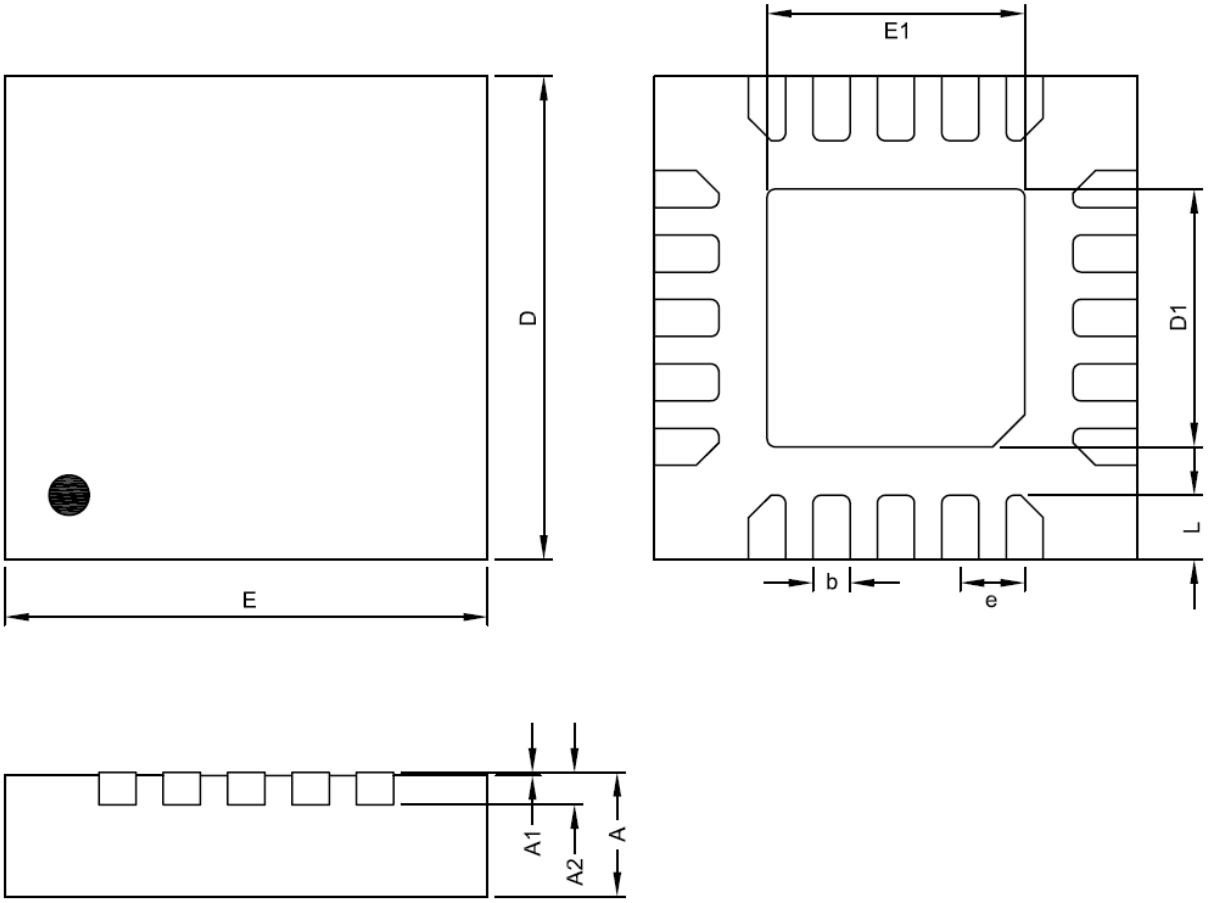
The over temperature protection function of the G6201 is built inside to prevent overheat damage. If the die temperature is over 150°C, the OTP function activates and makes all power rails shutdown.

Layout Considerations

The PCB layout and placement are very important in high frequency switching converter design. An Efficient PCB layout is critical for the optimal performance of the G6201. For best results, the following guidelines should be strictly followed

1. Place the high-current paths(GND, IN, and LX) very close to the power devices(MOSFETs and Inductor) with short, direct, and wide traces or polygons to reduce stray inductance. Keep the switching node (LX) short and away from the network of VOUT, CSP, CSN, and TRIP.
2. Place the input capacitors as close to VSYS and GND as possible on the same layer as the G6201. Connect output capacitors and also as close to the output pin as possible.
3. Connect between the gate drivers and the respective gate of the high-side or the low-side MOSFET should be as short as possible.
4. Place BST resistor and capacitor with IC at the same layer, close to BST and LX plane, larger than 15 mil width trace is recommended to reduce line parasitic inductance.
5. Connect a low-pass RC filter from VCC, (1µF to 10µF is recommended). Place the filter capacitor close to the IC.
6. All the sensitive analog traces and components, such as VOUT, RGND, CSP, CSN, FSWSEL, and TRIP should be routed away from high voltage switching nodes such as LX, DH, DL, and BST to prevent coupling.
7. Current sense connections must always be made by the Kelvin connections to ensure an accurate signal.

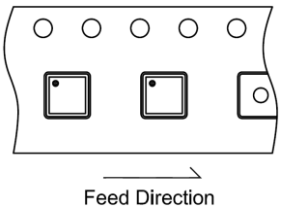
Package Information



TQFN3X3-20 Package

Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.0276	0.0295	0.0315
A1	0.00	---	0.05	0.0000	---	0.0020
A2	0.20 REF			0.0079 REF		
D	2.95	3.00	3.05	0.1161	0.1181	0.1201
E	2.95	3.00	3.05	0.1161	0.1181	0.1201
D1	1.45	1.60	1.75	0.0571	0.0630	0.0689
E1	1.45	1.60	1.75	0.0571	0.0630	0.0689
b	0.15	0.20	0.25	0.0059	0.0079	0.0098
e	0.40 BSC			0.0157 BSC		
L	0.35	0.40	0.45	0.0138	0.0157	0.0177

Taping Specification



PACKAGE	Q'TY/REEL
TQFN3X3-20	3,000 ea