M2068

3-Channel Half-Bridge Driver

Features

- **5V to 26V VDD**
- **±5.3A Peak Current Output**
- **Up to 1MHz PWM Frequency**
- **Protected Integrated Power 0.13Ω Switches**
- **10nS Switch Dead Time**
- **All Switches Current Limited**
- **Internal Under-Voltage Protection**
- **Internal Thermal Protection**
- **Short-Circuit Protection**
- **Fault Output Flag**

General Description

The M2068 is a 3-channel half-bridge driver IC intended to drive a 3-phase brushless DC motor.

The M2068 features a low-current shutdown mode, standby mode, input under-voltage protection, current limit, thermal shutdown, and fault flag signal output. All channels of the drivers interface with standard logic signals.

The M2068 is available in a 40 lead QFN 5mm x 5mm package.

Applications

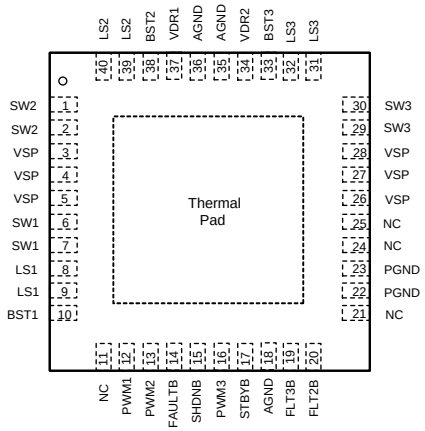
- **3-Phase BLDC Motor Drive**

Ordering Information

ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE (Green)
M2068QK1U	2068	0°C to +85°C	QFN5X5-40

Note:QK: QFN5X5-40
1: Bonding Code
U: Tube & Reel
Green : Lead Free / Halogen Free.

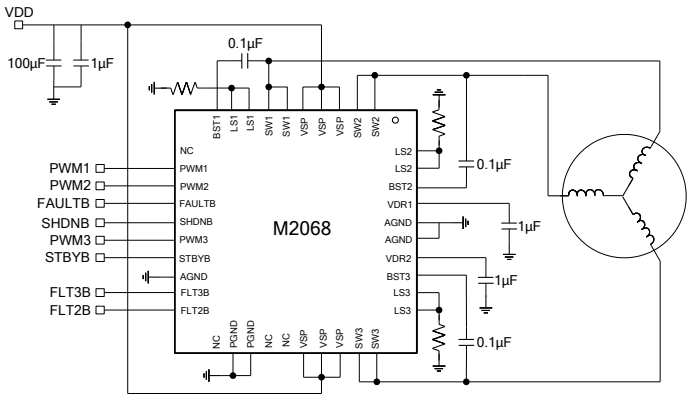
Pin Configuration



M2068 QFN5X5-40

Note: Recommend connecting the Thermal Pad to the Ground for excellent power dissipation

Typical Application Circuit



Absolute Maximum Ratings

VSP 28V
SWx Voltage . . . . . .-0.3V to VSP+0.3V
BSTx-SWx . . . . . -0.3V to 6V
Voltage at All Other Pins . . . . . .-0.3V to 6V
Thermal Resistance of Junction to Ambient (θ_{JA})
QFN5X5-40 . . . . . TBD°C/W
Continuous Power Dissipation (T_A = +25°C)
QFN5X5-40. . . . . TBDmW
Junction Temperature . . . . . 150°C
Storage Temperature . . . . . .-55°C to 150°C
Reflow Temperature (soldering, 10sec) . . . . . 260°C
ESD Susceptibility (HBM) 2kV

Recommend Operating Range

Input operating voltage (VSP) . . . . . 5V to 26V
Junction temperature (T_J) . . . . . .-40°C to 125°C

Electrical Characteristics

(V_{SP}=12V, V_{SHDNB}=5V, T_A=25°C)

The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
VSP Operating Current	I_{VSP}	I_{LOAD}=0A, PWM_X=0	---	1.2	1.5	mA
VSP Shutdown Current	I_Q	V_{SHDN}=0V	---	20	25	μA
Operating VSP Threshold Low	$VIL_{\_VSP}$		3.7	4	---	V
Operating VSP Threshold High	$VIH_{\_VSP}$		---	4.4	4.8	V
STBYB Threshold Low	$VIL_{\_STBYB}$		0.8	1.0	---	V
STBYB Threshold High	$VIH_{\_STBYB}$		---	1.6	1.8	V
SHDNB Threshold Low	$VIL_{\_SHDNB}$		0.8	1.0	---	V
SHDNB Threshold High	$VIH_{\_SHDNB}$		---	1.6	1.8	V
PWMx Input Bias Current			---	0.1	1.0	μA
PWMx Threshold Low	$VIL_{\_PWM}$		0.8	1.0	---	V
PWMx Threshold High	$VIH_{\_PWM}$		---	1.6	1.8	V
SWx On Resistance	$R_{ds(on)}$	VSP=12V, High-side and Low-side	---	0.13	---	Ω
SWx Current Limit	$Ilimit_{\_SW}$	V_{PWM} =0V, Sinking	---	5.3	---	A
		V_{PWM} =5V, Sourcing	---	5.3	---	A
SWx Switching Frequency	$FSW_{\_SW}$	V_{PWM} =0 to 5V, 50% Duty Cycle	---	---	1	MHz
BSTx Voltage UVLO	$UVLO_{\_BST}$	Falling Value	---	2.4	---	V
BSTx Current	I_{BST}	High-side MOSFET ON , V_{BST} – V_{SW} =5.5V	---	10	---	μA
SWx Rise/Fall Time	$t_{\_R/F}$	V_{PWM} =0V to 5V	---	10	---	nS
Minimum PWM Pulse Width	$t_{\_PULSE}$	V_{PWM} =0V to 5V, High or Low Pulse	---	30	---	nS
Dead Time		I_{OUT} = ±100mA	---	10	---	nS
PWMx to SWx Delay Time Rising	$t_{\_RD}$	V_{PWM} =0V to 5V	---	30	---	nS
PWMx to SWx Delay Time Falling	$t_{\_FD}$	V_{PWM} =5V to 0V	---	30	---	nS
Thermal Shutdown Temperature	T_{TRIP}	T_J Rising	---	160	---	°C
Thermal Shutdown Hysteresis	T_{HYST}		---	40	---	°C

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Note 2: θJA is measured in the natural convection at TA = 25°C on a four-layer Silergy Evaluation Board.

Note 3: The device is not guaranteed to function outside its operating conditions.

Pin Description

Pin NO.	Symbol	Description
1,2	SW2	Output 2. SW2 is valid approximately 100μs after VSP goes high.
3,4,5	VSP	Power Supply Input. Connect VSP to the positive side of the input power supply. Bypass VSP to PGND as close to the IC as possible.
6,7	SW1	Output 1. SW1 is valid approximately 100μs after VSP goes high.
8,9	LS1	Low-Side Source Connection of SW1.
10	BST1	Bootstrap Supply. BST1 powers the high-side gate of the SW1 stage. Connect a capacitor (0.1μF or greater) between BST1 and SW1.
11	NC	No Connection. NC must be kept floating.
12	PWM1	Driver Logic Input 1. Drive PWM1 with the signal that controls SW1. Drive PWM high to turn on the high-side switch ; drive PWM low to turn on the low-side switch.
13	PWM2	Driver Logic Input 2. Drive PWM2 with the signal that controls SW2. Drive PWM high to turn on the high-side switch ; drive PWM low to turn on the low-side switch.
14	FAULTB	Fault Output. A low output at FAULTB indicates that the M2068 has detected an over temperature or over-current condition. FAULTB is an open-drain output.
15	SHDNB	Shutdown Input. When SHDNB is low, the IC shuts off.
16	PWM3	Driver Logic Input 3. Drive PWM3 with the signal that controls SW3. Drive PWM high to turn on the high-side switch ; drive PWM low to turn on the low-side switch.
17	STBYB	Standby Input. Default low (internal pull-down). If driven high, the output of the driver is determined by PWM1/2/3. If driven low, all outputs are high impedance.
18	AGND	Analog Ground.
19	FLT3B	Fault Monitor. For details see the “Fault Output” section. FLT3B is an open-drain output.
20	FLT2B	Fault Monitor. For details see the “Fault Output” section. FLT2B is an open-drain output.
21	NC	No Connection. NC must be kept floating.
22,23	PGND	Power Ground. Connect the exposed pad on the bottom side to ground plane.
24,25	NC	No Connection. NC must be kept floating.
26,27,28	VSP	Power Supply Input. Connect VSP to the positive side of the input power supply. Bypass VSP to PGND as close to the IC as possible.
29,30	SW3	Output 3. SW3 is valid approximately 100μs after VSP goes high.
31,32	LS3	Low-Side Source Connection of SW3.
33	BST3	Bootstrap Supply. BST3 powers the high-side gate of the SW3 stage. Connect a capacitor (0.1μF or greater) between BST3 and SW3.
34	VDR2	Gate Drive Supply Bypass. The voltage at VDR2 is supplied from an internal regulator from VSP. VDR2 powers the internal MOSFET gate drive for the SW1/2/3 output stage. Bypass VDR2 to PGND with a 0.1μF to 10μF capacitor.
35,36	AGND	Analog Ground.
37	VDR1	Analog Supply Input. The voltage at VDR1 is supplied from an internal regulator from VSP. VDR1 powers the internal analog circuitry for the 3-channel stage. Bypass VDR1 to AGND with a 0.1μF to 10μF capacitor.
38	BST2	Bootstrap Supply. BST2 powers the high-side gate of the SW2 stage. Connect a capacitor (0.1μF or greater) between BST2 and SW2.
39,40	LS2	Low-Side Source Connection of SW2.

Block Diagram

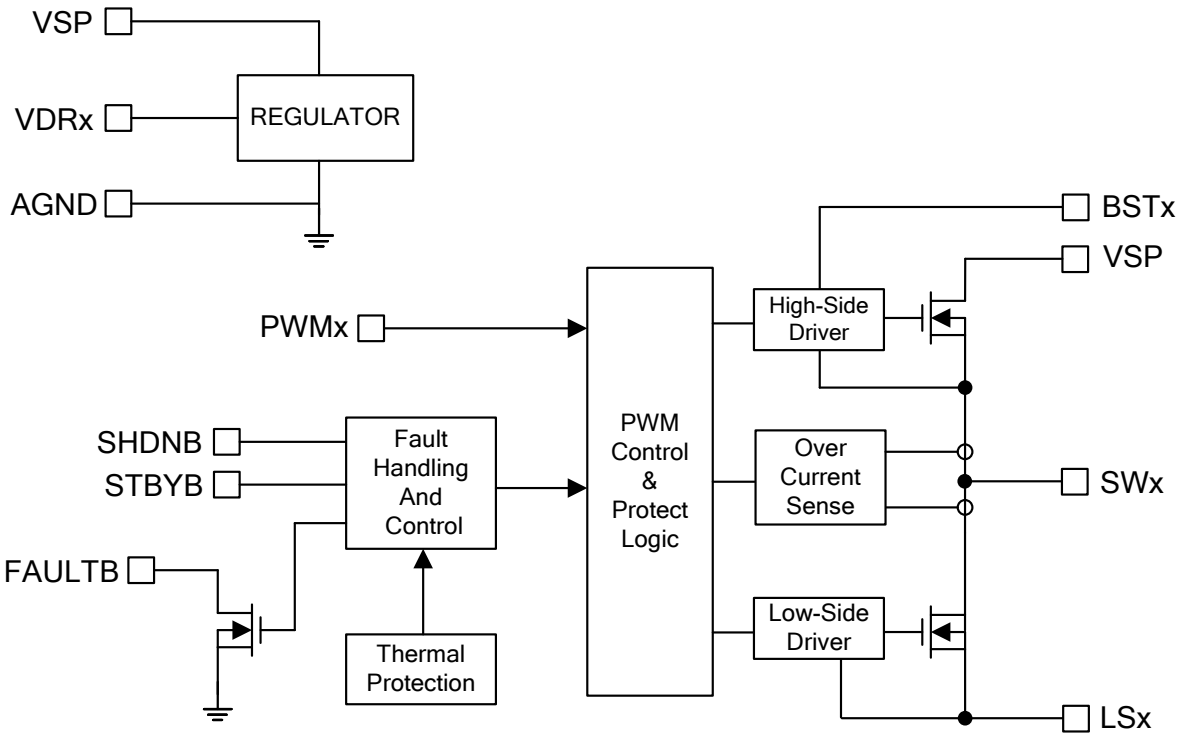


Figure1. Function Block Diagram (1 Half-Bridge Channel Only)

OPERATION

The M2068 is a 3-channel half-bridge driver intended to dive a brushless DC motor. The output is in phase with the input, and the dead time is optimized for symmetrical performance, regardless of load conditions.

When SHDNB is low, all channels are off. When STBYB is pulled low, it causes the outputs of all the channels to go into high impedance. However, when the voltage across BST1/2/3 and SW1/2/3 drops low significantly, the bottom MOSFET is turned on to refresh the external bootstrap capacitor. Connecting a capacitor (0.1μF or greater) between BST and SW (as the bootstrap capacitor) is recommended.

In order to prevent erratic operation, two under voltage lockout (UVLO) circuits are used. One ensures that the supply for the bottom gate drive circuit is sufficiently high, and the other is for the top gate driver.

Fault Protection

To protect the power MOSFETs, an internal current limit of 5.5A is set for all MOSFETs. When this limit is reached, all MOSFETs of the over-current bridge channel will go into high impedance for a fixed duration (35μS approximately) before resuming normal operation.

Thermal monitoring is integrated into the M2068. If the die temperature rises above 160°C, all switches are turned off. The temperature must fall below 125°C before normal operation resumes.

To enhance the robustness of the device under a short-circuit condition, a capacitor can be connected to FAULTB (see Fig. 2). The time constant of the RC must be greater than 50mS for the FAULTB node to reach 2V. Under a short-circuit condition, the FAULTB node re-sets to zero, and the part is placed in standby mode until the voltage at STBYB is above 2V.

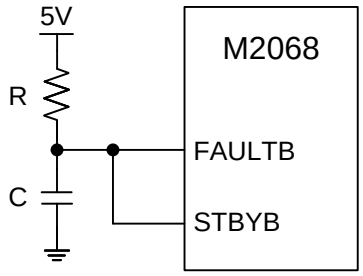


Figure 2. Fault Protection Enhancement Circuit

Fault Output

The M2068 includes an open drain, active-low fault indicator output (FAULTB). A fault is indicated if one of the following conditions is detected:

1. The current limit is tripped
2. Thermal shutdown is tripped.

A fault on any channel causes FAULTB to pull low. Once the fault is removed, the M2068 resumes normal operation.

Do not apply more than 6V to FAULTB.

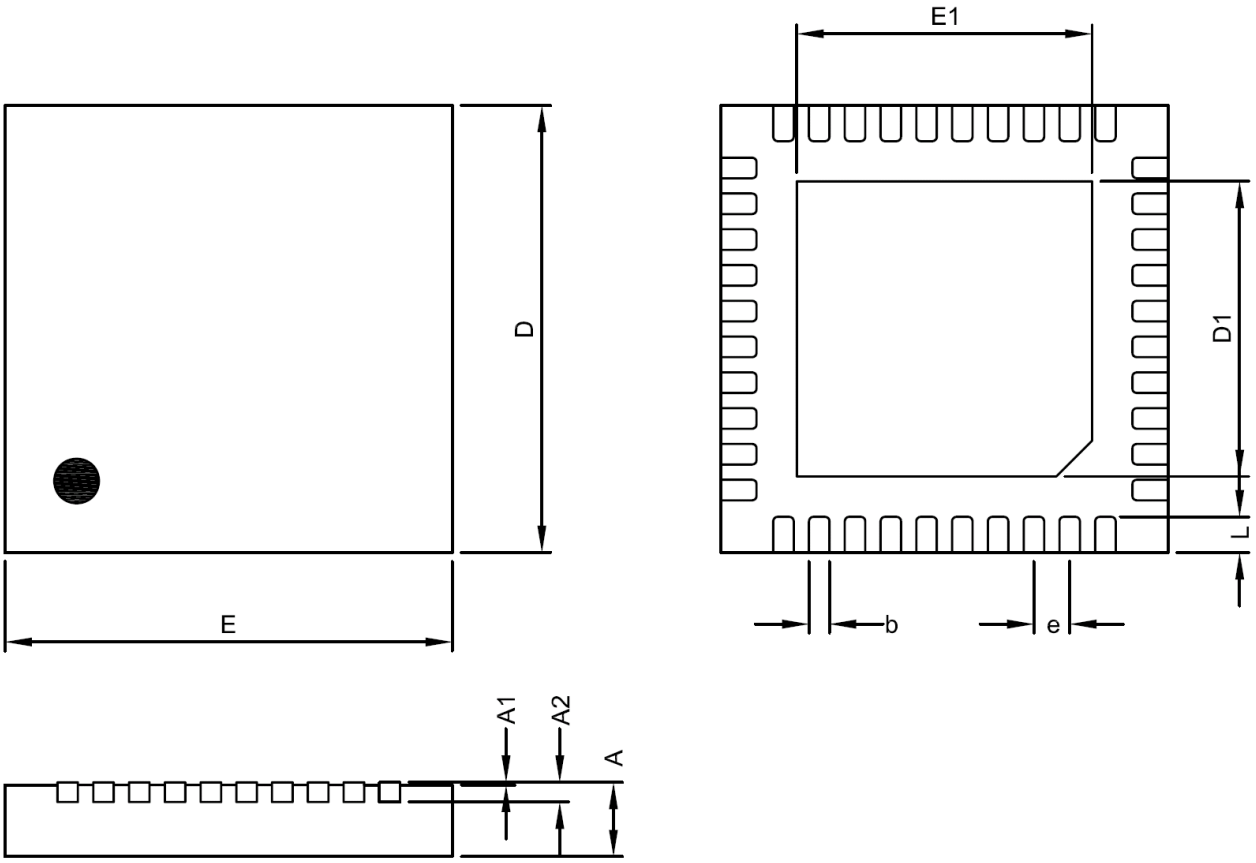
Error Reporting

The M2068 has two fault monitor pins (FLT3B and FLT2B), which are active low open-drain outputs. They provide protection-mode signaling to a PWM controller or another system control device (see Table 1).

Table1. Fault Output Logic

OCP	OTP	UVP	FLTB2	FLTB3
0	0	0	1	1
0	0	1	0	1
0	1	0	1	0
1	0	0	0	0

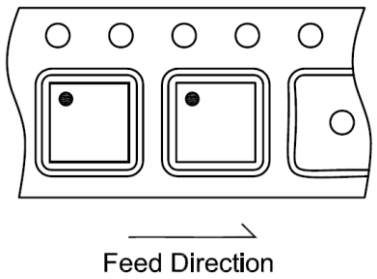
Package Information



QFN5X5-40 Package

Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.90	1.00	0.0315	0.0354	0.0394
A1	0.00	- - -	0.05	0.0000	- - -	0.0020
A2	0.20 REF			0.0079 REF		
D	4.95	5.00	5.05	0.1949	0.1969	0.1988
E	4.95	5.00	5.05	0.1949	0.1969	0.1988
D1	3.20	3.30	3.40	0.1260	0.1299	0.1339
E1	3.20	3.30	3.40	0.1260	0.1299	0.1339
b	0.15	0.20	0.25	0.0059	0.0079	0.0098
e	0.40 BSC			0.0157 BSC		
L	0.35	0.40	0.45	0.0138	0.0157	0.0177

Taping Specification



PACKAGE	Q'TY/REEL
MSOP-8	3,000 ea