

3.5A, 1.5MHz, COT Synchronous Step-Down Converter

Features

- Efficiency Up to 95%
- 90mΩ and 70mΩ Internal Power MOSFET
- V_{IN} Range 2.6V to 5.5V
- Power Save Mode for Light Load Efficiency
- Constant-On-Time Control Scheme Design for Fast Transient Response, Stability with MLCC Output Capacitor
- 100% Duty Cycle for Lowest Dropout
- 17μA Operating Quiescent Current
- Fixed Soft-Start 0.8ms
- Output Discharge
- Power Good Output
- Cycle-by-Cycle Over Current Protection
- Input Under Voltage Lockout
- Output Under Voltage Protection (Hiccup)
- Thermal Shutdown Protection

Applications

- Portable and Mobile Devices
- Wireless and Networking Devices
- LCD TV Power Supply
- Solid State Drive

General Description

The M2293 is a monolithic, step-down, switch mode converter with built-in internal power MOSFETs. It achieves 3.5A continuous output current from a 2.6V to 5.5V input voltage with excellent load and line regulation. The Output voltage can be regulated to 0.9V or 0.8V by setting DVFS high or low. At medium to heavy loads, the switching frequency is 1.5MHz. At light load, the device automatically enters PSM to maintain high efficiency.

The Constant-On-Time control scheme in M2293 provides fast transient response to be optimized over a wide range of loads and output capacitors. Thermal shutdown and cycle-by-cycle current limiting are used for protection.

The M2293 is available in TDFN2X2-8 package.

Ordering Information

ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE (Green)
M2293RC1U	2293	-40°C to +85°C	TDFN2X2-8

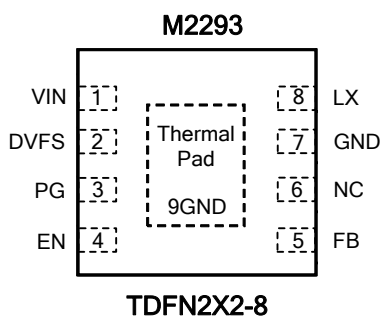
Note: RC: TDFN2X2-8

1: Bonding Code

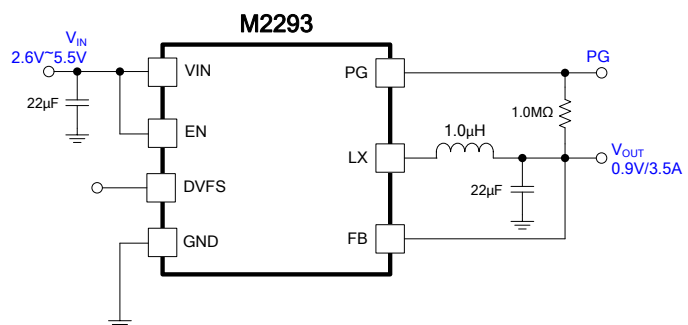
U : Tape & Reel

Green: Lead Free / Halogen Free

Pin Configuration



Typical Application Circuit



Absolute Maximum Ratings

VIN, LX, FB -0.3V to 6V
 EN -0.3V to (VIN+0.3V)
 LX (AC, less than 10nS) -3V to 10V
 Thermal Resistance of Junction to Ambient, (θ_{JA})
 TDFN2X2-8. 71.5°C/W
 Continuous Power Dissipation ($T_A = +25^\circ\text{C}$)
 TDFN2X2-8. 1.75W
 Thermal Resistance of Junction to Ambient, (θ_{JC})
 TDFN2X2-8. 8°C/W
 Junction Temperature -40°C to 150°C

Storage Temperature -65°C to 150°C
 Reflow Temperature (soldering, 10sec) 260°C
 ESD (HBM) 2KV

Recommended Operating Conditions

Supply Input Voltage. 2.6V to 5.5V
 Ambient Temperature Range. -40°C to 85°C
 Junction Temperature Range. -40°C to 125°C

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(VIN=5V, TA=25°C)

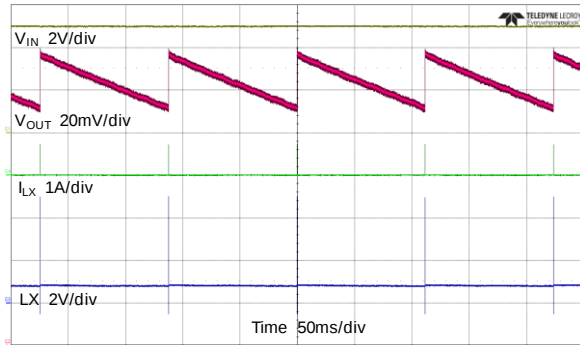
The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage	VIN		2.6	---	5.5	V
VIN Quiescent Current	IQ	No load, device not switching	---	17	27	μA
VIN Shutdown Current	ISD	VEN=0V, Shutdown	---	---	1	μA
VIN Under Voltage Lockout Threshold	VUVLO	VIN falling	---	2.4	2.5	V
VIN Under Voltage Lockout Hysteresis	VUVLO_HYS		---	100	---	mV
Thermal Shutdown Threshold	TJSD	TJ rising	---	150	---	°C
Thermal Shutdown Hysteresis	TJSD_HYS		---	30	---	°C
EN Input Logic High Voltage	VIH	2.6V ≤ VIN ≤ 5.5V	1.2	---	---	V
EN Input Logic Low Voltage	VIL	2.6V ≤ VIN ≤ 5.5V	---	---	0.4	V
EN Input Leakage Current	IEN	VEN=5V	---	---	0.1	μA
DVFS Input Logic High Voltage	VDVFSH	2.6V ≤ VIN ≤ 5.5V	1.2	---	---	V
DVFS Input Logic Low Voltage	VDVFSL	2.6V ≤ VIN ≤ 5.5V	---	---	0.4	V
DVFS Internal Pull-Low Resistance	RDVFS	2.6V ≤ VIN ≤ 5.5V	---	400	---	kΩ
Soft-Start Time	TSS	Time from EN high to 95% of VOUT nominal	---	0.8	1	mS
Power Good Threshold	VPG_R	VOUT rising, referenced to VOUT nominal	---	95	---	%
	VPG_F	VOUT falling, referenced to VOUT nominal	---	90	---	%
PG Low-Level Output Voltage	VPG(OL)	ISINK=1mA	---	---	0.4	V
PG Input Leakage Current	IPG(LK)	VPG=5V	---	---	0.1	μA
Power Good Delay	tPG_DLY	VFB falling	---	40	---	μS
Feedback Voltage	VFB	2.6V ≤ VIN ≤ 5.5V, VFB=0.8V/0.9V, IOUT=1A	-1.5	0	1.5	%
Feedback Leakage Current	IFB(LK)	VFB=0.9V	---	3	---	μA
Output discharge FET ON Resistance	RDIS	VEN=0V	---	10	---	Ω
Switching Frequency	fSW	IOUT=1A	---	1.5	---	MHz
Minimum Off Time	tOFF(MIN)	High side PFET	---	80	---	nS
PFET Switch ON Resistance	RDSON(P)	VIN=3.6V	---	90	---	mΩ
NFET Switch ON Resistance	RDSON(N)	VIN=3.6V	---	70	---	mΩ
PFET Switch Current Limit	ILIM(P)		---	6.5	---	A
NFET Switch Current Limit	ILIM(N)		---	4.5	---	A

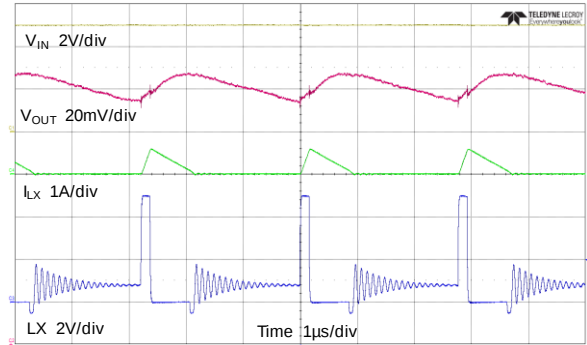
Typical Performance Characteristics

$V_{IN}=5V$, $V_{OUT}=0.9V$, $C_{IN}=22\mu F$, $C_{OUT}=22\mu F$, $L=1\mu H$, $T_A=25^\circ C$

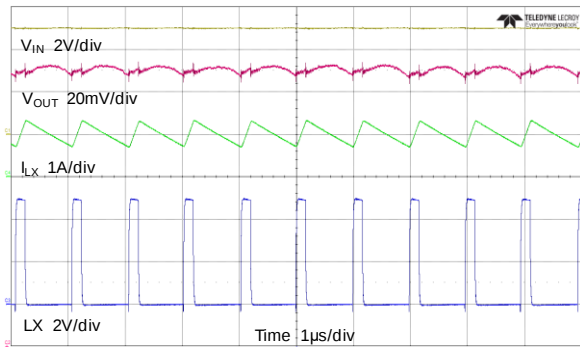
Steady State Operation
 $V_{OUT}=0.8V$, No Load



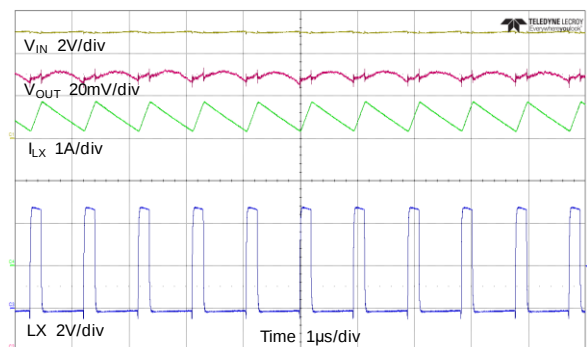
Steady State Operation
 $V_{OUT}=0.8V$, $I_{OUT}=100mA$



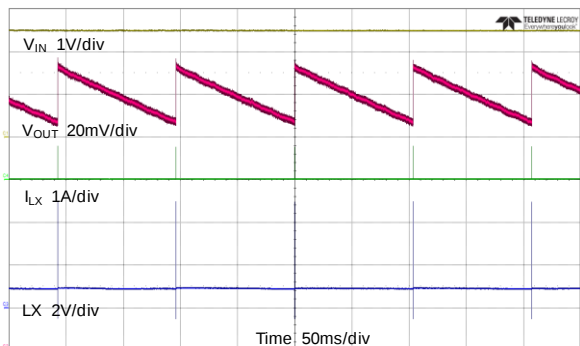
Steady State Operation
 $V_{OUT}=0.8V$, $I_{OUT}=1A$



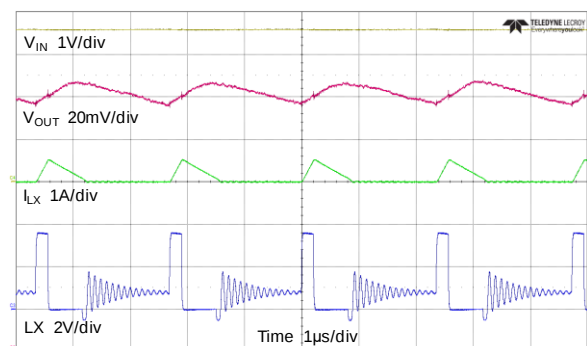
Steady State Operation
 $V_{OUT}=0.8V$, $I_{OUT}=3.5A$



Steady State Operation
 $V_{IN}=3.6V$, $V_{OUT}=0.8V$, No Load

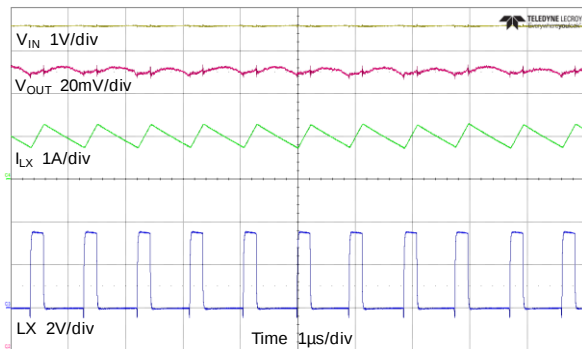


Steady State Operation
 $V_{IN}=3.6V$, $V_{OUT}=0.8V$, $I_{OUT}=100mA$

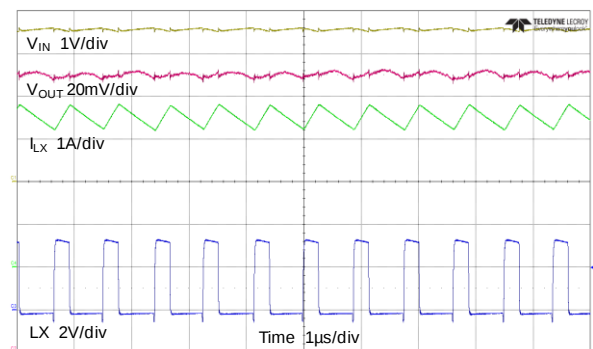


Typical Performance Characteristics (continued)

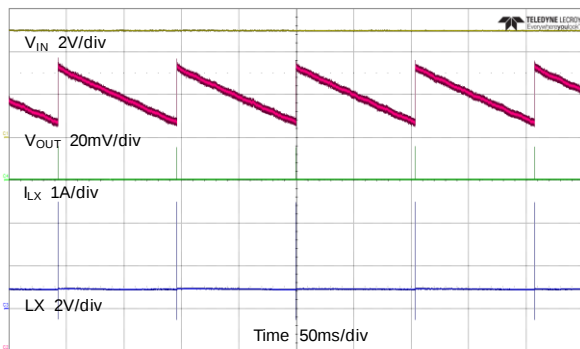
Steady State Operation
 $V_{IN}=3.6V$, $V_{OUT}=0.8V$, $I_{OUT}=1A$



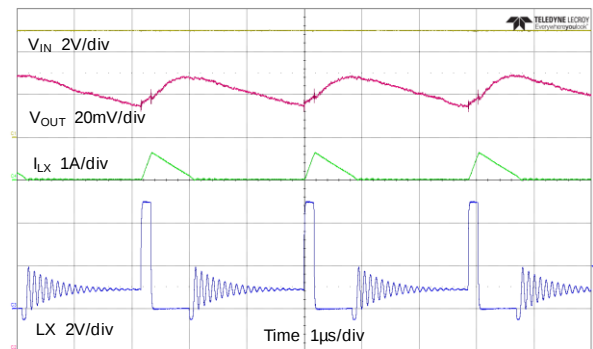
Steady State Operation
 $V_{IN}=3.6V$, $V_{OUT}=0.8V$, $I_{OUT}=3.5A$



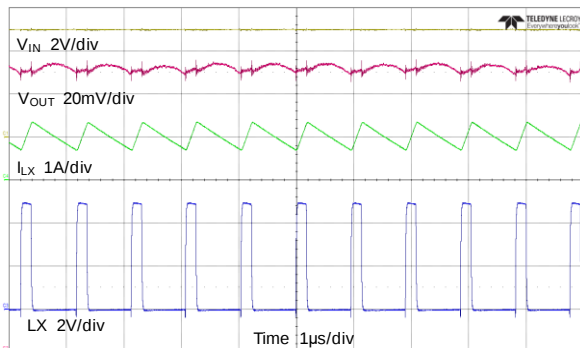
Steady State Operation
 $V_{OUT}=0.9V$, No Load



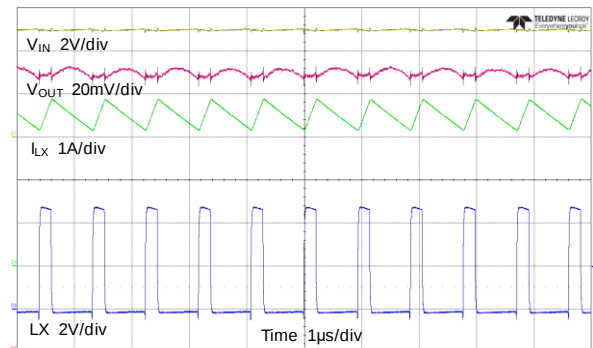
Steady State Operation
 $V_{OUT}=0.9V$, $I_{OUT}=100mA$



Steady State Operation
 $V_{OUT}=0.9V$, $I_{OUT}=1A$

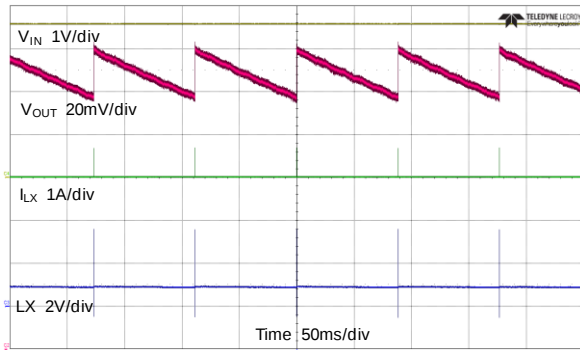


Steady State Operation
 $V_{OUT}=0.9V$, $I_{OUT}=3.5A$

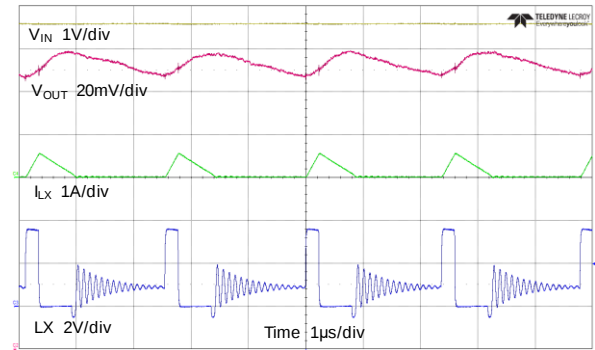


Typical Performance Characteristics (continued)

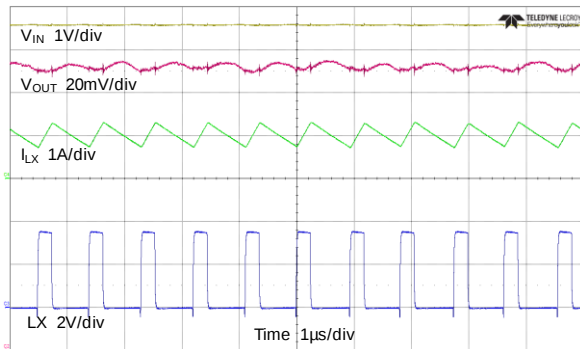
Steady State Operation
 $V_{IN}=3.6V, V_{OUT}=0.9V$, No Load



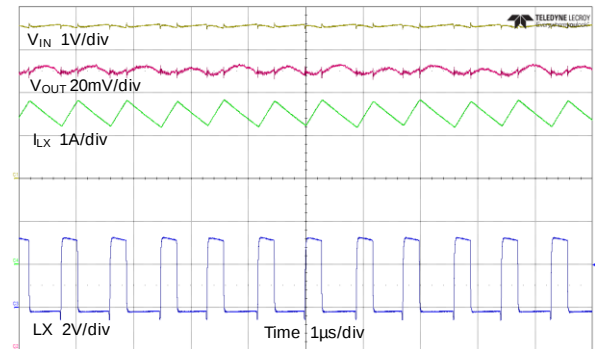
Steady State Operation
 $V_{IN}=3.6V, V_{OUT}=0.9V, I_{OUT}=100mA$



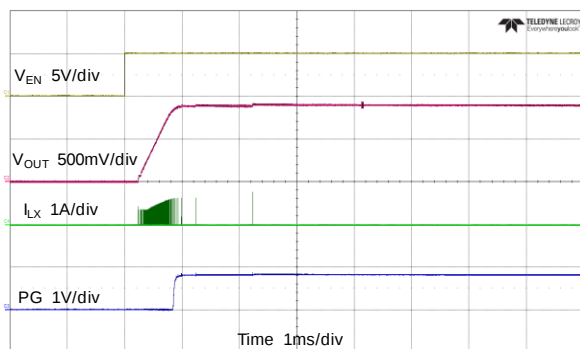
Steady State Operation
 $V_{IN}=3.6V, V_{OUT}=0.9V, I_{OUT}=1A$



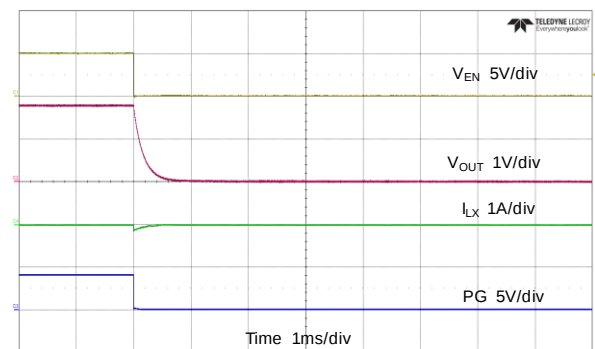
Steady State Operation
 $V_{IN}=3.6V, V_{OUT}=0.9V, I_{OUT}=3.5A$



Start-up Through Enable
 $V_{OUT}=0.9V$, No Load

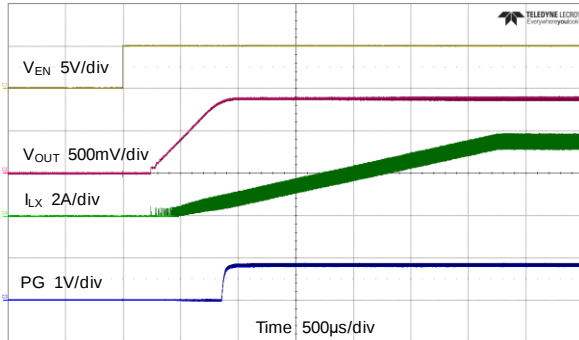


Start-down Through Enable
 $V_{OUT}=0.9V$, No Load

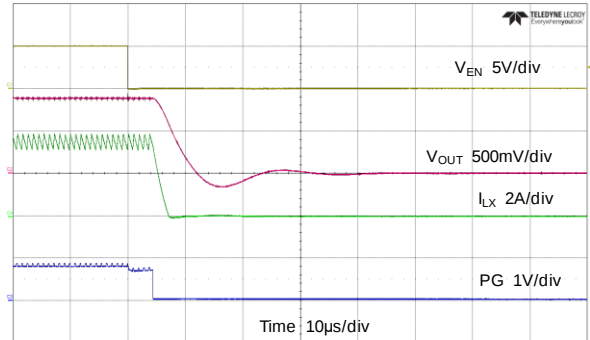


Typical Performance Characteristics (continued)

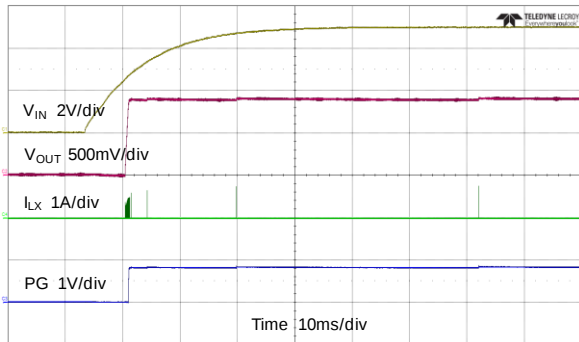
Start-up Through Enable
 $V_{OUT}=0.9V$, $I_{OUT}=3.5A$



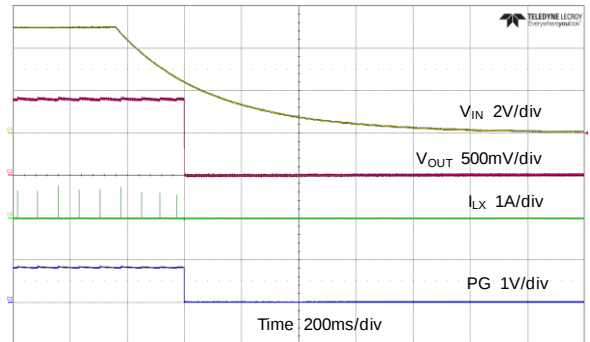
Start-down Through Enable
 $V_{OUT}=0.9V$, $I_{OUT}=3.5A$



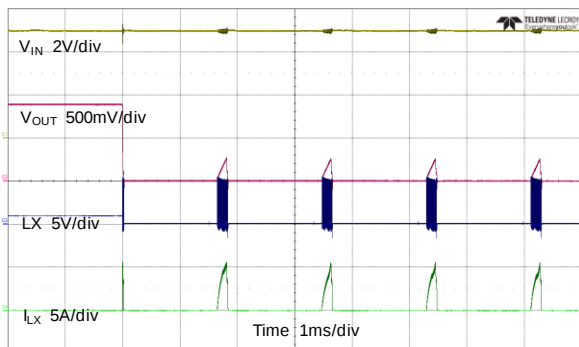
Start-up Through VIN
 $V_{OUT}=0.9V$, No Load



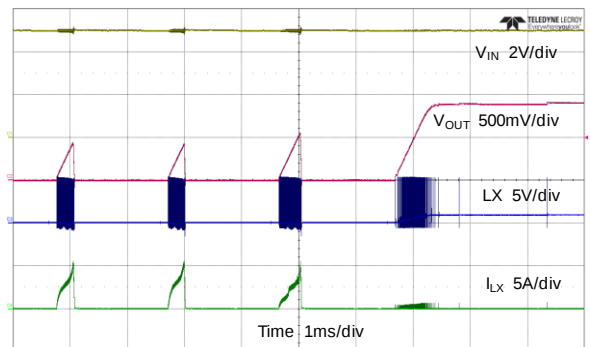
Start-down Through VIN
 $V_{OUT}=0.9V$, No Load



Short Circuit waveform
 $V_{OUT}=0.9V$

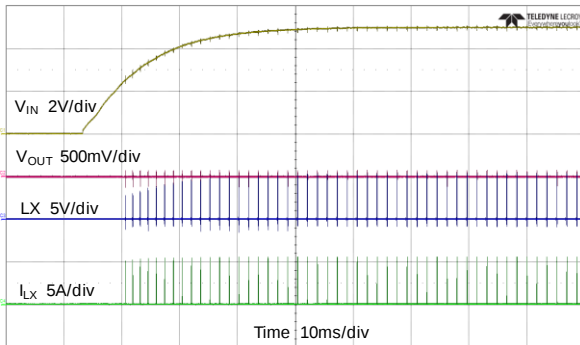


Short Circuit Recovery
 $V_{OUT}=0.9V$

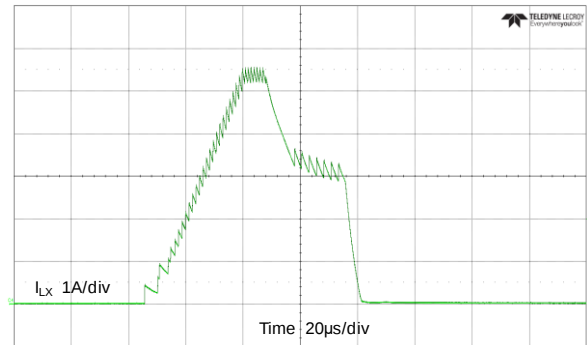


Typical Performance Characteristics (continued)

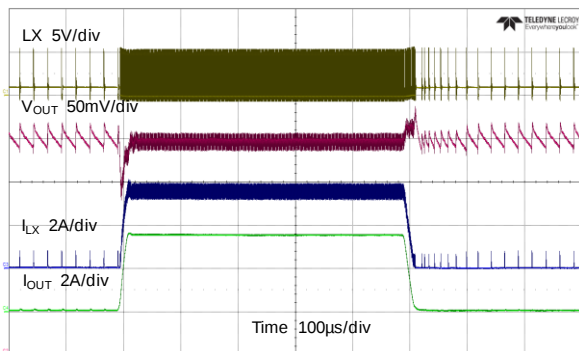
Short Circuit waveform
 $V_{OUT}=0.9V$



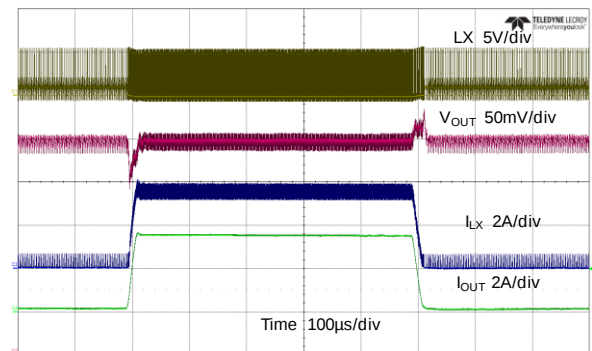
Current Limit
 $V_{OUT}=0.9V$



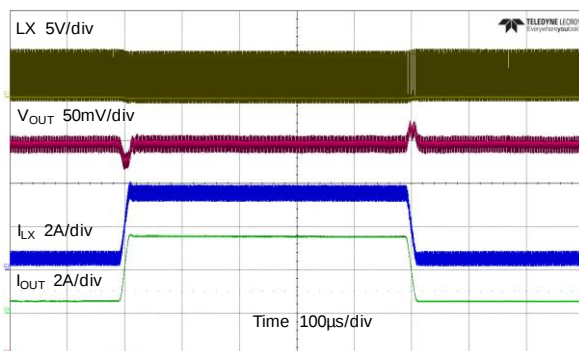
Load Transient Response
 $V_{OUT}=0.9V$, $I_{OUT}=0mA \sim 3.5A$



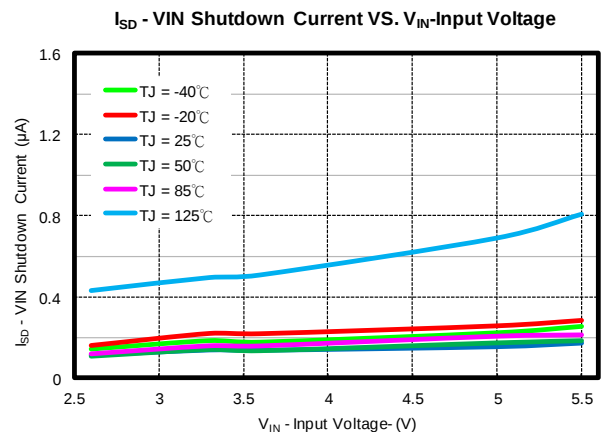
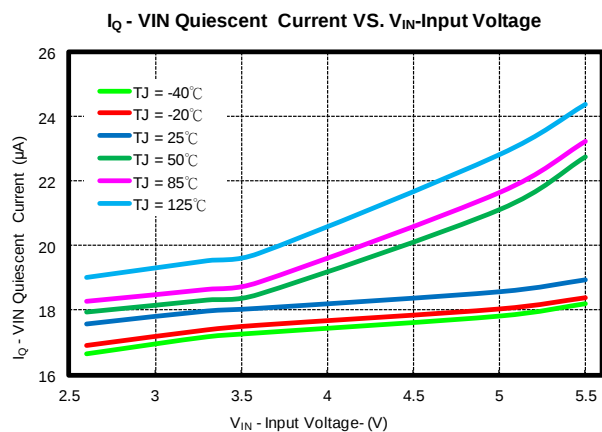
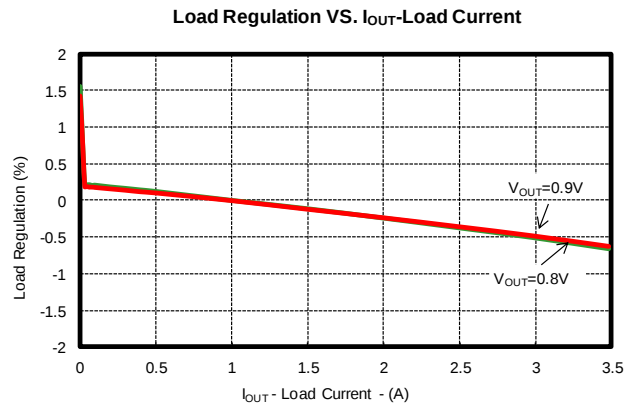
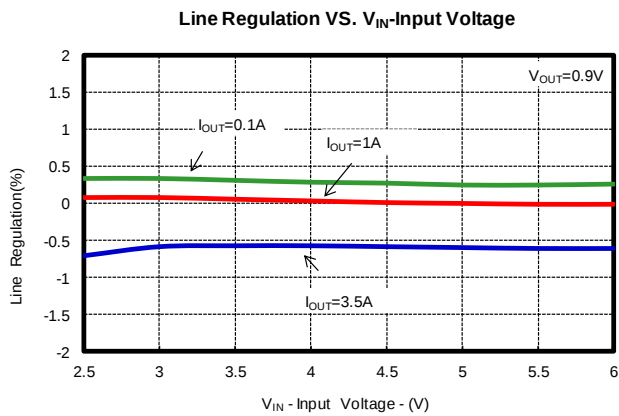
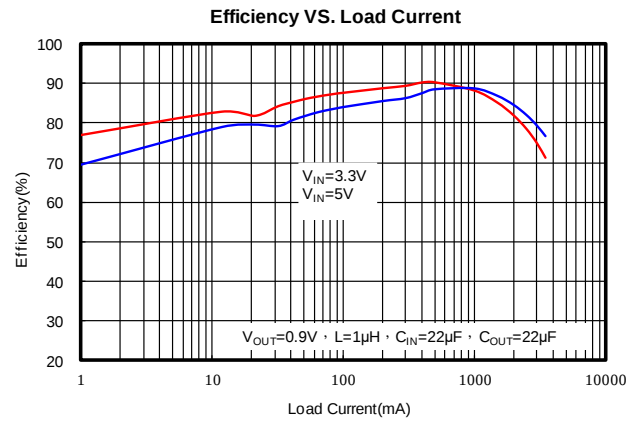
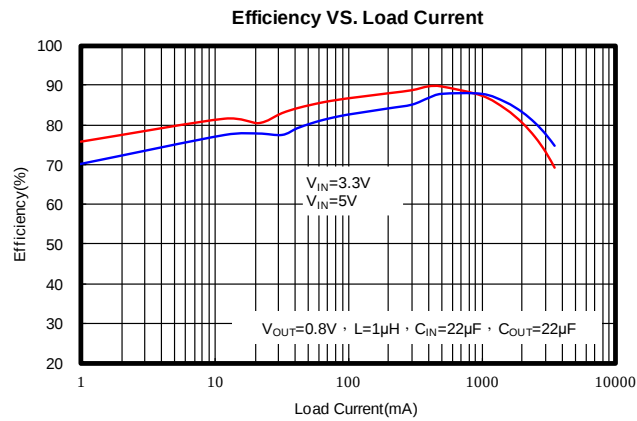
Load Transient Response
 $V_{OUT}=0.9V$, $I_{OUT}=100mA \sim 3.5A$



Load Transient Response
 $V_{OUT}=0.9V$, $I_{OUT}=500mA \sim 3.5A$



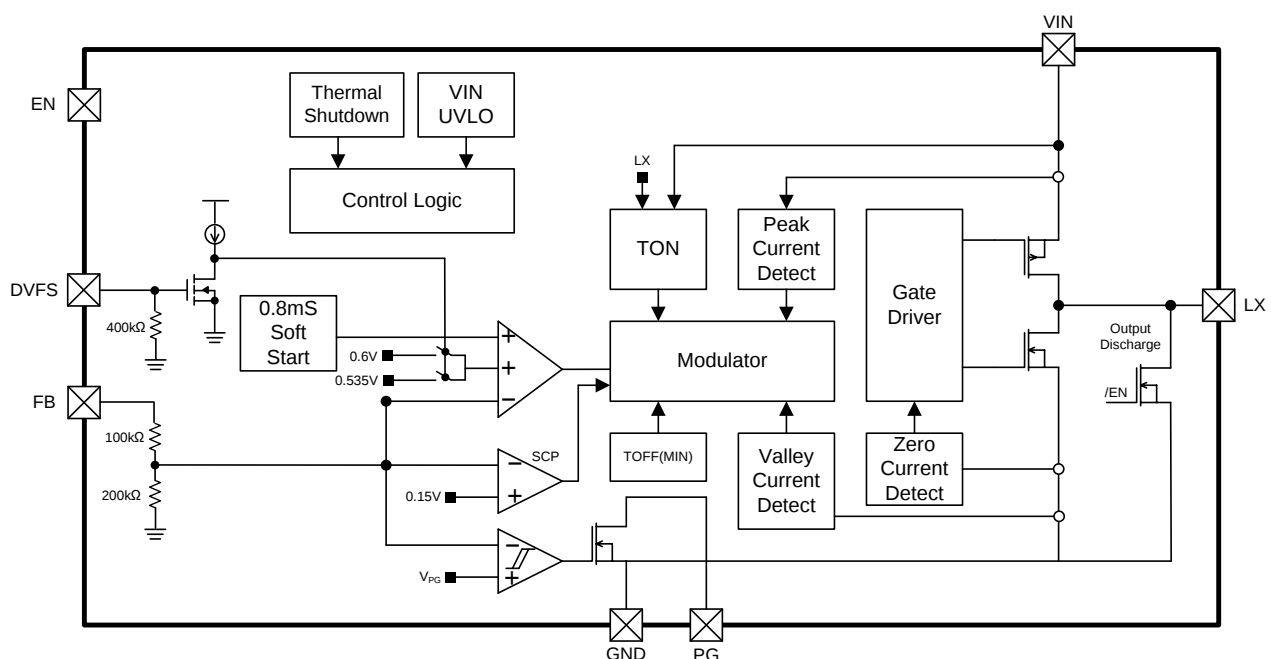
Typical Performance Characteristics (continued)



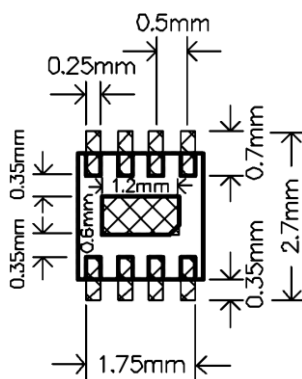
Pin Description

PIN No	NAME	FUNCTION
1	VIN	Supply Voltage Input.
2	DVFS	Pull this pin high/low to set $V_{REF}=0.6V/0.533V$ to output 0.9V/0.8V, respectively.
3	PG	Power good open drain output pin. The pull-up resistor cannot be connected to any voltage higher than 5.5V. If unused, leave it floating.
4	EN	Enable Control Input. Do not leave this pin floating.
5	FB	Input senses pin for the output voltage. An internal resistor divider for output to GND.
6	NC	No connection.
7	GND	Ground.
8	LX	Switch Node.
9	GND	Ground. Thermal PAD. Do not leave this pin floating.

Block Diagram



Minimum Footprint PCB Layout Section

TDFN2X2-8

Operation

The M2293 is a high efficiency synchronous step-down DC/DC converter. By setting DVFS to low or high, M2293 provides an adjustable regulated output voltage 0.8V or 0.9V while delivering up to 3.5A of output current with input voltage from 2.6V to 5.5V.

The M2293 uses the constant on-time control scheme. In normal operation, the high side P-MOSFET is turned on when the switch controller is set by the comparator and is turned off when the Ton comparator resets the switch controller.

Low side MOSFET current is measured. The error amplifier adjusts COMP voltage by comparing inner the feedback signal from VFB the output voltage with the internal 0.6V/0.533V reference. When the load current increases, it causes a drop in the feedback voltage relative to the reference, then the COMP voltage rises to allow higher inductor current to match the load current.

Enable

When the input voltage is greater than the under voltage lockout threshold, a logic-high (>1.2V) enables the converter; a logic-low (<0.4V) forces the IC into shutdown mode. Do not leave this pin floating. When the device is disabled, there is a resistive discharge path from LX pin.

Soft-Start (SS)

There is an internal built-in soft-start to ramp the output voltage at a fixed slew rate to avoid in-rush current. The typical soft-start time is 0.8ms.

Application Information

The M2293 is a single-phase step-down converter. It provides single feedback loop, constant on-time control with fast transient response. An internal 0.6V reference allows the output voltage to be precisely regulated for low output voltage applications and internal compensation are integrated to minimize external component count. Protection features include over current protection, under voltage protection and over temperature protection.

DVFS Setting for Output Voltage

There is an internal pull-low 400k-Ohm-resistor at the DVFS pin to GND to set the initial 0.8V for the output voltage. When DVFS pin is set high, V_{OUT} is 0.9V (typ.). The output voltage will be back to 0.8V with setting DVFS low again. The output voltage slew rate is well-controlled less than 8mV/us.

Chip Enable and Disable

The EN pin allows for power sequencing between

the controller bias voltage and another voltage rail.

The M2293 remains in shutdown if the EN pin is lower than 400mV. When the EN pin rises above the VEN trip point, the M2293 begins a new initialization and soft-start cycle.

Internal Soft-Start

The M2293 provides an internal soft-start function to prevent large inrush current and output voltage overshoot when the converter starts up. The soft-start (SS) automatically begins once the chip is enabled. During soft-start, the internal soft-start capacitor becomes charged and generates a linear ramping up voltage across the capacitor. This voltage clamps the voltage at the FB pin, causing PWM pulse width to increase slowly and in turn reduce the input surge current. The internal reference takes over the loop control once the internal ramping-up voltage becomes higher than internal reference.

UVLO Protection

The M2293 has input Under Voltage Lockout protection (UVLO). If the input voltage exceeds the UVLO rising threshold voltage (2.5V typ.), the converter resets and prepares the PWM for operation. If the input voltage falls below the UVLO falling threshold voltage during normal operation, the device will stop switching. The UVLO rising and falling threshold voltage has a hysteresis to prevent noise-caused reset.

Inductor Selection The switching frequency (on-time) and operating point (% ripple or LIR) determine the inductor value as shown below :

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{f_{SW} \times LIR \times I_{LOAD(MAX)} \times V_{IN}}$$

where LIR is the ratio of the peak-to-peak ripple current to the average inductor current. Find a low loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. The core must be large enough not to saturate at the peak inductor current (I_{PEAK}) :

$$I_{PEAK} = I_{LOAD(MAX)} + \left(\frac{LIR}{2} \times I_{LOAD(MAX)} \right)$$

The calculation above serves as a general reference. To further improve transient response, the output inductor can be further reduced. This relation should be considered along with the selection of the output capacitor. Inductor saturation current should be chosen over IC's current limit.

Input Capacitor Selection

High quality ceramic input decoupling capacitor, such as X5R or X7R, with values greater than 10uF are recommended for the input capacitor. The X5R and X7R ceramic capacitors are usually selected for power regulator capacitors because the dielectric material has less capacitance variation and more temperature stability. For most applications, a 10uF capacitor is sufficient. Higher output voltages may require a 22uF capacitor to increase system stability.

Voltage rating and current rating are the key parameters when selecting an input capacitor. Generally, selecting an input capacitor with voltage rating 1.5 times greater than the maximum input voltage is a conservatively safe design.

The input capacitor is used to supply the input RMS current, which can be approximately calculated using the following equation:

$$I_{IN_RMS} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The next step is selecting a proper capacitor for RMS current rating. One good design uses more than one capacitor with low equivalent series resistance (ESR) in parallel to form a capacitor bank.

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be approximately calculated using the following equation:

$$\Delta V_{IN} = \frac{I_{OUT(MAX)}}{C_{IN} \times f_{SW}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Output Capacitor Selection

The output capacitor and the inductor form a low pass filter in the Buck topology. In steady state condition, the ripple current flowing into/out of the capacitor results in ripple voltage. The output voltage ripple (VP-P) can be calculated by the following equation:

$$V_{P_P} = LIR \times I_{LOAD(MAX)} \times \left(ESR + \frac{1}{8 \times C_{OUT} \times f_{SW}}\right)$$

When load transient occurs, the output capacitor supplies the load current before the controller can respond. Therefore, the ESR will dominate the output voltage sag during load transient. The output voltage undershoot (VSAG) can be calculated by the following equation:

$$V_{SAG} = \Delta I_{LOAD} \times ESR$$

For a given output voltage sag specification, the ESR value can be determined.

Another parameter that has influence on the output voltage sag is the equivalent series inductance (ESL). The rapid change in load current results in di/dt during transient. Therefore, the ESL contributes to part of the voltage sag. Using a capacitor with low ESL can obtain better transient performance. Generally, using several capacitors connected in parallel can have better transient performance than using a single capacitor for the same total ESR. An output capacitor higher than 22uF is required to increase system stability for lower output voltage applications.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding air-flow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA} , is layout dependent. The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA} .

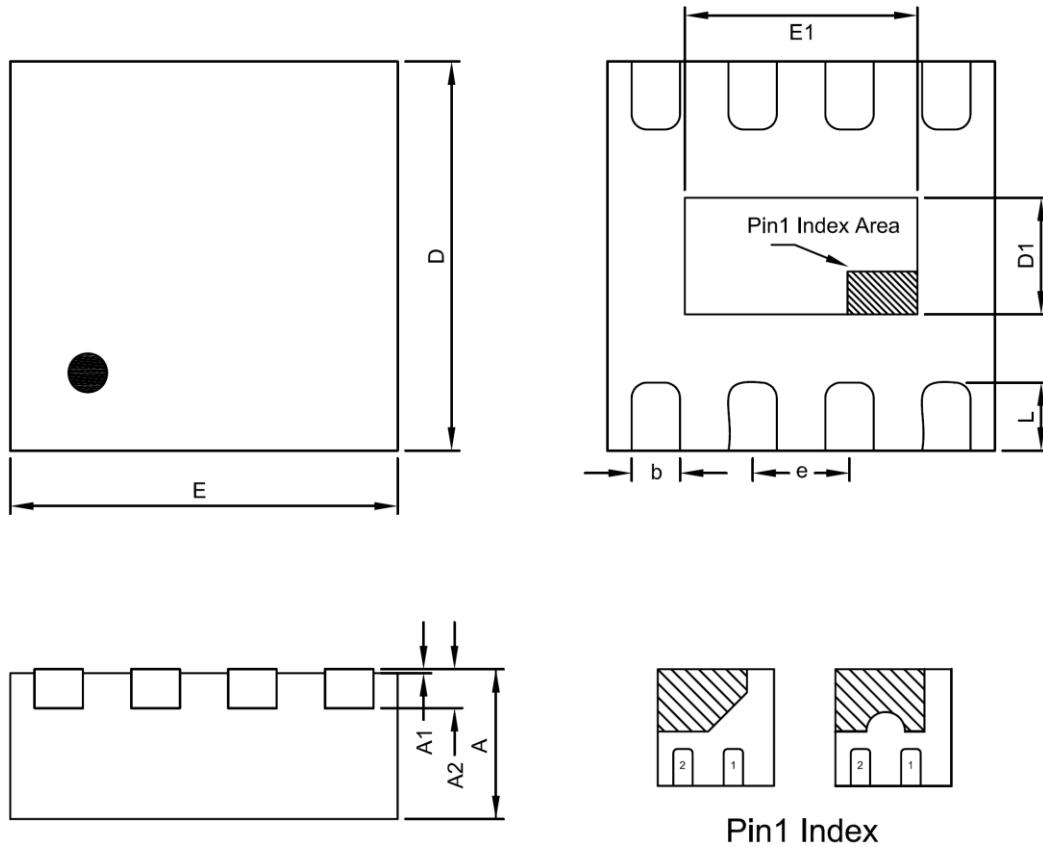
Layout Consideration**1. Component Placement:**

- Place input capacitors as close as possible to VIN.
- Place the feedback resistors and compensation components as close as possible to the IC.

2. Layout Recommendation

- To prevent electromagnetic interference (EMI) problems and reduce voltage ripple of the device, any high current copper trace which see high frequency switching should be optimized.
- Therefore, use short and wide traces for power current paths and for power ground tracks, power plane and ground plane are recommended if possible.
- It is important to minimize the area of the switching nodes and use the ground plane under them to minimize crosstalk to sensitive signals and ICs.
- It's suggested to keep as complete of a ground plane under M2293 if possible.
- It is always good practice to keep the sensitive tracks such as feedback connection (FB) away from switching signal connections (LX).

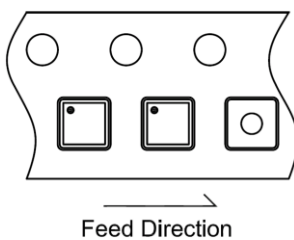
Package Information



TDFN2X2-8 Package

Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.0276	0.0295	0.0315
A1	0.00	---	0.05	0.0000	---	0.0020
A2	0.20 REF			0.0079 REF		
D	1.95	2.00	2.05	0.0768	0.0787	0.0807
E	1.95	2.00	2.05	0.0768	0.0787	0.0807
D1	0.55	0.65	0.75	0.0217	0.0256	0.0295
E1	1.15	1.25	1.35	0.0453	0.0492	0.0531
b	0.18	0.25	0.30	0.0071	0.0098	0.0118
e	0.50 BSC			0.0197 BSC		
L	0.30	0.35	0.40	0.0118	0.0138	0.0157

Taping Specification



PACKAGE	Q'TY/REEL
TDFN2X2-8	3,000 ea

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