7-bit Programmable VCOM Reference with Integrated Nonvolatile Memory

Features

- Integrated Nonvolatile Memory to Store VCOM Setting
- 100 Programming Times
- I^2C Interface
- 7-Bit, Adjustable Sink-Current Device
- Resistor-Adjustable, Full-Scale Range
- 2.5V to 3.6V Logic Supply Range
- 7V to 18V Analog Supply Range
- Protections:
  - Over Current Protection (OCP)
  - Over Temperature Protection (OTP)
- TDFN3X3-8 Package
- RoHS Compliant

General Description

The G1625 provides a programmable reference voltage for TFT-LCD panel VCOM adjustment. A 7-bit digital-to-analog converter (DAC) detects current from an external resistor-divider to create the VCOM reference voltage. This voltage is used as the input to a high current drive voltage buffer.

G1625 includes one time programmable (OTP) memory to store the DAC code on the chip, eliminating the need for external EEPROM. The chip supports up to 100 write operations to OTP memory. G1625 has an I^2C interface to set the VCOM reference voltage and write into OTP memory.

Applications

- TFT-LCD Panels

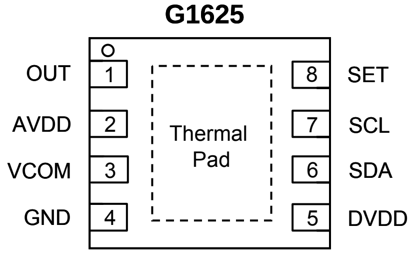
Ordering Information

ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE (Green)
G1625RD1U	DS961	-40°C to +85°C	TDFN 3X3-8

Note: RD: TDFN3X3-8
1: Bonding Code
U: Tape & Reel
Green : Lead Free / Halogen Free.

Pin Configuration

G1625



TDFN3X3-8

Absolute Maximum Ratings

Supply Voltage
DVDD, SET, SCL, and SDA to GND. . . . .-0.3V to +4V
AVDD to GND . . . . -0.3V to +20V
OUT to GND . . . . -0.3V to +20V
VCOM to GND . . . . -0.3V to AVDD + 0.3V
Continuous Current
SDA 10mA
VCOM . . . . ±100mA
Continuous Power Dissipation (TA = +70°C)
8-Pin TDFN-EP (derate 18.5 mW/°C above +70°C)
Single-Layer Board 1480mW
8-Pin TDFN-EP (derate 24.4 mW/°C above +70°C)
Multilayer Board . . . . 1952 mW
Thermal Resistance Junction to Ambient, (θ_{JA})
TDFN3X3-8 . . . . 28°C/W
Thermal Resistance Junction to Case, (θ_{JC})
TDFN3X3-8 . . . . 3°C/W
Operating Temperature Range . . . . -40°C to 85°C
Junction Temperature . . . . 150°C
Storage Temperature Range . . . .-65°C to 150°C
Reflow Temperature (soldering, 10s) . . . . 260°C

Electrical Characteristics

(VDVDD = 3.3V, VAVDD = 16V, VGND = 0, RSET = 6.8kΩ, no load, T_A = 25°C, unless otherwise noted. (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLIES						
Digital Supply Voltage Range	VDVDD		2.5	3.3	3.6	V
Analog Supply Voltage Range	VAVDD		7	12	18	V
DVDD Under Voltage Luckout	VUVLO	Rising	2.0	2.1	2.2	V
		Hysteresis	---	0.2	---	
Analog Quiescent Current	IAVDD		---	1.45	2	mA
Analog Supply Current Range for Programming OTP	IAVDD	TA = +25°C	---	7	7.5	mA
		TA = +85°C	---	---	15	mA
Digital Quiescent Current	IDVDD		---	150	250	µA
OTP Programming Times	OTPSET		---	---	100	
VCOM OUTPUT (VCOM)						
Common-Mode Range			0.2	---	VAVDD - 0.2	V
Total Output Error	VERR	TA = +25°C, VVCOM from 2V to AVDD-2V	-22	---	22	mV
Output Voltage Swing Low	V_{OL}	I_L = -5mA, V_{OUT} = 0	---	---	200	mV
Output Voltage Swing High	V_{OH}	I_L = +5mA, V_{OUT} = V_{AVDD}	V_{AVDD} - 310	---	---	mV
Output Load Regulation	LR	I_L = -80mA to +80mA	---	± 0.25	---	mV/mA
Short-Circuit Current (Note 2)	ISC	VCOM = AVDD	150	270	350	mA
		VCOM = GND	150	240	350	
Power-Supply Rejection Ratio	PSRR	8V ≤ V_{AVDD} ≤ 20V, V_{OUT} = 5V	75	---	---	dB
Slew Rate	SR	4V_{P-P} at VCOM, 10% to 90%, R_L = 10kΩ, C_L = 20pF	---	23	---	V/µs
Bandwidth	dB	R_L = 10kΩ, C_L = 20pF, VCOM = 100mV_{P-P}	---	20.5	---	MHz
DVR						
OUT Voltage Range	VOUT		VSET +0.5V	---	18	V
Resolution	RES		7	---	---	Bits
Integral Nonlinearity Error	INL		---	0.125	---	LSB
Differential Nonlinearity Error	DNL		---	0.125	---	LSB
AVDD to VSET Ratio	AVDD/VSET		---	20:1	---	V/V
Set External Resistance	RSET	AVDD = 8V	3.35	---	67	kΩ
		AVDD = 18V	6.75	---	135	
Set Current	ISET	Through RSET (Note 5)	---	59.74	134	µA
Set Zero-Scale Error	SETZSE		---	---	±2	LSB
Set Full-Scale Error	SETFSE		---	---	±4	LSB

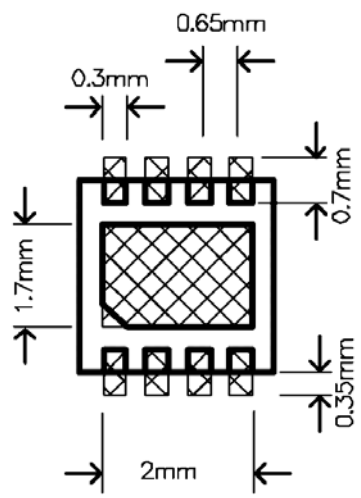
Electrical Characteristics

(VDVDD = 3.3V, VAVDD = 16V, VGND = 0, RSET = 6.8kΩ, no load, TA = 25°C, unless otherwise noted. (Note 1)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
LOGIC INPUTS (SDA, SCL)						
Input High Voltage	VIH		0.7 x DVDD	---	---	V
Input Low Voltage	VIL		---	---	0.3 x DVDD	V
SDA Output Low Voltage	VOL	ISINK = 6mA	---	---	0.4	V
Input Leakage Current	IIH, IIL	0V or DVDD	-3	0.01	+3	μA
Input Capacitance			---	5	---	pF
I2C TIMING CHARCTERISTICS						
Serial-Clock Frequency	fSCL		0	---	400	kHz
Bus Free Time Between STOP and START Conditions	tBUF		1.3	---	---	μs
Hold Time START Condition	tHD,STA		0.6	---	---	μs
SCL Pulse-Width Low	tLOW		1.3	---	---	μs
SCL Pulse-Width High	tHIGH		0.6	---	---	μs
Setup Time for a START Condition	tSU,STA		0.6	---	---	μs
Data Hold Time	tHD,DAT		0	---	900	ns
Data Setup Time	tSU,DAT	(Note 3)	100	---	---	ns
SDA and SCL Receiving Rise Time	tR	(Note 4)	20 + 0.1CB	---	300	ns
SDA and SCL Receiving Fall Time	tF	(Note 4)	20 + 0.1CB	---	300	ns
SDA Transmitting Fall Time	tF	(Note 4)	20 + 0.1CB	---	250	ns
Bus Capacitance	CB		---	---	400	pF
Pulse Width of Suppressed Spike	tSP		0	---	50	ns

Note 1: All devices are 100% production tested at T_A = +25°C. Specifications over temperature limits are guaranteed by design.
Note 2: Short-circuit current is for a 1μs pulsed current only, not to exceed thermal characteristics of package.
Note 3: Data hold time is tested in receive mode only.
Note 4: C_B is in pF.
Note 5: A typical current of 59.74μA is calculated using the AVDD = 16V and RSET = 6.8kΩ. Refer to “RSET Resistor” on page 6.
Note 6: Simulated and determined via design and NOT directly tested.

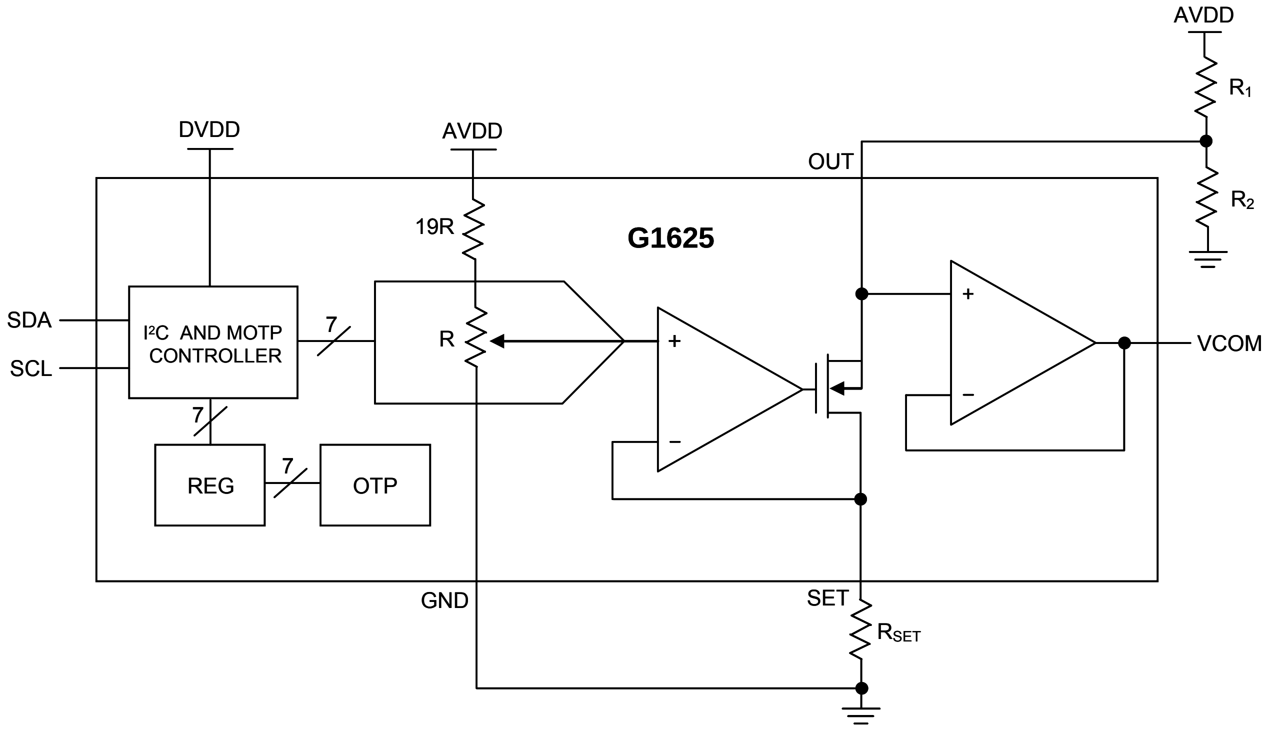
Minimum Footprint PCB Layout Section



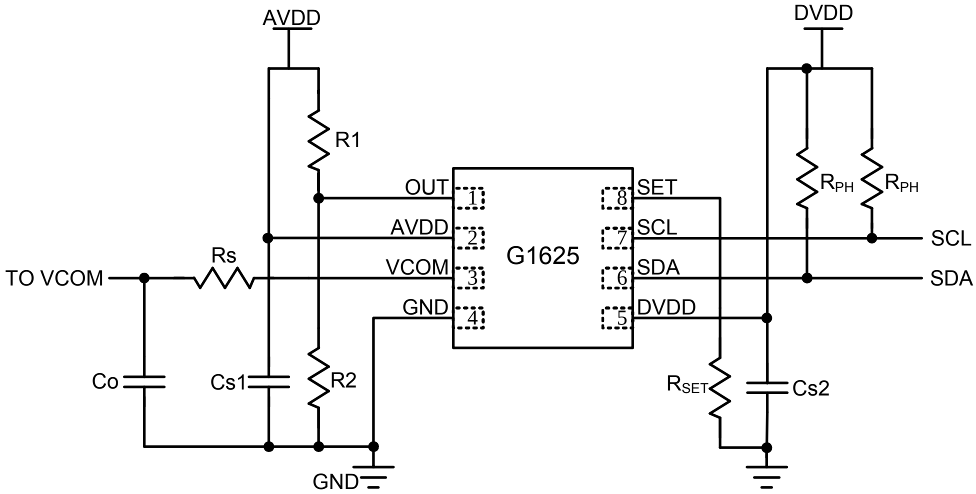
Pin Descriptions

PIN	NAME	FUNCTION
1	OUT	Adjustable Sink Current for Integrated VCOM Voltage Buffer. OUT connects to the resistive voltage divider between AVDD and GND.
2	AVDD	Analog Power Supply. Bypass AVDD with 0.1µF capacitor to GND.
3	VCOM	VCOM Output.
4	GND	Ground.
5	DVDD	Digital Power Supply. Bypass DVDD with 0.1µF capacitor to GND.
6	SDA	I2C-Compatible Serial-Data Input/Output.
7	SCL	I2C-Compatible Serial-Data Input.
8	SET	Full-Scale Sink-Current Adjustment Input. Connect a resistor, RSET, from SET to GND to set the full-scale adjustable sink current. The full-scale adjustable sink current is equal to: $\left(\frac{V_{AVDD}}{20 \times R_{SET}}\right)$
Thermal Pad		Exposed pad should be soldered to large area PCB board and connected to GND.

Block Diagram



Typical Application Circuit



Function Description

The G1625, a programmable VCOM buffer, replaces the mechanical potentiometer that is used for adjusting the VCOM voltage with an electrical solution (see the Typical Application Circuit). The G1625 attaches to an external resistor-divider (resistors R1 and R2) and sinks a programmable current IOUT to create the VCOM reference voltage. The resolution of the current DAC that generates IOUT is 7 bits. The DAC is ratio metric relative to VAVDD and is monotonic over all operating conditions. The external resistor RSET sets the full-scale sink current and the minimum value of the VCOM reference voltage. The external resistor-divider and the AVDD supply set the maximum value of the VCOM reference voltage.

The VCOM reference voltage is the input to the integrated voltage buffer, which can source and sink 300mA. The G1625 features output short-circuit protection.

The user can store the DAC setting in a type of non-volatile memory known as OTP. On power-up, OTP sets the DAC register to the last stored setting. The DAC register and the OTP can be programmed through the I2C interface.

An internal 7-bit DAC sinks current IOUT. The following equations determine the value of IOUT:

$$I_{OUT} = \left(\frac{CODE+1}{2^N}\right) \times \left(\frac{V_{AVDD}}{20 \times R_{SET}}\right)$$

where CODE is the numeric value of the DAC's binary input code and N is the bits of resolution. For the G1625, N = 7 and CODE ranges from 0 to 127.

The G1625 pulls IOUT through the external resistor divider comprised of R1 and R2. The resulting voltage VOUT is given by the following formula:

$$VCOM = \left(\frac{R_2}{R_1+R_2}\right) \times AVDD \times \left(1 - \left(\frac{CODE+1}{128}\right) \times \left(\frac{R_1}{20 \times R_{SET}}\right)\right)$$

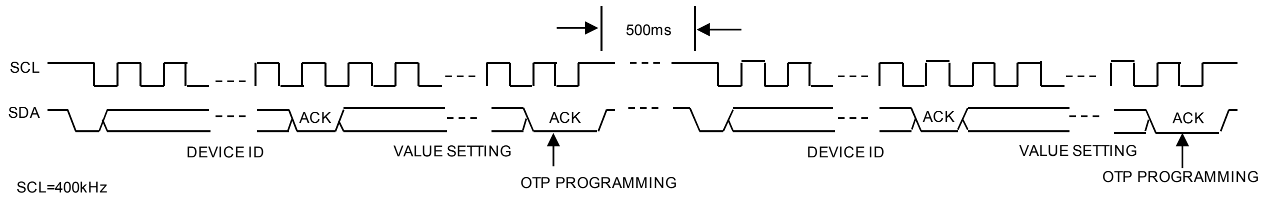


Figure 1. OTP programming interval. Wait 500ms after issuing a write command to OTP memory before starting another write command to OTP memory.

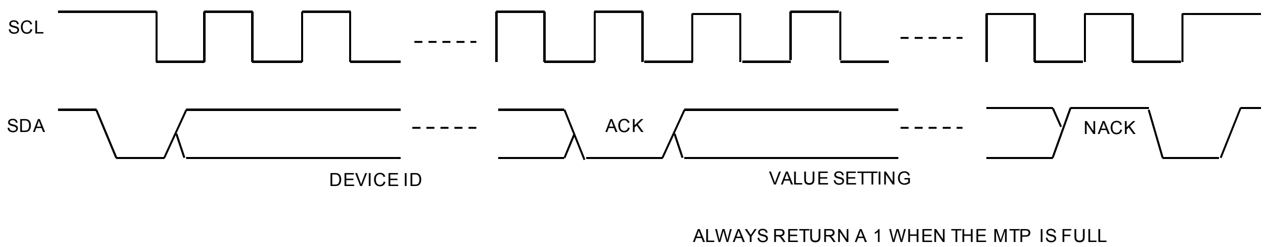


Figure 2. Example of a write command to OTP memory after OTP memory is full. The G1625 responds with a NACK.

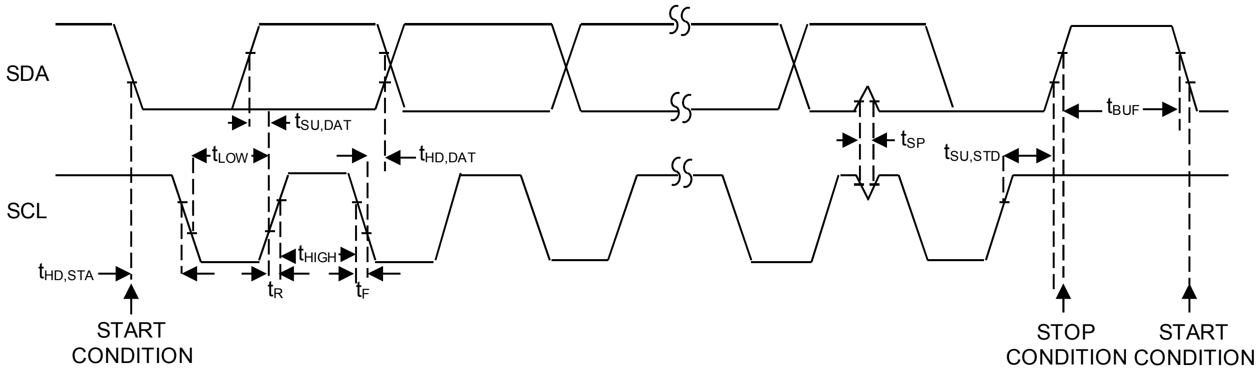


Figure 3. I²C Serial-Interface Timing Diagram

VCOM Amplifier
The buffer attached to VOUT holds the VCOM voltage stable while providing the ability to source and sink 300mA into the backplane of a TFT-LCD panel. The buffer can directly drive the capacitive load of the TFT LCD backplane. A series resistor (Rs) is suggested to be added for better stability. The VCOM amplifier has current limiting on its output to protect its bond wires.

One-Time Programmable Memory (OTP) Programming
DAC codes can be written into OTP memory up to 100 times because the OTP memory is a bank of 100 one-time programmable registers. See the Write Data Format section for a description of how to use the I²C interface to write data into OTP.
After an I²C write operation to OTP memory, the G1625 requires a maximum of 500ms to burn the data into the OTP register (see Figure 1). During this time, do not perform another write operation to OTP memory. If a write operation to OTP memory is attempted during this time, the G1625 responds with a not acknowledge (NACK).

The G1625 integrates OTP memory that can be programmed 100 times. After 100 writes to OTP memory, the G1625 responds with a not acknowledge (NACK) to all future write attempts (see Figure 2).

I²C Serial Interface
The G1625 features an I²C compatible, 2-wire serial interface consisting of a serial-data line (SDA) and a serial-clock line (SCL). SDA and SCL facilitate communication between the G1625 and the master at clock rates up to 400kHz. Figure 3 shows the 2-wire interface timing diagram. The master generates SCL and initiates data transfer on the bus. A master device writes data to the G1625 by transmitting the proper

slave address followed by the data word. Each transmit sequence is framed by a START (S) condition and a STOP (P) condition. Each word transmitted to the G1625 is 8 bits long and is followed by an acknowledge clock pulse. A master reading data from the G1625 transmits the proper slave address followed by a series of nine SCL pulses. The G1625 transmits data on SDA in sync with the master-generated SCL pulses. The master acknowledges receipt of each byte of data. Each read sequence is framed by a START (S) condition, a not acknowledge, and a STOP (P) condition. SDA operates as both an input and an open-drain output. A pull-up resistor, typically greater than 1000Ω, is required on the SDA bus. SCL operates as only an input. A pull-up resistor, typically greater than 1000Ω, is required on SCL if there are multiple masters on the bus, or if the master in a single-master system has an open-drain SCL output. Series resistors in line with SDA and SCL are optional. Series resistors protect the digital inputs of the G1625 from high-voltage spikes on the bus lines, and minimize crosstalk and undershoot of the bus signals.

Bit Transfer

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA while SCL is high are control signals (see the START and STOP Conditions section). SDA and SCL idle high when the I^2C bus is not busy.

START and STOP Conditions

SDA and SCL idle high when the bus is not in use. A master initiates communication by issuing a START (S) condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP (P) condition is a low to high transition on SDA while SCL is high (Figure 4). A START condition from the master signals the beginning of a transmission to the G1625. The master terminates transmission, and frees the bus, by issuing a STOP condition.

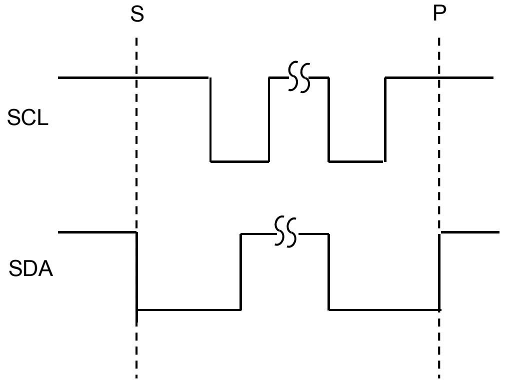


Figure 4. START and STOP Conditions

Early STOP Conditions

The G1625 recognizes a STOP condition at any point during data transmission except if the STOP condition occurs in the same high pulse as a START condition. For proper operation, do not send a STOP condition during the same SCL high pulse as the START condition.

Slave Address

The slave address is defined as the 7 most significant bits (MSBs) followed by the read/write (R/W) bit. Set the R/W bit to 1 to configure the G1625 to read mode. Set the R/W bit to 0 to configure the G1625 to write mode. The address is the first byte of information sent to the G1625 after the START condition. Table 1 shows the possible addresses for the G1625.

Acknowledge

The acknowledge bit (ACK) is a clocked 9th bit that the G1625 uses to handshake receipt of each byte of data when in write mode (see Figure 5). The G1625 pulls down SDA during the entire master-generated ninth clock pulse if the previous byte is successfully received. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master may retry communication. The master pulls down SDA during the ninth clock cycle to acknowledge receipt of data when the G1625 is in read mode. An acknowledge bit is sent by the master after each read byte to allow data transfer to continue. A not-acknowledge bit is sent when the master reads the final byte of data from the G1625, followed by a STOP condition.

Read Data Format

The master presets the address pointer by first sending the G1625's slave address with the R/W bit set to 1 after a START (S) condition. The G1625 acknowledges receipt of its slave address and the register address by pulling SDA low during the ninth SCL clock pulse. The G1625 transmits the contents of the DAC register as 7-bit data and the eighth bit, M, is don't care. Transmitted data is valid on the rising edge of the master-generated serial clock (SCL). A STOP condition is issued after reading the data byte. The master acknowledges receipt of the read byte during the acknowledge clock pulse. The final byte must be followed by a not acknowledge from the master and then a STOP condition. Figure 6 illustrates the frame format for reading data from the G1625.

Register Map

REG	B7	B6	B5	B4	B3	B2	B1	B0	FACTORY INITIALIZATION	R/$\overline{W}$
VCOM	D6	D5	D4	D3	D2	D1	D0	M	64	R/$\overline{W}$

Table 1. Slave Address

B7	B6	B5	B4	B3	B2	B1	B0	WRITE ADDRESS	READ ADDRESS
1	0	0	1	1	1	1	R/W	0x9E	0x9F

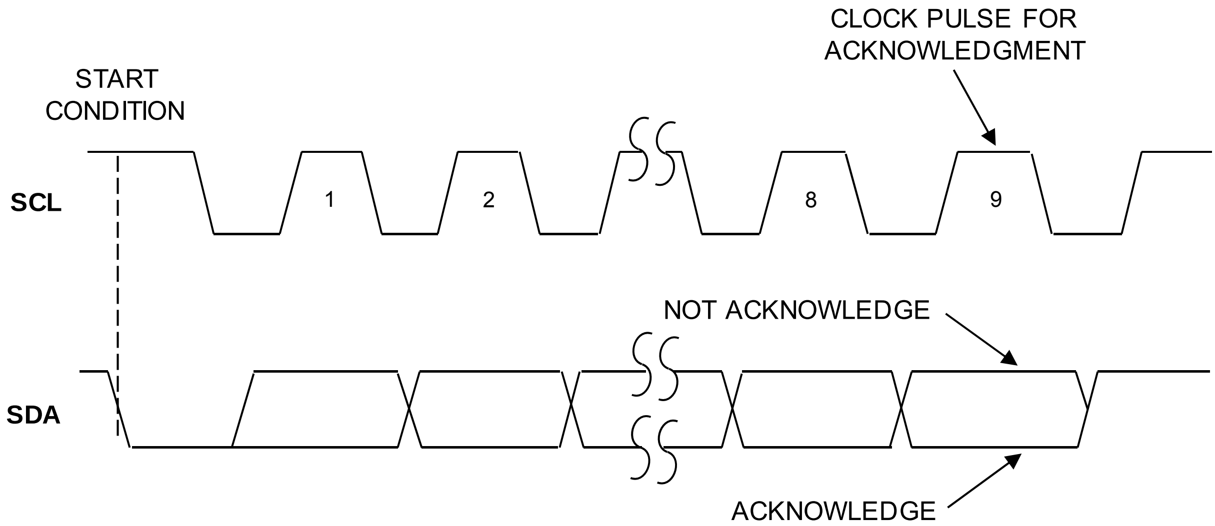


Figure 5. Acknowledge

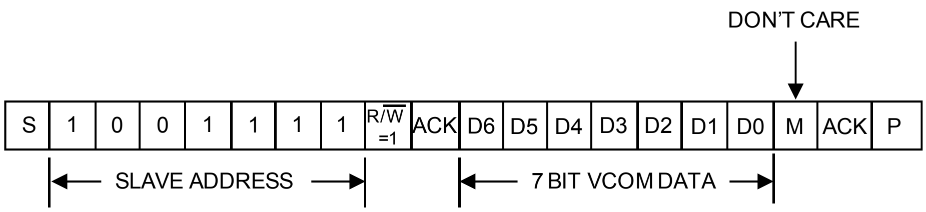


Figure 6.Read Operation to OTP or DAC Register

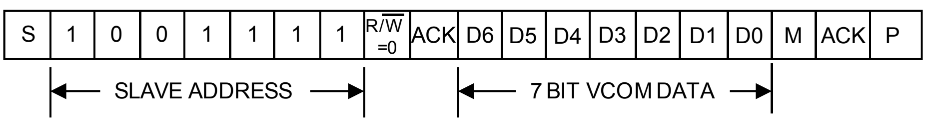


Figure 7. Write Operation to OTP or DAC Register

Table 2. I2C Register

BITS	DESCRIPTION
B7:B1	7-bit DAC data
B0	Data location indicator (M bit). The M bit identifies the register for the data to be written to. M = 0, the data is written to the OTP register. M = 1, the data is written to the DAC register.

Write Data Format

A write to the G1625 consists of transmitting a START condition, the slave address with the R/W bit set to 0, 7-bit data, M bit, and a STOP condition. Figure 7 illustrates the proper frame format for writing 7 bits of data to the G1625. The slave address with the R/W bit set to 0 indicates that the master intends to write data to the G1625. The G1625 acknowledges receipt of the address byte during the master-generated ninth SCL pulse. The second byte sent to the G1625 contains the 7-bit data that is written to the DAC latch or OTP. The M bit after the bit B0 identifies register to be written to, as shown in Table 2. When M = 0, the OTP is written to, and when M = 1, the DAC register is written to. An acknowledge pulse from the G1625 signals receipt of the VCOM data byte. The master signals the end of transmission by issuing a STOP (P) condition.

Applications Information Power-Up and Power-Down Operation

During power-up, the digital supply is recommended to be powered up first before analog supply. During this time, the OTP register value is loaded into the DAC register (0x40 is the factory-programmed default). Once AVDD is above 7V approximately, the VCOM amplifier has enough headroom and powers up proportionally with AVDD. For power-down, AVDD is recommended to be powered down first to 0V, and then DVDD can safely be powered down.

Power Supplies and Bypass Capacitors

The G1625 operates from a single 7V to 18V analog supply (AVDD) and a 2.5V to 3.6V digital supply (DVDD). Bypass AVDD to GND with 0.1μF and 10μF capacitors in parallel. Use an extensive ground plane to ensure optimum performance. Bypass DVDD to GND with a 0.1μF capacitor. The 0.1μF bypass capacitors should be placed as close as possible to their respective pins. Refer to the G1625 evaluation kit for a proven PCB layout.

Layout and Grounding Exposed Pad

The exposed pad on the TDFN package is electrically connected to AGND. Solder the exposed pad to a ground plane to provide a low thermal resistance to ground for heat dissipation. Do not route traces under these packages. The layout of the exposed pad should have multiple small through-holes over a single large through-hole as shown as Figure 8. Thermal resistance between top and ground layer can be reduced. In addition, the vias should be flooded with solder for best thermal performance.

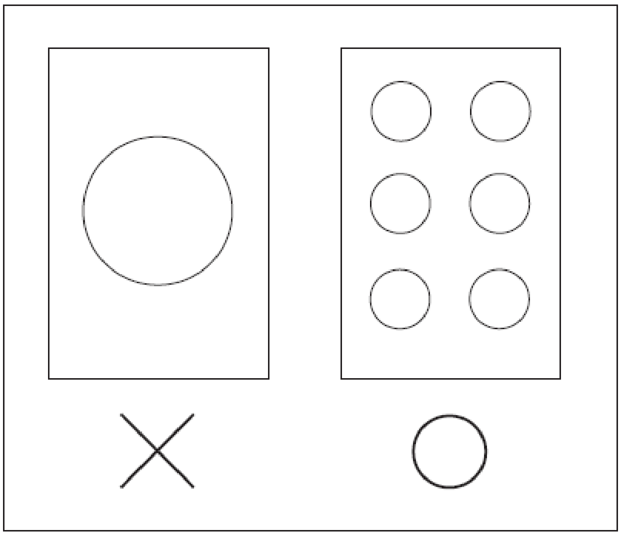
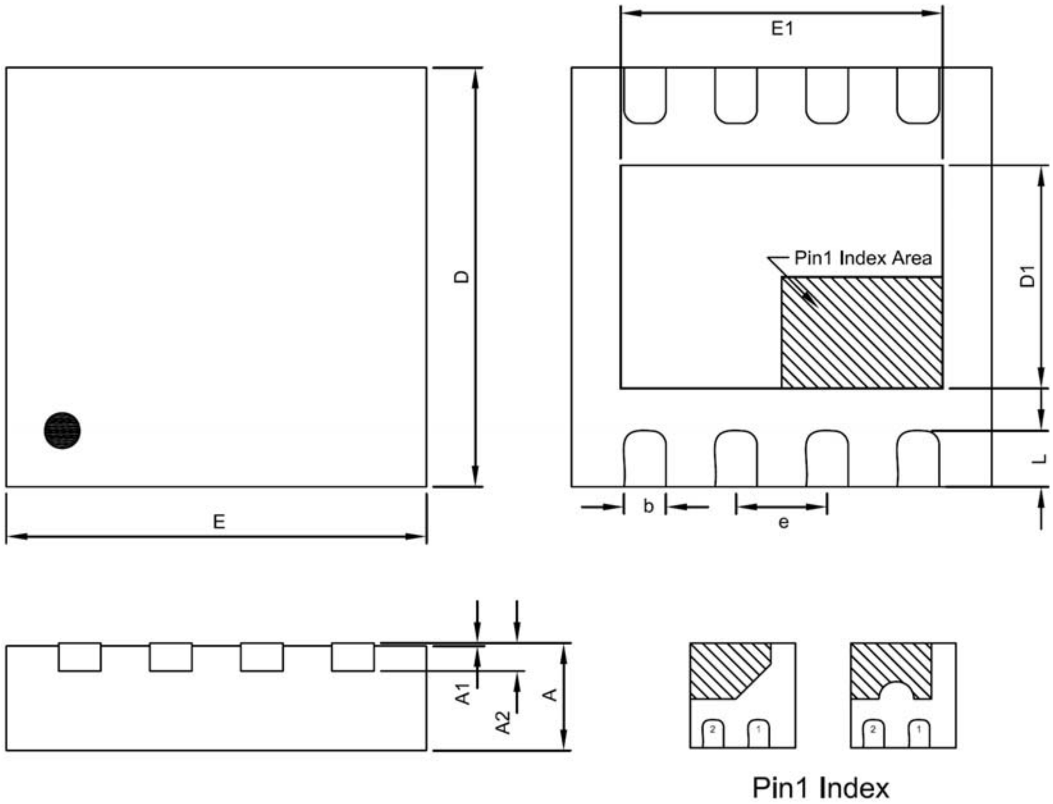


Figure 8. Multiple small through-holes are recommended over single large through-hole in PCB layout.

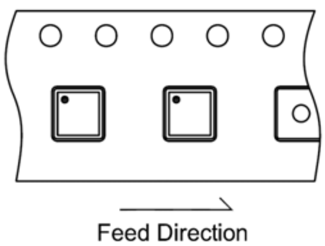
Package Information



TDFN3X3-8 Package

Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.0276	0.0295	0.0315
A1	0.00	- - -	0.05	0.0000	- - -	0.0020
A2	0.20 REF			0.0079 REF		
D	2.95	3.00	3.05	0.1161	0.1181	0.1201
E	2.95	3.00	3.05	0.1161	0.1181	0.1201
D1	1.60	1.70	1.80	0.0630	0.0669	0.0709
E1	1.90	2.00	2.10	0.0748	0.0787	0.0827
b	0.20	0.30	0.35	0.0079	0.0118	0.0138
e	0.65 BSC			0.0256 BSC		
L	0.25	0.35	0.45	0.0098	0.0138	0.0177

Taping Specification



PACKAGE	Q'TY/REEL
TDFN3X3-8	3,000 ea