DMOS Micro-stepping Driver with Translator and Over-current Protection

Features

- **Low $R_{DS(ON)}$ outputs**
- **Automatic current decay mode detection/selection**
- **Mixed and Slow current decay modes**
- **Synchronous rectification for low power dissipation**
- **Internal UVLO**
- **Crossover-current protection**
- **3.3 and 5 V compatible logic supply**
- **Thin profile QFN and TSSOP packages**
- **Thermal shutdown circuitry**
- **Short-to-ground protection**
- **Shorted load protection**
- **Low current Sleep mode, <10µA**

General Description

The G2035 is a complete micro-stepping motor driver with built-in translator for easy operation. It is designed to operate bipolar stepper motors in full-, half-, quarter-, and eighth-step modes. Step modes are selectable by MSx logic inputs. It has an output drive capacity of up to 35 V and ±2 A. The G2035 includes a fixed off-time current regulator which has the ability to operate in Slow or Mixed decay modes.

The translator is the key to the easy implementation of the G2035. Simply inputting one pulse on the STEP input drives the motor one micro-stepping. There are no phase sequence tables, high frequency control lines, or complex interfaces to program. The G2035 interface is an ideal fit for applications where a complex microprocessor is unavailable or is overburdened.

During stepping operation, the chopping control in the G2035 automatically selects the current decay mode, Slow or Mixed.

In Mixed decay mode, the device is set initially to a fast decay for a proportion of the fixed off-time, then to a slow decay for the remainder of the off-time. Mixed decay current control results in reduced audible motor noise, increased step accuracy, and reduced power dissipation.

Internal synchronous rectification control circuitry is provided to improve power dissipation during PWM operation. Internal circuit protection includes: thermal shutdown with hysteresis, undervoltage lockout (UVLO), and crossover-current protection. Special power-on sequencing is not required.

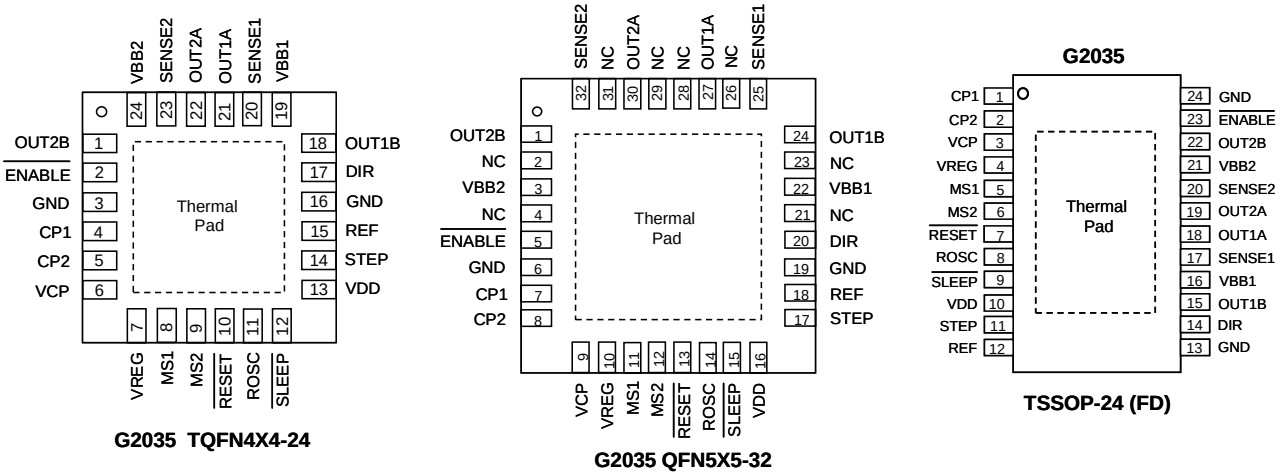
The G2035 is supplied in three surface mount packages: two QFN packages, the 4mm×4mm,0.75mm nominal overall height TQFN4X4-24 package, and the 5mm×5mm×0.90mm QFN5X5-32 package. The TSSOP package is a 24-pin. All three packages have exposed pads for enhanced thermal dissipation, and are lead (Pb) free, with 100% matte tin plated lead-frames.

Ordering Information

ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE (Green)
G2035R51U	2035	0°C to +85°C	TQFN4X4-24
G2035QA1U	2035	0°C to +85°C	QFN5X5-32
G2035F31U	G2035	0°C to +85°C	TSSOP-24 (FD)

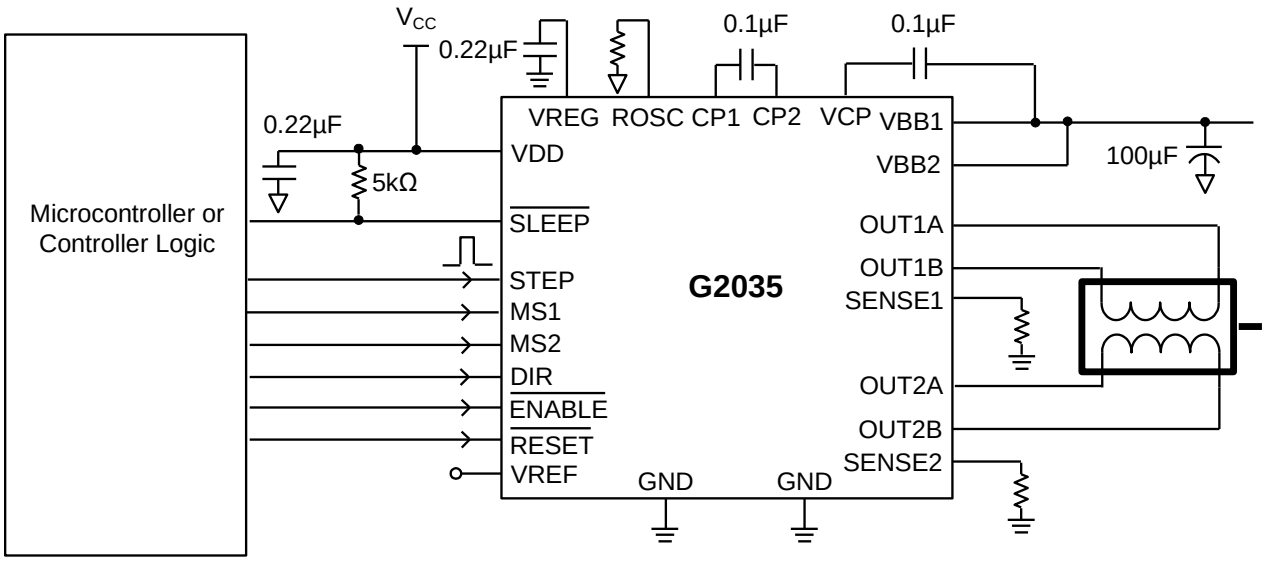
Note: R5: TQFN4X4-24 QA: QFN5X5-32 F3: TSSOP-24 (FD)
1: Bonding Code
U: Tape & Reel
Green : Lead Free / Halogen Free.

Pin Configuration



Note: Recommend connecting the Thermal Pad to the Ground for excellent power dissipation.

Typical Application Diagram



Absolute Maximum Ratings

Load Supply Voltage (V_{BB}) 35V
Output Current (I_{OUT}) . . . . . ±2A
Logic Input Voltage (V_{IN}) . . . . . -0.3V to 5.5V
Logic Supply Voltage (V_{DD}) . . . . . -0.3V to 5.5V
Motor Outputs Voltage. . . . . -2.0V to 37V
Sense Voltage (V_{SENSE}) . . . . . .-0.5V to 0.5V
Reference Voltage (V_{REF}) 5.5V
Thermal Resistance of Junction to Ambient (θ_{JA})
TQFN4X4-24. . . . . .TBD°C/W
QFN5X5-32. . . . . 39°C/W
TSSOP-24 (FD). . . . . TBD
Continuous Power Dissipation (T_A = +25°C)
TQFN4X4-24. . . . . .TBD
QFN5X5-32. . . . . 3.2W
TSSOP-24 (FD). . . . . TBD
Operating Ambient Temperature (T_A) . . . . -20 to 85°C
Maximum Junction (T_J(max)) . . . . . .150°C
Storage Temperature (T_{stg}) . . . . . -55 to150°C

1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Device are ESD sensitive. Handling precaution recommended. The Human Body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.

Electrical Characteristics(1)

(VBB= 24V, T_A=+25°C.)

The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP(2)	MAX	UNIT
Output Drivers						
Load Supply Voltage Range	V_{BB}	Operating	8	---	35	V
		During Sleep Mode	0	---	35	V
Logic Supply Voltage Range	V_{DD}	Operating	3	---	5.5	V
Output On Resistance	R_{DSON}	Source Driver, I_{OUT}= -1.5A	---	320	430	mΩ
		Sink Driver, I_{OUT}= 1.5A	---	320	430	mΩ
Body Diode Forward Voltage	V_F	Source Diode, I_F= -1.5A	---	---	1.3	V
		Sink Diode, I_F= -1.5A	---	---	1.3	V
Motor Supply Current	I_{BB}	f_{PWM}< 50kHz	---	---	4	mA
		Operating, outputs disabled	---	---	2	mA
		Sleep Mode	---	---	10	μA
Logic Supply Current	I_{DD}	f_{PWM}< 50kHz	---	---	8	mA
		Output off	---	---	5	mA
		Sleep Mode	---	---	10	μA

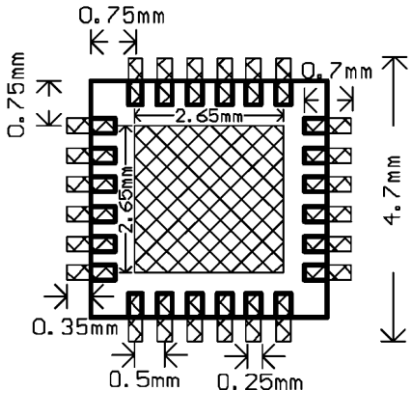
Electrical Characteristics (Continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP(2)	MAX	UNIT
Control Logic						
Logic Input Voltage	$V_{IN(1)}$		V_{DD}×0.7	---	---	V
	$V_{IN(0)}$		---	---	V_{DD}×0.3	V
Logic Input Current	$I_{IN(1)}$	V_{IN}=V_{DD}×0.7	-20	<1	20	μA
	$I_{IN(0)}$	V_{IN}=V_{DD}×0.3	-20	<1	20	μA
Microstep Select	R_{MS1}	MS1 pin	---	100	---	kΩ
	R_{MS2}	MS2 pin	---	50	---	kΩ
Logic Input Hysteresis	$V_{HYS(IN)}$	As a % of V_{DD}	5	11	19	%
Blank Time	t_{BLANK}		0.7	1	1.3	μs
Fixed Off-Time	t_{OFF}	OSC=VDD or GND	20	30	40	μs
		R_{OSC}=25kΩ	23	30	37	μs
Reference Input Voltage Range	V_{REF}		0	---	4	V
Reference Input Current	I_{REF}		-3	0	3	μA
Current Trip-Level Error(3)	err_I	V_{REF}=2V, %$I_{TripMAX}$=38.27%	---	---	±15	%
		V_{REF}=2V, %$I_{TripMAX}$=70.71%	---	---	±5	%
		V_{REF}=2V, %$I_{TripMAX}$=100%	---	---	±5	%
Crossover Dead Time	t_{DT}		100	475	800	ns
Protection						
Overcurrent Protection Threshold (4)	I_{OCPST}		2.1	---	---	A
Thermal Shutdown Temperature	T_{TSD}		---	165	---	°C
Thermal Shutdown Hysteresis	T_{TSDHYS}		---	15	---	°C
VDD Undervoltage Lockout	V_{DDUVLO}	V_{DD} rising	2.7	2.8	2.9	V
VDD Undervoltage Hysteresis	$V_{DDUVLOHYS}$		---	90	---	mV

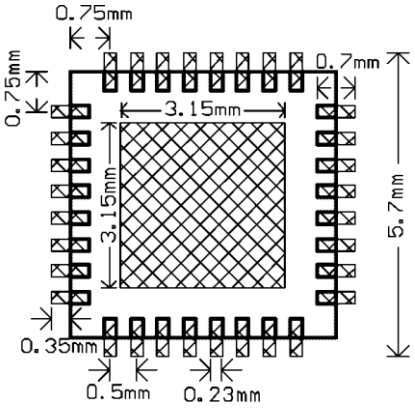
1. For input and output current specifications, negative current is defined as coming out of (sourcing) the specified device pin.
2. Typical data are for initial design estimations only, and assume optimum manufacturing and application conditions. Performance may vary for individual units, within the specified maximum and minimum limits.
3. V_{ERR} = [(V_{REF}/8) – V_{SENS}E] / (V_{REF}/8).
4. Overcurrent protection (OCP) is tested at T_A = 25°C in a restricted range and guaranteed by characterization.

Minimum Footprint PCB Layout Section

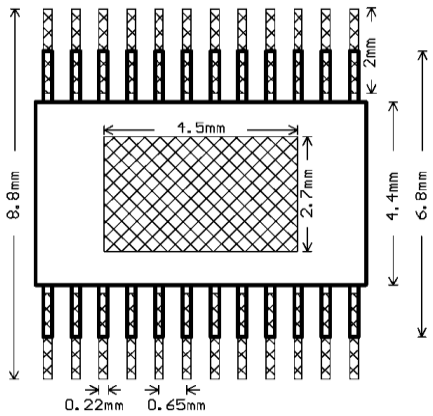
TQFN4X4-24



QFN5X5-32



TSSOP-24 (FD)

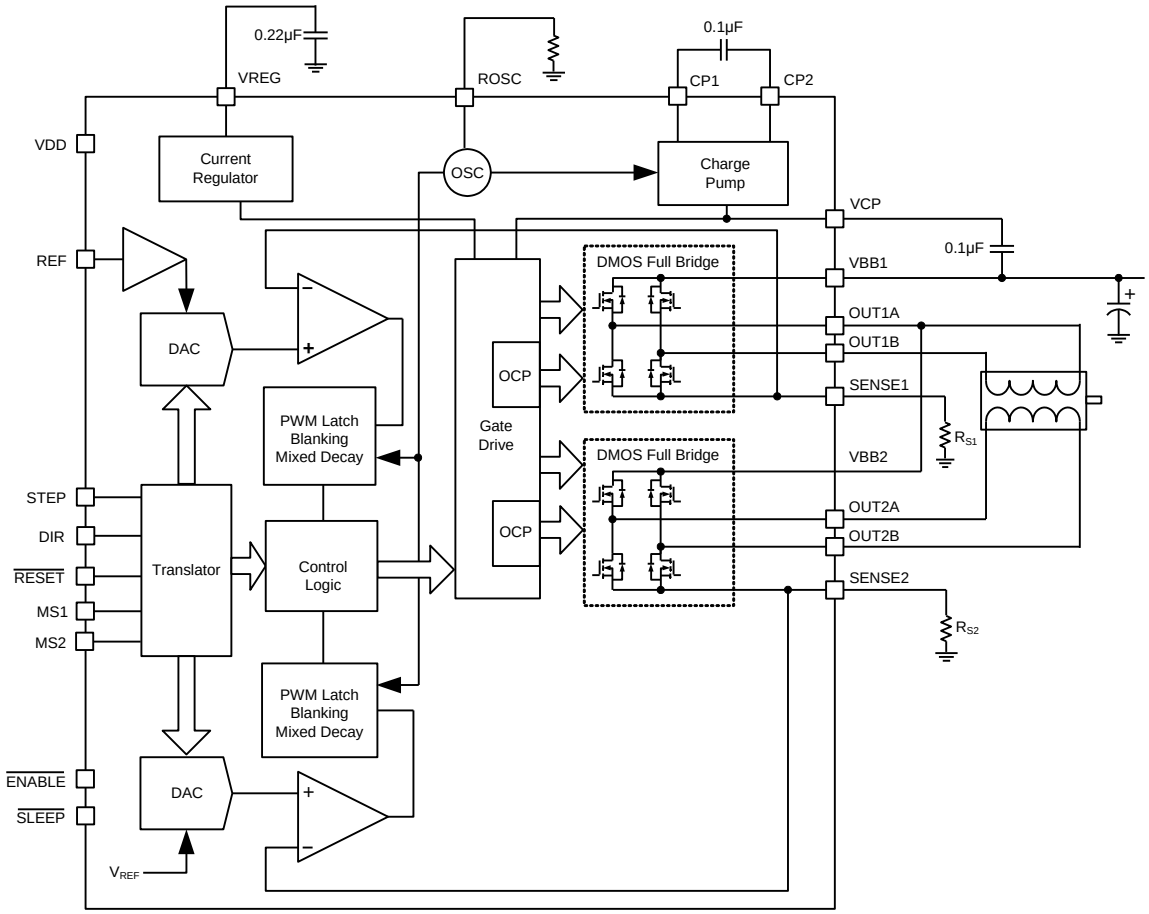


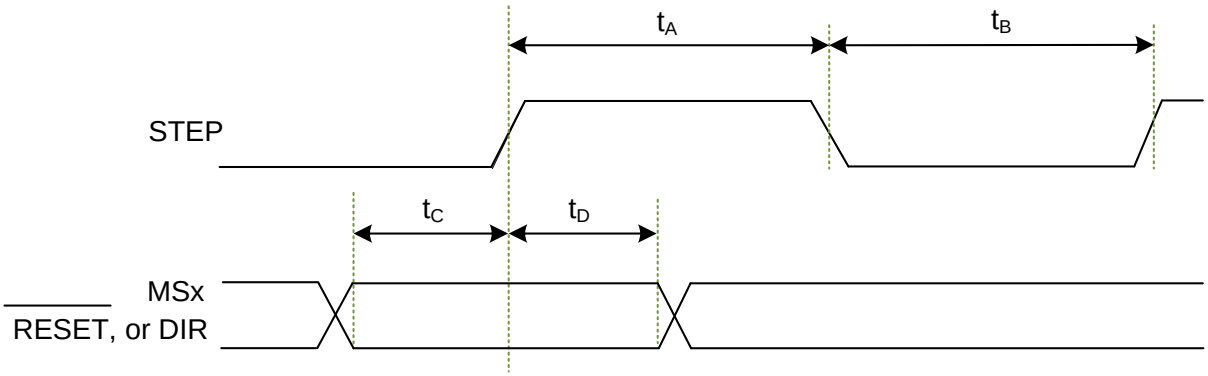
Pin Description

PIN			NAME	FUNCTION
TQFN4X4-24	QFN5X5-32	TSSOP-24 FD)		
1	1	22	OUT2B	DMOS Full Bridge 2 Output B
2	5	23	$\overline{\text{ENABLE}}$	Logic input
3,16	6,19	13,24	GND	Ground
4	7	1	CP1	Charge pump capacitor terminal
5	8	2	CP2	Charge pump capacitor terminal
6	9	3	VCP	Reservoir capacitor terminal
7	10	4	VREG	Regulator decoupling terminal
8	11	5	MS1	Logic input
9	12	6	MS2	Logic input
10	13	7	$\overline{\text{RESET}}$	Logic input
11	14	8	ROSC	Timing set
12	15	9	$\overline{\text{SLEEP}}$	Logic input
13	16	10	VDD	Logic supply
14	17	11	STEP	Logic input
15	18	12	REF	G_m reference voltage input
17	20	14	DIR	Logic input
18	24	15	OUT1B	DMOS Full Bridge 1 Output B
19	22	16	VBB1	Load supply
20	25	17	SENSE1	Sense resistor terminal for Bridge 1
21	27	18	OUT1A	DMOS Full Bridge 1 Output A
22	30	19	OUT2A	DMOS Full Bridge 2 Output A
23	32	20	SENSE2	Sense resistor terminal for Bridge 2
24	3	21	VBB2	Load supply
---	2,4,21,23,26, 28,29,31	---	NC	No connection
---	---	---	PAD	Exposed pad for enhanced thermal dissipation*

*The GND pins must be tied together externally by connecting to the PAD ground plane under the device.

Block Diagram





Time Duration	Symbol	TYP.	Unit
STEP minimum, HIGH pulse width	t_A	1	μs
STEP minimum, LOW pulse width	t_B	1	μs
Setup time, input change to STEP	t_C	200	ns
Hold time, input change to STEP	t_D	200	ns

Figure 1. Logic Interface Timing Diagram

Table 1. Microstep Resolution Truth Table

MS1	MS2	Microstep Resolution	Excitation Mode
L	L	Full Step	2 Phase
H	L	Half Step	1-2 Phase
L	H	Quarter Step	W1-2 Phase
H	H	Eighth Step	2W1-2 Phase

Function Description

Device Operation

The G2035 is a complete micro-stepping motor driver with a built-in translator for easy operation with minimal control lines. It is designed to operate bipolar stepper motors in full-, half-, quarter-, and eighth-step modes. The currents in each of the two output full-bridges and all of the N-channel DMOS FETs are regulated with fixed off-time PWM (pulse width modulated) control circuitry. At each step, the current for each full-bridge is set by the value of its external current-sense resistor (R_{S1} and R_{S2}), a reference voltage (V_{REF}), and the output voltage of its DAC (which in turn is controlled by the output of the translator).

At power-on or reset, the translator sets the DACs and the phase current polarity to the initial Home state (shown in figures 8 through 11), and the current regulator to Mixed Decay Mode for both phases. When a step command signal occurs on the STEP input, the translator automatically sequences the DACs to the next level and current polarity. (See table 2 for the current-level sequence.) The microstep resolution is set by the combined effect of the MSx inputs, as shown in table 1.

When stepping, if the new output levels of the DACs are lower than their previous output levels, then the decay mode for the active full-bridge is set to Mixed. If the new output levels of the DACs are higher than or equal to their previous levels, then the decay mode for the active full-bridge is set to Slow. This automatic current decay selection improves micro-stepping performance by reducing the distortion of the current waveform that results from the back EMF of the motor.

Microstep Select (MSx)

The microstep resolution is set by the voltage on logic inputs MSx, as shown in table 1. The MS1 pin has a 100kΩ pull-down resistance, and the MS2 pin has a 50kΩ pull-down resistance. When changing the step mode the change does not take effect until the next STEP rising edge.

If the step mode is changed without a translator reset, and absolute position must be maintained, it is important to change the step mode at a step position that is common to both step modes in order to avoid missing steps. When the device is powered down, or reset due to TSD or an over current event the translator is set to the home position which is by default common to all step modes.

Mixed Decay Operation

The bridge operates in Mixed decay mode, at power-on and reset, and during normal running according to the ROSC configuration and the step sequence, as shown in figures 8 through 11. During Mixed decay, when the trip point is reached, the G2035 initially goes into a fast decay mode for 31.25% of the off-time, t_{OFF}. After that, it switches to Slow decay mode for the remainder of t_{OFF}. A timing diagram for this feature appears on the next page.

Typically, mixed decay is only necessary when the current in the winding is going from a higher value to a lower value as determined by the state of the translator. For most loads automatically-selected mixed decay is convenient because it minimizes ripple when the current is rising and prevents missed steps when the current is falling. For some applications where micro-stepping at very low speeds is necessary, the lack of back EMF in the winding causes the current to increase in the load quickly, resulting in missed steps. This is shown in figure 2. By pulling the ROSC pin to ground, mixed decay is set to be active 100% of the time, for both rising and falling currents, and prevents missed steps as shown in figure 3. If this is not an issue, it is recommended that automatically-selected mixed decay be used, because it will produce reduced ripple currents. Refer to the Fixed Off-Time section for details.

Low Current Micro-stepping

Intended for applications where the minimum on-time prevents the output current from regulating to the programmed current level at low current steps. To prevent this, the device can be set to operate in Mixed decay mode on both rising and falling portions of the current waveform. This feature is implemented by shorting the ROSC pin to ground. In this state, the off-time is internally set to 30μs.

Reset Input ($\overline{\text{RESET}}$). The $\overline{\text{RESET}}$ input sets the translator to a predefined Home state (shown in figures 8 through 11), and turns off all of the FET outputs. All STEP inputs are ignored until the $\overline{\text{RESET}}$ input is set to high.

Step Input (STEP)

A low-to-high transition on the STEP input sequences the translator and advances the motor one increment. The translator controls the input to the DACs and the direction of current flow in each winding. The size of the increment is determined by the combined state of the MSx inputs.

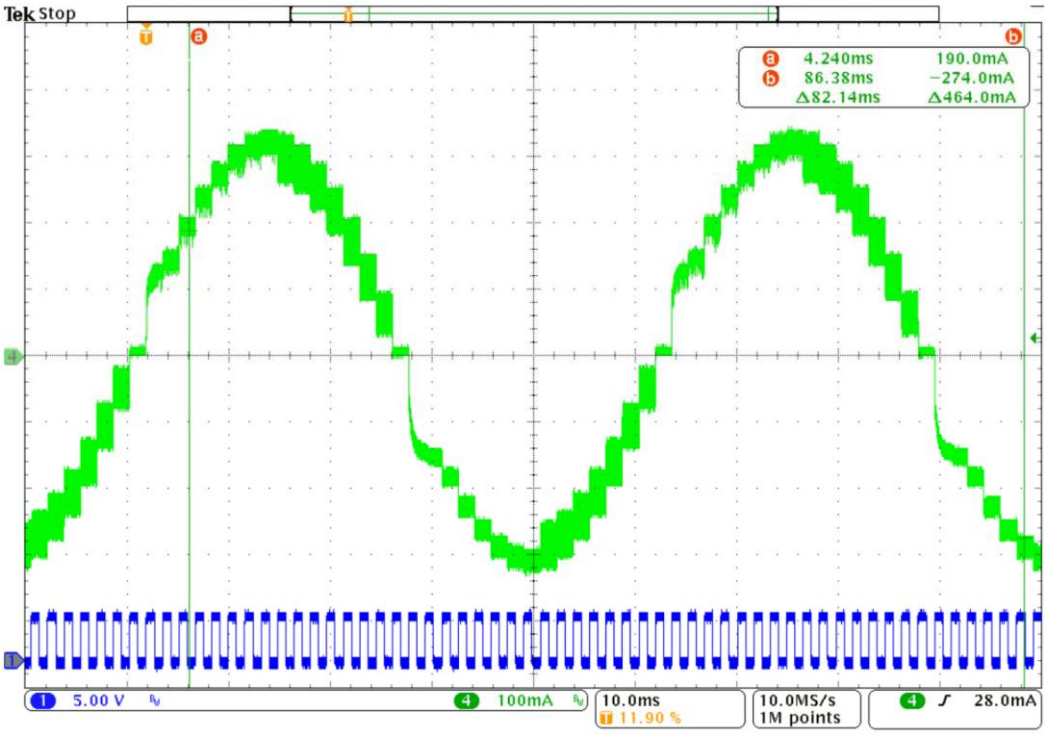


Figure 2. Missed steps in low-speed microstepping

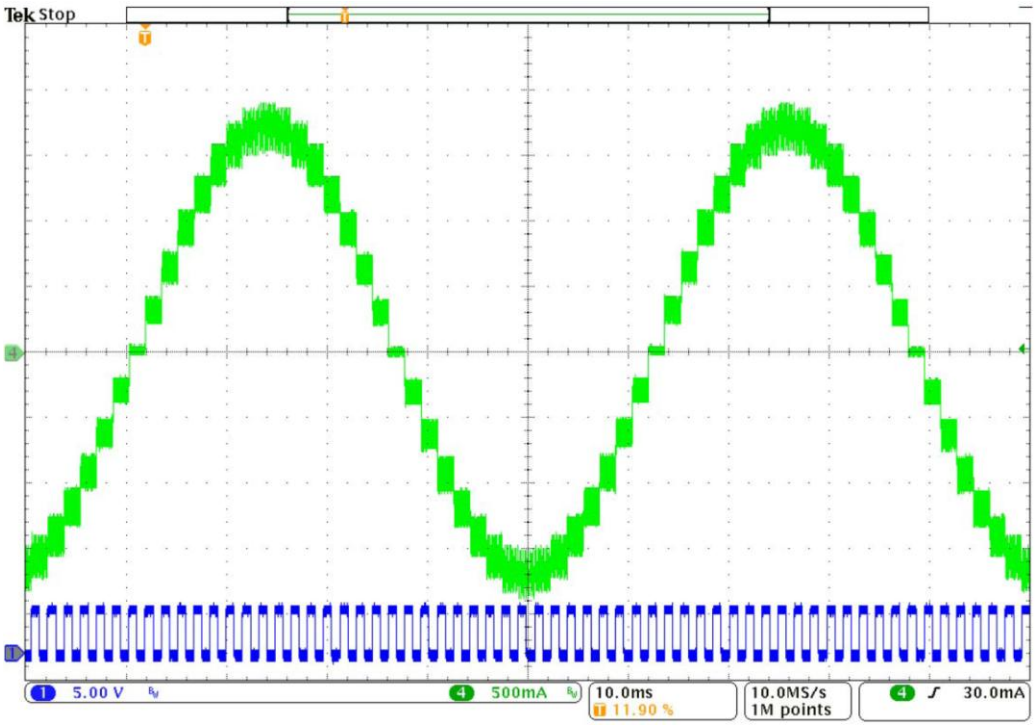


Figure 3. Continuous stepping using automatically-selected mixed stepping (ROSC pin grounded)

Direction Input (DIR)

This determines the direction of rotation of the motor. Changes to this input do not take effect until the next STEP rising edge.

Internal PWM Current Control

Each full-bridge is con-trolled by a fixed off-time PWM current control circuit that limits the load current to a desired value, I_{TRIP}. Initially, a diagonal pair of source and sink FET outputs are enabled and current flows through the motor winding and the current sense resistor, R_{Sx}. When the voltage across R_{Sx} equals the DAC output voltage, the current sense comparator resets the PWM latch. The latch then turns off either the source FET (when in Slow decay mode) or the sink and source FETs (when in Mixed decay mode).

The maximum value of current limiting is set by the selection of R_{Sx} and the voltage at the VREF pin. The trans-conductance function is approximated by the maximum value of current limiting, $I_{TripMAX}$ (A), which is set by

$$I_{TripMAX} = V_{REF} / (8 \times R_S)$$

where R_S is the resistance of the sense resistor (Ω) and V_{REF} is the input voltage on the REF pin (V). The DAC output reduces the V_{REF} output to the current sense comparator in precise steps, such that

$$I_{trip} = (\%I_{TripMAX} / 100) \times I_{TripMAX}$$

(See table 2 for $\%I_{TripMAX}$ at each step.)

It is critical that the maximum rating (0.5V) on the SENSE1 and SENSE2 pins is not exceeded.

Fixed Off-Time

The internal PWM current control circuitry uses a one-shot circuit to control the duration of time that the DMOS FETs remain off. The off-time, t_{OFF}, is determined by the ROSC terminal. The ROSC terminal has three settings:

- ROSC tied to VDD — off-time internally set to 30μs, decay mode is automatic Mixed decay except when in full step where decay mode is set to Slow decay
- ROSC tied directly to ground — off-time internally set to 30μs, current decay is set to Mixed decay for both increasing and decreasing currents for all step modes.
- ROSC through a resistor to ground — off-time is determined by the following formula, the decay mode is automatic Mixed decay for all step modes.

$$t_{OFF} \approx R_{OSC} \ / \ 825$$

Where t_{OFF} is in μs.

Blanking

This function blanks the output of the current sense comparators when the outputs are switched by the internal current control circuitry. The comparator outputs are blanked to prevent false over-current detection due to reverse recovery currents of the clamp diodes, and switching transients related to the capacitance of the load. The blank time, t_{BLANK} (μs), is approximately

$$t_{BLANK} \approx 1\mu s$$

Shorted-Load and Short-to-Ground Protection

If the motor leads are shorted together, or if one of the leads is shorted to ground, the driver will protect itself by sensing the over-current event and disabling the driver that is shorted, protecting the device from damage. In the case of a short-to-ground, the device will remain disabled (latched) until the $\overline{SLEEP}$ input goes high or VDD power is removed. A short-to-ground over-current event is shown in figure 4.

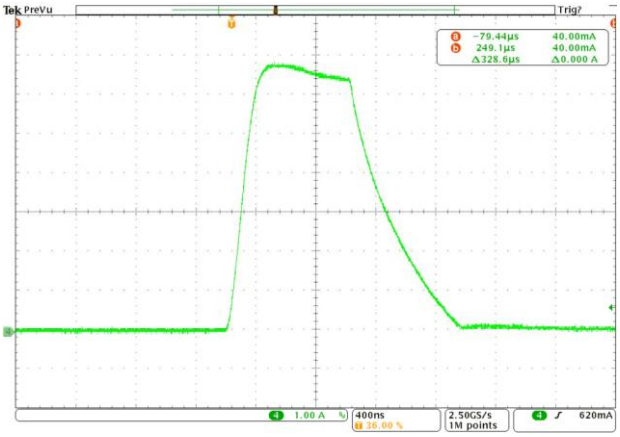


Figure 4. Short-to-ground event

Charge Pump (CP1 and CP2)

The charge pump is used to generate a gate supply greater than that of VBB for driving the source-side FET gates. A 0.1μF ceramic capacitor, should be connected between CP1 and CP2. In addition, a 0.1μF ceramic capacitor is required between VCP and VBB, to act as a reservoir for operating the high-side FET gates. Capacitor values should be Class 2 dielectric ±15% maximum, or tolerance R, according to EIA (Electronic Industries Alliance) specifications.

V_{REG} (VREG)

This internally-generated voltage is used to operate the sink-side FET outputs. The nominal output voltage of the V_{REG} terminal is 5.5 V. The V_{REG} pin must be decoupled with a 0.22μF ceramic capacitor to ground. VREG is internally monitored. In the case of a fault condition, the FET outputs of the G2035 are disabled.

Capacitor values should be Class 2 dielectric ±15%

maximum, or tolerance R, according to EIA (Electronic Industries Alliance) specifications. Enable Input ($\overline{\text{ENABLE}}$). This input turns on or off all of the FET outputs. When set to a logic high, the outputs are disabled. When set to a logic low, the internal control enables the outputs as required. The translator inputs STEP, DIR, and MSx, as well as the internal sequencing logic, all remain active, independent of the $\overline{\text{ENABLE}}$ input state.

Shutdown

In the event of a fault, overtemperature (excess T_J) or an undervoltage (on VCP), the FET outputs of the G2035 are disabled until the fault condition is removed. At power-on, the UVLO (undervoltage lockout) circuit disables the FET outputs and resets the translator to the Home state.

Sleep Mode ($\overline{\text{SLEEP}}$)

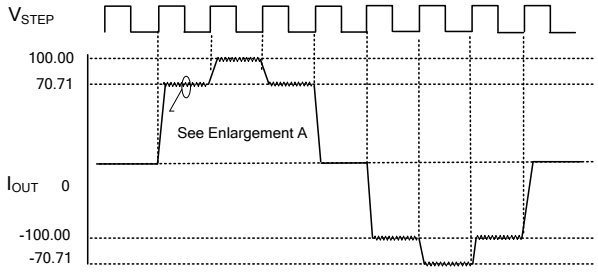
To minimize power consumption when the motor is not in use, this input disables much of the internal circuitry including the output FETs, current regulator, and charge pump. A logic low on the $\overline{\text{SLEEP}}$ pin puts the G2035 into Sleep mode. A logic high allows normal operation, as well as start-up (at which time the G2035 drives the motor to the Home microstep position). When emerging from Sleep mode, in order to allow the charge pump to stabilize, provide a delay of 1 ms before issuing a Step command.

Mixed Decay Operation

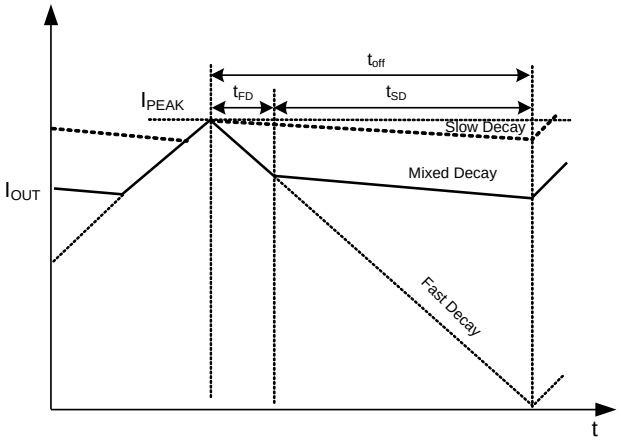
The bridge can operate in Mixed Decay mode, depending on the step sequence, as shown in figures 8 through 11. As the trip point is reached, the G2035 initially goes into a fast decay mode for 31.25% of the off-time, t_{OFF}. After that, it switches to Slow Decay mode for the remainder of t_{OFF}. A timing diagram for this feature appears in figure 5.

Synchronous Rectification

When a PWM-off cycle is triggered by an internal fixed-off time cycle, load current recirculates according to the decay mode selected by the control logic. This synchronous rectification feature turns on the appropriate FETs during current decay, and effectively shorts out the body diodes with the low FET $R_{DS(ON)}$. This reduces power dissipation significantly, and can eliminate the need for external Schottky diodes in many applications. Synchronous rectification turns off when the load current approaches zero (0A), preventing reversal of the load current.



Enlargement A



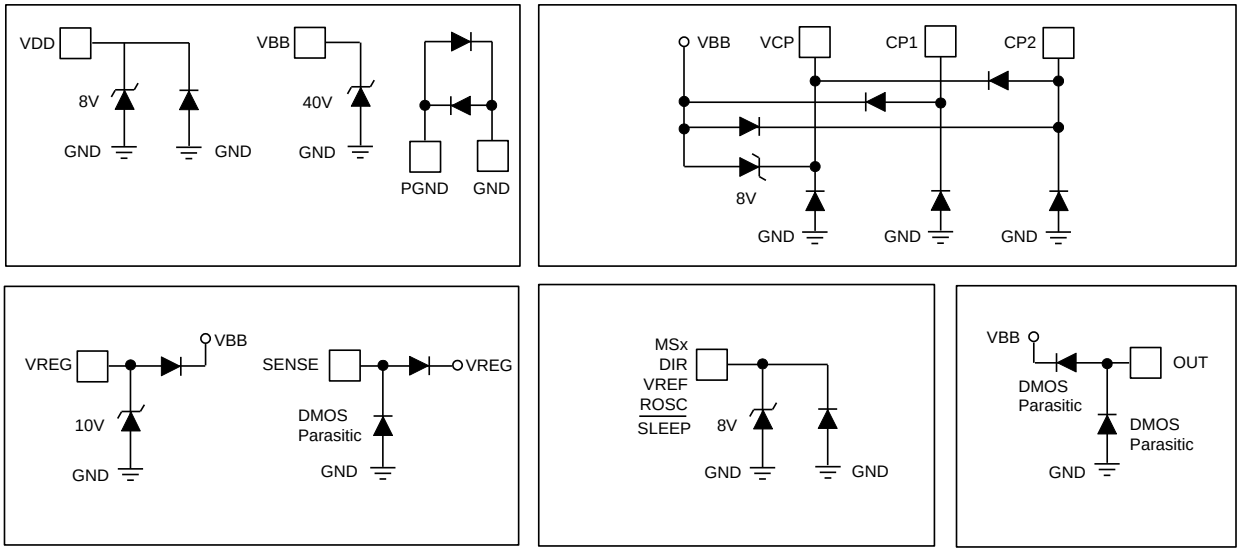
Symbol	Characteristic
t_{off}	Device fixed off-time
I_{PEAK}	Maximum output current
t_{SD}	Slow decay interval
t_{FD}	Fast decay interval
I_{OUT}	Device output current

Figure 5. Current Decay Modes Timing Chart

Application Layout

The printed circuit board should use a heavy ground-plane. For optimum electrical and thermal performance, the G2035 must be soldered directly onto the board. On the under-side of the G2035 package is an exposed pad, which provides a path for enhanced thermal dissipation. The thermal pad should be soldered directly to an exposed surface on the PCB. Thermal vias are used to transfer heat to other layers of the PCB.In order to minimize the effects of ground bounce and offset issues, it is important to have a low impedance single-point ground, known as a star ground, located very close to the device. By making the connection between the pad and the ground plane directly under the G2035, that area becomes an ideal location for a star ground point. A low impedance ground will prevent ground bounce during high current operation and ensure that the supply voltage remains stable at the input terminal.The two input capacitors should be placed in parallel, and as close to the device supply pins as possible. The ceramic capacitor (C7) should be closer to the pins than the bulk capacitor (C2). This is necessary because the ceramic capacitor will be responsible for delivering the high frequency current components.The sense resistors, RSx , should have a very low impedance path to ground, because they must carry a large current while supporting very accurate voltage measurements by the current sense comparators. Long ground traces will cause additional voltage drops, adversely affecting the ability of the comparators to accurately measure the current in the windings. The SENSEx pins have very short traces to the RSx resistors and very thick, low impedance traces directly to the star ground underneath the device. If possible, there should be no other components on the sense circuits.

Pin Circuit Diagrams



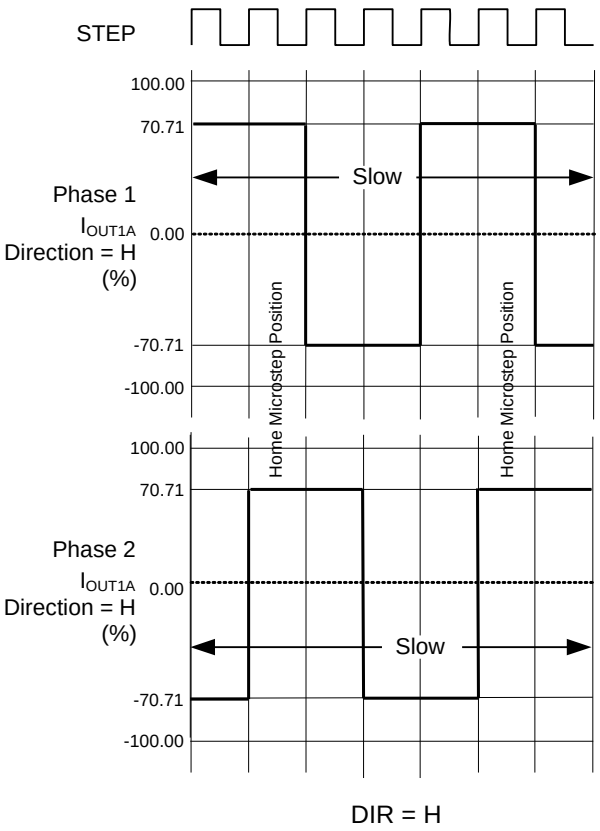


Figure 6. Decay Mode for Full-Step Increments

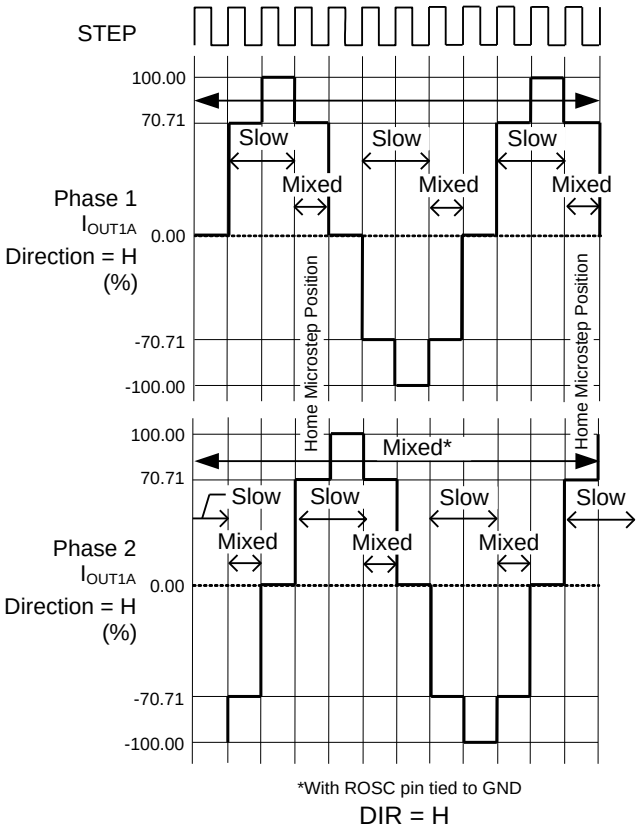


Figure 7. Decay Modes for Half-Step Increments

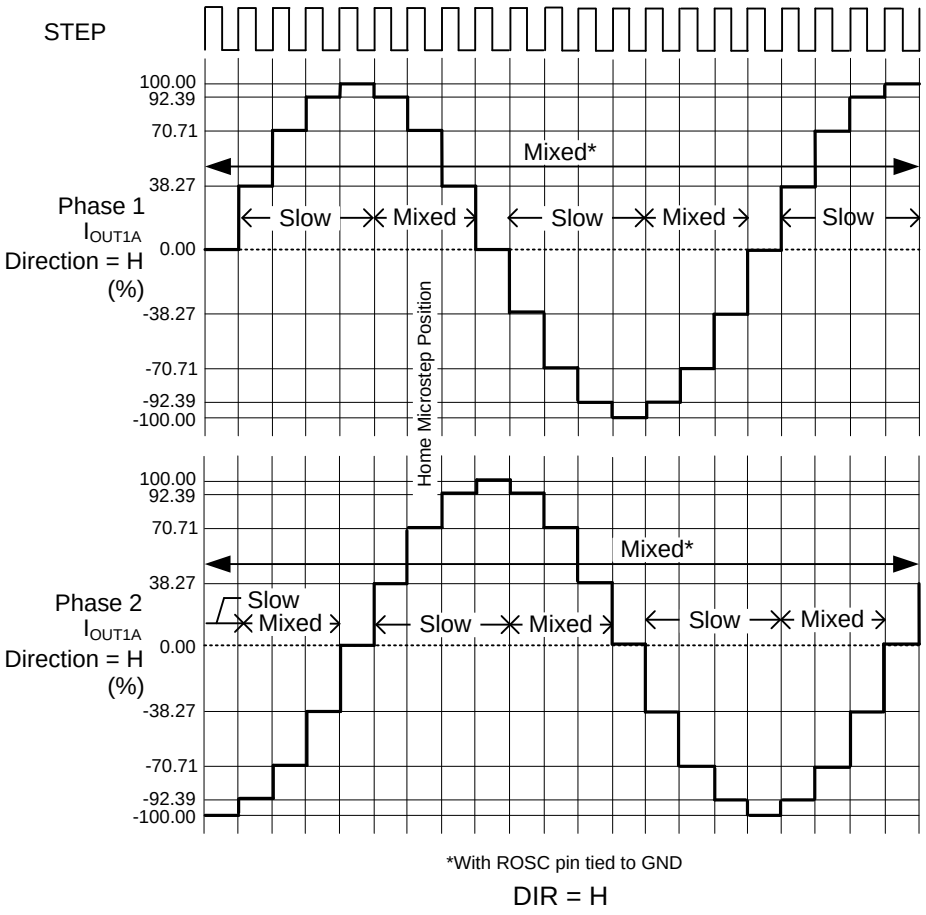


Figure 8. Decay Modes for Quarter-Step Increments

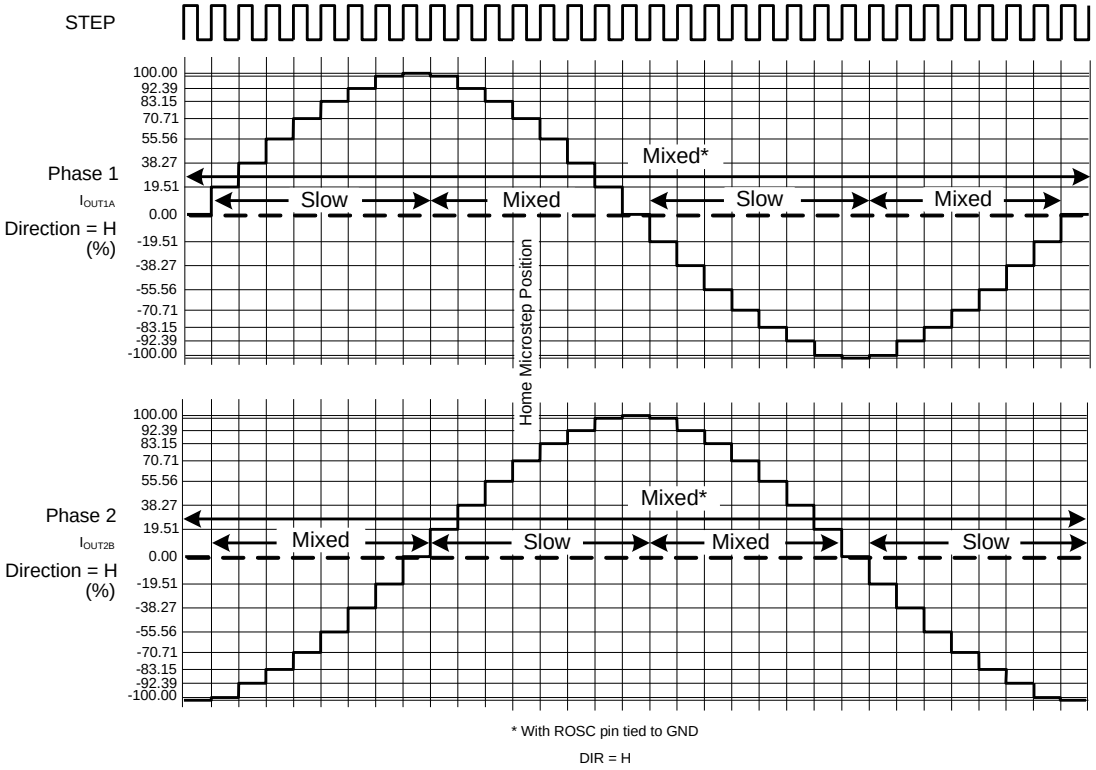


Figure 9. Decay Modes for Eighth-Step Increments

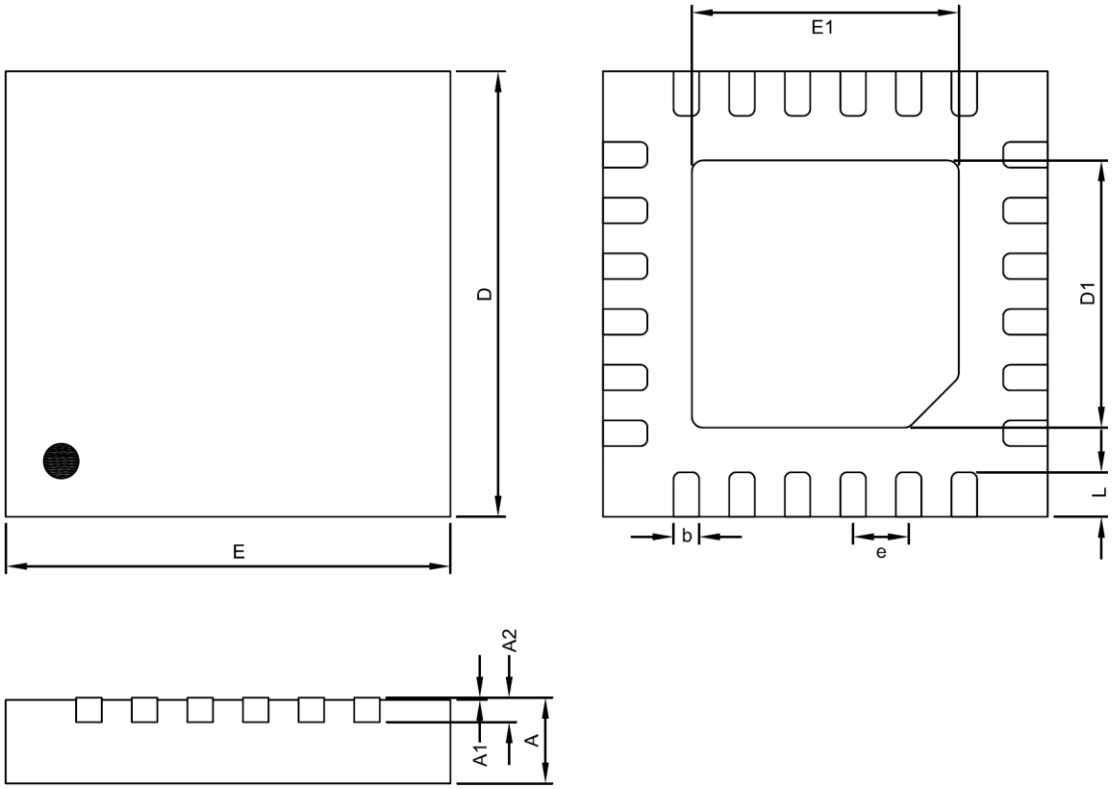
Table 2. Step Sequencing Settings

Home microstep position at Step Angle 45º; DIR = H

Full Step #	Half Step #	1/4 Step #	1/8 Step #	Phase 1 Current [%I tripMax] (%)	Phase 2 Current [%I tripMax] (%)	Step Angle (º)
	1	1	1	100.00	0.00	0.0
				99.52	9.80	5.6
			2	98.08	19.51	11.3
				95.69	29.03	16.9
		2	3	92.39	38.27	22.5
				88.19	47.14	28.1
			4	83.15	55.56	33.8
				77.30	63.44	39.4
1	2	3	5	70.71	70.71	45.0
				63.44	77.30	50.6
			6	55.56	83.15	56.3
				47.14	88.19	61.9
		4	7	38.27	92.39	67.5
				29.03	95.69	73.1
			8	19.51	98.08	78.8
				9.80	99.52	84.4
	3	5	9	0.00	100.00	90.0
				–9.80	99.52	95.6
			10	–19.51	98.08	101.3
				–29.03	95.69	106.9
		6	11	–38.27	92.39	112.5
				–47.14	88.19	118.1
			12	–55.56	83.15	123.8
				–63.44	77.30	129.4
2	4	7	13	–70.71	70.71	135.0
				–77.30	63.44	140.6
			14	–83.15	55.56	146.3
				–88.19	47.14	151.9
		8	15	–92.39	38.27	157.5
				–95.69	29.03	163.1
			16	–98.08	19.51	168.8
				–99.52	9.80	174.4

Full Step #	Half Step #	1/4 Step #	1/8 Step #	Phase 1 Current [%I] (%)	Phase 2 Current [%I tripMax] (%)	Step Angle (º)
	5	9	17	–100.00	0.00	180.0
				–99.52	–9.80	185.6
			18	–98.08	–19.51	191.3
				–95.69	–29.03	196.9
		10	19	–92.39	–38.27	202.5
				–88.19	–47.14	208.1
			20	–83.15	–55.56	213.8
				–77.30	–63.44	219.4
3	6	11	21	–70.71	–70.71	225.0
				–63.44	–77.30	230.6
			22	–55.56	–83.15	236.3
				–47.14	–88.19	241.9
		12	23	–38.27	–92.39	247.5
				–29.03	–95.69	253.1
			24	–19.51	–98.08	258.8
				–9.80	–99.52	264.4
	7	13	25	0.00	–100.00	270.0
				9.80	–99.52	275.6
			26	19.51	–98.08	281.3
				29.03	–95.69	286.9
		14	27	38.27	–92.39	292.5
				47.14	–88.19	298.1
			28	55.56	–83.15	303.8
				63.44	–77.30	309.4
4	8	15	29	70.71	–70.71	315.0
				77.30	–63.44	320.6
			30	83.15	–55.56	326.3
				88.19	–47.14	331.9
		16	31	92.39	–38.27	337.5
				95.69	–29.03	343.1
			32	98.08	–19.51	348.8
				99.52	–9.80	354.4

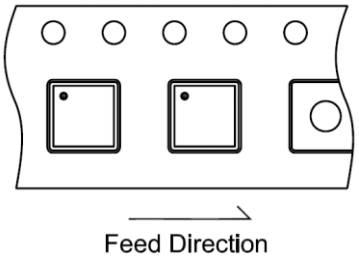
Package Information



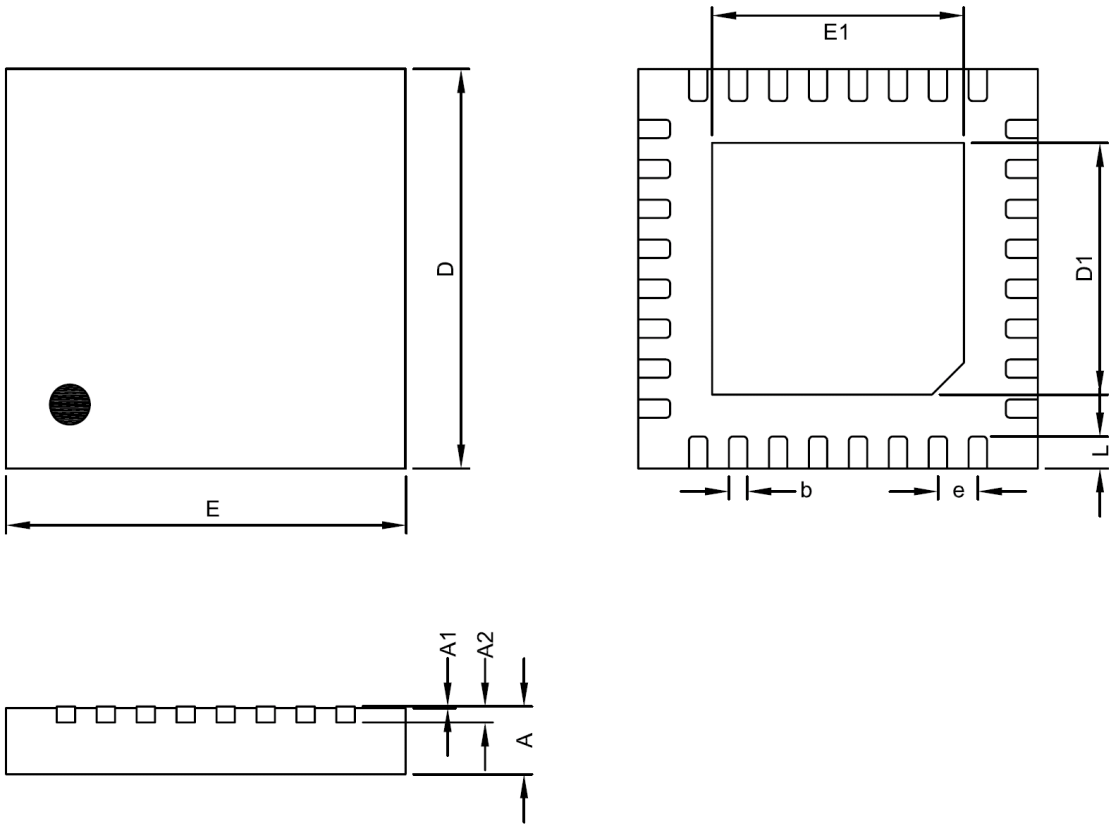
TQFN4X4-24 Package

Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.0276	0.0295	0.0315
A1	0.00	- - -	0.05	0.0000	- - -	0.0020
A2	0.20 REF			0.0079 REF		
D	3.95	4.00	4.05	0.1555	0.1575	0.1594
E	3.95	4.00	4.05	0.1555	0.1575	0.1594
D1	2.50	2.70	2.85	0.0984	0.1063	0.1122
E1	2.50	2.70	2.85	0.0984	0.1063	0.1122
b	0.18	0.23	0.30	0.0071	0.0091	0.0118
e	0.50 BSC			0.0197 BSC		
L	0.35	0.40	0.45	0.0118	0.0138	0.0177

Taping Specification



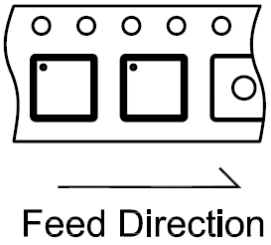
PACKAGE	Q'TY/REEL
TQFN4X4-24	3,000 ea



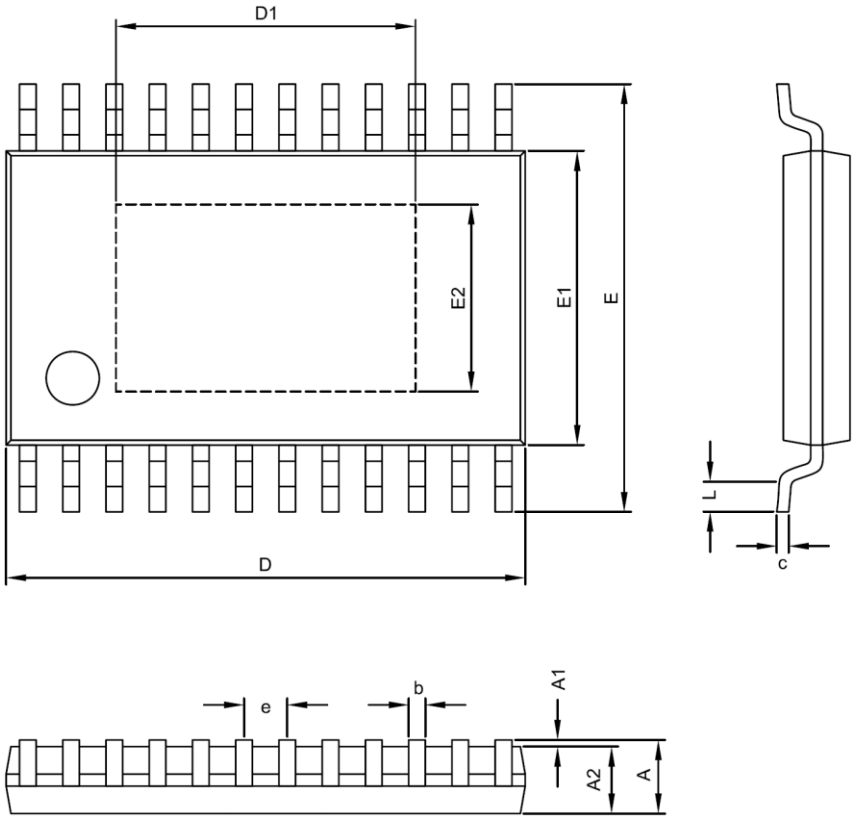
QFN5X5-32 Package

Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.90	1.00	0.0315	0.0354	0.0394
A1	0.00	- - -	0.05	0.0000	- - -	0.0020
A2	0.20 REF			0.0079 REF		
D	4.95	5.00	5.05	0.1949	0.1969	0.1988
E	4.95	5.00	5.05	0.1949	0.1969	0.1988
D1	3.05	3.20	3.30	0.1201	0.1260	0.1300
E1	3.05	3.20	3.30	0.1201	0.1260	0.1300
b	0.18	0.25	0.30	0.0071	0.0098	0.0118
e	0.50 BSC			0.0197 BSC		
L	0.30	0.40	0.45	0.0118	0.0157	0.0177

Taping Specification



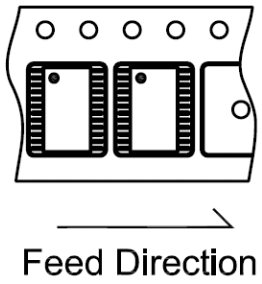
PACKAGE	Q'TY/REEL
QFN5X5-32	3,000 ea



TSSOP-24(FD) Package

Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	- - -	- - -	1.20	- - -	- - -	0.048
A1	0.00	- - -	0.15	0.000	- - -	0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
D	7.70	7.80	7.90	0.303	0.307	0.311
D1		4.50 REF			0.177 REF	
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.169	0.173	0.177
E2		2.70 REF			0.106 REF	
c	0.09	- - -	0.20	0.004	- - -	0.008
b	0.19	0.22	0.30	0.008	0.009	0.012
e		0.65 BSC			0.026 BSC	
L	0.45	0.60	0.75	0.018	0.024	0.030

Taping Specification



PACKAGE	Q'TY/REEL
TSSOP-24 (FD)	3,000 ea