CLAF-Like Plus (Close Loop Auto Focus-Like Plus) VCM Driver for Smart Phone

Features

- **Bi-direction :11bit or 10 bit resolution +/- 130mA current control**
  Uni-direction : 10 bit resolution 130mA current control
- **Tvib Compensation for All Operation Mode**
- **Supply voltage range(VCC) : 2.4V to 3.3V**
- **Supply voltage range(VDDIO) : 1.6V to 3.3V**
- **Fast mode I2C interface compatible(1.8V interface available)**
- **Support Two I2C Slave ID**
- **3W SPI interface for Gyro sensor**
- **Power on reset(POR)**
- **WLCSP2X5-10 package**

Applications

- **Mobile camera**
- **Digital still camera**
- **Camcorder**
- **Web camera**
- **Nano actuator**

General Description

The G2066 is a single 11-bit or 10-bit DAC with +/-130mA output current source and sinking capability. Designed for linear control of voice coil motors, the G2066 is capable of operating voltage up to 3.3V. The SRC mode highly improves the actuator's settling time and tolerance coverage compared with conventional LSC(Linear Slope Control) mode. The DAC is controlled via an I2C serial interface that operates DAC by clock rates up to 1MHz.

The G2066 incorporates with a POR(Power On Reset) circuit, power down mode and VCM open/short fault detection. POR circuit gets to operate when VCC(supply power) turns on. The output current keeps 0mA until valid register value takes place. During the power down mode, it consumes max.12μA.

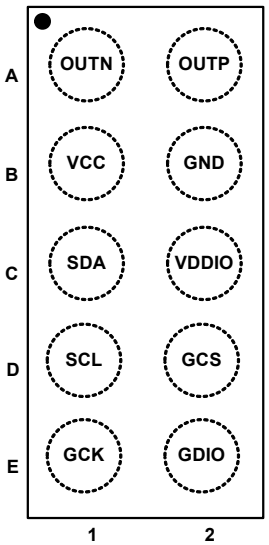
The G2066 is designed for auto focus and optical zoom for mobile cameras, digital still cameras, camcorders and other nano actuator applications.

Ordering Information

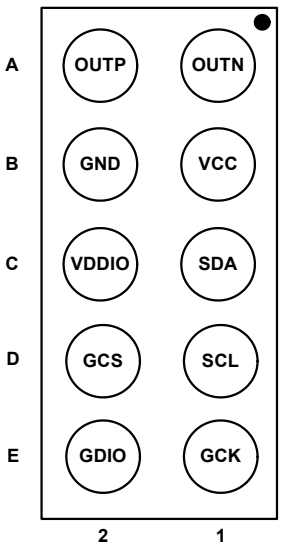
ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE (Green)
G2066L71U	2066	-40°C to +85°C	WLCSP2X5-10 (Ball Size: 0.055 MM)

Note: L7: WLCSP2X5-10
1: Ball Size
U: Tape & Reel
Green : Lead Free / Halogen Free.

Pin Configuration



Top View
WLCSP2X5-10



Bottom View
WLCSP2X5-10

Absolute Maximum Ratings*1

Power supply voltage (VCC,VDDIO) .... -0.3V to 3.6V
Control input voltage (SDA, SCL, GCS,GCK,GDIO) . . . . . -0.3 to VCC+0.3V
Thermal Resistance of Junction to Ambient (θ_{JA})
WLCSP2X5-10 . . . . . TBD°C/W
Continuous Power Dissipation (T_A = +25°C)
WLCSP2X5-10. . . . . TBDmW
Operating Temperature range (Topr). . . . .-40 to 85°C
Junction Temperature (T_J) . . . . . 125°C
Reflow Temperature (soldering, 10sec). . . . . .260°C
ESD (HBM) 2KV
ESD (MM) 200V

Recommended Operating Conditions

Power supply voltage (VCC) . . . . . 2.4V to 3.3V
Power supply voltage (VDDIO) . . . . . 1.6V to 3.3V
Control input voltage (SDA, SCL) . .. . 0 to VCC
Control input voltage (GCS, GCK, GDIO) . . . . . 0 to VDDIO
I^2C bus transmission rate (SCL) 400kHz
Operating Temperature range (Topr). . . . .-25 to 85°C

Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range (Topr) may result in IC damage. The implementation of a physical safety measures such as a fuse should be considered when you use the IC in a special mode in which you anticipate the absolute maximum ratings may be exceeded.

Electrical Characteristics

(VCC=2.8V, VDDIO=1.8V, T_A= 25°C)

The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified.

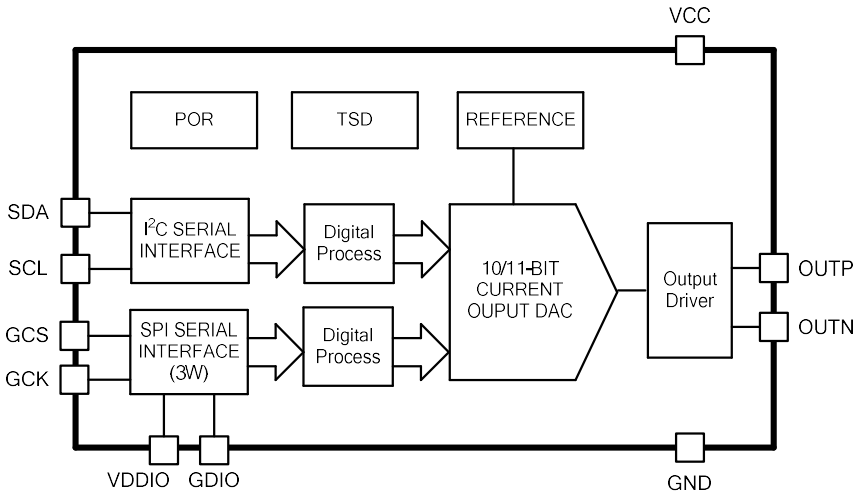
PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
General							
Power Voltage		VCC		2.4	---	3.6	V
		VDDIO		1.6	---	3.6	V
VCC Current		I_{PD}	Power down mode	0	---	12	μA
		I_Q	Quiescent mode	0.2	---	1.5	mA
VCC UVLO		VUVLO	Rising	---	2.2	---	V
			Falling	---	1.6	---	V
I2C PIN: SCL, SDA							
Input Current			SCL,SDA = 3.0V	-1	---	+1	μA
High Level Input Voltage		V_{IH}		1.4	---	---	V
Low Level Input Voltage		V_{IL}		---	---	0.54	V
Glitch rejection(1)				---	50	---	ns
SDA Low Level Output Voltage (open drain)		V_{OL}	Sink current = 3mA	---	---	0.4	V
Setup time for normal operation		t_{OPR}		200	---	---	μs
SPI PIN: GCS, GCK, GDIO							
Output High Voltage		V_{OH_G}	Source 3mA	V_{DDIO}-0.2	---	--	V
Output Low Voltage		V_{OL_G}	Sink 3mA	---	---	0.2	V
Input High Voltage		V_{IH_G}		1.3	---	---	V
Input Low Voltage		V_{IL_G}		---	---	0.85	V
VCM driver							
Current resolution(2)(3)			DACLM=0, 127μA/LSB	---	11	---	bits
			DACLM=1, 254.2μA/LSB	---	10	---	
Positive	INL(2) (3)	INL		-4	---	+4	LSB
	DNL(2) (3)	DNL		-1	---	+1	LSB
Negative	INL(2) (3)	INL		-4	---	+4	LSB
	DNL(2) (3)	DNL		-1	---	+1	LSB
Total Resistance of the Output(1) (Sensing Resistor + Tr On Resistance)			Output Current=100mA	---	2.5	4.5	Ω
Maximum output current		Imax		123.5	130	136.5	mA
Output current @ power down		I_{OUTPD}		-1	---	+1	μA

1. These are guaranteed by design and characterization.
2. Linearity is guaranteed for code 32 through code 992 in uni-direction setting.
3. Linearity is guaranteed for code 32 through code 992 and code1056 through code 2015 in 11bits, bi-direction setting.

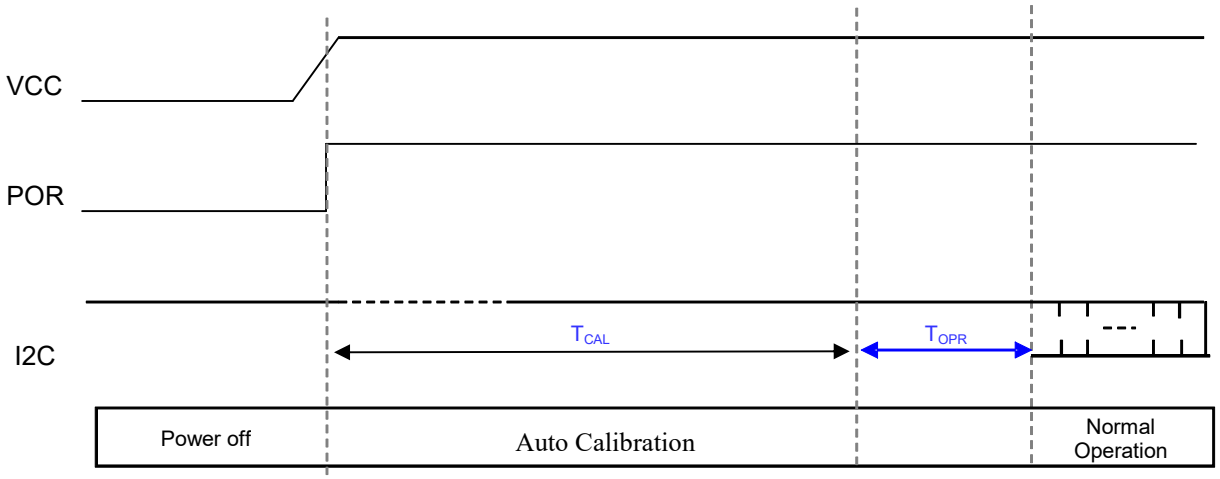
Pin Description

PIN	NAME	I/O	FUNCTION
A1	OUTN	O	Driver Output 1.
A2	OUTP	O	Driver Output 2
B1	VCC	POWER	Power supply voltage.
B2	GND	GROUND	GROUND
C1	SDA	I/O	I2C interface (Data)
C2	VDDIO	POWER	SPI interface Output Power Supply Voltage
D1	SCL	I/O	I2C Interface Clock pin.
D2	GCS	I/O	SPI interface CS
E1	GCK	I/O	SPI interface Clock
E2	GDIO	I/O	SPI interface Input / Output

Block Diagram

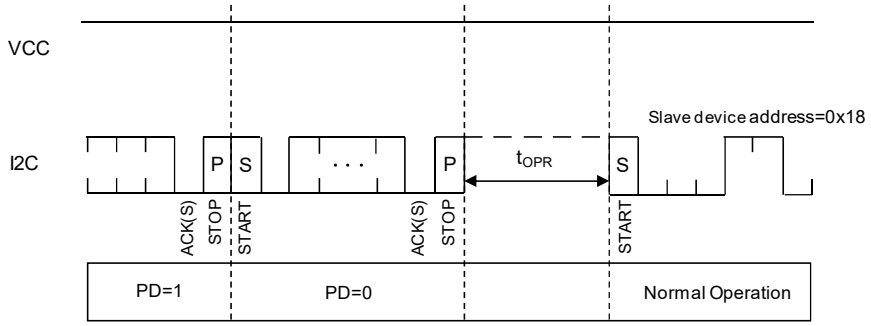


Power on sequence



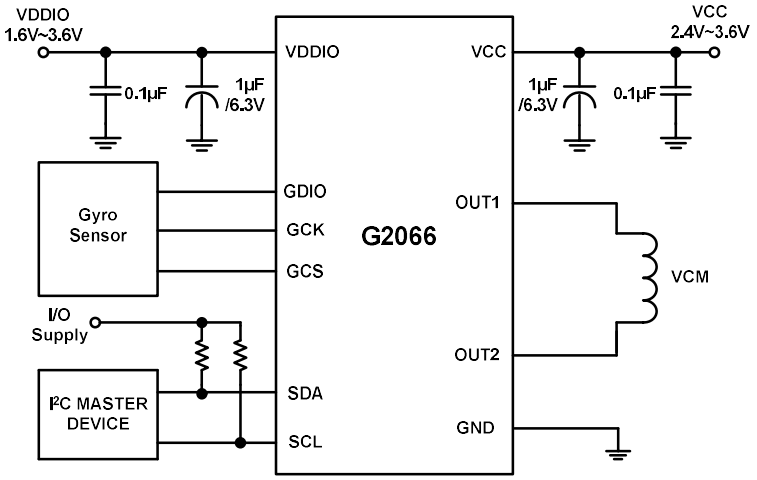
∗ G2066 requires waiting time (delay time) of T_{CAL} after VCC is set “High”.
∗ When VCC power on, offset-calibration function operate(T_{CAL}).
∗ t_{CAL} Approximate to 3ms for power on bias settle down.

PD (Power Down) sequence



∗ G2066 requires waiting time (delay time) for auto-calibration
∗ When PD reset takes place, VCM fault detecting function is operated.

Typical Application Circuit
Bi-direction Driving

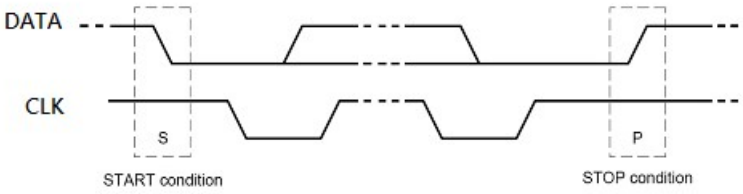


∗ Power supply decoupling capacitor should be placed as close to the VCC/VDDIO and GND as possible.
∗ The value of capacitor is recommended more than 1μF.
∗ PCB pattern of VCC, GND, OUT1 and OUT2 should be as short and wide as possible.

I2C Protocol

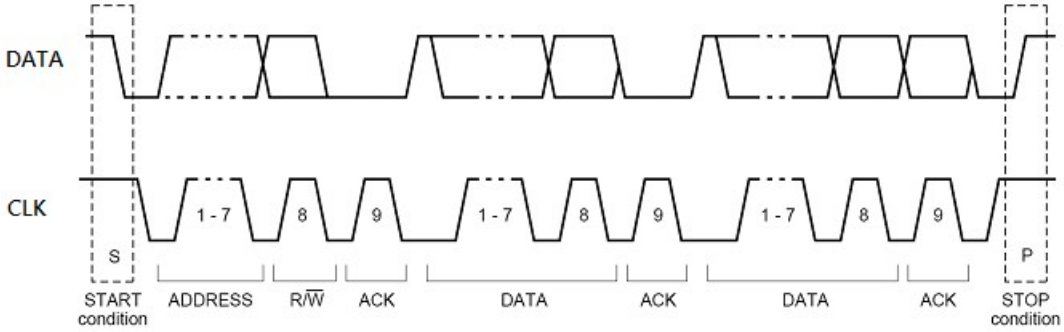
Register
I2C format
VCM driver access (Slave ID : 0x18, CLK=SCL, DATA=SDA)
VCM driver access (Slave ID : 0x7C,CLK=SDA, DATA=SCL)

Start and Stop condition



Within the procedure of the I2C-bus, unique situations arise which are defined as START(S) and STOP(P) conditions. A HIGH to LOW transition on the SDA line while SCL is HIGH is one of such unique cases. This situation indicates a START condition. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition.

Complete I2C Data Transfer



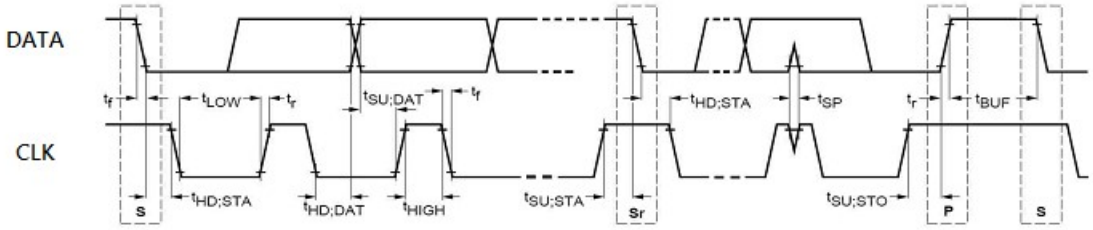
Data transfers follow the above format. After the START condition(S), a slave address is sent. A data transfer is always terminated by a STOP condition(P) generated by the master. However, if the master still needs to communicate on the bus, it can generate a repeated data transfer.

I²C Timing

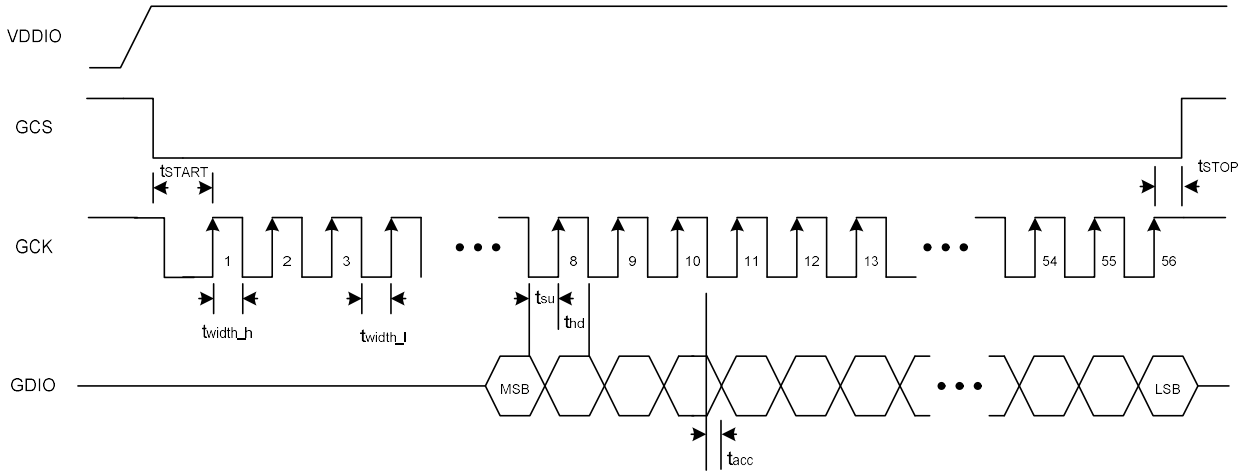
PARAMETER	SYMBOL	MIN.	MAX.	UNIT
SCL clock frequency	f_{SCL}	0	1000	kHz
Hold time (repeated) START condition.	$t_{HD;STA}$	0.6	---	µs
Low period of the SCL clock	t_{LOW}	1.3	---	µs
High period of the SCL clock	t_{HIGH}	0.6	---	µs
Set-up time for a repeated START condition	$t_{SU;STA}$	0.6	---	µs
Data hold time	$t_{HD;DAT}$(1)	---	0.9	µs
Data set-up time	$t_{SU;DA}T$	100	---	ns
Rise time of both SDA and SCL signals	t_r	$20+0.1C_b$(2)	300	ns
Fall time of both SDA and SCL signals	t_f	$20+0.1C_b$(2)	300	ns
Set-up time for STOP condition	$t_{SU;STO}$	0.6	---	µs
Bus free time between a STOP and START condition	t_{BUF}	1.3	---	µs
Capacitive load for each bus line	C_b	---	400	pF
Pulse width of spike suppress	t_{SP}	0	50	ns

(1) A master device must provide a hold time of at least 100ns for the SDA signal to bridge the undefined region of the falling edge of SCL. The maximum $t_{HD;DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.

(2) C_b is the total capacitance of one bus line in pF, tr and tf are measured between $0.3V_{CC}$ to $0.7V_{CC}$.



SPI Timing



*No power on sequence for VDDIO, GCS, CCK and GDIO are tracking VDDIO as use for output.

Symbol	Parameter	Min	Max	Unit
F_{GCK}	GCK clock frequency	0	10	MHz
t_{START}	GCS falling to GCK rising edge	10	-	ns
t_{STOP}	GCK rising to GCS rising edge	10	-	ns
t_{width_h}	GCK high pulse width	50	-	ns
t_{width_l}	GCK low pulse width	50	-	ns
t_{SU}	GDIO to GCK Setup time	10	-	ns
t_{HD}	GDIO to GCK hold time	10	-	ns
t_{acc}	GDIO access time after GCK falling edge	-	20	ns

Serial Control Map Table

NAME	Addr.	Default	R/W	Data							
				D7	D6	D5	D4	D3	D2	D1	D0
IC Info.	0x00	0X66	R	IC Manufacturer ID				IC Model			
Control	0x02	0x00	R/W	BiDEn				DACLM	reserved	RING	PD
VCM MSB	0x03	0x04	R/W						D10	D9	D8
VCM LSB	0x04	0x00	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Status	0x05	0x00	R				TSD			SpiStsErr	BUSY
Ring Mode Prescale	0x06	0xE3	R/W	SRC2	SRC1	SRC0		MS	PRESC2	PRESC1	PRESC0
Resonance0 (SRC Mode)	0x07	0x20	R/W	HSRCT2x		SRCT2x[5:0]					
S2 (ASRC)	0x07	0x20	R/W	S2							
S0 (ASRC)	0x08	0x20	R/W	S0							
S1 (ASRC)	0x09	0x20	R/W	S1							
S3 (ASRC)	0x0A	0x20	R/W	S3							
S4 (ASRC)	0x0B	0x20	R/W	S4							
D0	0x0C	0x33	R/W	D0							
D1	0x0D	0x66	R/W	D1							
D2	0x0E	0x99	R/W	D2							
D3	0x0F	0xCC	R/W	D2							
A1	0x10	0x00	R/W	A1							
A2	0x11	0x00	R/W	A2							
LM	0x12	0xE3	R/W	LM							
LH	0x13	0x00	R/W	LH							
LL	0x14	0x00	R/W	LL							
LT	0x15	0x00	R/W	LT							

Please contact GMT Engineer while using register table above.

Register Description

NAME	Addr.	Default	R/W	Data
IC Info	0x00	0x66	R	0x66

NAME	Addr.	Default	R/W	Data							
CONTROL	0x02	0x00	R/W	BiDEn				DACLM	reserved	RING	PD

BiDEn : Bi-direction mode selection
0 : Uni-direction mode(default)
1 : Bi-direction mode

DACLM: DAC length mode
0 : 11 bits(default)
1 : 10 bits

RING : Ringing Control mode selection
0 : Direct mode
1 : Ringing control mode

PD : Power down mode
0 : Normal operation mode
1 : Power down mode(active HIGH)

∗ G2066 requires waiting time(delay time) of t_{OPR} after PD reset takes place.

NAME	Addr.	Default	R/W	Data							
VCM MSB	0x03	0x04	R/W						D10	D9	D8
VCM LSB	0x04	0x00	R/W	D7	D6	D5	D4	D3	D2	D1	D0

When BiDEn='0'
D[9:0]: DAC data input
output current = (D[9:0]/1023) X 130mA

When BiDEn='1' , DACLM='0'
D[10] : DAC Direction bit
0 : Negative direction
1 : Positive direction
D[9:0]: DAC data input
Positive output current = (D[9:0]) X 130/1023 [mA]
Negative output current = - (1024 - D[9:0]) X 130/1023 [mA]

* Zero current code = 1024code

When BiDEn='1' , DACLM='1'
D[9] : DAC Direction bit
0 : Negative direction
1 : Positive direction
D[8:0]: DAC data input
Positive output current = (D[8:0]) X 130/511 [mA]
Negative output current = - (512 - D[8:0]) X 130/511 [mA]

* Zero current code = 512code

NAME	Addr.	Default	R/W	Data							
Status	0x05	0x00	R/W				TSD			SpiStsErr	BUSY

BUSY : Busy status 1:DAC output is busy 0:DAC output is not busy. User can't write any register excepts control register (0x02) when IC is busy
SpiStsErr : Indicate SPICtl or SPIContDiv setting error.
TSD : Thermal status flag 0:temperature over 150°l ,status flag active

NAME	Addr.	Default	R/W	Data							
MODE	0x06	0xE3	R/W	SRC2	SRC1	SRC0		MS	PRESC2	PRESC1	PRESC0

PRESC0=Default value is “H”

SRC[2:0]: SRC mode select

SRC[2:0]	Mode
000	SRC4
001	SRC2
010	SRC2.5
011	SRC3
100	SRC3.5
101	ASRC1
110	ASRC2(75%)
111	ASRC2.5(50%)

PRESC[2:0]: Pre-scale

PRESC[2:0]	Period	pre-scale divider
000	Tvib x 2 (double)	x 8
001	Tvib x 1 (default)	x 4
010	Tvib x 1/2 (half)	x 2
011	Tvib x 1/4 (quarter)	x 1
100	Tvib x 8 (octuple)	x 32
101	Tvib x4 (quadruple)	x 16
110	reserved	
111	reserved	

MS: Mode Select, MS=1 for ASRC Mode, MS=0 for SRC mode.

Ringing Control Set up Method

SRC Slew Rate Control scheme

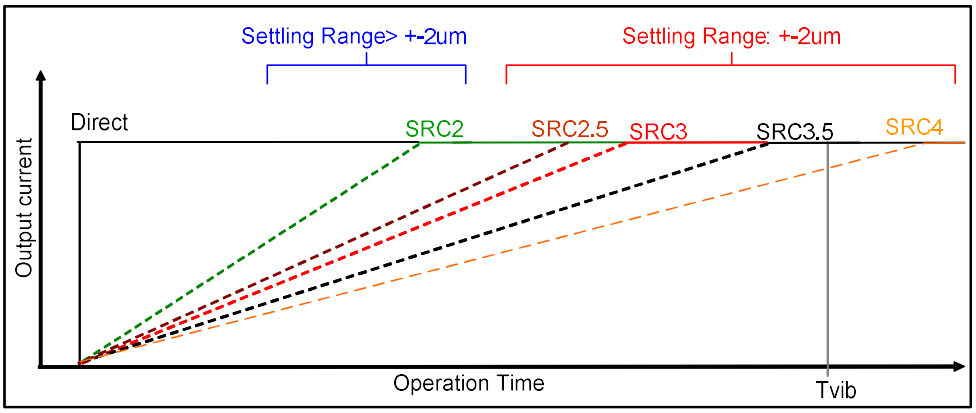
Ring	SRC[2:0]	Mode	Current Operation time(1)	Actuator Tvib Tolerance Coverage(2)	Settling Range
0	Xxx	Direct	---	---	---
1	000	SRC4	1.2*Tvib(3)	± 37 %	≤2μm
1	001	SRC2	0.48*Tvib	± 9 %	>2μm
1	010	SRC2.5	0.64*Tvib	± 17 %	≤2μm
1	011	SRC3	0.72*Tvib	± 19 %	
1	100	SRC3.5	0.92*Tvib	± 25 %	

(1) Driver current moving time

(2) This is just design spec. Tolerance can be changed by mechanical characteristics of specific VCM Convergence range is moving stroke of ±10%.

(3) Tvib is a vibration(resonance)period of VCM.

SRC Actuation Time



NAME	Addr.	Default	R/W	Data		
RSNCX	0x07~0x0B	0x20	R/W	HSRCT		SRCT

SRCT[5]=Default value is “H”

When use for Tvib

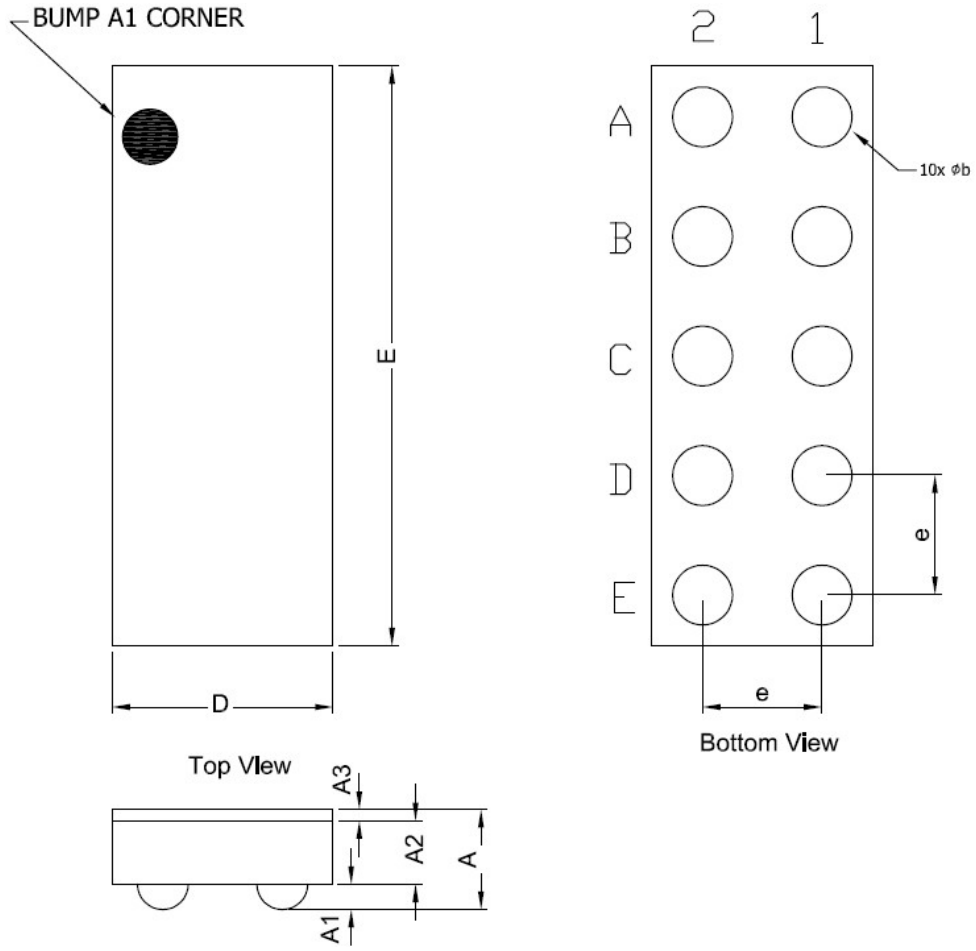
HSRCT=0 : SRCT[5:0] SRC period(T_{SRC})=6.3ms+SRCT[5:0]*0.1ms

HSRCT=1 : SRCT[5:0] SRC period(T_{SRC})=3.1ms+SRCT[5:0]*0.05ms

NAME	Addr.	Default	R/W	Data							
				D7	D6	D5	D4	D3	D2	D1	D0
S2 (ASRC)	0x07	0x20	R/W	S2							
S0 (ASRC)	0x08	0x20	R/W	S0							
S1 (ASRC)	0x09	0x20	R/W	S1							
S3 (ASRC)	0x0A	0x20	R/W	S3							
S4 (ASRC)	0x0B	0x20	R/W	S4							
D0	0x0C	0x33	R/W	D0							
D1	0x0D	0x66	R/W	D1							
D2	0x0E	0x99	R/W	D2							
D3	0x0F	0xCC	R/W	D2							
A1	0x10	0x00	R/W	A1							
A2	0x11	0x00	R/W	A2							
LM	0X12	0x00	R/W	LM							
LH	0X13	0x00	R/W	LH							
LL	0X14	0x00	R/W	LL							
LT	0X15	0X00	R/W	LT							

Please contact GMT Engineer while using register table above.

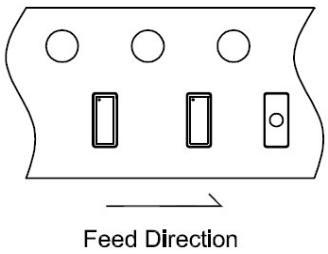
Package Information



WLCSP2X5-10 Package

Symble	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.270	0.300	0.330	0.0106	0.0118	0.0130
A1	0.045	0.055	0.065	0.0018	0.0022	0.0026
A2	0.200	0.220	0.240	0.0079	0.0087	0.0094
A3	0.025			0.0010		
D	0.700	0.740	0.780	0.0276	0.0291	0.0307
E	2.040	2.080	2.120	0.0803	0.0819	0.0835
b	0.185	0.200	0.215	0.0073	0.0079	0.0085
e	0.40 BSC			0.0157 BSC		

Taping Specification



PACKAGE	Q'TY/REEL
WLCSP2X5-10	3,000 ea