G2194

PMIC for Color Electronic Paper Display

Features

- **2.9V to 9.0V Input Voltage Range**
- **Auto Buck-Boost Converter VP1/VP2 and Boost Converter VP3 for the Power Input of Positive Rails**
- **Inverting Buck-Boost Converter VN1/VN2/VN3 for the Power Input of Negative Rails**
- **Six Adjustable LDOs for Source Driver Supply:**
  -VPOS1/VNEG1: ±2V to ±12V, 200mA(max.)
  -VPOS2/VNEG2: ±5V to ±20V, 300mA(max.)
  -VPOS3/VNEG3: ±9V to ±30V, 500mA(max.)
  -Accurate Output Voltage Tracking
  VPOS2/3+VNEG2/3= ±50mV @ ±15V
  -DVS function
- **Three Charge Pumps for Gate Driver Supply:**
  -VGH1/VGH2: 10V to 50V, 30mA(max.)
  -VGL: -15V to -40V, 30mA(max.)
- **Adjustable DC VCOM and Toggle VCOM Driver for Accurate Panel Backplane Biasing**
  - **-5V to +5V**
  - **±1.5% Accuracy**
  - **9-Bit DACs control**
- **Internal Active Discharge for VPOSx/VNEGx /VCOM, and external VGHx Discharge control**
- **Thermistor Monitoring**
  - **-10°C to +85°C Temperature Range**
  - **±1.0°C Accuracy from 0°C to 50°C**
- **I²C Compatible Interface (Slave Address 0x48H)**
- **Support Post Drive Mode(Night Mode)**
- **Protection: UVLO, OTP, OCP, SCP, UVP**
- **QFN8x8-72**

Applications

- **Color EPD Power Supplies**

General Description

The G2194 is a single-chip power management IC (PMIC) for color electronic paper displays (EPD) that provides source and gate-driver power supplies, a VCOM amplifier, and a temperature sensor. All rails are adjustable through the I²C interface to accommodate specific panel requirements.

The G2194 is available in 72-pin QFN (8X8) package and is specified over the -40°C to +85°C extended temperature range.

Ordering Information

ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE (Green)
G2194HJ1U	2194	-40°C to +85°C	QFN8X8-72

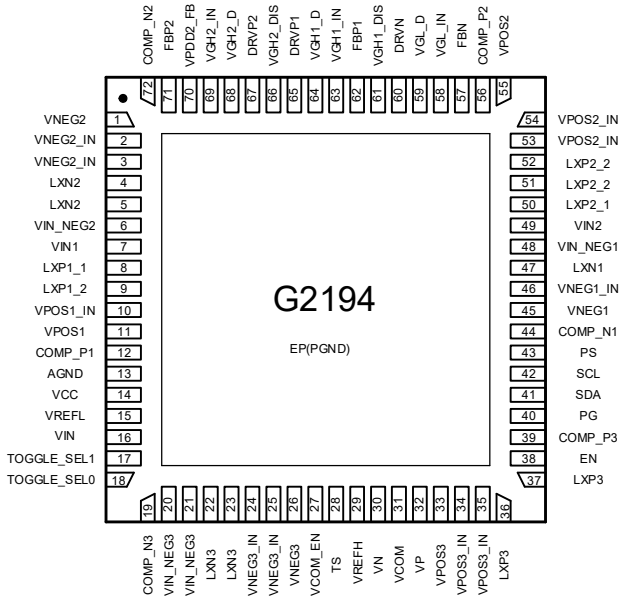
Note: HJ:QFN8x8-72

1: Bonding code

U: Tape & Reel

Green: Lead Free / Halogen Free

Pin Configuration



Absolute Maximum Ratings*1

VINx, VIN_NEGx Input Voltage. . . . . .-0.3V to +9.5V
VPOS1_IN, VPOS1, LXP1_x input Voltage.. .-0.3V to 14V
VNEG1_IN, VNEG1, LXN1, VNEG1 input Voltage . . . . . -14V to -0.3V
VPOS2_IN, VPOS2, LXP2_xinput Voltage. . .-0.3V to 20V
VNEG2_IN, VNEG2, LXN2, VNEG2 input Voltage . . . . . -20V to -0.3V
VPOS3_IN, VPOS3, LXP3, VGHx_IN, VGHx_D, DRVPx , VP, VCOM input Voltage . . . . . .-0.3V to 35V
VNEG3_IN, VNEG3, LXN3, VNEG3,VGL_IN, VGL_D, DRVN, VN, VCOM input Voltage . . . . . .-35V to -0.3V
SDA, SCL, EN, VCOM_EN, TS, PG, FBPx, FBN, VCC, VPDD_FB, COMP_Px,COMP_Nx, VREFH, VREFHL, PS, Toggle_SEL0, Toggle_SEL1 Input Voltage . . . . . -0.3V to +3.6V

Thermal Resistance Junction to Ambient, (θ_{JA})*
QFN8X8-72 . . . . . .24.9 °C/W
Continuous Power Dissipation (T_A = +25°C)*
QFN8X8-72 . . . . . 5020 mW
Operation Temperature . . . . . .-40°C to +85°C
Junction Temperature . . . . . 160°C
Storage Temperature Range . . . . . -65°C to 160°C
ESD Susceptibility (HBM) 2kV (Note2)
Reflow Temperature (soldering, 10sec) . . . . . 260°C

Recommended Operation Conditions

VINx,VIN_NEGx . . . . . 2.9V to 9V
VGHx_IN . . . . . 5V to 30V
VGL_IN . . . . . 30V to -5V
Operating Ambient Temperature (T_A) . . .-10°C to 85°C

* Please refer to Minimum Footprint PCB Layout Section.

1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Device are ESD sensitive. Handling precaution recommended. The Human Body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.

Electrical Characteristics

(VIN=VIN1=VIN2=VIN_NEG1=VIN_NEG2=VIN_NEG3= 3.6V, T_A=25°C)

The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
GENERAL						
Supply Voltage	V_{IN}	VPOS3[9:0] setting≧9.5V	2.9	---	9	V
		VPOS3[9:0] setting< 9.5V	2.9	---	VPOS3[9:0]-0.5	V
VIN UVLO	V_{IN_UVLO}		---	2.8	---	V
VIN UVLO Hysteresis	V_{IN_HYS}		---	0.2	---	V
Quiescent Current in Normal Mode	I_{IN}	EN=High, ON/OFF bit=”0”	---	2	---	mA
Quiescent Current in Standby Mode	I_{STD}	EN=Low, ON/OFF bit=”X”	---	160	---	μA
Quiescent Current in Shutdown Mode	I_{SD}	PS=High	---	15	---	μA
Regulated Voltage for Internal Circuit	V_{CC}	Bypass Cap. Is 2.2μF	---	3.3	---	V
REF High Voltage	V_{REFH}	Bypass Cap. Is 0.1μF	---	2.5	---	V
REF Low Voltage	V_{REFL}	Bypass Cap. Is 0.1μF	---	1.5	---	V
Thermal Shutdown Trip Point	T_{SD}		---	160	---	°C
Thermal Shutdown Hysteresis	T_{HYS}		---	20	---	°C

Electrical Characteristics (Continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
VP1(AUTO BUCK-BOOST REGULATOR)						
Switch Frequency	F_{SW_VP1}	FREQ_VP1[2]=0	---	1000	---	KHz
Power Good Threshold		Fraction of nominal voltage	---	90	---	%
Soft-Start period	T_{SS_VP1}		---	3	---	ms
Switch ON Resistance	R_{ON_P}	V_{IN}=3.6V	---	200	---	mΩ
	R_{ON_N}	V_{IN}=3.6V	---	250	---	mΩ
Switch Current Limit	I_{LIMIT_VP1}	V_{IN}=3.6V	---	2.0	---	A
LX Leakage Current	I_{LXP1_1}, I_{LXP1_2}	V_{LXP1_1}=V_{LXP1_2}=10.3V	-5	---	+5	uA
VPOS1_IN Leakage Current	I_{VPOS1_IN}	V_{LXP1_2}=0V, V_{VPOS1_IN}=10.3V	-5	---	+5	uA
Fault Protection		Fraction of nominal voltage, Falling	---	85	---	%
		Fault Timer	---	16	---	ms
VPOS1(Positive LDO)						
Output Voltage Range	VPOS1	VPOS1[9:0] SET output voltage	2	---	12	V
Soft-Start period	T_{SS_VPOS1}	SS[7:6]=”00”	---	3	---	ms
Power Good Threshold		Fraction of nominal voltage	---	90	---	%
Output Accuracy		VPOS1[9:0]=10V, I_{Load}=20mA	-1	---	1	%
Dropout Voltage	$V_{DROPOUT}$	I_{LOAD}=200mA	---	300	---	mV
Load Regulation-DC	$V_{LOADREG}$	I_{LOAD}=10% to 90%	---	---	1	%
Load Current Range	I_{LOAD}	2.9V≦VIN<3.6V, for maximum output	---	---	150	mA
		VIN≧3.6V, for maximum output	---	---	200	mA
Output Current Limit	I_{LIMIT}		250	---	---	mA
Discharge Impedance to Ground	R_{DIS}		---	250	---	Ω
Fault Protection		Fraction of nominal voltage, Falling	---	85	---	%
		Fault Timer	---	16	---	ms
VP2(AUTO BUCK-BOOST REGULATOR)						
Switch Frequency	F_{SW_VP2}	FREQ_VP2[2]=1	---	1000	---	KHz
Power Good Threshold		Fraction of nominal voltage	---	90	---	%
Soft-Start period	T_{SS_VP2}		---	3	---	ms
Switch ON Resistance	R_{ON_P}	V_{IN}=3.6V	---	150	---	mΩ
	R_{ON_N}	V_{IN}=3.6V	---	200	---	mΩ
Switch Current Limit	I_{LIMIT_VP2}	V_{IN}=3.6V	---	3	---	A
LX Leakage Current	I_{LXP2_1}, I_{LXP2_2}	V_{LXP2_1}=V_{LXP2_2}=15.35V	-5	---	+5	μA
VPOS2_IN Leakage Current	I_{VPOS2_IN}	V_{LXP2_2}=0V, V_{VPOS2_IN}=15.35V	-5	---	+5	μA
Fault Protection		Fraction of nominal voltage, Falling	---	85	---	%
		Fault Timer	---	16	---	ms
VPOS2(Positive LDO)						
Output Voltage Range	VPOS2	VPOS2[9:0] SET output voltage	5	---	20	V
Soft-Start period	T_{SS_VPOS2}	SS[7:6]=”00”	---	3	---	ms
Power Good Threshold		Fraction of nominal voltage	---	90	---	%
Output Accuracy		VPOS2[9:0]=15V, I_{Load}=30mA	-1	---	1	%
Dropout Voltage	$V_{DROPOUT}$	I_{LOAD}=300mA	---	350	---	mV
Load Regulation-DC	$V_{LOADREG}$	I_{LOAD}=10% to 90%	---	---	1	%
Load Current Range	I_{LOAD}	2.9V≦VIN<3.6V,for maximum output	---	---	150	mA
		VIN≧3.6V,for maximum output	---	---	300	mA
Output Current Limit	I_{LIMIT}		350	---	---	mA
Discharge Impedance to Ground	R_{DIS}		---	400	---	Ω
Fault Protection		Fraction of nominal voltage, Falling	---	85	---	%
		Fault Timer	---	16	---	ms

Electrical Characteristics (Continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
VP3(BOOST REGULATOR)						
Switch Frequency	F_{SW_VP3}	FREQ_VP3[2]=0	---	500	---	KHz
Power Good Threshold		Fraction of nominal voltage	---	90	---	%
Soft-Start period	T_{SS_VP3}		---	3	---	ms
Switch ON Resistance	R_{ON_P}	V_{IN}=3.6V	---	150	---	mΩ
	R_{ON_N}	V_{IN}=3.6V	---	100	---	mΩ
Switch Current Limit	I_{LIMIT_VP3}	V_{IN}=3.6V	---	5	---	A
LX Leakage Current	I_{LXP3}	V_{LXP3}=24.4V	-10	---	+10	μA
VPOS3_IN Leakage Current	I_{VPOS3_IN}	V_{LXP3}=0V, V_{VPOS3_IN}=24.4V	-10	---	+10	μA
Fault Protection		Fraction of nominal voltage, Falling	---	85	---	%
		Fault Timer	---	16	---	ms
VPOS3(Positive LDO)						
Output Voltage Range	VPOS3	VPOS3[9:0] SET output voltage	9	---	30	V
Soft-Start period	T_{SS_VPOS3}	SS[7:6]="00"	---	3	---	ms
Power Good Threshold		Fraction of nominal voltage	---	90	---	%
Output Accuracy		VPOS3[9:0]=24V, I_{Load}=30mA	-1	---	1	%
Dropout Voltage	$V_{DROPOUT}$	I_{LOAD}=400mA	---	400	---	mV
Load Regulation-DC	$V_{LOADREG}$	I_{LOAD}=(10% to 90%)*300mA	---	---	1	%
Load Current Range	I_{LOAD}	2.9V≦VIN <3.6V, for maximum output	---	---	200	mA
		3.6V≦VIN <5.0V, for maximum output	---	---	300	mA
		VIN≧5.0V, for default output	---	---	500	mA
Output Current Limit	I_{LIMIT}		510	550	---	mA
Discharge Impedance to Ground	R_{DIS}		---	500	---	Ω
Fault Protection		Fraction of nominal voltage, Falling	---	85	---	%
		Fault Timer	---	16	---	ms
VN1(INVERTING BUCK-BOOST REGULATOR)						
Switch Frequency	F_{SW_VN1}	FREQ_VN1[2]=1	---	1000	---	KHz
Power Good Threshold		Fraction of nominal voltage	---	90	---	%
Soft-Start period	T_{SS_VN1}		---	3	---	ms
Switch ON Resistance	R_{ON_P}	V_{IN}=3.6V	---	250	---	mΩ
	R_{ON_N}	V_{IN}=3.6V	---	250	---	mΩ
Switch Current Limit	I_{LIMIT_VN1}	V_{IN}=3.6V	---	1.8	---	A
LX Leakage Current	I_{LXN1}	V_{LXN1}=V_{VNEG1}=-10.3V	-5	---	+5	μA
Fault Protection		Fraction of nominal voltage, Falling	---	85	---	%
		Fault Timer	---	16	---	ms
VNEG1(Negative LDO)						
Output Voltage Range	VNEG1	VNEG1[9:0] SET output voltage	-12	---	-2	V
Soft-Start period	T_{SS_VNEG1}	SS[7:6]="00"	---	3	---	ms
Power Good Threshold		Fraction of nominal voltage	---	90	---	%
Output Accuracy		VNEG1[9:0]=-10V, I_{Load}=20mA	-1	---	1	%
Dropout Voltage	$V_{DROPOUT}$	I_{LOAD}=200mA	---	300	---	mV
Load Regulation-DC	$V_{LOADREG}$	I_{LOAD}=10% to 90%	---	---	1	%
Load Current Range	I_{LOAD}	2.9V≦VIN<3.6V, for maximum output	---	---	150	mA
		VIN≧3.6V, for maximum output	---	---	200	mA
Output Current Limit	I_{LIMIT}		250	---	---	mA
Discharge Impedance to Ground	R_{DIS}		---	300	---	Ω
Fault Protection		Fraction of nominal voltage, Falling	---	85	---	%
		Fault Timer	---	16	---	ms

Electrical Characteristics (Continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
VN2(INVERTING BUCK-BOOST REGULATOR)						
Switch Frequency	F_{SW_VN2}	FREQ_VN2[2]=1	---	1000	---	KHz
Power Good Threshold		Fraction of nominal voltage	---	90	---	%
Soft-Start period	T_{SS_VN2}		---	3	---	ms
Switch ON Resistance	R_{ON_P}	V_{IN}=3.6V	---	200	---	mΩ
	R_{ON_N}	V_{IN}=3.6V	---	150	---	mΩ
Switch Current Limit	I_{LIMIT_VN2}	V_{IN}=3.6V	---	3	---	A
LX Leakage Current	I_{LXN2}	V_{LXN2}=V_{VNEG2}=-15.35V	-5	---	+5	uA
Fault Protection		Fraction of nominal voltage, Falling	---	85	---	%
		Fault Timer	---	16	---	ms
VNEG2(Negative LDO)						
Output Voltage Range	VNEG2	VNEG2[9:0] SET output voltage	-20	---	-5	V
Soft-Start period	T_{SS_VNEG2}	SS[7:6]="00"	---	3	---	ms
Power Good Threshold		Fraction of nominal voltage	---	90	---	%
Output Accuracy		VNEG2[9:0]=-15V, I_{Load}=30mA	-1	---	1	%
Dropout Voltage	$V_{DROPOUT}$	I_{LOAD}=300mA	---	350	---	mV
Load Regulation-DC	$V_{LOADREG}$	I_{LOAD}=10% to 90%	---	---	1	%
Load Current Range	I_{LOAD}	2.9V≦VIN<3.6V, for maximum output	---	---	150	mA
		VIN≧3.6V, for maximum output	---	---	300	mA
Output Current Limit	I_{LIMIT}		350	---	---	mA
Discharge Impedance to Ground	R_{DIS}		---	500	---	Ω
Fault Protection		Fraction of nominal voltage, Falling	---	85	---	%
		Fault Timer	---	16	---	ms
VN3(INVERTING BUCK-BOOST REGULATOR)						
Switch Frequency	F_{SW_VN3}	FREQ_VN3[2]=0	---	500	---	KHz
Power Good Threshold		Fraction of nominal voltage	---	90	---	%
Soft-Start period	T_{SS_VN3}		---	3	---	ms
Switch ON Resistance	R_{ON_P}	V_{IN}=3.6V	---	150	---	mΩ
	R_{ON_N}	V_{IN}=3.6V	---	100	---	mΩ
Switch Current Limit	I_{LIMIT_VN3}	V_{IN}=3.6V	---	5	---	A
LX Leakage Current	I_{LXN3}	V_{LXN3}=V_{VNEG3}=-24.4V	-10	---	+10	μA
Fault Protection		Fraction of nominal voltage, Falling	---	85	---	%
		Fault Timer	---	16	---	ms
VNEG3(Negative LDO)						
Output Voltage Range	VNEG3	VNEG3[9:0] SET output voltage	-30	---	-9	V
Soft-Start period	T_{SS_VNEG3}	SS[7:6]="00"	---	3	---	ms
Power Good Threshold		Fraction of nominal voltage	---	90	---	%
Output Accuracy		VNEG3[9:0]=-24V, I_{Load}=30mA	-1	---	1	%
Dropout Voltage	$V_{DROPOUT}$	I_{LOAD}=400mA	---	400	---	mV
Load Regulation-DC	$V_{LOADREG}$	I_{LOAD}=(10% to 90%)*300mA	---	---	1	%
Load Current Range	I_{LOAD}	2.9V≦VIN <3.6V, for maximum output	---	---	200	mA
		3.6V≦VIN <5.0V, for maximum output	---	---	300	mA
		VIN≧5.0V, for default output	---	---	500	mA
Output Current Limit	I_{LIMIT}		510	550	---	mA
Discharge Impedance to Ground	R_{DIS}		---	800	---	Ω
Fault Protection		Fraction of nominal voltage, Falling	---	85	---	%
		Fault Timer	---	16	---	ms
VPOS2/3 and VNEG2/3 Tracking(Only for VPOS/VNEG are of opposite sign but same magnitude)						
Difference between VPOS2/3 and VNEG2/3 for 3-Level Output	V_{DIFF}	(VPOS2/3,VNEG2/3)=(+15V ,-15V), I_{LOAD}=±20mA, 0°C to 60°C, 3/7 LEVEL[3]="1" & TRACK2/3="1"	-50	---	50	mV

Electrical Characteristics (Continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
VGH1(Positive Charge-Pump)						
Soft-Start period	T_{SS_VGH1}		---	6	---	ms
Power Good Threshold		Fraction of nominal voltage	---	95	---	%
Switching Frequency	F_{DRVP1}		---	1000	---	KHz
Switch ON Resistance	R_{ON_UP}		---	1.5	3	Ω
	R_{ON_DOWN}		---	1.5	3	Ω
Output Voltage Range	VGH1		10	---	50	V
FBP1 Regulation Voltage	V_{FBP1}		---	1.2	---	V
FBP1 Accuracy	V_{FBP1_REG}		-1	---	1	%
Load Current Range	I_{LOAD}		---	---	30	mA
Fault Protection		V_{FBP1} Falling	---	85	---	%
		Fault Timer	---	16	---	ms
VGH2(Positive Charge-Pump & Post Drive Mode)						
Soft-Start period	T_{SS_VGH2}		---	6	---	ms
Power Good Threshold		Fraction of nominal voltage	---	95	---	%
Switching Frequency	F_{DRVP2}		---	1000	---	KHz
Switch ON Resistance	R_{ON_UP}		---	1.5	3	Ω
	R_{ON_DOWN}		---	1.5	3	Ω
Output Voltage Range	VGH2		10	---	50	V
FBP2 Regulation Voltage	V_{FBP2}		---	1.2	---	V
FBP2 Accuracy	V_{FBP2_REG}		-1	---	1	%
Post Drive VPDD_FB Regulation Voltage	V_{VPDD_FB}		---	VPDD/10	---	V
VPDD_FB Accuracy	$V_{VPDD\_FB\_REG}$	VPDD[7:3]=2.0V,V_{VPDD_FB} tolerance	-10	---	10	mV
VPDD Output Range	V_{VPDD}	VPDD[7:3] SET output voltage	2	---	10	V
VPDD delay time	$T_{VPDD-LEN}$	VPDD_LEN[7:0] SET delay time	0	---	30	s
VPDD delay time accuracy	$T_{VPDD-LEN-A}$		-16	---	+16	%
VDDH_EXT delay time	$T_{VDDH-EXT}$	VDDH_EXT[4:0] SET delay time	0	---	1	s
VDDH_EXT delay time accurcy	$T_{VDDH-EXT-A}$		-16	---	+16	%
Load Current Range	I_{LOAD}		---	---	30	mA
Fault Protection		V_{FBP2} Falling	---	85	---	%
		Fault Timer	---	16	---	ms
VGL(Negative Charge-Pump & Post Drive Mode)						
Soft-Start period	T_{SS_VGH1}		---	6	---	ms
Power Good Threshold		Fraction of nominal voltage	---	95	---	%
Switching Frequency	F_{DRVN}		---	1000	---	KHz
Switch ON Resistance	R_{ON_UP}		---	1.5	3	Ω
	R_{ON_DOWN}		---	1.5	3	Ω
Output Voltage Range	VGL		-40	---	-15	V
FBN Regulation Voltage	V_{FBN}		---	0.3	---	V
FBN Accuracy	V_{FBN_REG}		-10	---	10	mV
VEE_EXT delay time	$T_{VDDH-EXT}$	VEE_EXT[7:1] SET delay time	0	---	6.3	s
VEE_EXT delay time accuracy	$T_{VDDH-EXT-A}$		-16	---	+16	%
Load Current Range	I_{LOAD}		---	---	30	mA
Fault Protection		Falling	---	85	---	%
		Fault Timer	---	16	---	ms

Electrical Characteristics (Continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
VCOM						
VCOM Output Current		Souring	40	---	---	mA
		Sinking	40	---	---	mA
Operating Range-DC	VCOM	VCOM[8:0] SET output voltage	-5	---	+5	V
	VCOMH	VCOMH[8:0] SET output voltage	9	---	18	V
	VCOML	VCOML[8:0] SET output voltage	-18	---	-9	V
Operating Range-AC	VP	VP3>VCOMH+VCOM	---	VCOMH+ VCOM	---	V
	VN	VN3<VCOML+VCOM	---	VCOML+ VCOM	---	V
Accuracy		VCOM=-2V, or VOMH=15V, VCOML=-15V, @VCOM=0V VIN=2.9V to 9.0V, no load	-1.5	---	+1.5	%
Discharge Impedance to Ground	R_{DIS}		---	800	---	Ω
Thermistor Monitor(Use 10KΩ Murata NCP15XH103F03RC)						
Offset	$Offset_{TMS}$	Temperature=0°C	---	1.22	---	V
Maximum Input Level	V_{TMS_MAX}	VREF	---	2.5	---	V
External Pull Up Resistor	$R_{NTC\ UP}$		---	9.53	---	KΩ
External Linearization Resistor	R_{Linear}		---	13.7	---	KΩ
ADC Resolution	ADC_{RES}	Not Tested in production, 1-bit	---	10	---	mV
ADC Conversion Time	ADC_{DEL}	Not Tested in production	---	300	---	us
Accuracy	TMS_{ACC}	Not Tested in production, 1-bit	-1	---	1	LSB
Logic Levels and Timing Characteristics (SCL, SDA, PG, EN, VCOM_EN, Toggle_VCOM_CTL, PS)						
Output Low Threshold Level	V_{OL}	I_O=3mA, sink current (SDA,PG)	---	---	0.4	V
Input Low Threshold Level	V_{IL}		---	---	0.6	V
Input High Threshold Level	V_{IH}		1.5	---	---	V
Deglitch Time, EN pin	$t_{Deglitch}$		---	100	---	µs
SCL Clock Frequency	F_{SCL}		---	---	400	KHz
I^2C Slave Address		7-bit slave address	---	0x48h	---	

Data Transmission Timing

(VIN= 3.6V±5%, T_A=25°C, CL=100pF, unless otherwise specified**)**

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
I²C TIMING CHARCTERISTICS						
Serial-Clock Frequency	f_{SCL}		---	---	400	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}	F_{SCL}=100KHz	4.7	---	---	µs
		F_{SCL}=400KHz	1.3	---	---	
Hold Time (Repeated) START Condition	$t_{HD,STA}$	F_{SCL}=100KHz	4.0	---	---	µs
		F_{SCL}=400KHz	0.6	---	---	
SCL Pulse-Width Low	t_{LOW}	F_{SCL}=100KHz	4.7	---	---	µs
		F_{SCL}=400KHz	1.3	---	---	
SCL Pulse-Width High	t_{HIGH}	F_{SCL}=100KHz	4.0	---	---	µs
		F_{SCL}=400KHz	0.6	---	---	
Setup Time for a Repeated START Condition	$t_{SU,STA}$	F_{SCL}=100KHz	4.7	---	---	µs
		F_{SCL}=400KHz	0.6	---	---	
Data Hold Time	$t_{HD,DAT}$	F_{SCL}=100KHz	0	---	3.45	µs
		F_{SCL}=400KHz	0	---	0.9	
Data Setup Time	$t_{SU,DAT}$	F_{SCL}=100KHz	250	---	---	ns
		F_{SCL}=400KHz	100	---	---	
SDA and SCL Receiving Rise Time	t_R	F_{SCL}=100KHz	---	---	1000	ns
		F_{SCL}=400KHz	---	---	300	
SDA and SCL Receiving Fall Time	t_F	F_{SCL}=100KHz	---	---	300	ns
		F_{SCL}=400KHz	---	---	300	
Setup Time for STOP Condition	$t_{SU,STO}$	F_{SCL}=100KHz	4	---	---	µs
		F_{SCL}=400KHz	0.6	---	---	
Bus Capacitance	C_B		---	---	400	pF
Pulse Width of Suppressed Spike	t_{SP}		0	---	50	ns

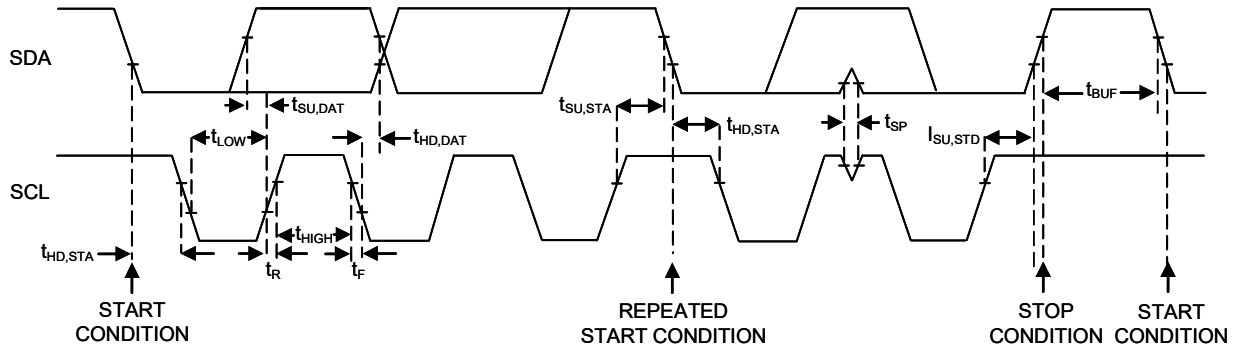
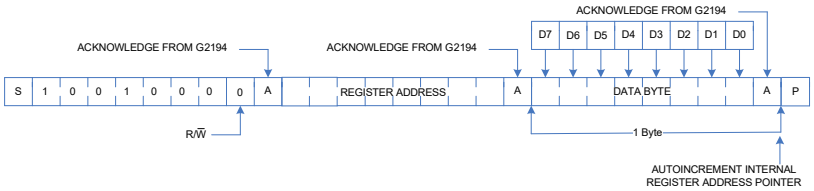


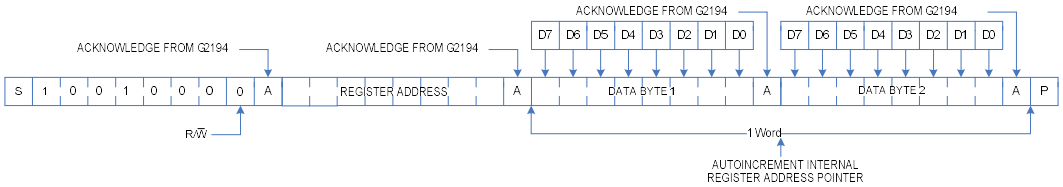
Figure 1. IC Serial-Interface Timing Diagram

I²C Protocol

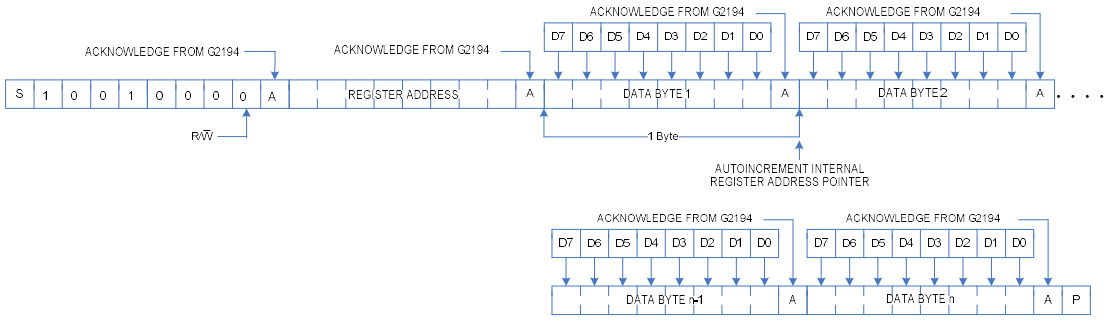
Write a Byte of Data to the G2194



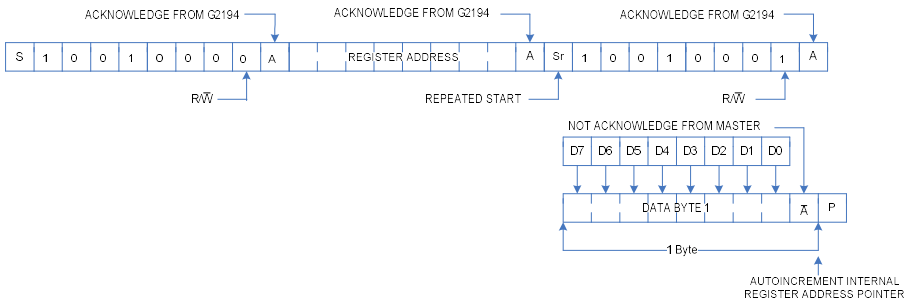
Write a Word of Data to the G2194



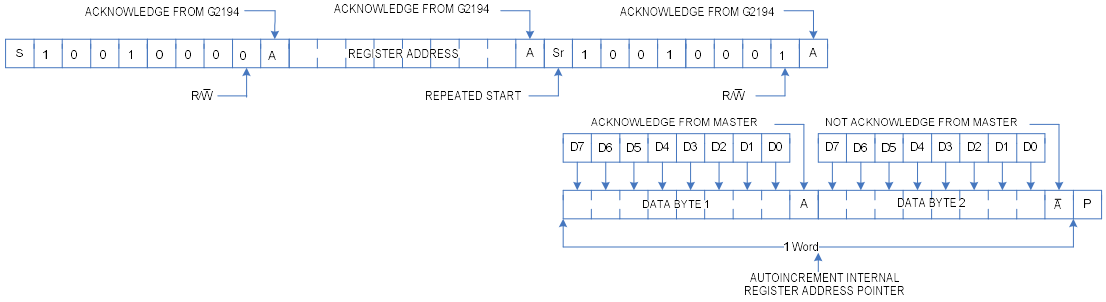
Write n Bytes of Data to the G2194



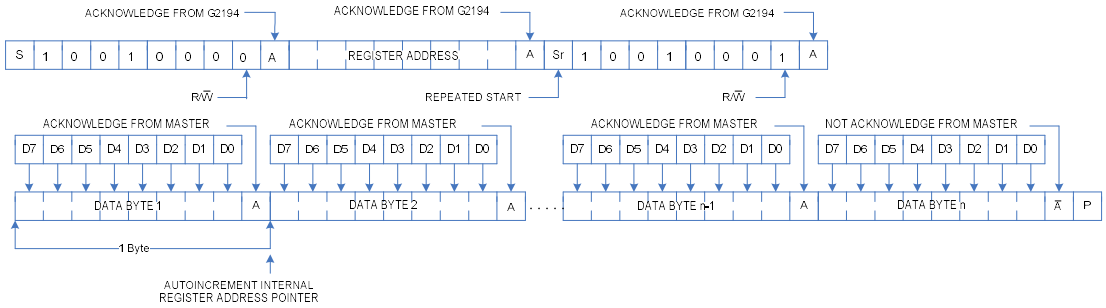
Read a Byte of Data to the G2194



Read a Word of Data to the G2194

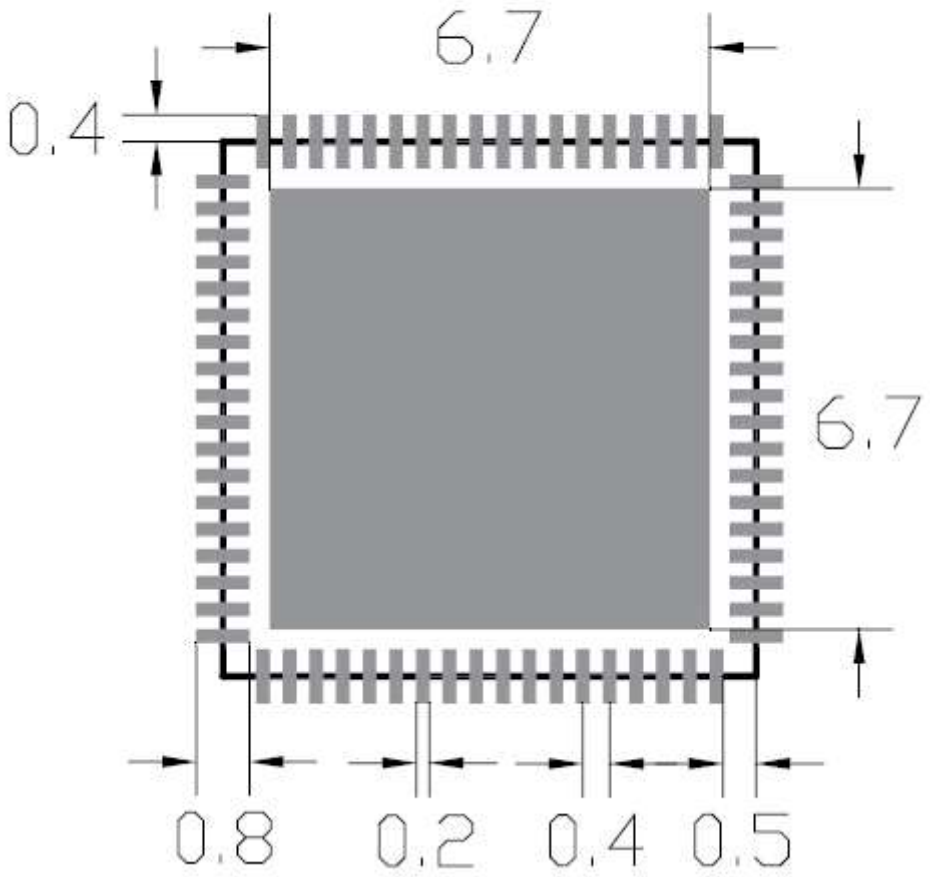


Read n Bytes of Data to the G2194

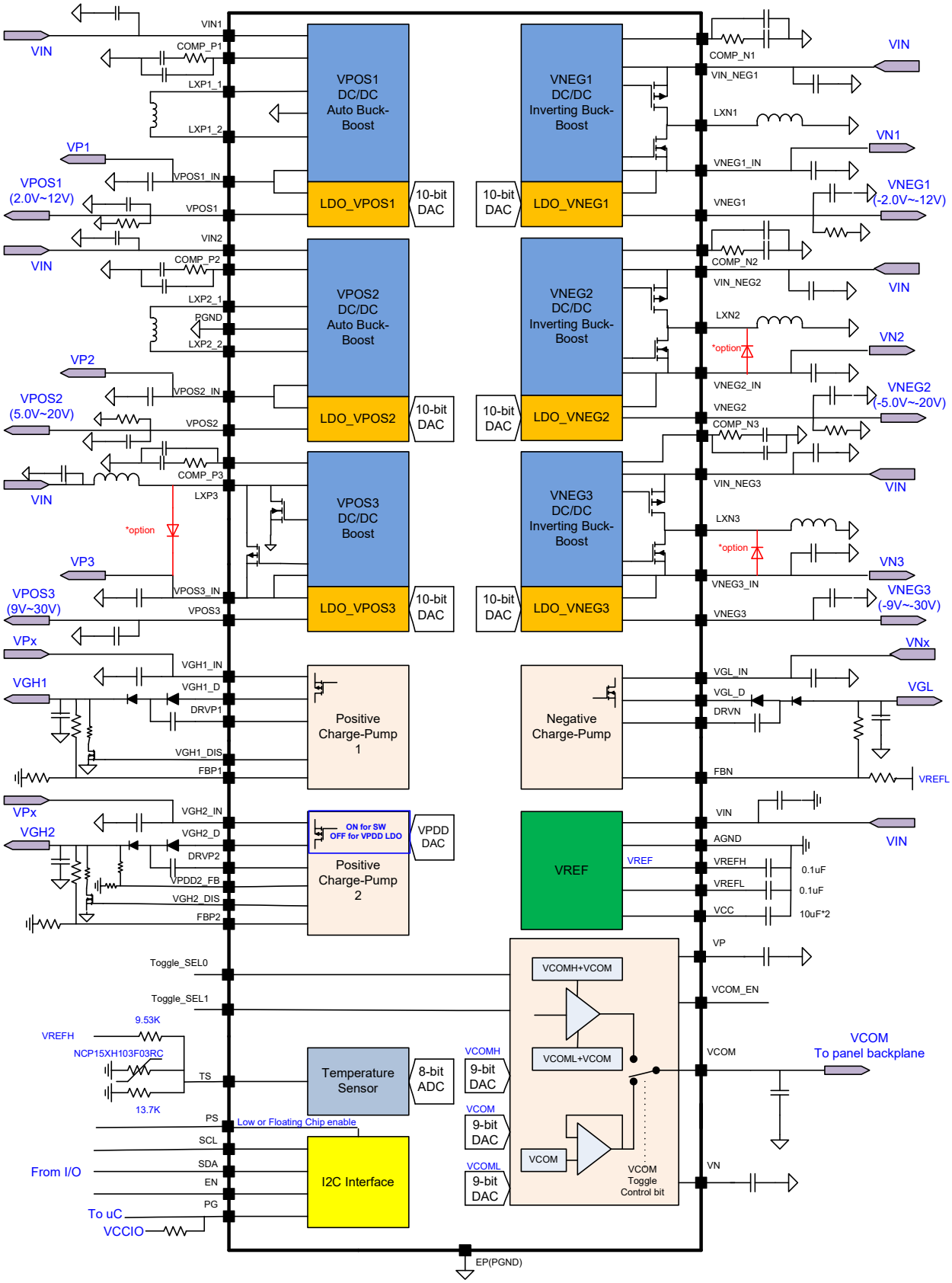


Minimum Footprint PCB Layout Section

QFN8X8-72



Typical Applications



Pin Description

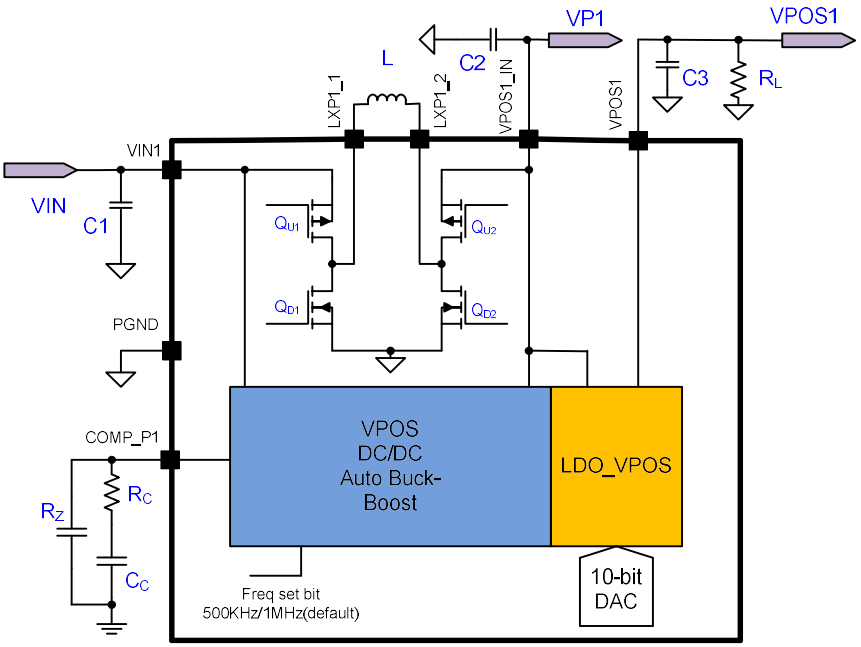
Pin No.	Symbol	Descript
1	VNEG2	Negative supply output pin for panel source drivers. Discharge VNEG2 to Ground whenever the rail is disable.
2	VNEG2_IN	Feedback pin for VN2 and supply for VNEG2 rail
3	VNEG2_IN	Feedback pin for VN2 and supply for VNEG2 rail
4	LXN2	VN2 Inductor Switch Node
5	LXN2	VN2 Inductor Switch Node
6	VIN_NEG2	Input Power Supply to VN2 rail
7	VIN1	Input Power Supply to VP1 rail
8	LXP1_1	VP1 Inductor Switch Node
9	LXP1_2	VP1 Inductor Switch Node
10	VPOS1_IN	Feedback pin for VP1 and supply for VPOS1 rail
11	VPOS1	Positive supply output pin for panel source drivers. Discharge VPOS1 to Ground whenever the rail is disable.
12	COMP_P1	VP1 Compensation pin
13	AGND	Analog ground for general alalog circuitry
14	VCC	Filter pin for 3.3V internal supply
15	VREFL	Filter pin for internal reference 1.5V for Temp. sense pull-high voltage.
16	VIN	Input power supply to general circuitry
17	Toggle_SEL1	VCOM AC+DC output control pin
18	Toggle_SEL0	VCOM AC+DC output control pin
19	COMP_N3	VN3 Compensation pin
20	VIN_NEG3	Input Power Supply to VN3 rail
21	VIN_NEG3	Input Power Supply to VN3 rail
22	LXN3	VN3 Inductor Switch Node
23	LXN3	VN3 Inductor Switch Node
24	VNEG3_IN	Feedback pin for VN3 and supply for VNEG3 rail
25	VNEG3_IN	Feedback pin for VN3 and supply for VNEG3 rail
26	VNEG3	Negative supply output pin for panel source drivers. Discharge VNEG3 to Ground whenever the rail is disable.
27	VCOM_EN	VCOM enable pin when VCOMCTL[7]=1. Pull this pin high to enable the VCOM
28	TS	Thermistor input pin.
29	VREFH	Filter pin for internal reference 2.5V for Temp. sense pull-high voltage.
30	VN	VCOML output level is shifted with DC VCOM value
31	VCOM	Power for panel common-voltage driver. Discharge VCOM to ground whenever the rail is disable.
32	VP	VCOMH output level is shifted with DC VCOM value
33	VPOS3	Positive supply output pin for panel source drivers. Discharge VPOS3 to Ground whenever the rail is disable.
34	VPOS3_IN	Feedback pin for VP3 and supply for VPOS3 rail
35	VPOS3_IN	Feedback pin for VP3 and supply for VPOS3 rail
36	LXP3	VP3 Inductor Switch Node
37	LXP3	VP3 Inductor Switch Node
38	EN	Pull this pin high to power up all output rails.
39	COMP_P3	VP3 Compensation pin
40	PG	Open-drain power good output pin. Pin is pulled low when one or more rails are not in regulation. **VPx, VNx, VCOM** have no effect on this pin.

Pin Description (Continued)

Pin No.	Symbol	Descript
41	SDA	Serial interface(I^2C) data input/output
42	SCL	Serial interface(I^2C) clock input
43	PS	Pull this pin high to enter power save mode(IC shutdown)
44	COMP_N1	VN1 Compensation pin
45	VNEG1	Negative supply output pin for panel source drivers. Discharge VNEG1 to Ground whenever the rail is disable.
46	VNEG1_IN	Feedback pin for VN1 and supply for VNEG1 rail
47	LXN1	VN1 Inductor Switch Node
48	VIN_NEG1	Input Power Supply to VN1 rail
49	VIN2	Input Power Supply to VP2 rail
50	LXP2_1	VP2 Inductor Switch Node
51	LXP2_2	VP2 Inductor Switch Node
52	LXP2_2	VP2 Inductor Switch Node
53	VPOS2_IN	Feedback pin for VP2 and supply for VPOS2 rail
54	VPOS2_IN	Feedback pin for VP2 and supply for VPOS2 rail
55	VPOS2	Positive supply output pin for panel source drivers. Discharge VPOS2 to Ground whenever the rail is disable.
56	COMP_P2	VP2 Compensation pin
57	FBN	VGL Feedback pin
58	VGL_IN	Input Supply pin for negative charge-pump VGL
59	VGL_D	Base voltage output pin for negative charge-pump VGL
60	DRVN	Driver output pin for negative charge pump VGL
61	VGH1_DIS	VGH1 discharge control pin
62	FBP1	VGH1 Feedback pin
63	VGH1_IN	Input Supply pin for positive charge-pump VGH1
64	VGH1_D	Base voltage output pin for positive charge-pump VGH1
65	DRVP1	Driver output pin for positive charge pump VGH1
66	VGH2_DIS	VGH2 discharge control pin
67	DRVP2	Driver output pin for positive charge pump VGH2
68	VGH2_D	Base voltage output pin for positive charge-pump VGH2
69	VGH2_IN	Input Supply pin for positive charge-pump VGH2
70	VPDD2_FB	VGH2 Feedback pin for Post Drive Mode VPDD
71	FBP2	VGH2 Feedback pin
72	COMP_N2	VN2 Compensation pin
73	**EP**(PGND)	Exposed Pad. Connect exposed pad to PGND(Power Ground of DC/DC Converter)

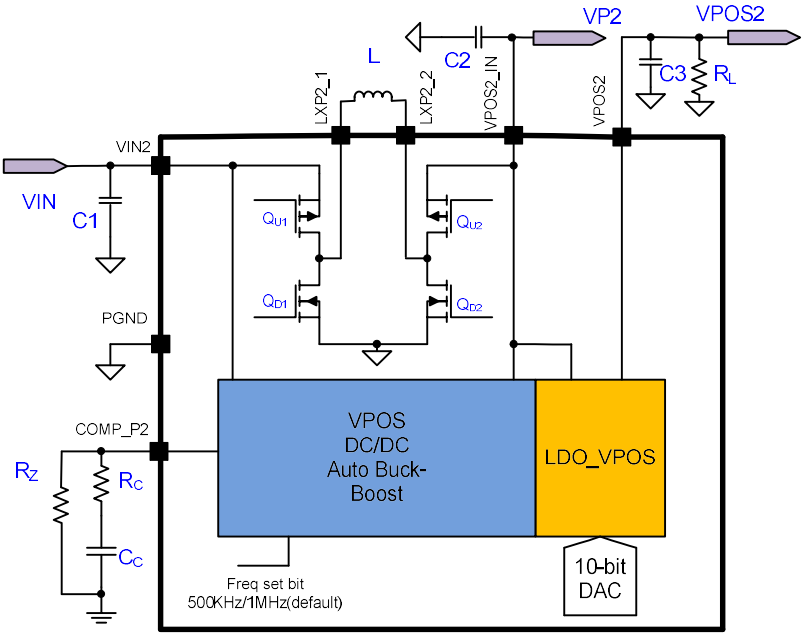
Power Rails Topology

(1) VP1 & VPOS1



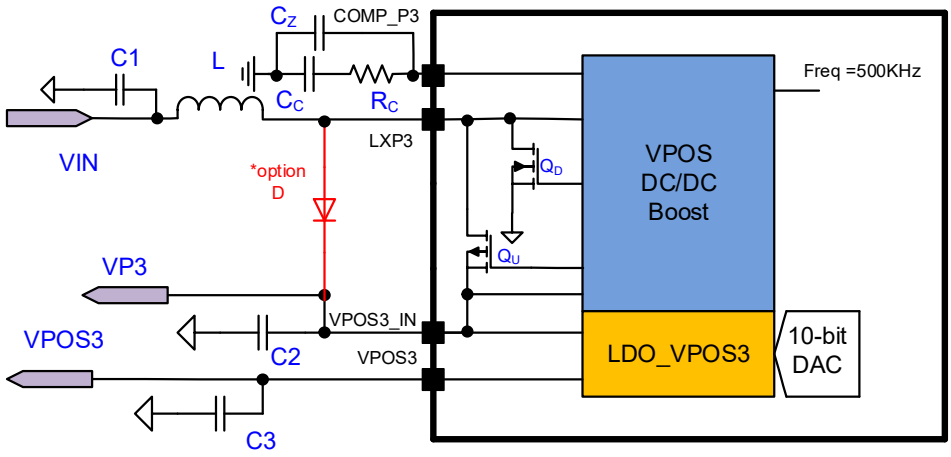
Design Parameter	VPOS1=10V/100mA, VIN=1-cell Li-ion or 2-cells Li-ion in series input
C1	muRata, GRM21BR61C106K (10μF/16V/X5R, 0805)*1
C2	muRata, GRM21BR61C106K(10μF/16V/X5R, 0805)*2
C3	muRata, GRM21BR61C106K (10μF/16V/X5R, 0805)*1
L	TOKO, A915AY-4R7M(4.7μH/1.5A/45mΩ, 5.2x5.2x3.0mm) Yuden, NRS5030T 4R7MMGJ(4.7μH/2.6A/35mΩ, 5.0x5.0x3.0mm)
R_L	82KΩ
R_C	47KΩ
C_C	470pF
R_Z	10MΩ

(2) VP2 & VPOS2



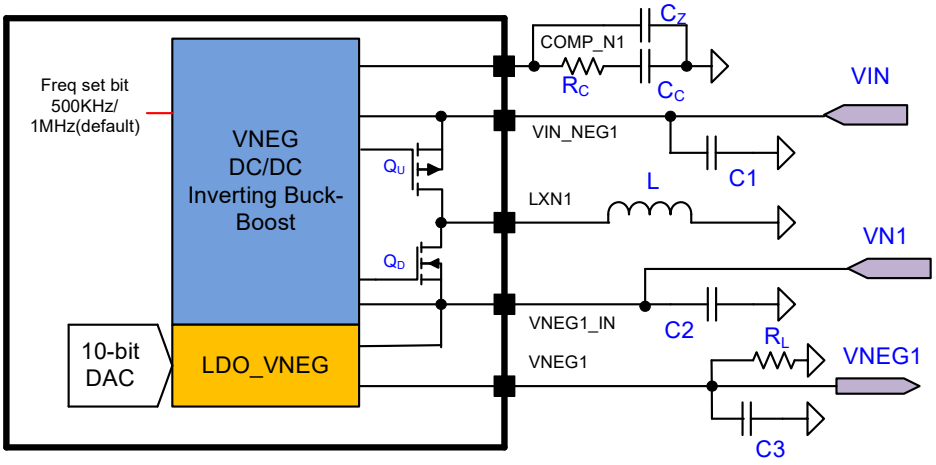
Design Parameter	VPOS2=17V/150mA, VIN=1-cell Li-ion or 2-cells Li-ion in series input
C1	muRata, GRM21BR61C106K (10μF/16V/X5R, 0805)*1
C2	muRata, GRM31CR61E106K(10μF/25V/X5R, 1206)*1
C3	muRata, GRM31CR61E106K(10μF/25V/X5R, 1206)*1
L1	TOKO, A915AY-4R7M(4.7μH/1.5A/45mΩ, 5.2x5.2x3.0mm) Yuden, NRS5030T 4R7MMGJ(4.7μH/2.6A/35mΩ, 5.0x5.0x3.0mm)
R_L	100KΩ
R_C	51 KΩ
C_C	220pF
R_Z	10MΩ

(3) VP3 & VPOS3



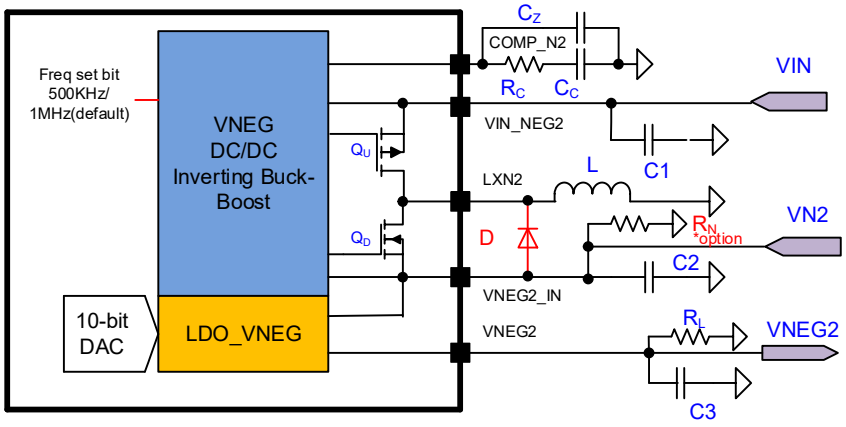
Design Parameter	VPOS3=24V/300mA, VIN=1-cell Li-ion or 2-cells Li-ion in series input
C1	muRata, GRM21BR61C106K (10μF/16V/X5R, 0805)*1
C2	muRata, GRM319R6YA106MA12(10μF/35V/X5R, 1206)*2
C3	muRata, GRM319R61H475MA12(4.7μF/50V/X5R, 1206)*1
L1	Sumida, CDRH8D28NP-3R3NC(3.3μH/4A/18.2mΩ, 8.3x8.3x3.0mm) Yuden, NRS8030T 3R3MJGJ(3.3μH/4A/19mΩ, 8.0x8.0x3.0mm)
D	ON Semiconductor , MBR130T1 , 30V/1A single Schottky diodes (SOD123)
R_C	150KΩ
C_C	1.5nF
C_Z	NC

(4) VN1 & VNEG1



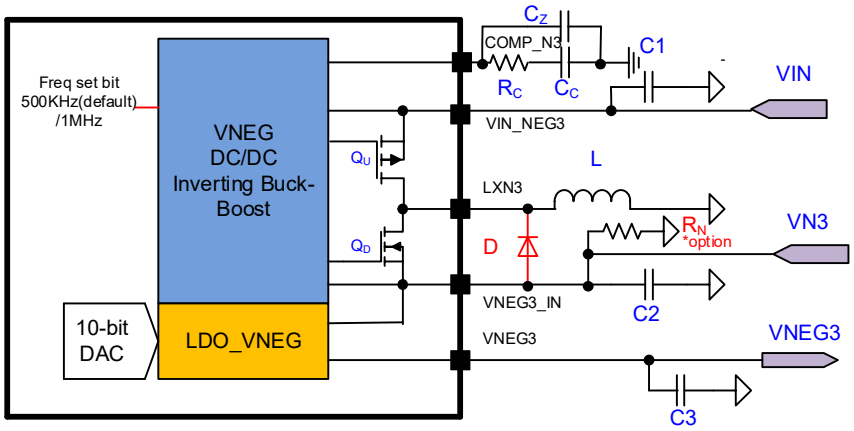
Design Parameter	VNEG1=-10V/100mA, VIN=1-cell Li-ion or 2-cells Li-ion in series input
C1	muRata, GRM21BR61C106K (10μF/16V/X5R, 0805)*1
C2	muRata, GRM21BR61C106K(10μF/16V/X5R, 0805)*1
C3	muRata, GRM21BR61C106K(10μF/16V/X5R, 0805)*1
L	TOKO, A915AY-10R0M(10μH/1.0A/ 90mΩ, 5.2x5.2x3.0mm) Yuden, NRS5030T 100MMGJ(10μH/1.7A/70mΩ,5.0x5.0x3.0mm)
R_L	82KΩ
R_C	75KΩ
C_C	120pF
C_Z	NC

(5) VN2 & VNEG2



Design Parameter	VNEG2=-17V/150mA, VIN=1-cell Li-ion or 2-cells Li-ion in series input
C1	muRata, GRM21BR61C106K (10μF/16V/X5R, 0805)*1
C2	muRata, GRM31CR61E106K(10μF/25V/X5R, 1206)*1
C3	muRata, GRM319R61E475K (4.7μF/25V/X5R, 1206)*1
L1	TOKO, A915AY-4R7M(4.7μH/1.5A/45mΩ, 5.2x5.2x3.0mm) Yuden, NRS5030T 4R7MMGJ(4.7μH/2.6A/35mΩ, 5.0x5.0x3.0mm)
R_L	100KΩ
R_C	68 KΩ
R_N	NC(*option 10K~18K)
C_C	220pF
C_Z	NC
D	ON Semiconductor , MBR130T1 , 30V/1A single Schottky diodes (SOD123)

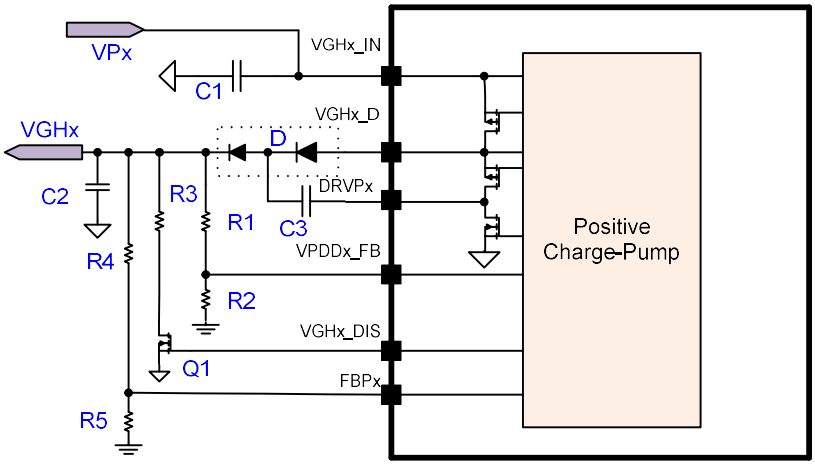
(6) VN3 & VNEG3



Design Parameter	VNEG3=-24V/300mA, VIN=1-cell Li-ion or 2-cells Li-ion in series input
C1	muRata, GRM21BR61C106K (10μF/16V/X5R, 0805)*1
C2	muRata, GRM319R6YA106MA12(10μF/35V/X5R, 1206)*2~3
C3	muRata, GRM319R61H475MA12(4.7μF/50V/X5R, 1206)*1
L1	Sumida, CDRH8D28NP-3R3NC(3.3μH/4A/18.2mΩ, 8.3x8.3x3.0mm) Yuden, NRS8030T 3R3MJGJ(3.3μH/4A/19mΩ, 8.0x8.0x3.0mm)
D	ON Semiconductor , MBR130T1 , 30V/1A single Schottky diodes (SOD123)
R_C	33KΩ
C_C	1.5nF
R_N	NC(*option 10K~18K)
C_Z	NC

(7) VGH1/VGH2

(A) When 2xVPx > VGH, the charge pump architecture with twice the input voltage is used.

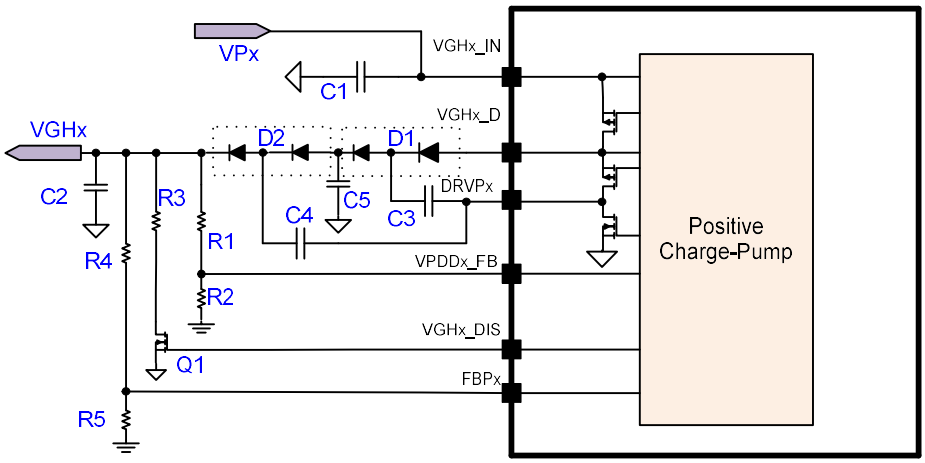


Design Parameter	VGHx=35V/20mA, VP3=24V
C1	muRata, GRM21BR61H225KA73(2.2μF/50V/X5R, 0805)*1
C2	muRata, GRM21BR61H225KA73(2.2μF/50V/X5R, 0805)*1
C3	muRata, GRM155R61H104KE19(0.1μF/50v/X5R,0402)*1
D	Dual small-signal diodes (SOT23),Fairchild MMBD4148SE/ BAV99
R1	18KΩ
R2	2KΩ
R3	10KΩ
Q1	2N7002(SOT23)
R4	51KΩ
R5	1.8KΩ

* only VGH2 has the post drive mode(VPDD LDO)

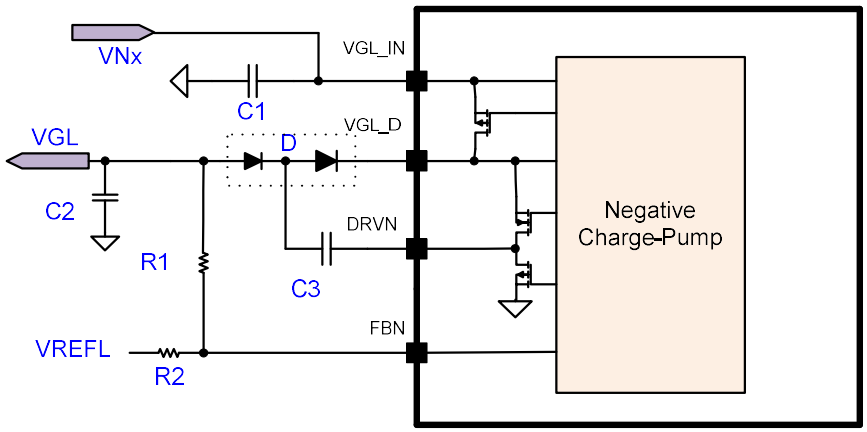
$$* VGH = V_{FBP} \times \frac{R4 + R5}{R5}$$

(B) When 2xVPx ≦ VGH, the following charge pump architecture with triple input voltage is required.
C2=C5=1μF, C4=0.1μF



(8) VGL

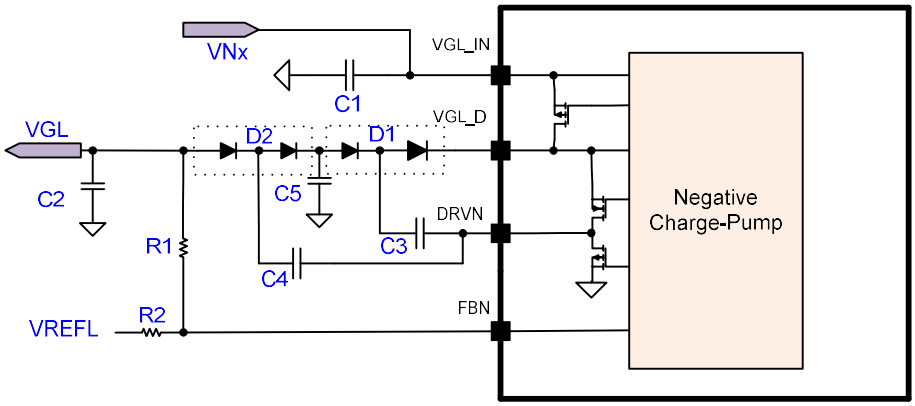
(A) When 2xVNx < VGL, the charge pump architecture with twice the input voltage is used.



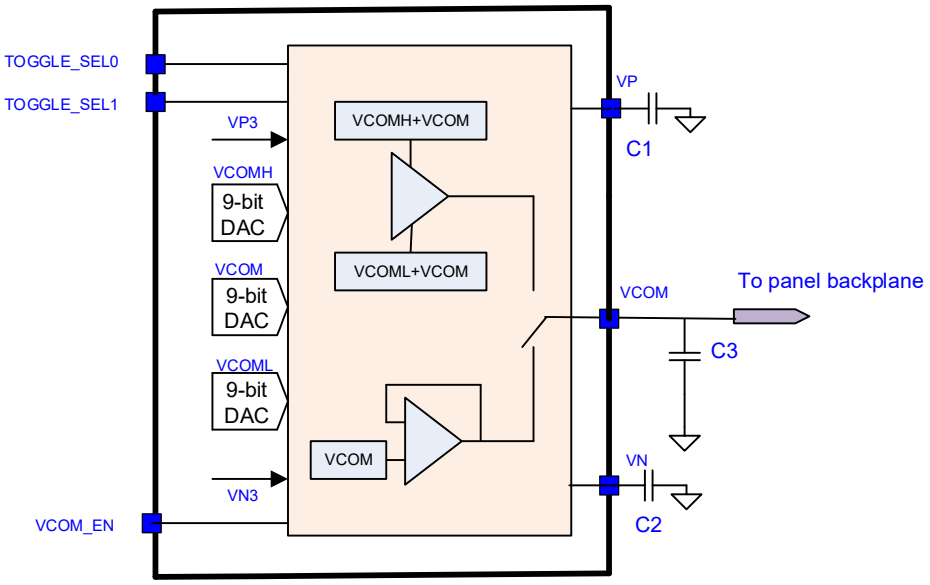
Design Parameter	VGH=-35V/20mA, VN3=-24V
C1	muRata, GRM21BR61H225KA73(2.2μF/50V/X5R, 0805)*1
C2	muRata, GRM319R61H475MA12(4.7μF/50V/X5R, 1206)*1
C3	muRata, GRM155R61H104KE19(0.1μF/50v/X5R,0402)*1
D	Dual small-signal diodes (SOT23),Fairchild MMBD4148SE/ BAV99
R1	237KΩ
R2	8.06KΩ

$$VGL = V_{FBN} - (V_{REFL} - V_{FBN}) \times \frac{R1}{R2}$$

(B) When 2xVNx ≧ VGL, the following charge pump architecture with triple input voltage is required. (C2=C5=2.2μF, C4=0.1μF)



(9) VCOM



Design Parameter	DCVCOM=-1V/40mA, (0x16H, 3/7 LEVEL[5]=”0”)
C1	muRata, ME05GRM155R61H105ME05 (1μF/50v/X5R,0402)*1
C2	muRata, ME05GRM155R61H105ME05 (1μF/50v/X5R,0402)*1
C3	muRata, GRM21BR61H105KA01(1μF/50V/X5R,0805)*1~10μF/25V/X5R*1

3/7-Level VCOM Register table setting:

0x16H	0x0DH	0x0DH	Function	Power Rail active	
3/7 LEVEL[5]	TOGGLE_VCOM[4]	VCOM_3L_MODE[3]		DC/DC	Source Power
0	0	x	7_LEVEL DCVCOM	VP1/VP2/VP3, VN1/VN2/VN3	VPOS1/VNEG1 VPOS2/VNEG2 VPOS3/VNEG3
0	1	x	7_LEVEL ACVCOM+DCVCOM	VP1/VP2/VP3, VN1/VN2/VN3	VPOS1/VNEG1 VPOS2/VNEG2 VPOS3/VNEG3
1	0	0	3_LEVEL DCVCOM	VP3/VN3	VPOS3/VNEG3
1	1	0	3_LEVEL ACVCOM+DCVCOM	VP3/VN3	VPOS3/VNEG3
1	0	1	3_LEVEL DCVCOM	VP3/VN3, VP2/VN2	VPOS2/VNEG2
1	1	1	3_LEVEL ACVCOM+DCVCOM	VP3/VN3, VP2/VN2	VPOS2/VNEG2

*If VPOS3 setting is more than VCOMH+DCVCOM & VNEG3 setting is less than VCOML+DCVCOM@ 3-Level application, it can be set the VCOM_3L_MODE[3]="0".
*TOGGLE_VCOM[4]=0→VP=VCOM{8:0}+10V, VN=VCOM[8:0]-10V

3/7-Level VCOM Hardware pin Setting Table

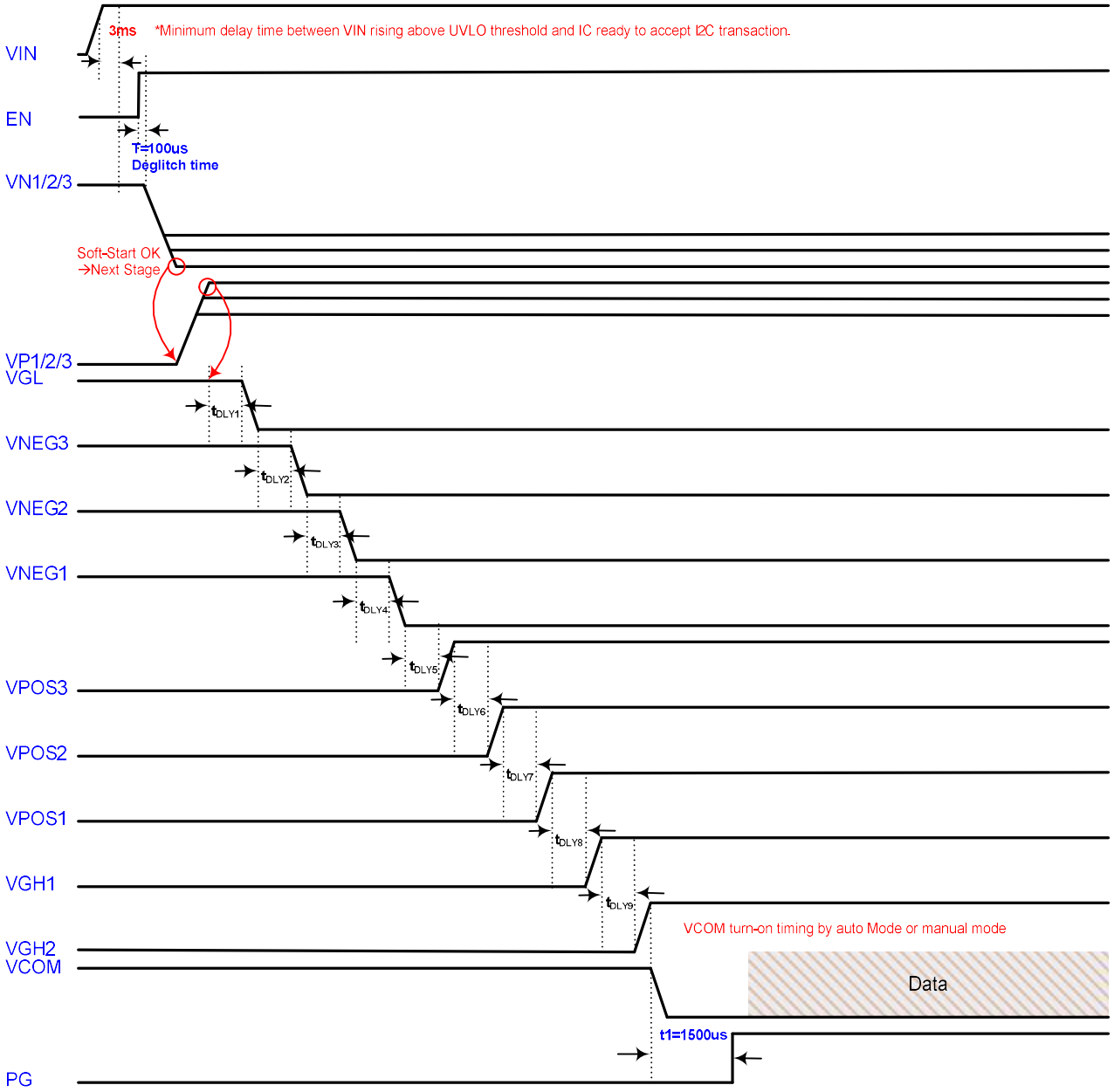
0x0DH	Toggle_SEL0	Toggle_SEL1	VCOM Function
TOGGLE_VCOM[4]			
0	x	x	DCVCOM
1	0	0	DCVCOM
1	0	1	VCOMH+DCVCOM
1	1	0	VCOML+DCVCOM
1	1	1	DCVCOM

EN pin and 0x18h ON_OFF[6]

Hardware pin	ON_OFF[6]	Status
EN		
0	x	Standby Mode, Only I^2C block enable
1	1	Normal Operation
1	0	Power Rails OFF (VPx,VNx,VPOSx,VNEGx,VGH1,VGH2, VGL,VCOM);

Power-up and Power-down Sequence

(A) Power-ON Sequence(7-Level Output, Normal):

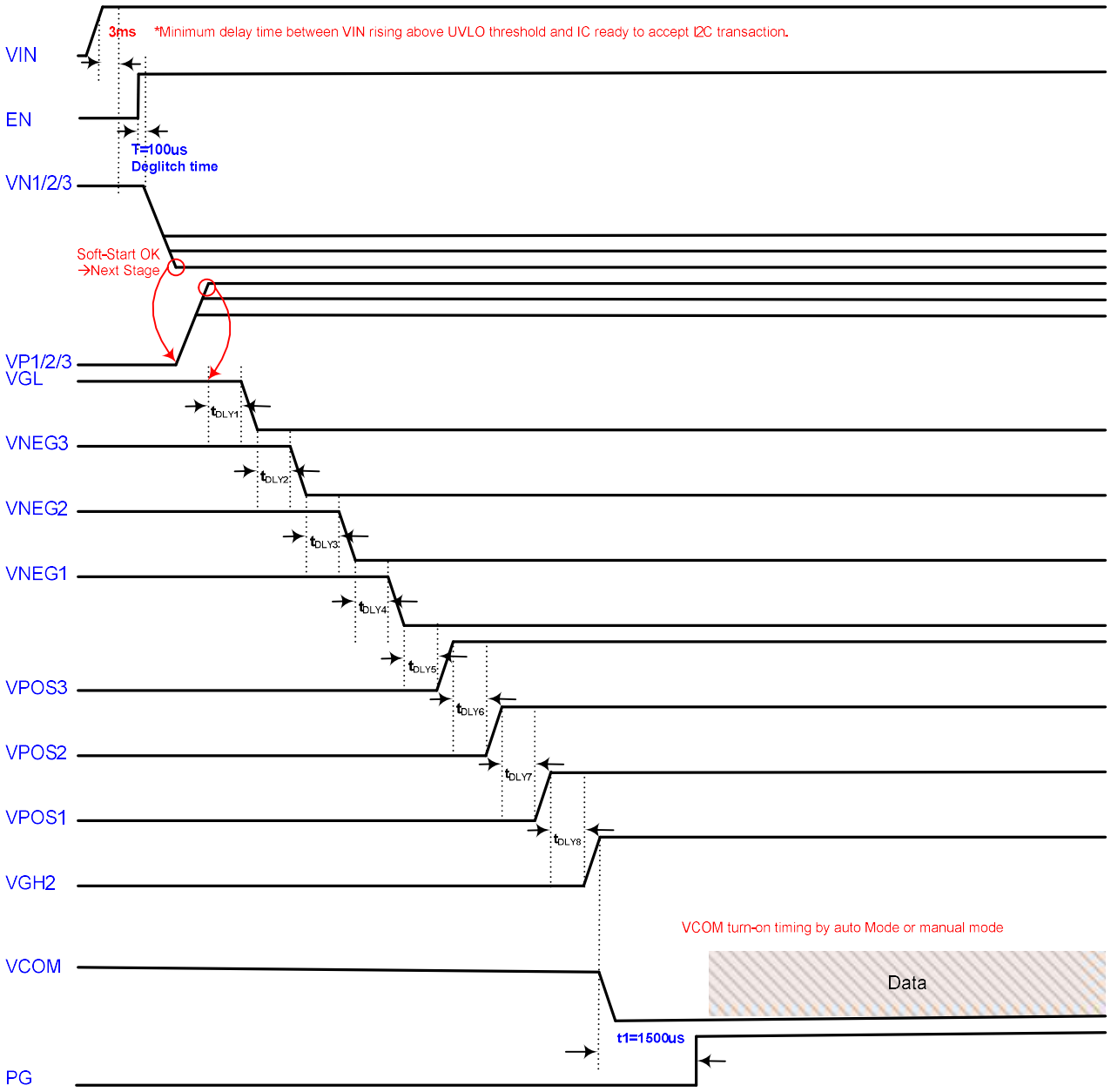


1. Soft-start time(VPOSx/VNEGx) is setting by register 0x16 (**3ms**,4ms,5ms,6ms).
2. Discharge function only for VNEG3/2/1, VPOS3/2/1, VGH1, VGH2 & VCOM. VN3/2/1, VP3/2/1 & VGL are no discharge function.
3. 3-Level or 7-Level output mode is setting by register 0x16 bit3 (3/7 LEVEL[5]).
   7-Level :VCOM DC or VCOM AC mode
   3-Level: VCOM DC or VCOM AC mode
4. For manual mode, after the last rail power-on(VGH2), VCOM starts ramping as VCOM_EN pull high. As VCOM_EN pull-low & VPx/VNx power ready, VCOM is shutdown.
5. t_{DLY1}~t_{DLY9} is programmable by register 0x13,0x14,0x15 (2-bit 0ms,1ms,**2ms**,4ms) and 0x16(soft-start time SS[7:6]).

Item	Formula
t_{DLY1}	t_{DLY1}[7:6] *1+SS[7:6]*0.2
t_{DLY2}	t_{DLY2}[5:4] *1+SS[7:6]*0.2
t_{DLY3}	t_{DLY3}[3:2] *1+SS[7:6]*0.2
t_{DLY4}	t_{DLY4}[1:0] *1+SS[7:6]*0.2
t_{DLY5}	t_{DLY5}[7:6] *1
t_{DLY6}	t_{DLY6}[5:4] *1+SS[7:6]*0.2
t_{DLY7}	t_{DLY7}[3:2] *1+SS[7:6]*0.2
t_{DLY8}	t_{DLY8}[1:0] *1+SS[7:6]*0.2
t_{DLY9}	t_{DLY9}[7:6] *1-0.3

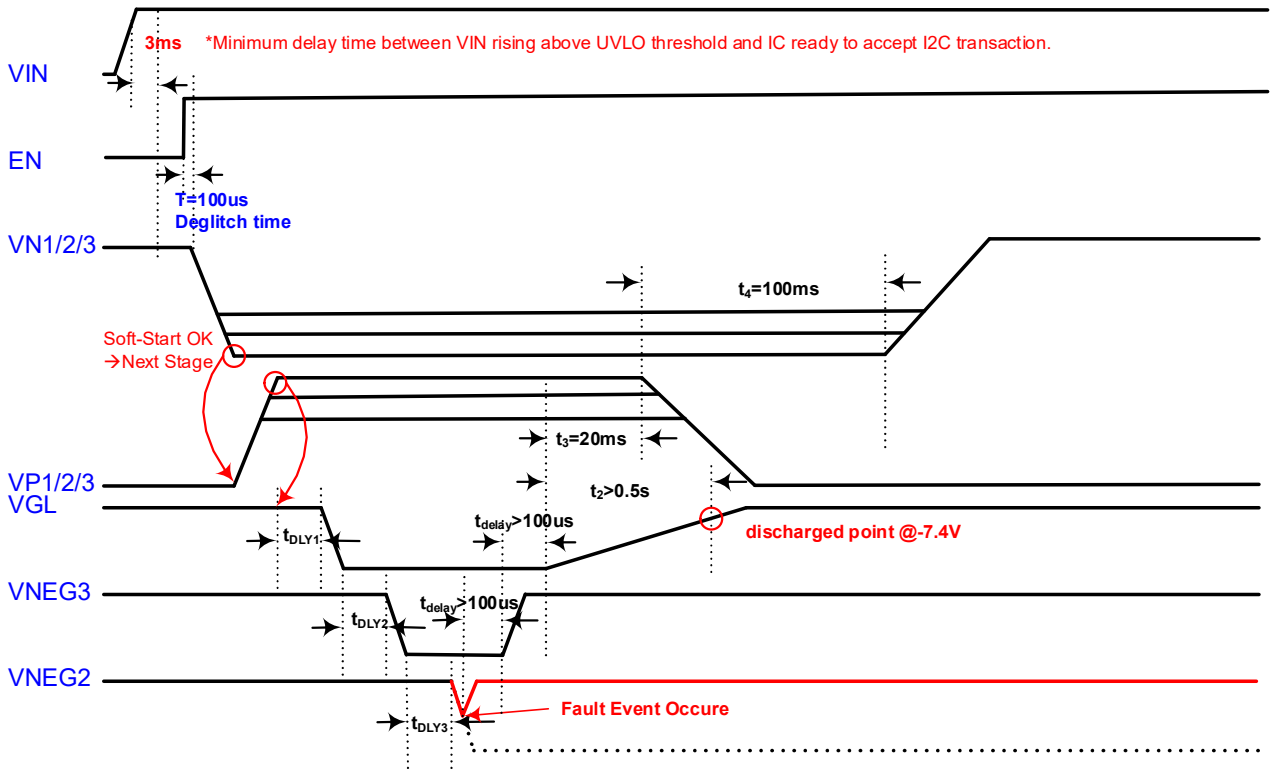
.

(B) Power-ON Sequence(7-Level Output, Normal, Only VGH2/VGL output):

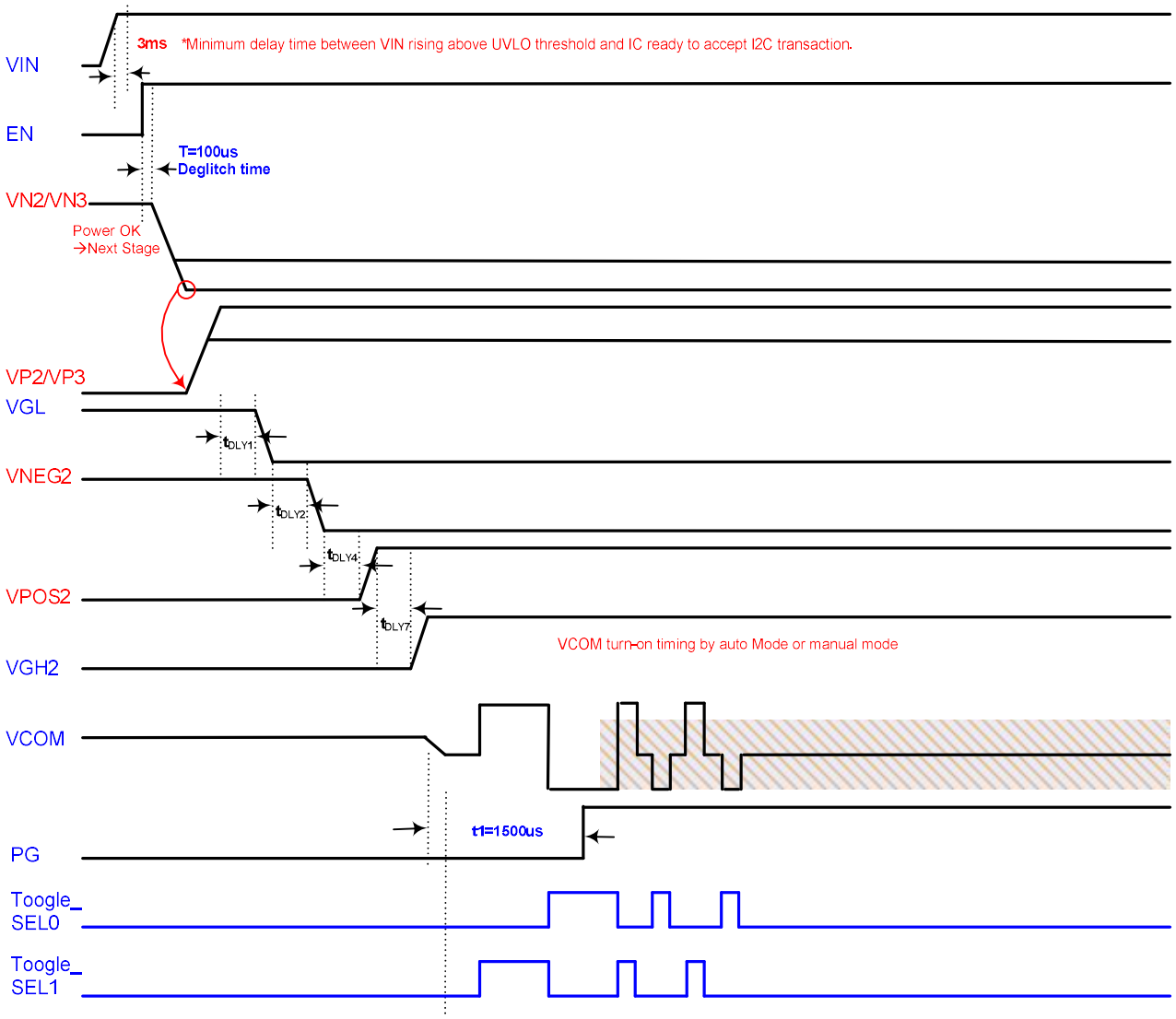


1. 3/7_LEVEL[5]="0" & VGH_7_SEL[4]="1" by register 0x16H, Gate driver supply are output VGH2/VGL.

(C) Power-ON Sequence with Fault Event (7-Level Output, Normal, FLT_VNEG2[3]=1):



(D) Power-ON Sequence(3-Level Output, Normal, ACVCOM+DCVCOM):



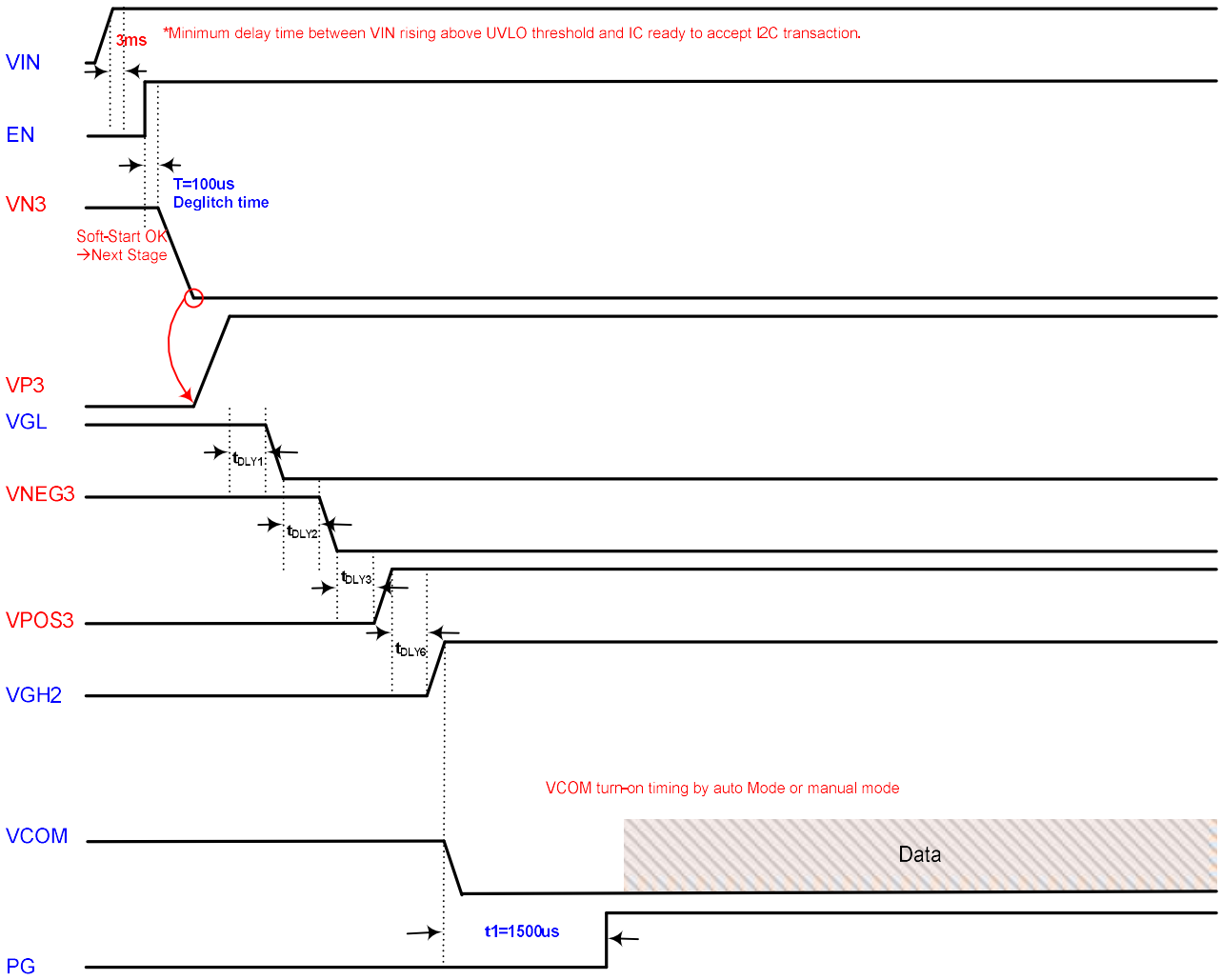
1. AC-VCOM toggle f_{osc}=85Hz=11.7ms
2. Register Setting:

0x16H	0x0DH	0x0DH	Function	Power Rail active	
3/7 LEVEL[5]	TOGGLE_VCOM[4]	VCOM_3L_MODE[3]		DC/DC	Source Power
0	0	x	7_LEVEL DCVCOM	VP1/VP2/VP3, VN1/VN2/VN3	VPOS1/VNEG1 VPOS2/VNEG2 VPOS3/VNEG3
0	1	x	7_LEVEL ACVCOM+DCVCOM	VP1/VP2/VP3, VN1/VN2/VN3	VPOS1/VNEG1 VPOS2/VNEG2 VPOS3/VNEG3
1	0	0	3_LEVEL DCVCOM	VP3/VN3	VPOS3/VNEG3
1	1	0	3_LEVEL ACVCOM+DCVCOM	VP3/VN3	VPOS3/VNEG3
1	0	1	3_LEVEL DCVCOM	VP3/VN3, VP2/VN2	VPOS2/VNEG2
1	**1**	**1**	**3_LEVEL ACVCOM+DCVCOM**	**VP3/VN3, VP2/VN2**	**VPOS2/VNEG2**

3. 3/7- level VCOM output by hardware pin Toggle_SEL0 & Toggle_SEL1

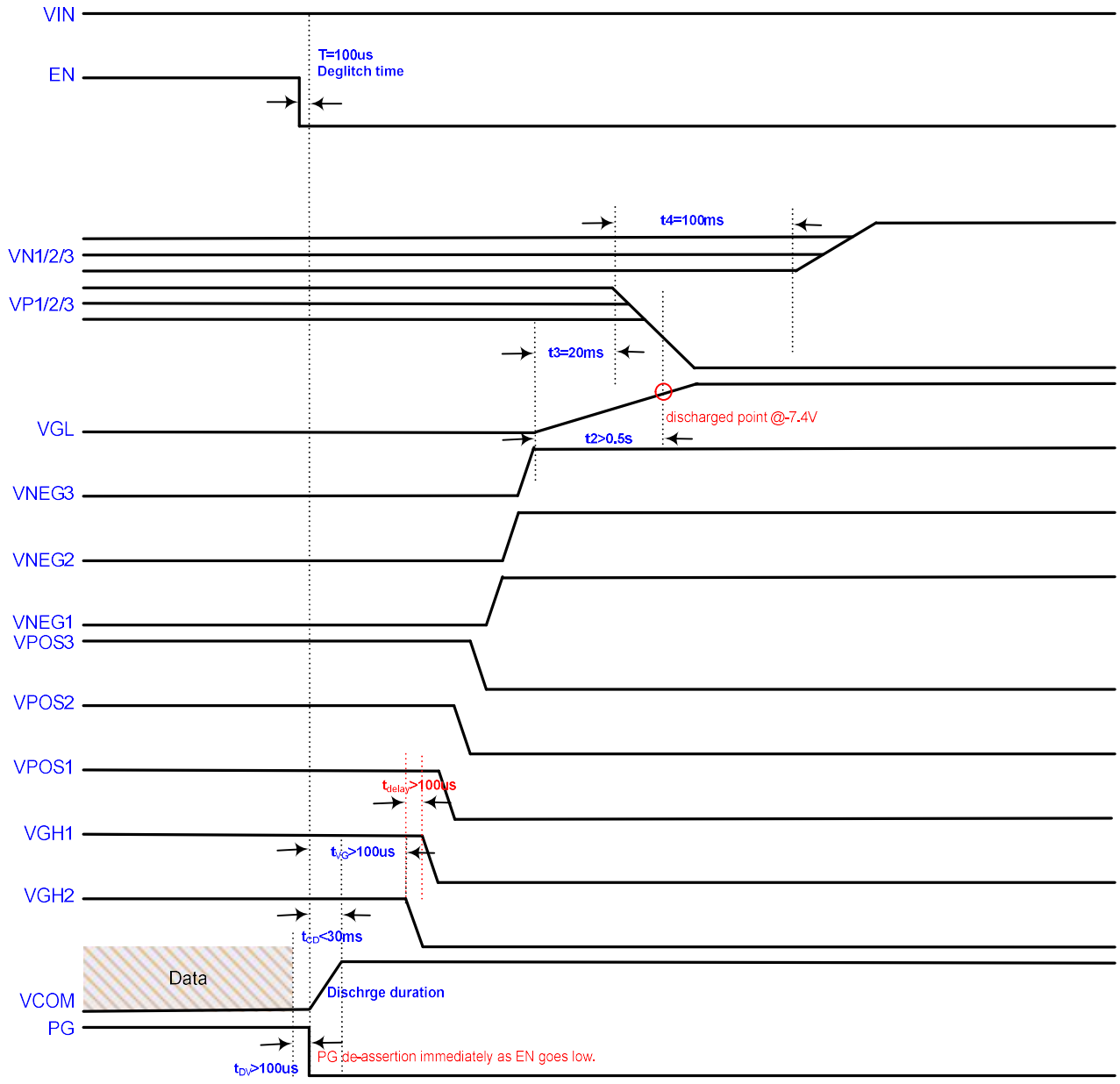
0x0DH TOGGLE_VCOM[4]	Toggle_SEL0	Toggle_SEL1	VCOM Function
0	x	x	DCVCOM
1	0	0	DCVCOM
1	0	1	VCOMH+DCVCOM
1	1	0	VCOML+DCVCOM
1	1	1	DCVCOM

(E) Power-ON Sequence(3-Level Output, Normal, DCVCOM):



0x16H	0x0DH	0x0DH	Function	Power Rail active	
3/7 LEVEL[5]	TOGGLE_VCOM[4]	VCOM_3L_MODE[3]		DC/DC	Source Power
0	0	x	7_LEVEL DCVCOM	VP1/VP2/VP3, VN1/VN2/VN3	VPOS1/VNEG1 VPOS2/VNEG2 VPOS3/VNEG3
0	1	x	7_LEVEL ACVCOM+DCVCOM	VP1/VP2/VP3, VN1/VN2/VN3	VPOS1/VNEG1 VPOS2/VNEG2 VPOS3/VNEG3
1	**0**	**0**	**3_LEVEL DCVCOM**	**VP3/VN3**	**VPOS3/VNEG3**
1	1	0	3_LEVEL ACVCOM+DCVCOM	VP3/VN3	VPOS3/VNEG3
1	0	1	3_LEVEL DCVCOM	VP3/VN3, VP2/VN2	VPOS2/VNEG2
1	1	1	3_LEVEL ACVCOM+DCVCOM	VP3/VN3, VP2/VN2	VPOS2/VNEG2

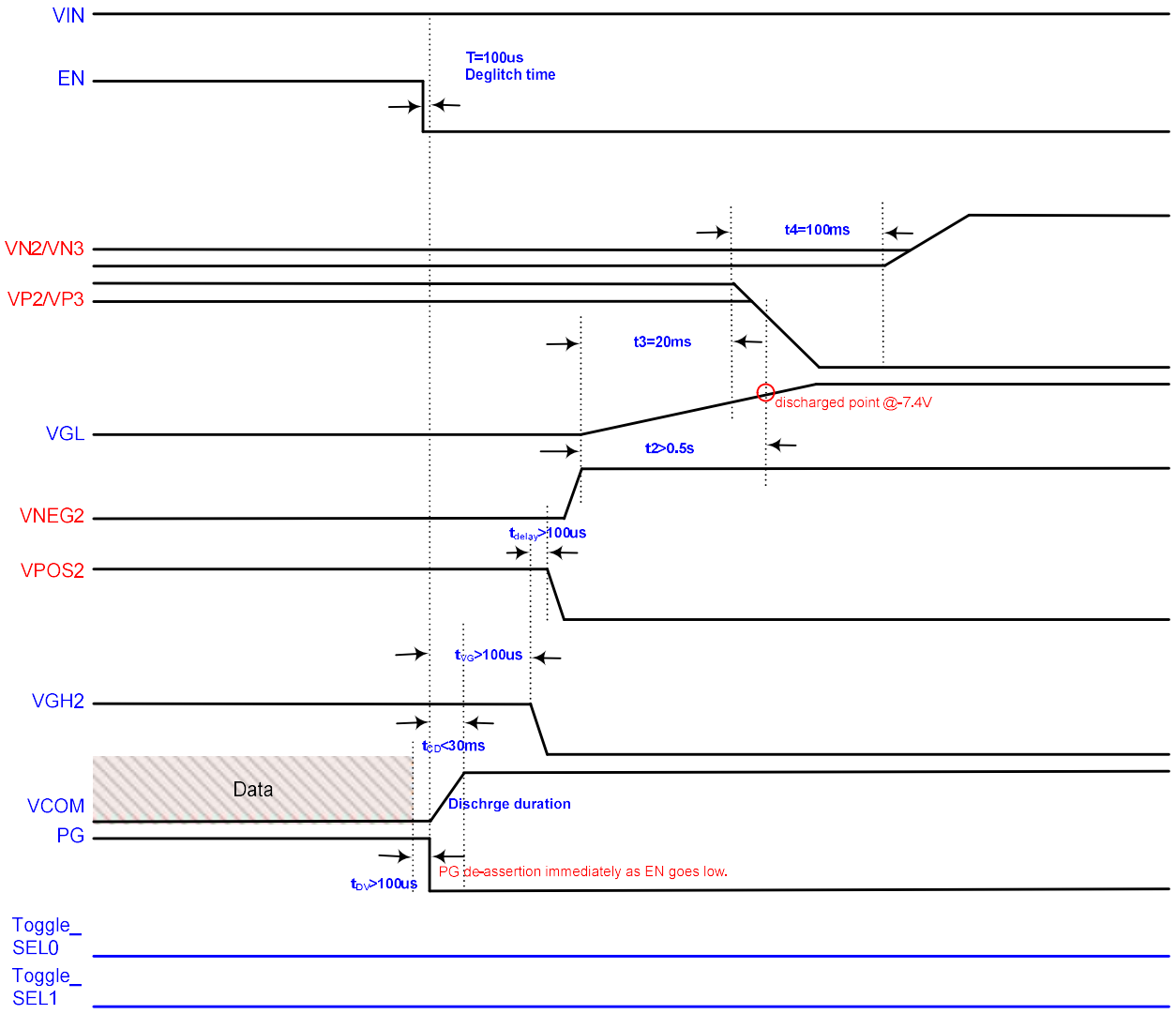
(F) Power-OFF Sequence (7-Level Output, Normal):



Normal Mode:

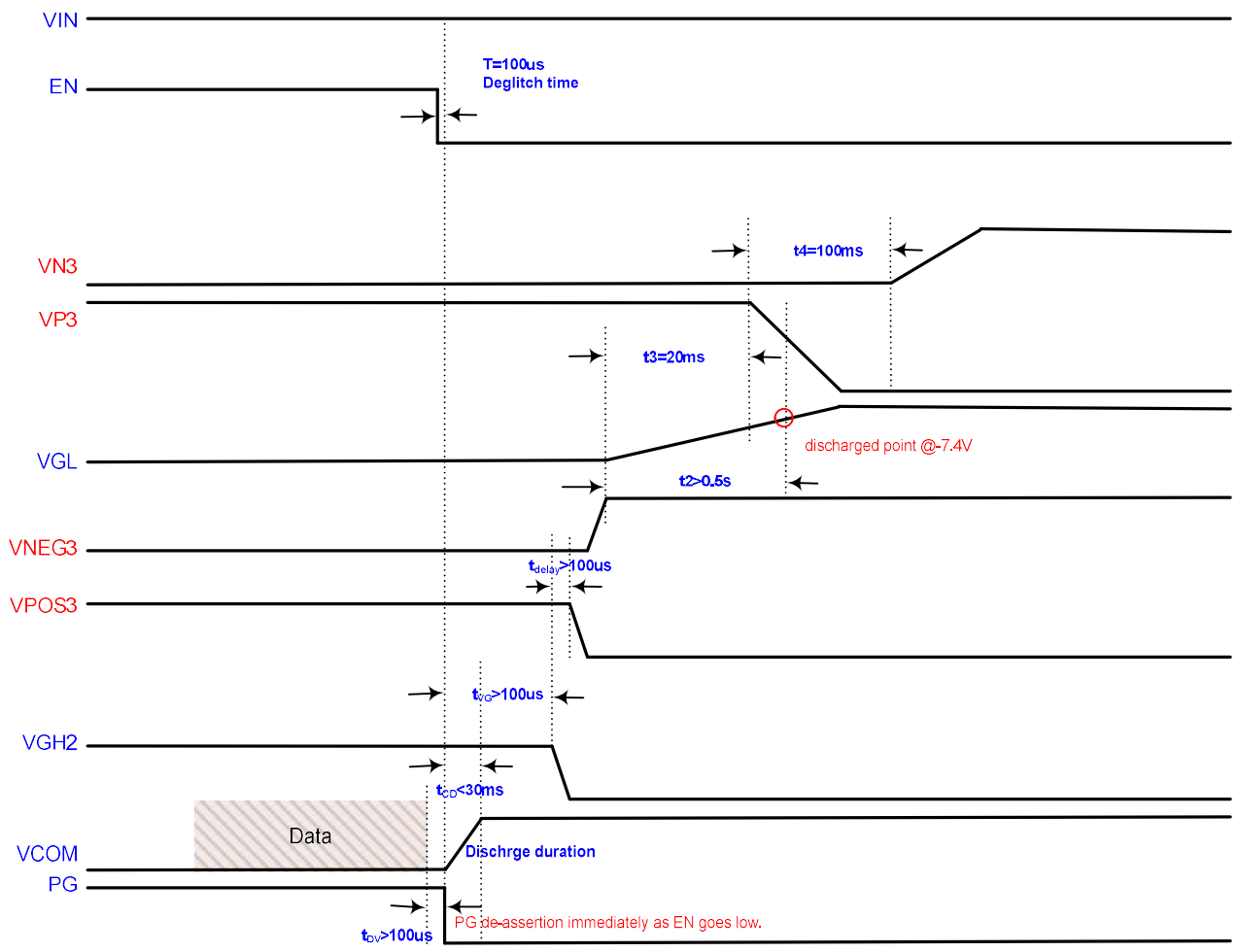
1. Supply voltage decay through pull-down resistors.
2. Normal mode off sequence is setting by 0x15 MODE[5] register.

(G) Power-OFF Sequence (3-Level Output Mode, Normal, AC-VCOM+DC-VCOM):



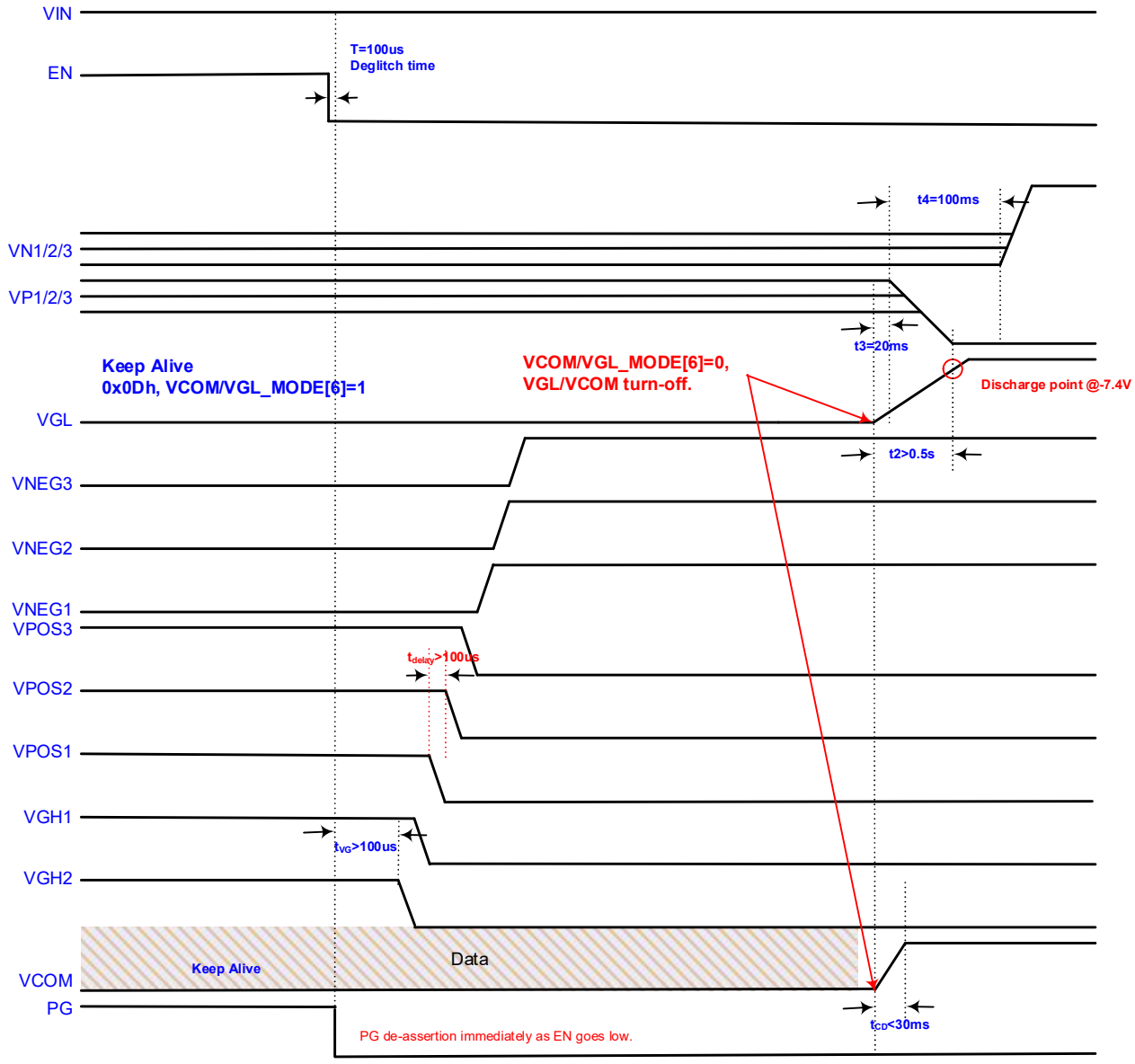
0x16H	0x0DH	0x0DH	Function	Power Rail active	
3/7 LEVEL[5]	TOGGLE_VCOM[4]	VCOM_3L_MODE[3]		DC/DC	Source Power
0	0	x	7_LEVEL DCVCOM	VP1/VP2/VP3, VN1/VN2/VN3	VPOS1/VNEG1 VPOS2/VNEG2 VPOS3/VNEG3
0	1	x	7_LEVEL ACVCOM+DCVCOM	VP1/VP2/VP3, VN1/VN2/VN3	VPOS1/VNEG1 VPOS2/VNEG2 VPOS3/VNEG3
1	0	0	3_LEVEL DCVCOM	VP3/VN3	VPOS3/VNEG3
1	1	0	3_LEVEL ACVCOM+DCVCOM	VP3/VN3	VPOS3/VNEG3
1	0	1	3_LEVEL DCVCOM	VP3/VN3, VP2/VN2	VPOS2/VNEG2
1	**1**	**1**	**3_LEVEL ACVCOM+DCVCOM**	**VP3/VN3, VP2/VN2**	**VPOS2/VNEG2**

(H) Power-OFF Sequence (3-Level Output Mode, Normal, DC-VCOM):



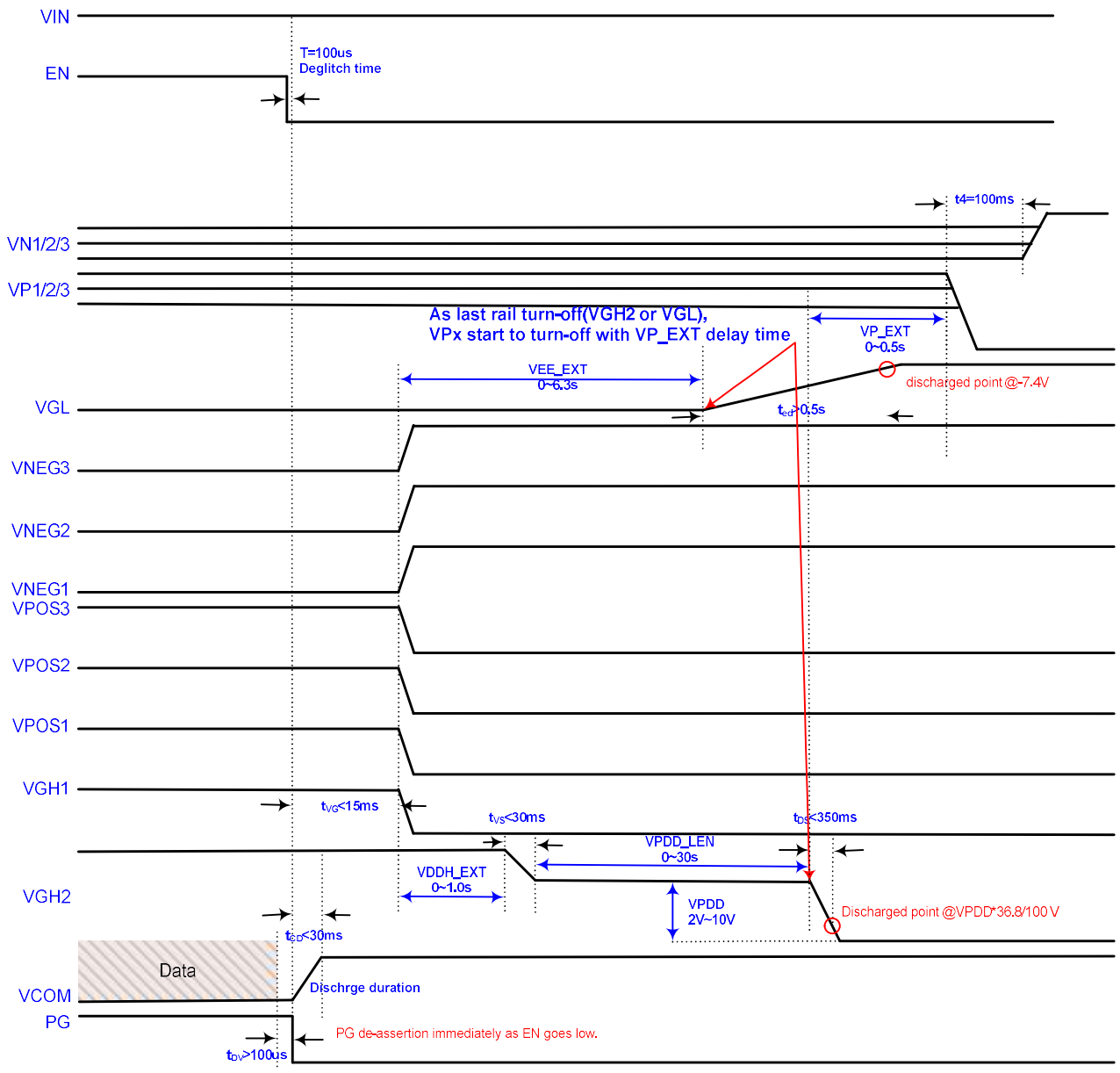
0x16H	0x0DH	0x0DH	Function	Power Rail active	
3/7 LEVEL[5]	TOGGLE_VCOM[4]	VCOM_3L_MODE[3]		DC/DC	Source Power
0	0	x	7_LEVEL DCVCOM	VP1/VP2/VP3, VN1/VN2/VN3	VPOS1/VNEG1 VPOS2/VNEG2 VPOS3/VNEG3
0	1	x	7_LEVEL ACVCOM+DCVCOM	VP1/VP2/VP3, VN1/VN2/VN3	VPOS1/VNEG1 VPOS2/VNEG2 VPOS3/VNEG3
1	**0**	**0**	**3_LEVEL DCVCOM**	**VP3/VN3**	**VPOS3/VNEG3**
1	1	0	3_LEVEL ACVCOM+DCVCOM	VP3/VN3	VPOS3/VNEG3
1	0	1	3_LEVEL DCVCOM	VP3/VN3, VP2/VN2	VPOS2/VNEG2
1	1	1	3_LEVEL ACVCOM+DCVCOM	VP3/VN3, VP2/VN2	VPOS2/VNEG2

(I) Power-OFF Sequence (7-Level Output Mode, VCOM/VGL Keep Alive):



1. For VCOM/VGL_MODE[6] =”1” set by I²C (register 0x0D), VCOM and VGL continue power-on after EPD update.

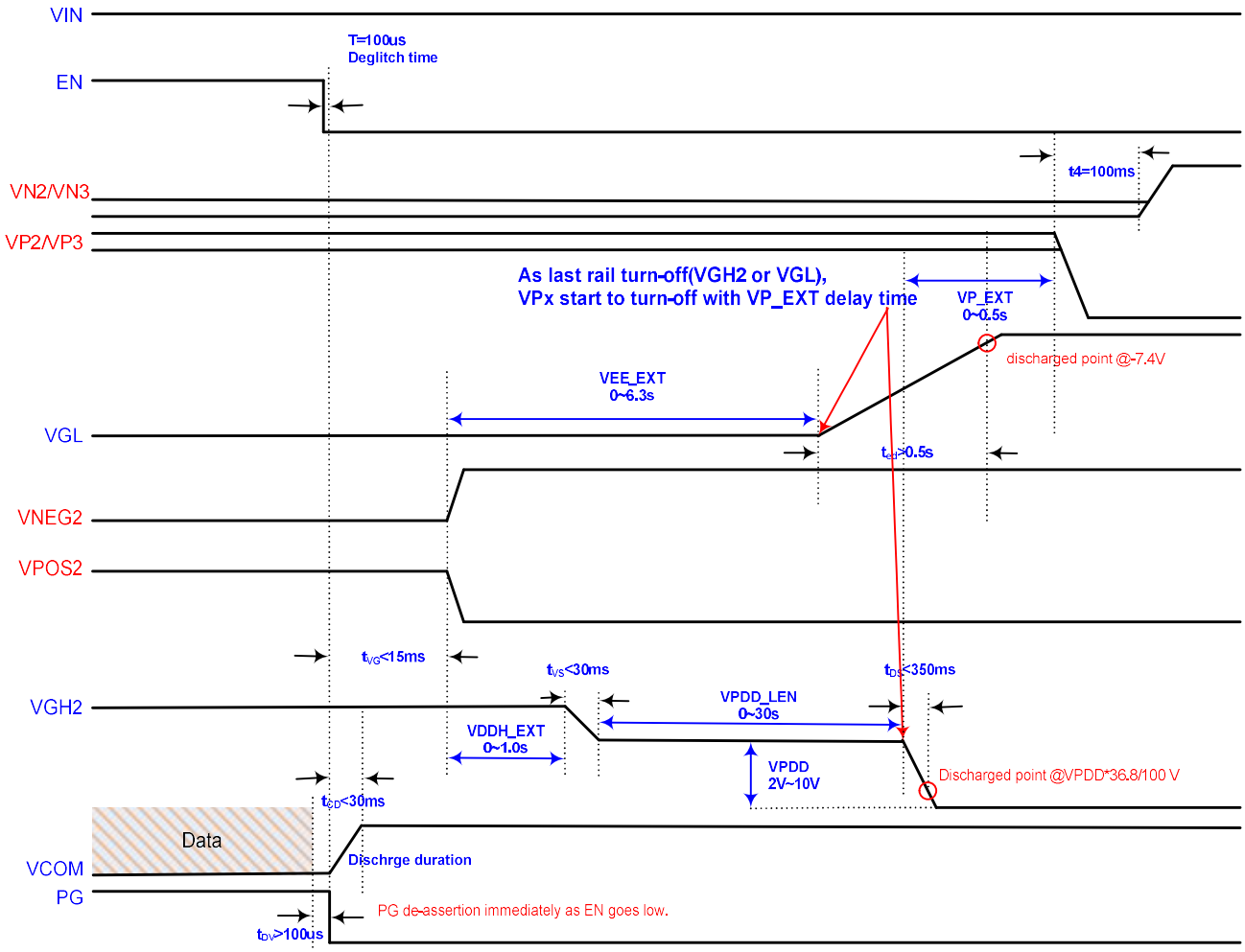
(J) Power-OFF Sequence (Post Drive Mode, 7-Level, DC-VCOM):



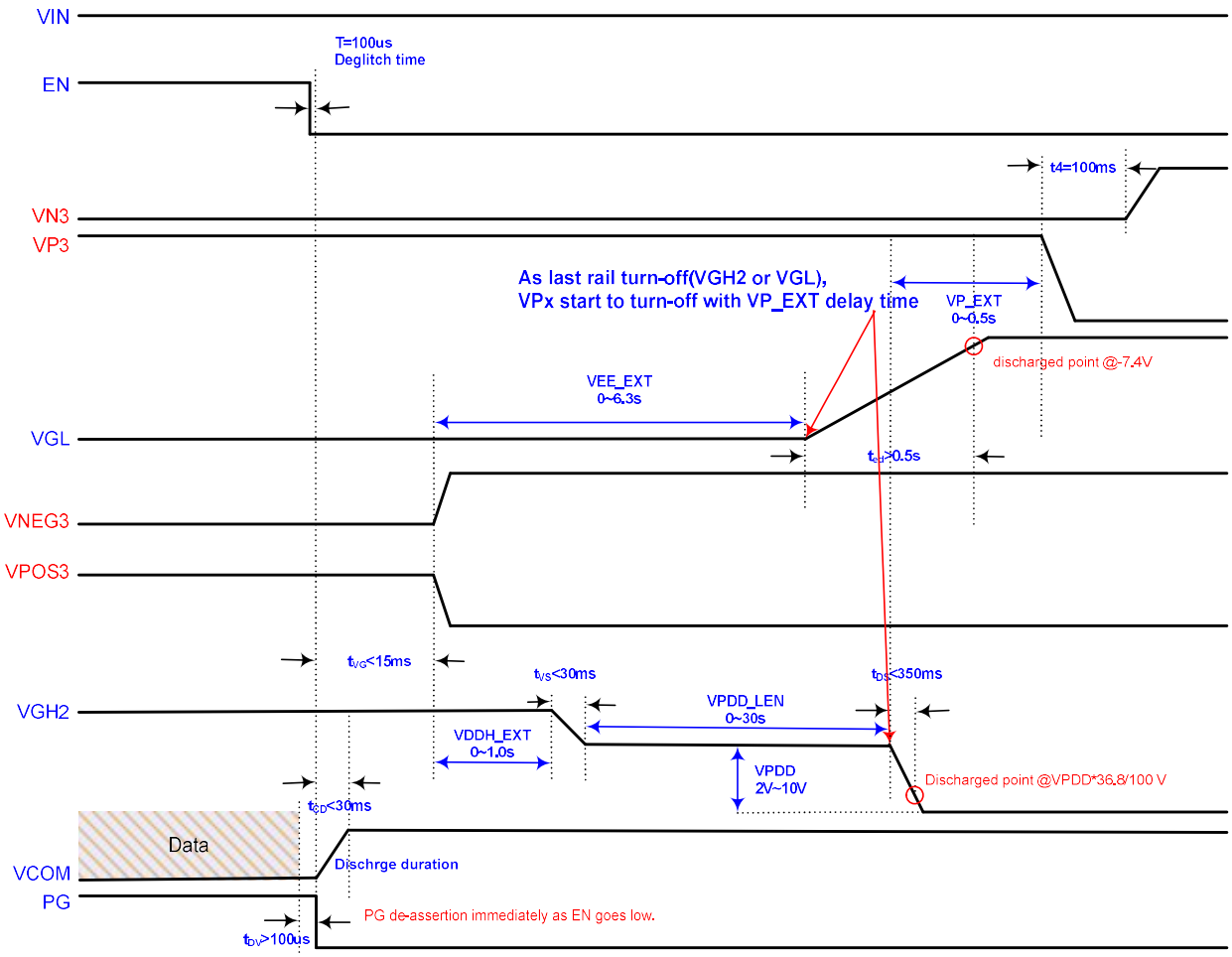
Post Drive Mode:

1. Only VGH2 has post drive mode (Lightness Mode).
2. The gate high voltage (VGH2) can be extended beyond that required for the normal active update. The extension time is given by VDDH_EXT. VDDH_EXT starts after t_{VG} time where t_{VG} must be less than 15ms.
3. In addition, VGH2 is pulled to VPDD in less than 30~50ms(t_{VS}) when the PMIC powers down the standard VGH2 voltage. VPDD will be powered on for the time duration of VPDD_LEN. In addition, VGH2 powers down with RC decay of t_{DS} (<350ms).
4. The low gate voltage (VGL) can be extended beyond that which is required for the normal active update. The extension time is given by VEE_EXT.
5. VCOM will quickly be pulled to ground through a low resistance path (<30ms) after the active drive. A low resistance path of less than 1kΩ is desirable.
6. As last rail turn-off(VGL or VGH2), VPx start to turn-off with VP_EXT delay time.

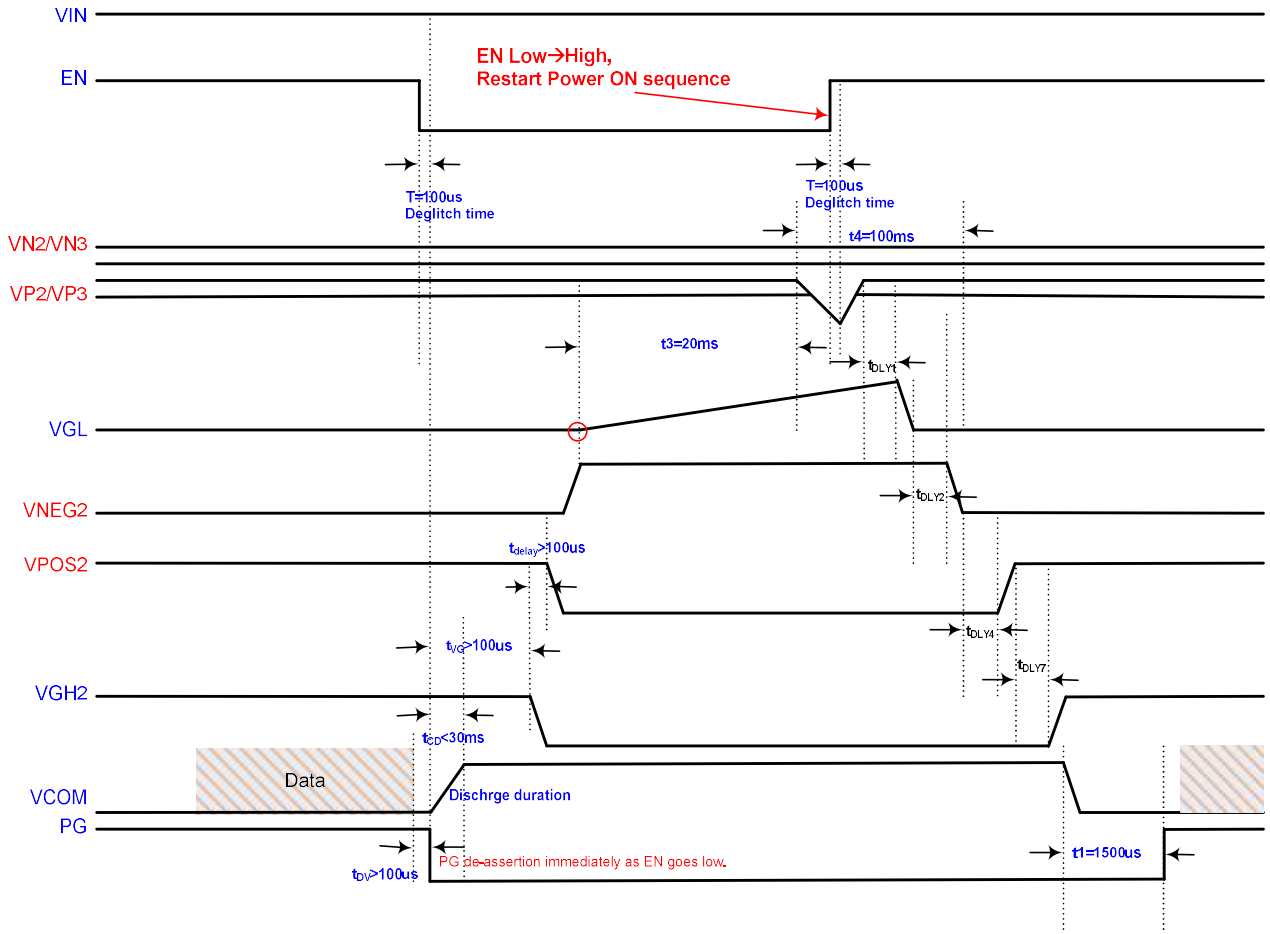
(K) Power-OFF Sequence (Post Drive Mode, 3-Level, AC-VCOM+DC-VCOM):



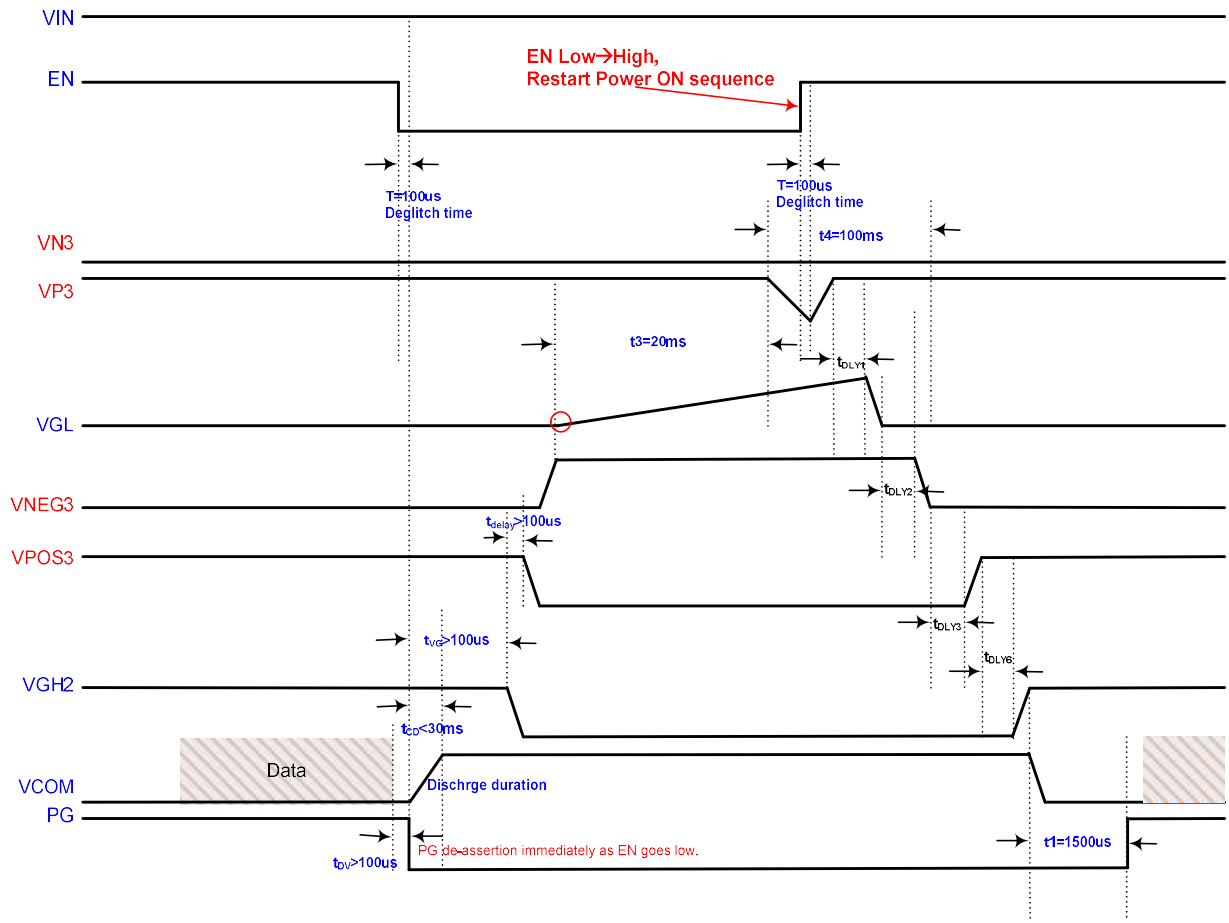
(M) Power-OFF Sequence (Post Drive Mode, 3-Level, DC-VCOM):



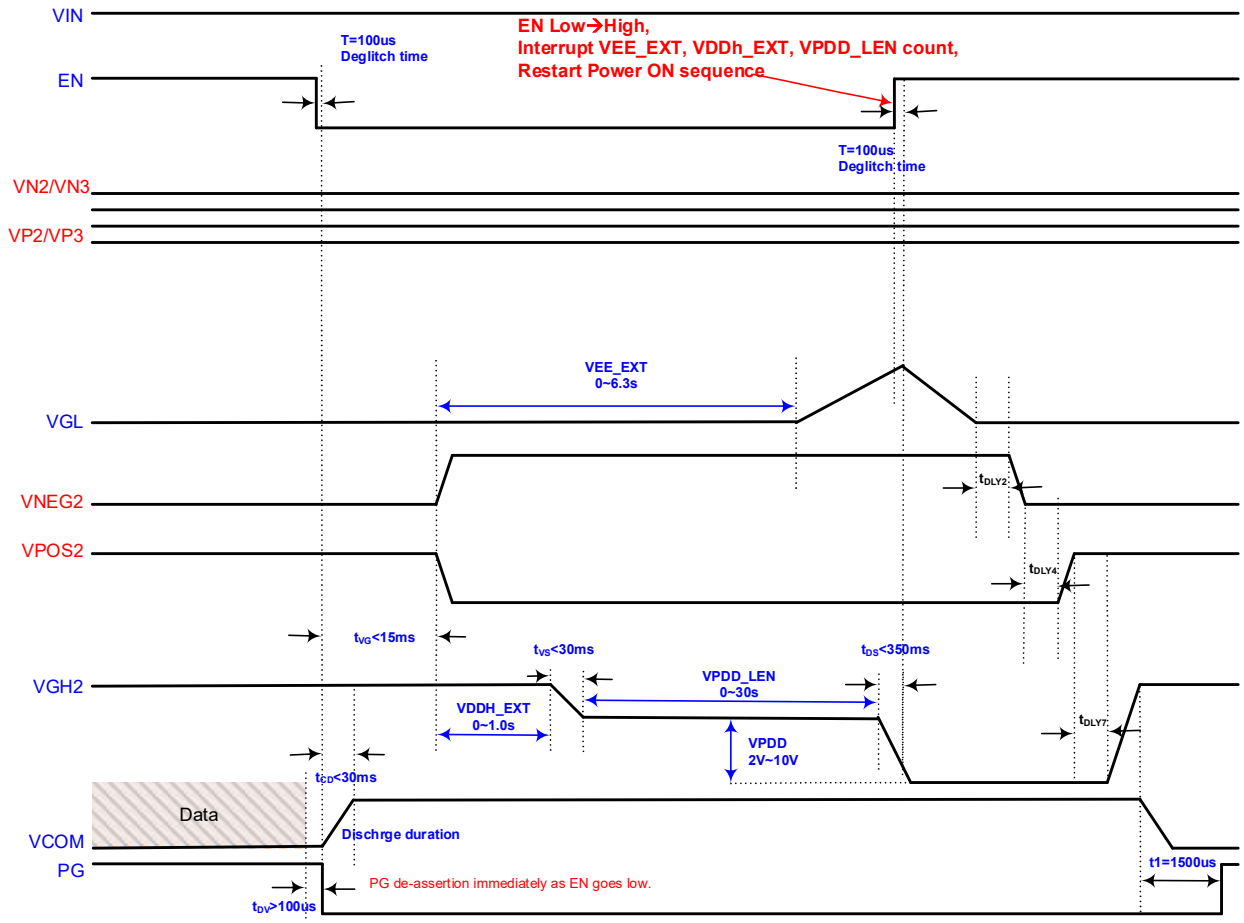
(N) Power-OFF to ON Sequence (3-Level Output, Normal, AC-VCOM):



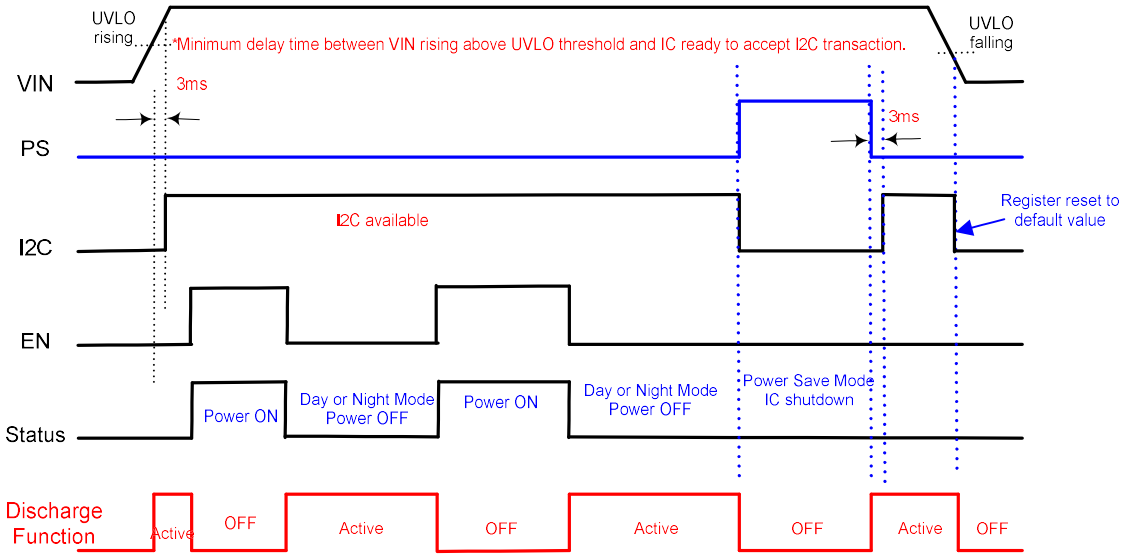
(O) Power-OFF to ON Sequence (3-Level Output, Normal, DC-VCOM):



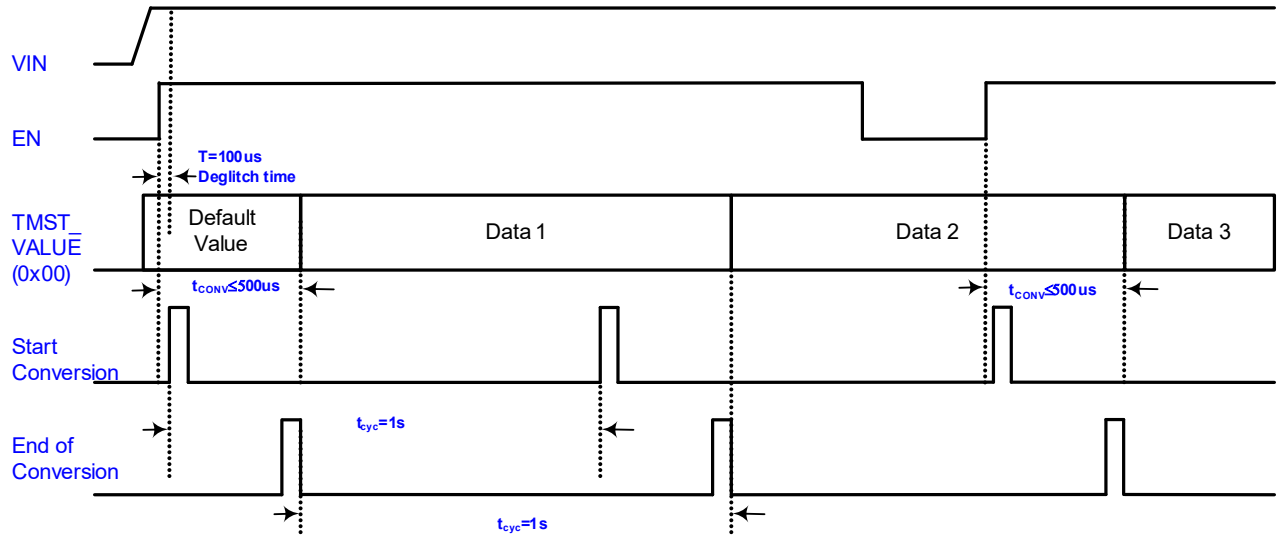
(P) Power-OFF to ON Sequence (Post Drive Mode, 3-Level, AC-VCOM+DC-VCOM):



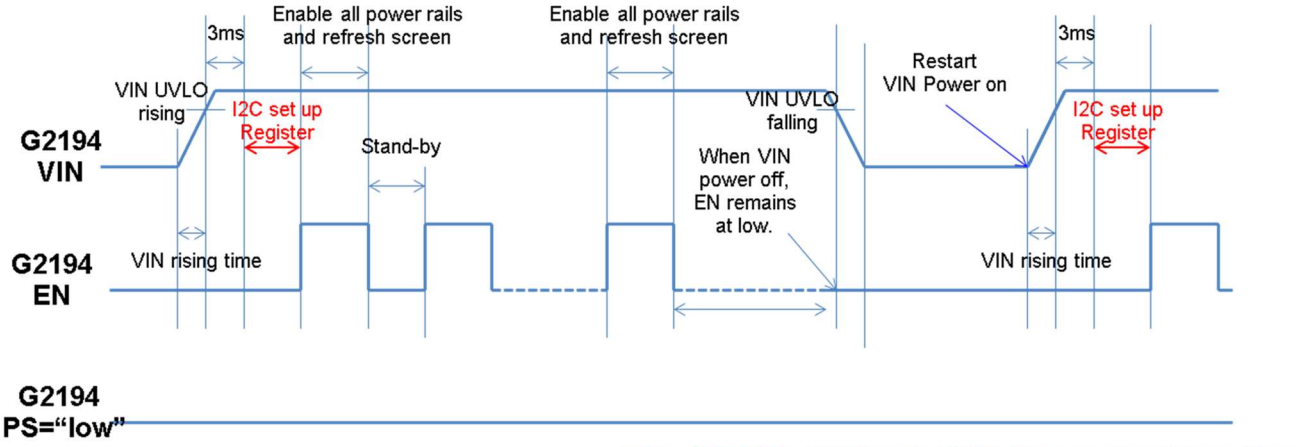
(Q) EN vs. I²C



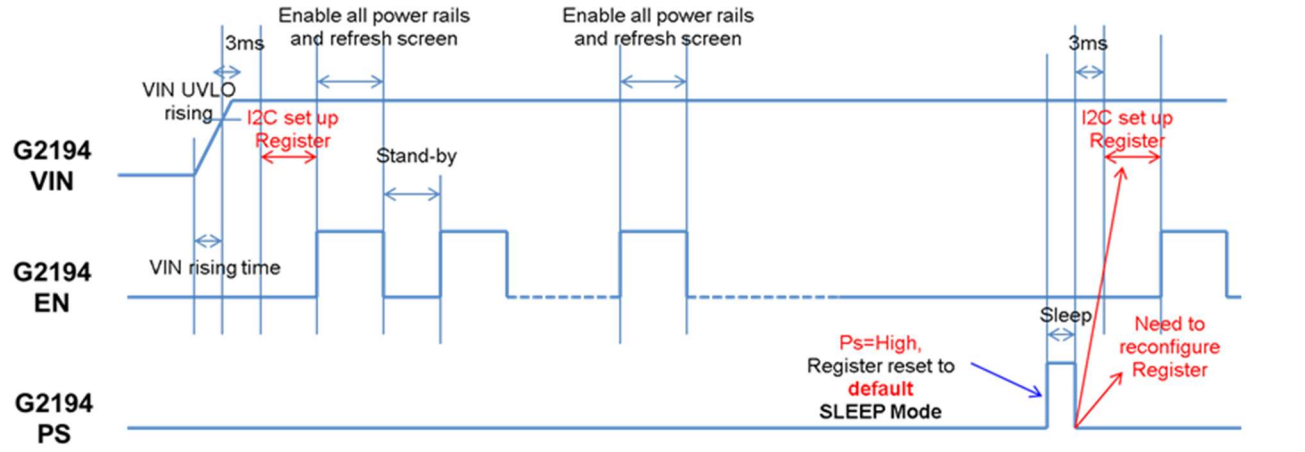
(R) EN vs. Temperature Acquisition



(S) VIN vs. EN/PS Power On Timing



*Note: If VCC(pin 14) drops to UVLO, it resets all register settings.



*Note: If VCC(pin 14) drops to UVLO, it resets all register settings.

G2194 I²C Command Set up Example for 8" ACeP2

G2194 GPIO setting	**PS=0 or floating (Normal operating, Standby or Active)**			
	EN=0 (Standby Mode, disable all power rails, allow to accept I²C register settings)			
Normal Mode	**The following I²C command settings follow the register definition in the datasheet.**			
Step1. Set VOUT	**ID(No include R/W Bit)**	**Address**	**Data**	**Note**
VPOS1 Voltage	48	01	0720	Set VPOS1= +10V, enable discharge
VNEG1 Voltage	48	03	0720	Set VNEG1= -10V, enable discharge
VPOS2 Voltage	48	05	0720	Set VPOS2= +17V, enable discharge
VNEG2 Voltage	48	07	0720	Set VNEG2= -17V, enable discharge
VPOS3 Voltage	48	09	02CB	Set VPOS3= +24V, enable discharge
VNEG3 Voltage	48	0B	02CB	Set VNEG3= -24V, enable discharge
Step2. Set delay time	**ID(No include R/W Bit)**	**Address**	**Data**	**Note**
	48	13	FF	t_{DYL1}~t_{DYL4}=4ms
	48	14	FF	t_{DYL5}~t_{DYL8}=4ms
	48	15	C0	t_{DYL9}=4ms
Step3. Set VCOM	**ID(No include R/W Bit)**	**Address**	**Data**	**Note**
VCOM Voltage	48	0D	0932	Set VCOM= **-1V**, enable discharge
Step4. Set Mode	**ID(No include R/W Bit)**	**Address**	**Data**	**Note**
	48	16	**D0**	7 level only VGH2/VGL,SS time=6ms Enable VGH2 discharge function.
GPIO setting	**EN=1(Active Mode, enable all power rails)**			

G2194 I²C Command Set up Example with Post Drive Mode for 8" ACeP2

G2194 GPIO setting)	**PS=0 (Normal operating, Standby or Active)**			
	EN=0 (Standby Mode, disable all power rails, allow to accept I2C register settings)			
Normal Mode	**The following I2C command settings follow the register definition in the datasheet.**			
Step1. Set VOUT	**ID(No include R/W Bit)**	**Address**	**Data**	**Note**
VPOS1 Voltage	48	01	0590	Set VPOS1= +6V, enable discharge
VNEG1 Voltage	48	03	0590	Set VNEG1= -6V, enable discharge
VPOS2 Voltage	48	05	05D3	Set VPOS2= +12V, enable discharge
VNEG2 Voltage	48	07	05D3	Set VNEG2= -12V, enable discharge
VPOS3 Voltage	48	09	02CB	Set VPOS3= +24V, enable discharge
VNEG3 Voltage	48	0B	02CB	Set VNEG3= -24V, enable discharge
Step2. Set delay time	**ID(No include R/W Bit)**	**Address**	**Data**	**Note**
	48	13	FF	t_{DYL1}~t_{DYL4}=4ms
	48	14	FF	t_{DYL5}~t_{DYL8}=4ms
	48	**15**	**E0**	**t_{DYL9}=4ms, enable POST, VDDH_EXT=0ms**
Step3. Set VCOM	**ID(No include R/W Bit)**	**Address**	**Data**	**Note**
VCOM Voltage	48	0D	0932	Set VCOM= **-1V**, enable discharge
Step4. Set Mode	**ID(No include R/W Bit)**	**Address**	**Data**	**Note**
	48	**16**	**D0**	7 level only VGH2/VGL,SS time=6ms enable VGH2 discharge, **VP_EXT=0ms**
Step5. Post Drive Mode setting	**ID(No include R/W Bit)**	**Address**	**Data**	**Note**
	48	**0F**	**18**	**VPDD=3.5V**
	48	**11**	**01**	**VEE_EXT=0s**
	48	**17**	**5F**	**VPDD_LEN=6s**
GPIO setting	**EN=1(Active Mode, enable all power rails)**			

Register Address Map

Register	Address(Hex)	Name	Default Value	Description
0	0x00	TMST_VALUE	0001 1001	Thermistor value read by ADC
1	0x01*	VPOS1_SETTING & VPOS1_DIS, FREQ_VP1	0000 0111	Voltage settings for VPOS1(10-bit) & VPOS1 discharge function
2	0x02*		0010 0000	
3	0x03*	VNEG1_SETTING & VNEG1_DIS, FREQ_VN1	0000 0111	Voltage settings for VNEG1(10-bit) & VNEG1 discharge function
4	0x04*		0010 0000	
5	0x05*	VPOS2_SETTING & VPOS2_DIS, TRACK2, FREQ_VP2	0000 0110	Voltage settings for VPOS2(10-bit) & VPOS2 discharge function & Tracking
6	0x06*		1001 1011	
7	0x07*	VNEG2_SETTING & VNEG2_DIS, FREQ_VN2	0000 0110	Voltage settings for VNEG2(10-bit) & VNEG2 discharge function
8	0x08*		1001 1011	
9	0x09*	VPOS3_SETTING VPOS3_DIS, TRACK3, FREQ_VP3	0000 0010	Voltage settings for VPOS3(10-bit) & VPOS3 discharge function & Tracking
10	0x0A*		1100 1011	
11	0x0B*	VNEG3_SETTING & VNEG3_DIS, FREQ_VN3	0000 0010	Voltage settings for VNEG3(10-bit) & VNEG3 discharge function
12	0x0C*		1100 1011	
13	0x0D*	DC VCOM_SETTING, VCOM_CTL, VCOM/VGL Keep alive , VCOM_DIS &VCOM toggle, VCOM_3L_MODE	0000 1001	Voltage settings for VCOM(9-bit) & VCOM Control , VCOM/VGL power off sequence mode , VCOM discharge function , DC/Toggle VCOM switch(1-bit) & Source Power select for 3-LEVEL
14	0x0E*		0110 0110	
15	0x0F*	VCOMH_SETTING & VPDD	0001 0000	Voltage settings for VCOMH(9-bit) & VPDD voltage setting for post drive discharge function(5-bit)
16	0x10*		1010 1010	
17	0x11*	VCOML_SETTING & VEE_EXT SETTING	0000 0001	Voltage settings for VCOML(9-bit) & VEE_EXT delay setting for post drive discharge function(7-bit)
18	0x12*		0101 0101	
19	0x13	PWRON_DELAY1	1010 1010	Power on delay time set for VGL & VNEGx
20	0x14	PWRON_DELAY2	1010 1010	Power on delay time set for VPOSx & VGH1 or VGH2
21	0x15	PWRON_DELAY3 , MODE & VDDH_EXT SETTING	1000 0000	Power on delay time set for VGH2, Normal Mode or Post Drive Mode and VDDH_EXT delay setting for post drive discharge function
22	0x16	CONTROL_REG1 & VP_EXT	0000 0100	Soft-Start time setting(2-bit) 3 level and 7-level output switch(1-bit) 7-Level VGH2/VGH1 or VGH2 select VGH1/VGH2 Discharge function
				VP_EXT delay setting for post drive discharge function(2-bit)
23	0x17	VPDD_LEN	0000 0000	VPDD_LEN delay setting for post drive discharge function(8-bit)
24	0x18	KEEP ALIVE & ON_OFF	0100 0000	Power On/Off Control(1-bit) VN1/2/3 & VP1/2/3 Keep alive channel for VCOM/VGL power off keep alive sequence mode
25	0x19	Fault Flag1	0000 0000	Show error code and Power-Good signal
26	0x1A	Fault Flag2	0000 0000	Show error code
27	0x1B	Fault Flag3	0000 0000	Show error code

***As long as the DAC settings in the Register need to be more than 8bits, such as VPOSx[9:0]/VNEGx[9:0]/VCOM[8:0] /VCOMH[8:0]/ VCOML[8:0], I²C command should use word write for continuous writing.**
If the I²C command uses byte write mode on these registers, only the low byte of DAC will be written.

0x00h

Address-0x00h								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	TMST_VALUE[7:0]							
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	1	1	0	0	1

Field Name	BIT Definition
TMST_VALUE[7:0]	Temperature read-out 1111 0110 : < -10°C 1111 0110 : -10°C 1111 0111 : -9°C …….. 1111 1110 : -2°C 1111 1111 : -1°C 0000 0000 : 0°C 0000 0001 : 1°C 0000 0010 : 2°C …….. 0001 1001 : 25°C …….. 0101 0101 : 85°C 0101 0101 : > 85°C

0x01h & 0x02h

Address-0x01h								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VPOS1_DIS	Reserved				FREQ_VP1	VPOS1[9:8]	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	1	1	1
Address-0x02h								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VPOS1[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	1	0	0	0	0	0

Field Name	BIT Definition
VPOS1_DIS[7]	**0: enable VPOS1 discharge function** 1: disable VPOS1 discharge function
Reserved[6:3]	Reserved bit
FREQ_VP1[2]	VP1 Switching Frequency 0: 500KHz **1: 1MHz**
VPOS1[9:0]	VPOS1 voltage adjustment **VPOS1=VPOS1[9:0]*10mV+2.0V**

0x03h & 0x04h

Address-0x03h								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VNEG1_DIS	Reserved				FREQ_VN1	VNEG1[9:8]	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	1	1	1
Address-0x04h								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VNEG1[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	1	0	0	0	0	0

Field Name	BIT Definition
VNEG1_DIS[7]	**0: enable VNEG1 discharge function** 1: disable VNEG1 discharge function
Reserved[6:3]	Reserved bit
FREQ_VN1[2]	VN1 Switching Frequency 0: 500KHz **1: 1MHz**
VNEG1[9:0]	VNEG1 voltage adjustment **VNEG1=VNEG1[9:0]*-10mV-2.0V**

0x05h & 0x06h

Address-0x05h								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VPOS2_DIS	TRACK2	Reserved			FREQ_VP2	VPOS2[9:8]	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	1	1	0
Address-0x06h								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VPOS2[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	0	0	1	1	0	1	1

Field Name	BIT Definition
VPOS2_DIS[7]	**0: enable VPOS2 discharge function** 1: disable VPOS2 discharge function
TRACK2[6]	VPOS2/VNEG2 Tracking function **0: disable** 1: enable(Only for VPOS/VNEG are of opposite sign but same magnitude)
Reserved[5:3]	Reserved bit
FREQ_VP2[2]	VP2 Switching Frequency 0: 500KHz **1: 1MHz**
VPOS2[9:0]	VPOS2 voltage adjustment **VPOS2=VPOS2[9:0]*15mV+5.0V**

0x07h & 0x08h

Address-0x07h								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VNEG2_DIS	Reserved				FREQ_VN2	VNEG2[9:8]	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	1	1	0
Address-0x08h								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VNEG2[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	0	0	1	1	0	1	1

Field Name	BIT Definition
VNEG2_DIS[7]	**0: enable VNEG2 discharge function** 1: disable VNEG2 discharge function
Reserved[6:3]	Reserved bit
FREQ_VN2[2]	VN2 Switching Frequency 0: 500KHz **1: 1MHz**
VNEG2[9:0]	VNEG2 voltage adjustment **VNEG2=VNEG2[9:0]*-15mV-5.0V**

0x09h & 0x0Ah

Address-0x09h								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VPOS3_DIS	TRACK3	Reserved			FREQ_VP3[	VPOS3[9:8]	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	1	0
Address-0x0Ah								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VPOS3[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	0	0	1	0	1	1

Field Name	BIT Definition
VPOS3_DIS[7]	**0: enable VPOS3 discharge function** 1: disable VPOS3 discharge function
TRACK3[6]	VPOS3/VNEG3 Tracking function **0: disable** 1: enable(Only for VPOS/VNEG are of opposite sign but same magnitude)
Reserved[5:3]	Reserved bit
FREQ_VP3[2]	VP3 Switching Frequency **0: 500KHz** 1: 1MHz
VPOS3[9:0]	VPOS3 voltage adjustment **VPOS3=VPOS3[9:0]*21mV+9.0V**

0x0Bh & 0x0Ch

Address-0x0Bh								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VNEG3_DIS	Reserved				FREQ_VN3	VNEG3[9:8]	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	1	0
Address-0x0Ch								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VNEG3[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	0	0	1	0	1	1

Field Name	BIT Definition
VNEG3_DIS[7]	**0: enable VNEG3 discharge function** 1: disable VNEG3 discharge function
Reserved[6:2]	Reserved bit
FREQ_VN3[2]	VN3 Switching Frequency **0: 500KHz** 1: 1MHz
VNEG3[9:0]	VNEG3 voltage adjustment **VNEG3=VNEG3[9:0]*-21mV-9.0V**

0x0Dh & 0x0Eh

Address-0x0Dh								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VCOMCTL	VCOM/VGL_MODE	VCOM_DIS	TOGGLE_VCOM	VCOM_3L_MODE	Reserved		VCOM[8]
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	1	0	0	1
Address-0x0Eh								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VCOM[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	1	1	0	0	1	1	0

Field Name	BIT Definition
VCOMCTL[7]	**0: VCOM on/off will follow the default sequence** 1: VCOM on/off is controlled by external VCOM_EN pin
VCOM/VGL_MODE[6]	**0: normal power off sequence for VCOM/VGL** 1: VCOM/VGL keep alive when power off after EPD update
VCOM_DIS[5]	**0: enable VCOM discharge function** 1: disable VCOM discharge function
TOGGLE VCOM[4]	**0: DC VCOM output** 1: Toggle VCOM output
VCOM_3L_MODE[3]	0: 3 LEVEL source power from VPOS3/VNEG3 **1: 3 LEVEL source power from VPOS2/VNEG2**
Reserved[2:1]	Reserved Bit
VCOM[8:0]	VCOM voltage adjustment **VCOM=5.0V-VCOM[8:0]*19.6mV**

0x0Fh & 0x10h

Address-0x0Fh								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VPDD[7:3]					Reserved		VCOMH[8]
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	1	0	0	0	0
Address-0x10h								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VCOMH[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	0	1	0	1	0	1	0

Field Name	BIT Definition
VPDD[7:3]	VPDD voltage setting for post drive discharge function **VPDD=VPDD[7:3]*500mV+2.0V**
Reserved[2:1]	**Reserved bit**
VCOMH[8:0]	VCOMH voltage adjustment **VCOMH=18V-VCOMH[8:0]*17.6mV**

0x11h & 0x12h

Address-0x11h								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VEE_EXT[7:1]							VCOML[8]
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	1
Address-0x12h								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VCOML[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	1	0	1	0	1	0	1

Field Name	BIT Definition
VEE_EXT[7:1]	VEE_EXT delay setting for post drive discharge function(0~6.3s) **VEE_EXT=VEE_EXT[7:1]*50ms**
VCOML[8:0]	VCOML voltage adjustment **VCOML=-9.0V -VCOML[8:0]*-17.6mV**

0x13h

Address-0x13h								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	t_{DYL1}		t_{DYL2}		t_{DYL3}		t_{DYL4}	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	0	1	0	1	0	1	0

Field Name	BIT Definition
t_{DYL1}[7:6]	Delay time set from VPx to VGL 00: 0ms 01: 1ms **10: 2ms** 11: 4ms
t_{DYL2}[5:4]	Delay time set from VGL to VNEG3 00: 0ms 01: 1ms **10: 2ms** 11: 4ms
t_{DYL3}[3:2]	Delay time set from VNEG3 to VNEG2 00: 0ms 01: 1ms **10: 2ms** 11: 4ms
t_{DYL4}[1:0]	Delay time set from VNEG2 to VNEG1 00: 0ms 01: 1ms **10: 2ms** 11: 4ms

0x14h

Address-0x14h								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	t_{DYL5}		t_{DYL6}		t_{DYL7}		t_{DYL8}	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	0	1	0	1	0	1	0

Field Name	BIT Definition
t_{DYL5}[7:6]	Delay time set from VNEG1 to VPOS3 00: 0ms 01: 1ms **10: 2ms** 11: 4ms
t_{DYL6}[5:4]	Delay time set from VPOS3 to VPOS2 00: 0ms 01: 1ms **10: 2ms** 11: 4ms
t_{DYL7}[3:2]	Delay time set from VPOS2 to VPOS1 00: 0ms 01: 1ms **10: 2ms** 11: 4ms
t_{DYL8}[1:0]	Delay time set from VPOS1 to VGH1 00: 0ms 01: 1ms **10: 2ms** 11: 4ms

0x15h

Address-0x15h								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	t_{DYL9}		MODE	VDDH_EXT[4:0]				
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	0	0	0	0	0	0	0

Field Name	BIT Definition
t_{DYL9}[7:6]	Delay time set from VGH1 to VGH2 00: 0ms 01: 1ms **10: 2ms** 11: 4ms
MODE[5]	**0: normal mode power off sequence** 1: post drive discharge mode power off sequence
VDDH_EXT[4:0]	VDDH_EXT delay setting for post drive discharge function(0~1s) **VDDH_EXT=VDDH_EXT[4:0]*50ms**

0x16h

Address-0x16h								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	SS		3/7 LEVEL	VGH_7_SEL	VGH1_DIS	VGH2_DIS	VP_EXT	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	1	0	0

Field Name	BIT Definition
SS[7:6]	PMIC soft-start time(VPOS1/VPOS2/VPOS3/VNEG1/VNEG2/VNEG3) **00: 3ms** 01: 4ms 10: 5ms 11: 6ms
3/7 LEVEL[5]	**0: 7-Level output** 1: 3-Level output
VGH_7_SEL[4]	**0: 7-Level output VGH2/VGH1/VGL** 1: 7-Level output only VGH2/VGL
VGH1_DIS[3]	**0: enable VGH1 discharge function** 1: disable VGH1 discharge function
VGH2_DIS[2]	0: enable VGH2 discharge function **1: disable VGH2 discharge function**
VP_EXT[1:0]	VP_EXT delay setting for post drive discharge function(0~500ms) **00: 0ms** 01: 250ms 10: 500ms 11: Reserved

0x17h

Address-0x17h								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VPDD_LEN[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Field Name	BIT Definition
VPDD_LEN[7:0]	VPDD_LEN delay setting(0~30s) **VPDD_LEN follow reguest as below**

Index	Time(ms)	Index	Time(ms)	Index	Time(ms)	Index	Time(ms)
0	0	64	3820	128	8850	192	16230
1	50	65	3890	129	8950	193	16380
2	110	66	3960	130	9040	194	16530
3	160	67	4030	131	9130	195	16680
4	210	68	4090	132	9230	196	16830
5	270	69	4160	133	9320	197	16980
6	320	70	4230	134	9420	198	17140
7	380	71	4300	135	9510	199	17290
8	430	72	4370	136	9610	200	17450
9	490	73	4440	137	9710	201	17610
10	540	74	4510	138	9810	202	17770
11	600	75	4580	139	9900	203	17930
12	650	76	4650	140	10000	204	18100
13	710	77	4720	141	10100	205	18260
14	760	78	4800	142	10200	206	18430
15	820	79	4870	143	10300	207	18600
16	870	80	4940	144	10400	208	18770
17	930	81	5010	145	10510	209	18940
18	990	82	5080	146	10610	210	19120
19	1040	83	5160	147	10710	211	19290
20	1100	84	5230	148	10820	212	19470
21	1160	85	5310	149	10920	213	19650
22	1210	86	5380	150	11030	214	19830
23	1270	87	5450	151	11130	215	20020
24	1330	88	5530	152	11240	216	20210
25	1390	89	5600	153	11350	217	20390

Index	Time(ms)	Index	Time(ms)	Index	Time(ms)	Index	Time(ms)
26	1440	90	5680	154	11460	218	20590
27	1500	91	5760	155	11570	219	20780
28	1560	92	5830	156	11680	220	20980
29	1620	93	5910	157	11790	221	21170
30	1680	94	5990	158	11900	222	21370
31	1740	95	6060	159	12010	223	21580
32	1800	96	6140	160	12120	224	21780
33	1860	97	6220	161	12240	225	21990
34	1920	98	6300	162	12350	226	22200
35	1980	99	6380	163	12470	227	22420
36	2040	100	6460	164	12580	228	22640
37	2100	101	6540	165	12700	229	22860
38	2160	102	6620	166	12820	230	23080
39	2220	103	6700	167	12940	231	23300
40	2280	104	6780	168	13060	232	23530
41	2340	105	6860	169	13180	233	23770
42	2400	106	6940	170	13300	234	24000
43	2460	107	7020	171	13420	235	24240
44	2530	108	7110	172	13540	236	24490
45	2590	109	7190	173	13670	237	24730
46	2650	110	7270	174	13790	238	24990
47	2710	111	7360	175	13920	239	25240
48	2780	112	7440	176	14050	240	25500
49	2840	113	7520	177	14170	241	25760
50	2900	114	7610	178	14300	242	26030
51	2970	115	7700	179	14430	243	26300
52	3030	116	7780	180	14570	244	26580
53	3100	117	7870	181	14700	245	26860
54	3160	118	7960	182	14830	246	27150
55	3230	119	8040	183	14970	247	27440
56	3290	120	8130	184	15100	248	27740
57	3360	121	8220	185	15240	249	28050
58	3420	122	8310	186	15380	250	28360
59	3490	123	8400	187	15520	251	28670
60	3550	124	8490	188	15660	252	28990
61	3620	125	8580	189	15800	253	29320
62	3690	126	8670	190	15940	254	29660
63	3750	127	8760	191	16090	255	30000

0x18h

Address-0x18h								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	Reserved	ON_OFF	VP3_Alive	VP2_Alive	VP1_Alive	VN3_Alive	VN2_Alive	VN1_Alive
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	1	0	0	0	0	0	0

Field Name	BIT Definition
Reserved[7]	**Reserved bit**
ON_OFF[6]	0: turn off all power rails (VPx,VNx,VPOSx,VNEGx,VGH1,VGH2,VGL,VCOM) **1: turn on all power rails (VPx,VNx,VPOSx,VNEGx,VGH1,VGH2,VGL,VCOM)**
Keep_Alive[5:0]	Keep Alive Control @ VCOM/VGL keep alive power off sequence **0: Normal power off** 1: Keep Alive

0x19h

Address-0x19h								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	PG	TSD	FLT_VP1	FLT_VP2	FLT_VP3	FLT_VN1	FLT_VN2	FLT_VN3
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0

Field Name	BIT Definition
PG[7]	**0: VPOS1/2/3, VNEG1/2/3, VGH1/2, VGL are not in regulation or turn off** 1: VPOS1/2/3, VNEG1/2/3, VGH1/2, VGL are in regulation
TSD[6]	**0: no fault event** 1: Thermal shutdown
FLT_VP1[5]	**0: no fault event** 1: UVP or SCP
FLT_VP2[4]	**0: no fault event** 1: UVP or SCP
FLT_VP3[3]	**0: no fault event** 1: UVP or SCP
FLT_VN1[2]	**0: no fault event** 1: UVP or SCP
FLT_VN2[1]	**0: no fault event** 1: UVP or SCP
FLT_VN3[0]	**0: no fault event** 1: UVP or SCP

0x1Ah

Address-0x1Ah								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	FLT_VPOS1	FLT_VPOS2	FLT_VPOS3	FLT_VNEG1	FLT_VNEG2	FLT_VNEG3	FLT_VGH1	FLT_VGH2
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0

Field Name	BIT Definition
FLT_VPOS1[7]	**0: no fault event**
	1: UVP or SCP
FLT_VPOS2[6]	**0: no fault event**
	1: UVP or SCP
FLT_VPOS3[5]	**0: no fault event**
	1: UVP or SCP
FLT_VNEG1[4]	**0: no fault event**
	1: UVP or SCP
FLT_VNEG2[3]	**0: no fault event**
	1: UVP or SCP
FLT_VNEG3[2]	**0: no fault event**
	1: UVP or SCP
FLT_VGH1[1]	**0: no fault event**
	1: UVP or SCP
FLT_VGH2[0]	**0: no fault event**
	1: UVP or SCP

0x1Bh

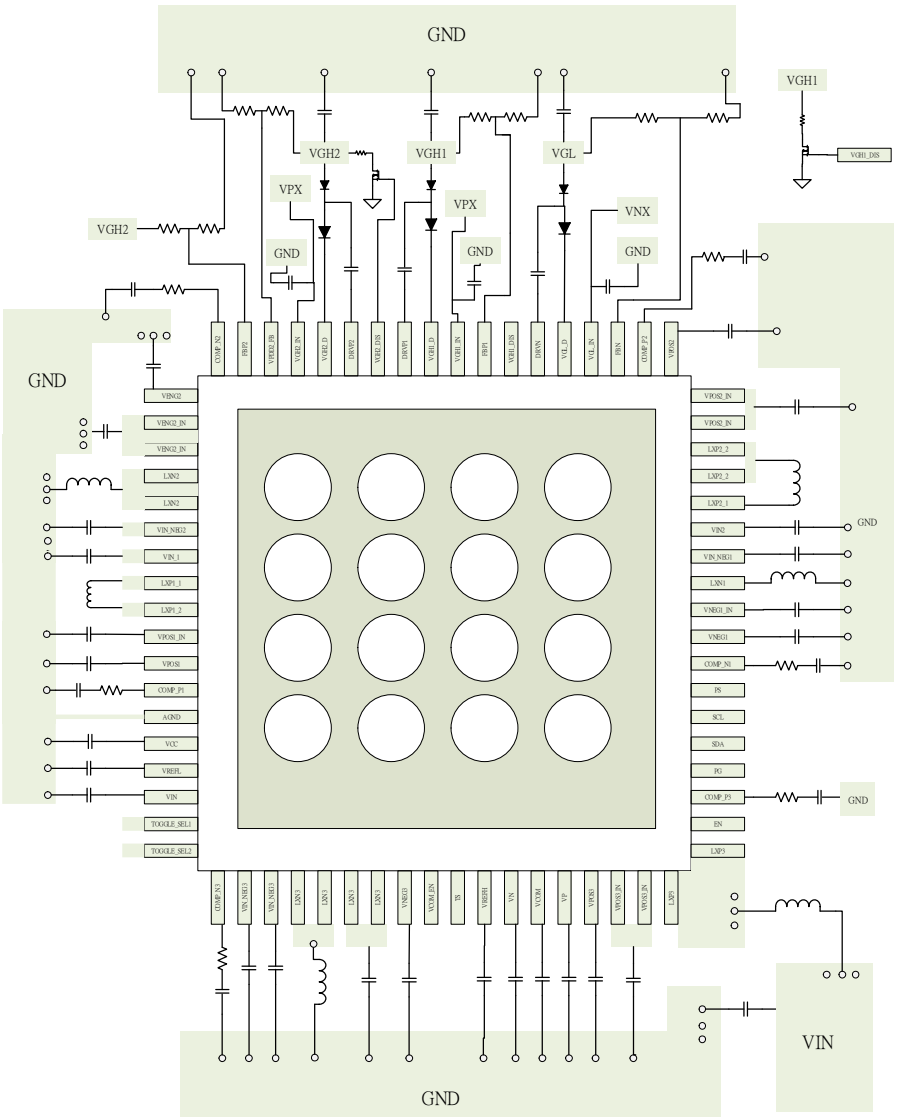
Address-0x1Bh								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	FLT_VGL	FLT_VCOM	Reserved					
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0

Field Name	BIT Definition
FLT_VGL[7]	**0: no fault event**
	1: UVP or SCP
FLT_VCOM[6]	**0: no fault event**
	1: SCP
Reserved[5:0]	**Reserved bit**

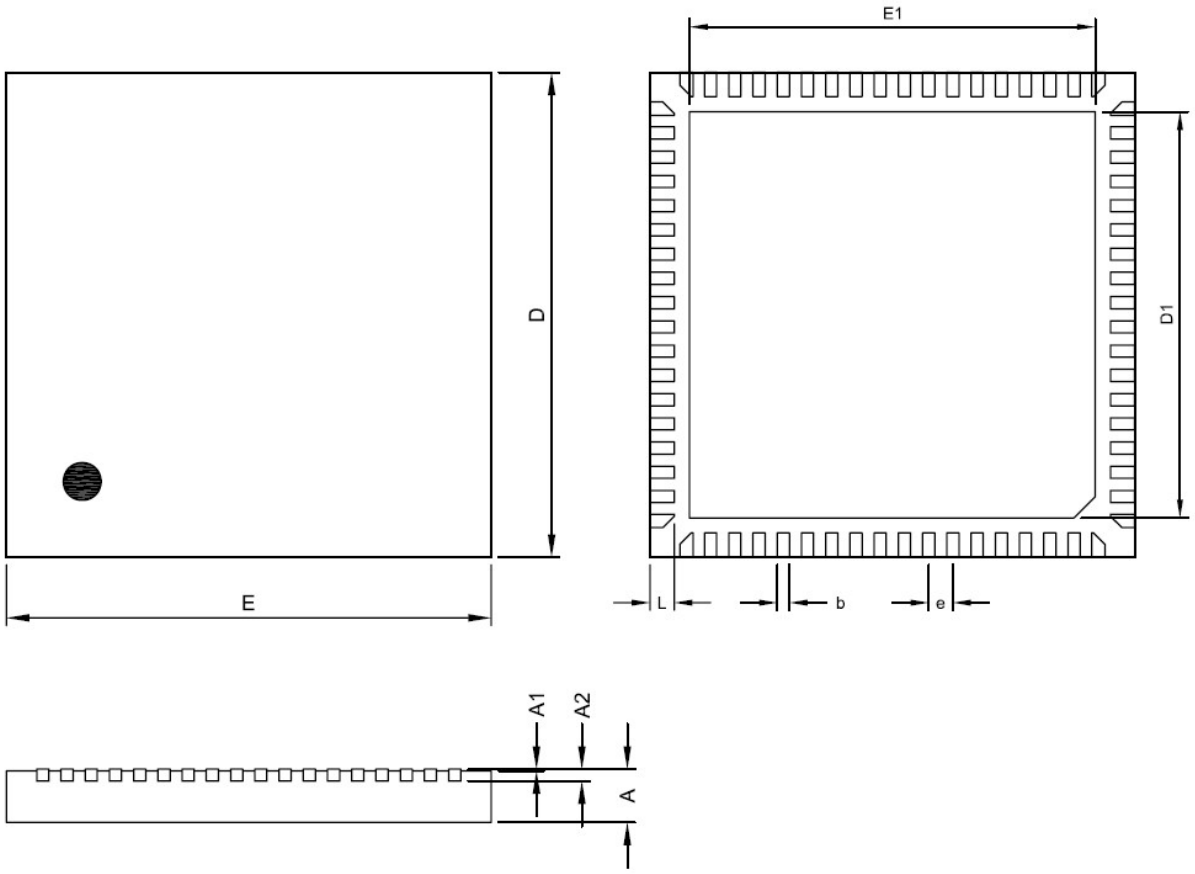
PCB Layout Guide

Layout is very important of good power supply design. The PCB traces can radiate excessive noise and contribute to converter instability with improper layout. The following layout recommendations will help guide you through a good layout.

- The VIN1、VIN2、VIN_NEG1、VIN_NEG2、VIN_NEG3、VGH1_IN、VGH2_IN and VGL_IN pins should be by-passed to ground with a low ESR ceramic by-pass capacitor. The optimum placement is close-set to the VIN1、VIN2、VIN_NEG1、VIN_NEG2、VIN_NEG3、VGH1_IN、VGH2_IN and VGL_IN pins of the de-vice.
- The FBP1、FBP2、VPDD2_FB、FBN、VPOS1_IN、VPOS2_IN 、VPOS3_IN、VNEG1_IN、VNEG2_IN and VNEG3_IN pins traces should be routed away from any potential noise source to avoid coupling.
- The LXx trace should be kept on the PCB top layer and free of any vias.
- The PGND should be tied to the PCB ground plane with multiple vias. .
- The VCC、VREFH and VREFL pin to AGND with a low ESR ceramic bypass capacitor, bypass capacitor should be as close as possible to the VCC pin.
- The AGND pin should not be connected to the PGND on the PCB top layer.
- COMP_P1、COMP_P2 、COMP_P1 、COMP_N1、COMP_N2 and 、COMP_N3 pins to AGND with compensation Resistor and Capacitance.



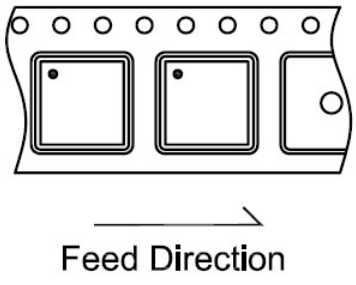
Package Information



QFN8X8-72 Package

Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.85	0.90	0.0315	0.0335	0.0354
A1	0.00	- - -	0.05	0.0000	- - -	0.0020
A2	0.20 REF			0.0079 REF		
D	7.90	8.00	8.10	0.3110	0.3150	0.3189
E	7.90	8.00	8.10	0.3110	0.3150	0.3189
D1	6.60	6.70	6.80	0.2598	0.2638	0.2677
E1	6.60	6.70	6.80	0.2598	0.2638	0.2677
b	0.13	0.20	0.27	0.0051	0.0079	0.0106
e	0.40 BSC			0.0157 BSC		
L	0.30	0.40	0.45	0.0118	0.0157	0.0177

Taping Specification



PACKAGE	Q'TY/REEL
QFN8X8-72	3,000ea