G2198A

PMIC for Color Electronic Paper Display

Features

- **3.0V to 5.5V Input Voltage Range**
- **Shutdown current <1uA**
- **Boost Converter VP1/VP2/VP3 for the Power Input of Positive Rails**
- **Inverting Buck-Boost Converter VN1/VN2/VN3 for the Power Input of Negative Rails**
- **Six Adjustable LDOs for Source Driver Supply:**
  -VPOS1/VNEG1: ±2V to ±12V, 200mA(max.)
  -VPOS2/VNEG2: ±5V to ±20V, 300mA(max.)
  -VPOS3/VNEG3: ±9V to ±26V, 400mA(max.)/ 500mA(max.) @±24V output
  -Accurate Output Voltage Tracking
  VPOS1+VNEG1=±50mV @ ±6V,
  VPOS2/3+VNEG2/3= ±50mV @ ±15V
- **Two Charge Pumps for Gate Driver Supply:**
  -VGH: 10V to 40V, 60mA(max.)
  -VGL: -10V to -40V, 60mA(max.)
- **Adjustable DC VCOM Driver for Accurate Panel Backplane Biasing**
  - **-5V to +0V, Source/Sink 60mA**
  - **±1.5% Accuracy**
  - **8-Bit DACs control**
- **Internal Active Discharge for VPOSx/VNEGx /VGH/ VGL /VCOM**
- **Thermistor Monitoring**
  - **-10°C to +85°C Temperature Range**
  - **±1.0°C Accuracy from 0°C to 50°C**
- **2-Wire I²C Slave Mode Interface (Address 0x48H,0x49H configured with A0)**
- **Protection: UVLO, OTP, OCP, SCP, UVP**
- **TQFN7X7-64**

General Description

The G2198A is a single-chip power management IC (PMIC) for color electronic paper displays EPD that provides source- and gate-driver power supplies, a VCOM amplifier, and a temperature sensor. All rails are adjustable through the I2C interface to accommodate specific panel requirements.

The G2198A is available in TQFN7X7-64 package and is specified over the -40°C to +85°C extended temperature range.

Ordering Information

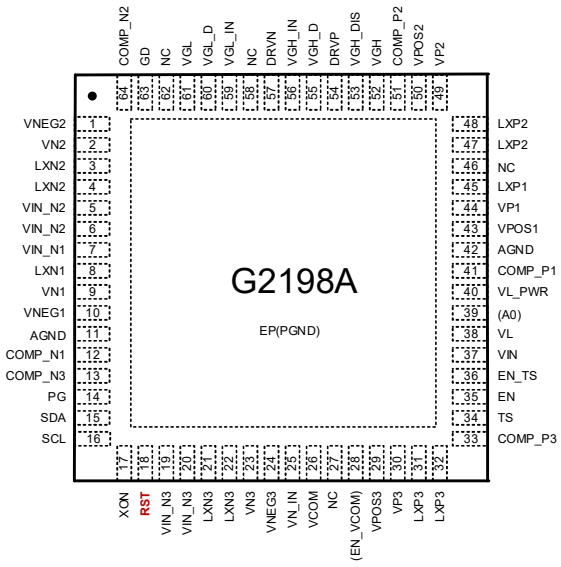
ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE (Green)
G2198AKW1U	2198A	-40°C to +85°C	TQFN7X7-64

Note: KW:TQFN7X7-64
1: Bonding code
U: Tape & Reel
Green: Lead Free / Halogen Free

Applications

- **Color EPD Power Supplies**

Pin Configuration



TQFN7X7-64

Absolute Maximum Ratings*1

VIN, VIN_Nx, VL, Input Voltage. . . . . .-0.3V to +6.0V
VP1, VPOS1,LXP1,VL_PWR input Voltage.. .-0.3V to 14V
VN1, LXN1, VNEG1 input Voltage . . . . . -14V to -0.3V
VP2,VPOS2,LXP2 input Voltage.. . .-0.3V to 22V
VN2, LXN2, VNEG2 input Voltage . . . . . -22V to -0.3V
VP3,VPOS3, LXP3, VGH_IN, VGH_D, DRVP input Voltage . . . . . -0.3V to 27V
VN3, VNEG3, LXN3, VN_IN,VGL_IN, VGL_D, DRVN input Voltage . . . .-27V to -0.3V
VGH, VGH_DIS input Voltage . . . . -0.3V to 42V
VGL input Voltage . . . . -42V to -0.3V
VCOM input Voltage . . . . -6.0V to 0.3V
SDA, SCL, EN, VCOM_EN, TS, PG, XON, GD, RST, COMP_Px, COMP_Nx Input Voltage . . . -0.3V to +5.5V
Thermal Resistance Junction to Ambient, (θ_{JA})
TQFN7X7-64. . . . . .27.5°C/W
Continuous Power Dissipation (T_A = +25°C)
TQFN7X7-64 . . . . . .4.5W
Operation Temperature . . . . . .-40°C to +85°C
Junction Temperature . . . . . .160°C
Storage Temperature Range . . . . . -65°C to 160°C
ESD Susceptibility (HBM) . . . . . .2kV(Note2)
Reflow Temperature (soldering, 10sec) . . . . . 260°C

Recommended Operation Conditions

VINx,VIN_Nx . . . . . 3.0V to 5.5V
VGH_IN . . . . . 6V to 26V
VGL_IN . . . . . -26V to -6V
Operating Ambient Temperature (T_A) . . .-10°C to 85°C

1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Device are ESD sensitive. Handling precaution recommended. The Human Body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.

Electrical Characteristics

(VIN=VIN_N1=VIN_N2=VIN_N3=3.6V, T_A=25°C)

The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
GENERAL						
Supply Voltage	V_{IN}		3.0	---	5.5	V
VIN UVLO	V_{IN_UVLO}	VIN Rising	---	---	2.9	V
VIN UVLO Hysteresis	V_{IN_HYS}		---	0.2	---	V
Quiescent Current in Standby Mode	I_{IN}	EN=EN_TS=High, ON/OFF bit=”0”	---	1.5	---	mA
Quiescent Current in Shutdown Mode	I_{SD}	EN=EN_TS=Low, ON/OFF bit=”X”	---	---	1	μA
VL Output Voltage	V_{VL}		---	5	---	V
Thermal Shutdown Trip Point	T_{SD}		---	150	---	°C
Thermal Shutdown Hysteresis	T_{HYS}		---	20	---	°C
VP1(BOOST REGULATOR)						
Switch Frequency	F_{SW_VP1}	FREQ_VP1[2]=1	---	1000	---	KHz
Power Good Threshold		Fraction of nominal voltage	---	90	---	%
Soft-Start period	T_{SS_VP1}	SS[7:6]=”00”,SS_CTL[0]=”0”	---	6	---	ms
Switch ON Resistance	R_{ON_P}	$V_{GATE}=V_{P1-5V}$	---	200	---	mΩ
	R_{ON_N}	$V_{GATE}=V_L$	---	200	---	mΩ
Switch Current Limit	I_{LIMIT_VP1}	V_{IN}=3.6V	---	2.5	---	A
LX Leakage Current	I_{LXP1}	V_{LXP1}=6.3V	-5	---	+5	μA
VPOS1_IN Leakage Current	I_{VPOS1_IN}	V_{LXP1}=0V, V_{VPOS1_IN}=6.3V	-5	---	+5	μA
Fault Protection		Fraction of nominal voltage, Falling	---	85	---	%
		Fault Timer	---	16	---	ms
VPOS1(Positive LDO)						
Output Voltage Range	VPOS1	VPOS1[9:0] SET output voltage	2	---	12	V

Electrical Characteristics (Continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Soft-Start period	T_{SS_VPOS1}	SS[7:6]="00",SS_CTL[0]="0"	---	6	---	ms
Power Good Threshold		Fraction of nominal voltage	---	90	---	%
Output Accuracy		VPOS1[9:0]=6V, I_{Load}=20mA	-1	---	1	%
Dropout Voltage	$V_{DROPOUT}$	I_{LOAD}=200mA	---	300	---	mV
Load Regulation-DC	$V_{LOADREG}$	I_{LOAD}=10% to 90%	---	---	1	%
Load Current Range	I_{LOAD}	3.0V≦VIN<3.6V, for maximum output	---	---	150	mA
		VIN≧3.6V, for maximum output	---	---	200	mA
		VPOS1[9:0] SET<6V	---	100	---	mA
Output Current Limit	I_{LIMIT}		250	---	---	mA
Discharge Impedance to Ground	R_{DIS}		---	550	---	Ω
Fault Protection		Fraction of nominal voltage, Falling	---	85	---	%
		Fault Timer	---	16	---	ms
VP2(BOOST REGULATOR)						
Switch Frequency	F_{SW_VP2}	FREQ_VP2[2]=1	---	1000	---	KHz
Power Good Threshold		Fraction of nominal voltage	---	90	---	%
Soft-Start period	T_{SS_VP2}	SS[7:6]="00",SS_CTL[0]="0"	---	6	---	ms
Switch ON Resistance	R_{ON_N}	V_{GATE}=V_L	---	100	---	mΩ
Switch Current Limit	I_{LIMIT_VP2}	V_{IN}=3.6V	---	3	---	A
LX Leakage Current	I_{LXP2}	V_{LXP2}=12.35V	-5	---	+5	μA
VPOS1_IN Leakage Current	I_{VPOS2_IN}	V_{LXP2}=0V, V_{VPOS2_IN}=12.35V	-5	---	+5	μA
Fault Protection		Fraction of nominal voltage, Falling	---	85	---	%
		Fault Timer	---	16	---	ms
VPOS2(Positive LDO)						
Output Voltage Range	VPOS2	VPOS2[9:0] SET output voltage	5	---	20	V
Soft-Start period	T_{SS_VPOS2}	SS[7:6]="00",SS_CTL[0]="0"	---	6	---	ms
Power Good Threshold		Fraction of nominal voltage	---	90	---	%
Output Accuracy		VPOS2[9:0]=12V, I_{Load}=30mA	-1	---	1	%
Dropout Voltage	$V_{DROPOUT}$	I_{LOAD}=300mA	---	350	---	mV
Load Regulation-DC	$V_{LOADREG}$	I_{LOAD}=10% to 90%	---	---	1	%
Load Current Range	I_{LOAD}	3.0V≦VIN<3.6V,for maximum output	---	---	150	mA
		VIN≧3.6V,for maximum output	---	---	300	mA
Output Current Limit	I_{LIMIT}		350	---	---	mA
Discharge Impedance to Ground	R_{DIS}		---	550	---	Ω
Fault Protection		Fraction of nominal voltage, Falling	---	85	---	%
		Fault Timer	---	16	---	ms
VP3(BOOST REGULATOR)						
Switch Frequency	F_{SW_VP3}	FREQ_VP3[2]=0	---	500	---	KHz
Power Good Threshold		Fraction of nominal voltage	---	90	---	%
Soft-Start period	T_{SS_VP3}	SS[7:6]="00",SS_CTL[0]="0"	---	6	---	ms
Switch ON Resistance	R_{ON_N}	V_{GATE}=V_L	---	100	---	mΩ
Switch Current Limit	I_{LIMIT_VP3}	V_{IN}=3.6V	---	6	---	A
LX Leakage Current	I_{LXP3}	V_{LXP3}=24.4V	-10	---	+10	μA
VPOS3_IN Leakage Current	I_{VPOS3_IN}	V_{LXP3}=0V, V_{VPOS3_IN}=24.4V	-10	---	+10	μA
VP3 OFF delay time for PDD	T_{VN_EXT}	VN_EXT[1:0] SET delay time	0	---	0.5	s
Fault Protection		Fraction of nominal voltage, Falling	---	85	---	%
		Fault Timer	---	16	---	ms
VPOS3(Positive LDO)						
Output Voltage Range	VPOS3	VPOS3[9:0] SET output voltage	9	---	26	V
Soft-Start period	T_{SS_VPOS3}	SS[7:6]="00",SS_CTL[0]="0"	---	6	---	ms
Power Good Threshold		Fraction of nominal voltage	---	90	---	%
Output Accuracy		VPOS3[9:0]=24V, I_{Load}=30mA	-1	---	1	%
Dropout Voltage	$V_{DROPOUT}$	I_{LOAD}=400mA	---	400	---	mV

Electrical Characteristics (Continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Load Regulation-DC	$V_{LOADREG}$	I_{LOAD}=10% to 90%	---	---	1	%
Load Current Range	I_{LOAD}	3.0V≦VIN <3.6V, for maximum output	---	---	300	mA
		VIN≧3.6V,for maximum output	---	---	400	mA
		VIN≧3.6V,for +24V output*1	---	---	500	mA
Output Current Limit	I_{LIMIT}		550	---	---	mA
Discharge Impedance to Ground	R_{DIS}		---	800	---	Ω
Fault Protection		Fraction of nominal voltage, Falling	---	85	---	%
		Fault Timer	---	16	---	ms
VN1(INVERTING BUCK-BOOST REGULATOR)						
Switch Frequency	F_{SW_VN1}	FREQ_VN1[2]=1	---	1000	---	KHz
Power Good Threshold		Fraction of nominal voltage	---	90	---	%
Soft-Start period	T_{SS_VN1}	SS[7:6]="00",SS_CTL[0]="0"	---	6	---	ms
Switch ON Resistance	R_{ON_P}	V_{GATE}=0V	---	200	---	mΩ
	R_{ON_N}	V_{GATE}=V_{N1+5V}	---	200	---	mΩ
Switch Current Limit	I_{LIMIT_VN1}	V_{IN}=3.6V	---	1.8	---	A
LX Leakage Current	I_{LXN1}	V_{LXN1}=V_{VNEG1}=-6.3V	-5	---	+5	μA
Fault Protection		Fraction of nominal voltage, Falling	---	85	---	%
		Fault Timer	---	16	---	ms
VNEG1(Negative LDO)						
Output Voltage Range	VNEG1	VNEG1[9:0] SET output voltage	-12	---	-2	V
Soft-Start period	T_{SS_VNEG1}	SS[7:6]="00",SS_CTL[0]="0"	---	6	---	ms
Power Good Threshold		Fraction of nominal voltage	---	90	---	%
Output Accuracy		VNEG1[9:0]=-6V, I_{Load}=20mA	-1	---	1	%
Dropout Voltage	$V_{DROPOUT}$	I_{LOAD}=200mA	---	300	---	mV
Load Regulation-DC	$V_{LOADREG}$	I_{LOAD}=10% to 90%	---	---	1	%
Load Current Range	I_{LOAD}	3.0V≦VIN<3.6V, for maximum output	---	---	150	mA
		VIN≧3.6V, for maximum output	---	---	200	mA
Output Current Limit	I_{LIMIT}		250	---	---	mA
Discharge Impedance to Ground	R_{DIS}		---	550	---	Ω
Fault Protection		Fraction of nominal voltage, Falling	---	85	---	%
		Fault Timer	---	16	---	ms
VN2(INVERTING BUCK-BOOST REGULATOR)						
Switch Frequency	F_{SW_VN2}	FREQ_VN2[2]=1	---	1000	---	KHz
Power Good Threshold		Fraction of nominal voltage	---	90	---	%
Soft-Start period	T_{SS_VN2}	SS[7:6]="00",SS_CTL[0]="0"	---	6	---	ms
Switch ON Resistance	R_{ON_P}	V_{GATE}=0V	---	100	---	mΩ
Switch Current Limit	I_{LIMIT_VN2}	V_{IN}=3.6V	---	3	---	A
LX Leakage Current	I_{LXN2}	V_{LXN2}=V_{VNEG2}=-12.35V	-5	---	+5	μA
Fault Protection		Fraction of nominal voltage, Falling	---	85	---	%
		Fault Timer	---	16	---	ms
VNEG2(Negative LDO)						
Output Voltage Range	VNEG2	VNEG2[9:0] SET output voltage	-20	---	-5	V
Soft-Start period	T_{SS_VNEG2}	SS[7:6]="00",SS_CTL[0]="0"	---	6	---	ms
Power Good Threshold		Fraction of nominal voltage	---	90	---	%
Output Accuracy		VNEG2[9:0]=-12V, I_{Load}=30mA	-1	---	1	%
Dropout Voltage	$V_{DROPOUT}$	I_{LOAD}=300mA	---	350	---	mV
Load Regulation-DC	$V_{LOADREG}$	I_{LOAD}=10% to 90%	---	---	1	%
Load Current Range	I_{LOAD}	3.0V≦VIN<3.6V, for maximum output	---	---	150	mA
		VIN≧3.6V, for maximum output	---	---	300	mA
Output Current Limit	I_{LIMIT}		350	---	---	mA
Discharge Impedance to Ground	R_{DIS}		---	550	---	Ω

Electrical Characteristics (Continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Fault Protection		Fraction of nominal voltage, Falling	---	85	---	%
		Fault Timer	---	16	---	ms
VN3(INVERTING BUCK-BOOST REGULATOR)						
Switch Frequency	F_{SW_VN3}	FREQ_VN3[2]=0	---	500	---	KHz
Power Good Threshold		Fraction of nominal voltage	---	90	---	%
Soft-Start period	T_{SS_VN3}	SSN3[5:4]="00",SS_CTLN3[1]="0"	---	6	---	ms
Switch ON Resistance	R_{ON_P}	V_{GATE}=0V	---	100	---	mΩ
Switch Current Limit	I_{LIMIT_VN3}	V_{IN}=3.6V	---	7	---	A
LX Leakage Current	I_{LXN3}	V_{LXN3}=V_{VNEG3}=-24.4V	-10	---	+10	μA
VN3 OFF delay time for PDD	T_{VN_EXT}	VN_EXT[1:0] SET delay time	0	---	0.5	s
Fault Protection		Fraction of nominal voltage, Falling	---	85	---	%
		Fault Timer	---	16	---	ms
VNEG3(Negative LDO)						
Output Voltage Range	VNEG3	VNEG3[9:0] SET output voltage	-26	---	-9	V
Soft-Start period	T_{SS_VNEG3}	SSN3[5:4]="00",SS_CTLN3[1]="0"	---	6	---	ms
Power Good Threshold		Fraction of nominal voltage	---	90	---	%
Output Accuracy		VNEG3[9:0]=-24V, I_{Load}=30mA	-1	---	1	%
Dropout Voltage	$V_{DROPOUT}$	I_{LOAD}=400mA	---	400	---	mV
Load Regulation-DC	$V_{LOADREG}$	I_{LOAD}=10% to 90%	---	---	1	%
Load Current Range	I_{LOAD}	3.0V≦VIN <3.6V, for maximum output	---	---	300	mA
		VIN≧3.6V, for maximum output	---	---	400	mA
		VIN≧3.6V, for -24V output[*1]	---	---	500	mA
Output Current Limit	I_{LIMIT}		550	---	---	mA
Discharge Impedance to Ground	R_{DIS}		---	800	---	Ω
Fault Protection		Fraction of nominal voltage, Falling	---	85	---	%
		Fault Timer	---	16	---	ms
VPOS1/2/3 and VNEG1/2/3 Tracking(Only for VPOS/VNEG are of opposite sign but same magnitude)						
Difference between VPOS2/3 and VNEG2/3	V_{DIFF}	(VPOS2/3,VNEG2/3)=(+15V ,-15V), I_{LOAD}=±20mA, 0°C to 60°C, TRACK2/3="1"	-50	---	50	mV
Difference between VPOS1 and VNEG1	V_{DIFF}	(VPOS1,VNEG1)=(+6V ,-6V), I_{LOAD}=±20mA, 0°C to 60°C, TRACK1="1"	-50	---	50	mV
VGH(Positive Charge-Pump)						
Soft-Start period	T_{SS_VGH}	SS[7:6]="00",SS_CTL[0]="0"	---	6	---	ms
Power Good Threshold		Fraction of nominal voltage	---	95	---	%
Switching Frequency	F_{DRVP}		---	1000	---	KHz
Switch ON Resistance	R_{ON_UP}		---	1.5	3	Ω
	R_{ON_DOWN}		---	1.5	3	Ω
Output Voltage Range	VGH		10	---	40	V
VGH Accuracy	VGH_A	VGH[8:0]=35V, I_{Load}=10mA	-3	---	3	%
VGH_DIS Open-Drain Discharge Resistor	R_{DIS}		---	760	---	Ω
VPDD Output Range	V_{VPDD}	VPDD[7:3] SET output voltage	2	---	10	V
VPDD_LEN delay time	$T_{VPDD-LEN}$	VPDD_LEN[7:0] SET delay time	0	---	30	s
VDDH_EXT delay time	$T_{VDDH-EXT}$	VDDH_EXT[4:0] SET delay time	0	---	1	s
Load Current Range	I_{LOAD}		---	---	60	mA
Fault Protection		V_{FBP} Falling	---	85	---	%
		Fault Timer	---	16	---	ms
VGL(Negative Charge-Pump)						
Soft-Start period	T_{SS_VGH1}	SS[7:6]="00",SS_CTL[0]="0"	---	6	---	ms

Electrical Characteristics (Continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Power Good Threshold		Fraction of nominal voltage	---	95	---	%
Switching Frequency	F_{DRVN}		---	1000	---	KHz
Switch ON Resistance	R_{ON_UP}		---	1.5	3	Ω
	R_{ON_DOWN}		---	1.5	3	Ω
Output Voltage Range	VGL		-40	---	-15	V
VGL Accuracy	VGL_A	VGL[8:0]=-35V, I_{Load}=10mA	-3	---	3	%
Load Current Range	I_{LOAD}		---	---	60	mA
VEE_EXT delay time	$T_{VEE-EXT}$	VEE_EXT[7:1] SET delay time	0	---	6.3	s
Fault Protection		Falling	---	85	---	%
		Fault Timer	---	16	---	ms
VCOM						
VCOM Output Current		Souring	60	---	---	mA
		Sinking	60	---	---	mA
Operating Range-DC	VCOM	VCOM[7:0] SET output voltage	-5	---	+0	V
Accuracy		VCOM=-1V, VIN=3.0V to 5.5V, no load	-1.5	---	+1.5	%
Discharge Impedance to Ground	R_{DIS}		---	800	---	Ω
Thermistor Monitor(Use 10KΩ Murata NCP15XH103F03RC)						
Internal Pull Up Resistor	R_{NTC_UP}		---	9.53	---	KΩ
External Linearization Resistor	R_{Linear}		---	13.7	---	KΩ
ADC Resolution	ADC_{RES}	Not Tested in production, 1-bit	---	10	---	mV
ADC Conversion Time	ADC_{DEL}	Not Tested in production	---	300	---	µs
Accuracy	TMS_{ACC}	Not Tested in production, 1-bit	-1	---	1	LSB
Logic Levels and Timing Characteristics (SCL, SDA, PG, EN, VCOM_EN, Toggle_VCOM_CTL, PS,XON,RST)						
Output Low Threshold Level	V_{OL}	I_O=3mA, sink current (SDA,PG,XON, RST)	---	---	0.4	V
XON_DELAY delay time	T_{XON_DELAY}	XON_DELAY[7:1] SET delay time	0	---	0.5	s
XON_LEN delay time	T_{XON_LEN}	XON_LEN[7:0] SET delay time	0	---	25	s
Input Low Threshold Level	V_{IL}		---	---	0.6	V
Input High Threshold Level	V_{IH}		1.5	---	---	V
EN/EN_TS Pull-low Resistor	R_{EN/EN_TS}		---	1	---	MΩ
Deglitch Time, EN pin	$t_{Deglitch}$		---	100	---	µs
Deglitch Time, RST pin	$t_{Deglitch}$		---	1	---	ms
SCL Clock Frequency	F_{SCL}		---	---	400	KHz
I^2C Slave Address		7-bit slave address,A0=0	---	0x48h	---	
		7-bit slave address,A0=1	---	0x49h	---	

Data Transmission Timing

(VIN= 3.6V±5%, T_A=25°C, CL=100pF, unless otherwise specified**)**

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
I²C TIMING CHARCTERISTICS						
Serial-Clock Frequency	f_{SCL}		---	---	400	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}	F_{SCL}=100KHz	4.7	---	---	µs
		F_{SCL}=400KHz	1.3	---	---	
Hold Time (Repeated) START Condition	$t_{HD,STA}$	F_{SCL}=100KHz	4.0	---	---	µs
		F_{SCL}=400KHz	0.6	---	---	
SCL Pulse-Width Low	t_{LOW}	F_{SCL}=100KHz	4.7	---	---	µs
		F_{SCL}=400KHz	1.3	---	---	
SCL Pulse-Width High	t_{HIGH}	F_{SCL}=100KHz	4.0	---	---	µs
		F_{SCL}=400KHz	0.6	---	---	
Setup Time for a Repeated START Condition	$t_{SU,STA}$	F_{SCL}=100KHz	4.7	---	---	µs
		F_{SCL}=400KHz	0.6	---	---	
Data Hold Time	$t_{HD,DAT}$	F_{SCL}=100KHz	0	---	3.45	µs
		F_{SCL}=400KHz	0	---	0.9	
Data Setup Time	$t_{SU,DAT}$	F_{SCL}=100KHz	250	---	---	ns
		F_{SCL}=400KHz	100	---	---	
SDA and SCL Receiving Rise Time	t_R	F_{SCL}=100KHz	---	---	1000	ns
		F_{SCL}=400KHz	---	---	300	
SDA and SCL Receiving Fall Time	t_F	F_{SCL}=100KHz	---	---	300	ns
		F_{SCL}=400KHz	---	---	300	
Setup Time for STOP Condition	$t_{SU,STO}$	F_{SCL}=100KHz	4	---	---	µs
		F_{SCL}=400KHz	0.6	---	---	
Bus Capacitance	C_B		---	---	400	pF
Pulse Width of Suppressed Spike	t_{SP}		0	---	50	ns

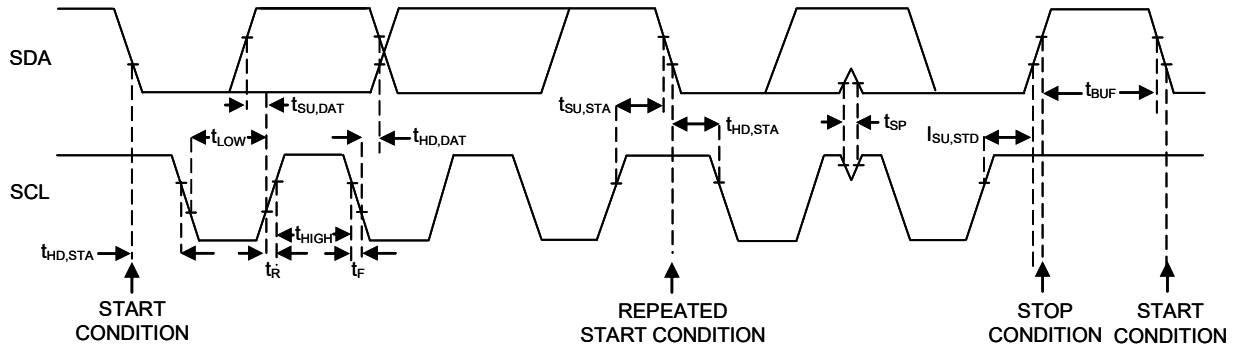
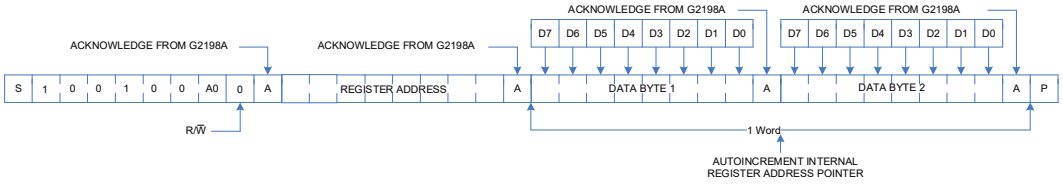


Figure 1. IC Serial-Interface Timing Diagram

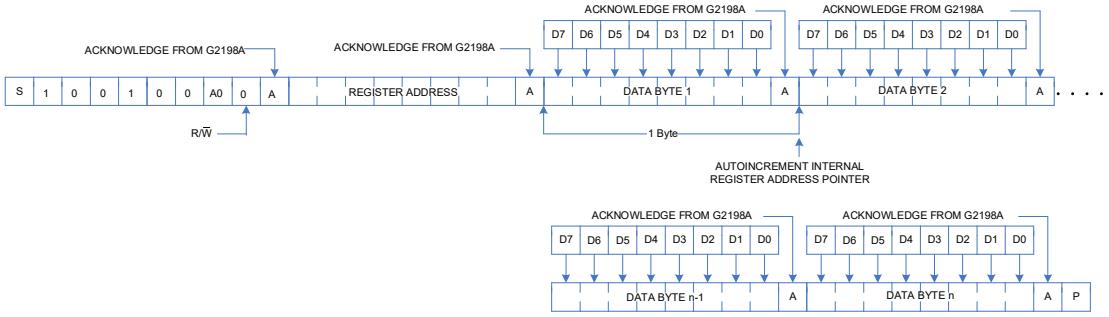
I²C Protocol

Write a Byte of Data to the G2198A

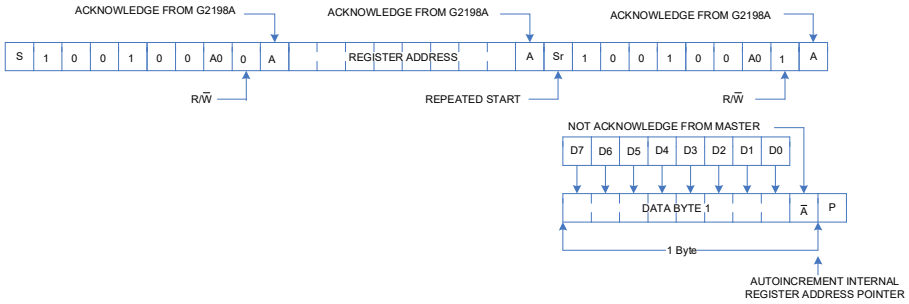
Write a Word of Data to the G2198A



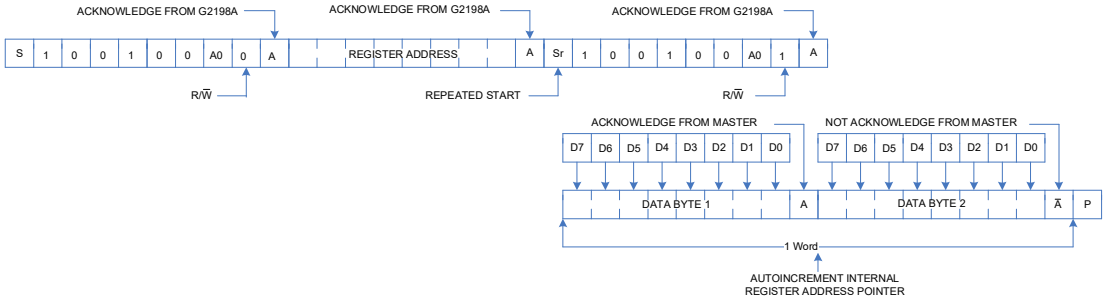
Write n Bytes of Data to the G2198A



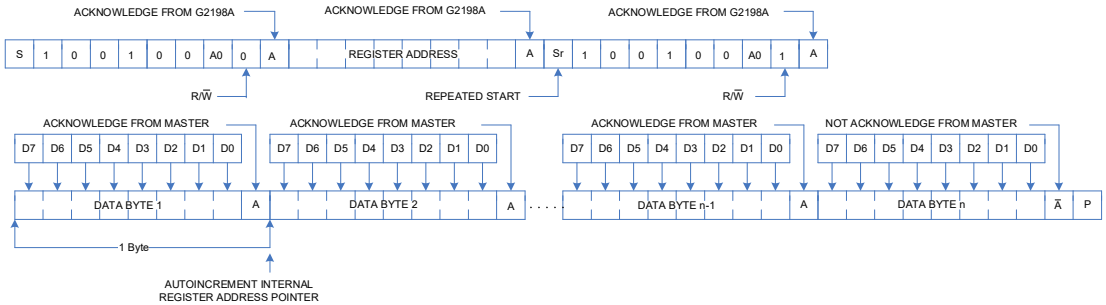
Read a Byte of Data to the G2198A



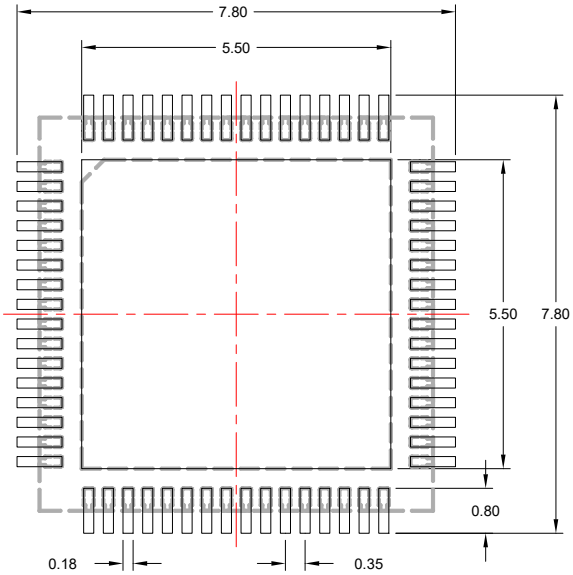
Read a Word of Data to the G2198A



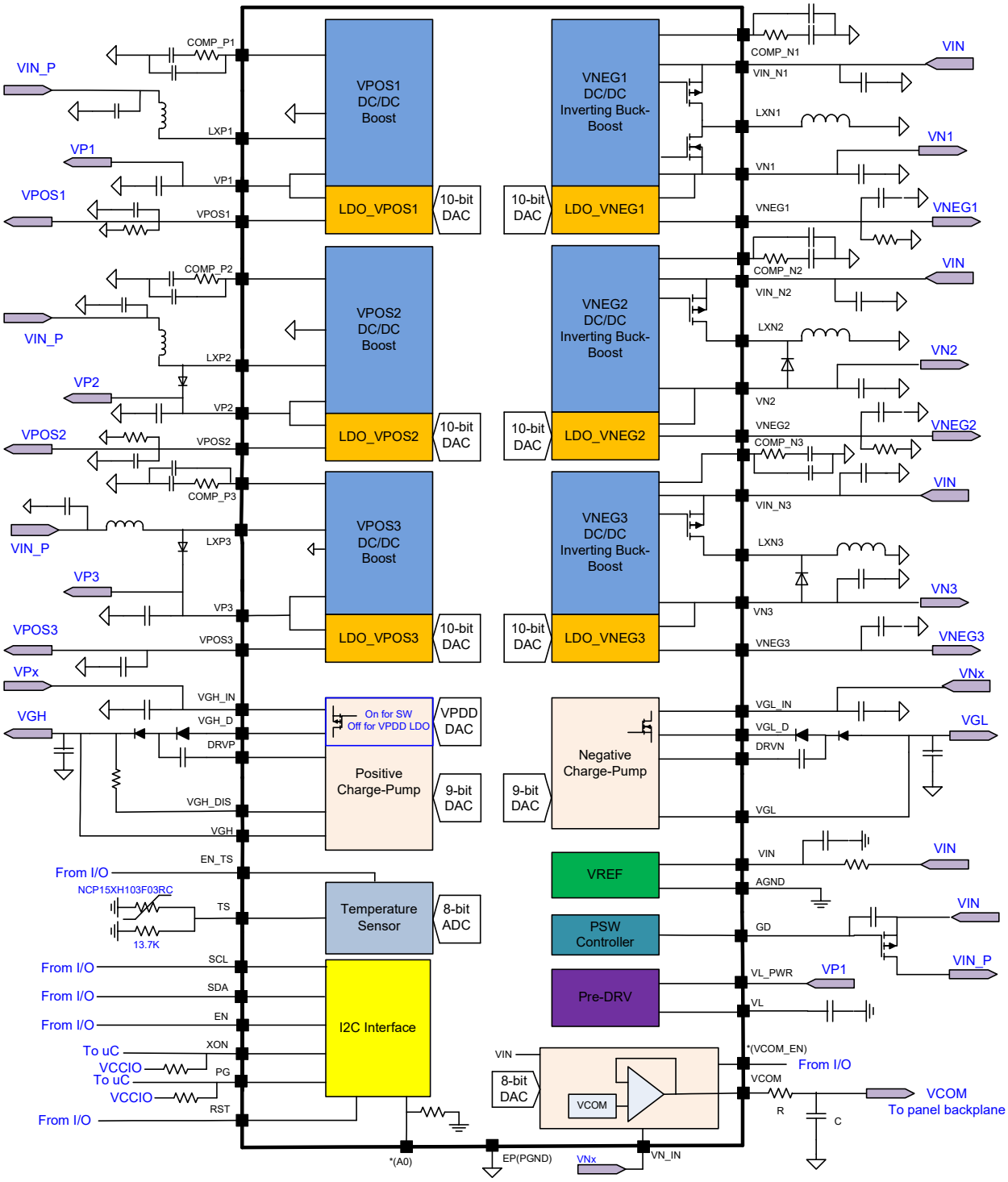
Read n Bytes of Data to the G2198A



Minimum Footprint PCB Layout Section



Typical Applications



Pin Description

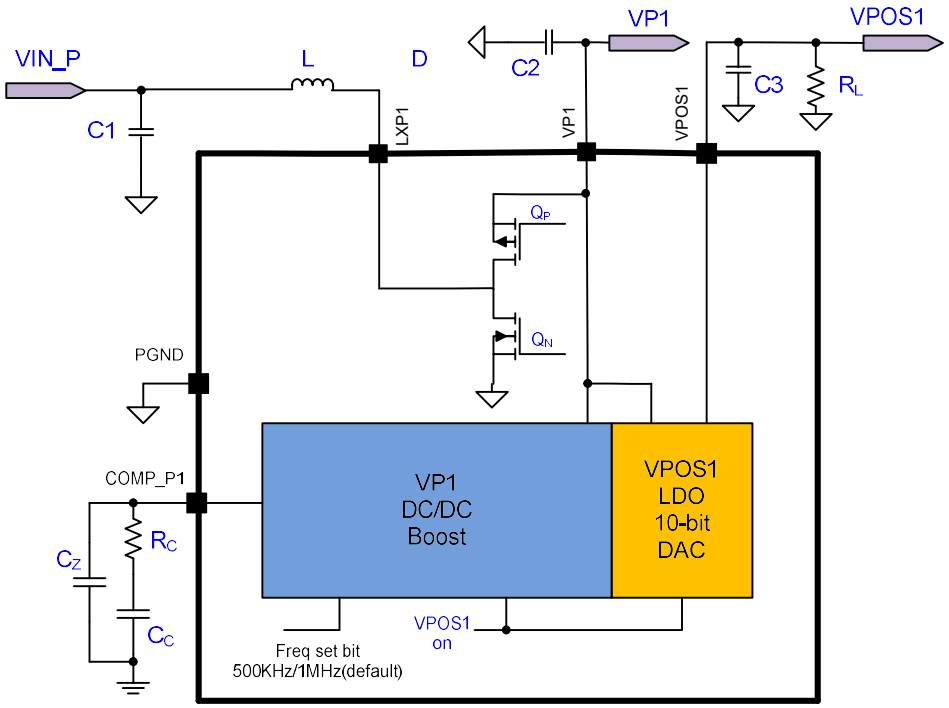
Pin No.	NAME	DESCRIPTION
1	VNEG2	Negative supply output pin for panel source drivers. Discharge VNEG2 to Ground whenever the rail is disable.
2	VN2	Feedback pin for VN2 and supply for VNEG2 rail
3	LXN2	VN2 Inductor Switch Node
4	LXN2	VN2 Inductor Switch Node
5	VIN_N2	Input Power Supply to VN2 rail
6	VIN_N2	Input Power Supply to VN2 rail
7	VIN_N1	Input Power Supply to VN1 rail
8	LXN1	VN1 Inductor Switch Node
9	VN1	Feedback pin for VN1 and supply for VNEG1 rail
10	VNEG1	Negative supply output pin for panel source drivers. Discharge VNEG1 to Ground whenever the rail is disable.
11	AGND	Analog ground for general analog circuitry
12	COMP_N1	VN1 Compensation pin
13	COMP_N3	VN3 Compensation pin
14	PG	Open-drain power good output pin. Pin is pulled low when one or more rails are not in regulation.
15	SDA	Serial interface(I^2C) data input/output
16	SCL	Serial interface(I^2C) clock input
17	XON	XON signal for post drive mode power off sequence
18	RST	Reset input for clear all registers to default(active High)
19	VIN_N3	Input Power Supply to VN3 rail
20	VIN_N3	Input Power Supply to VN3 rail
21	LXN3	VN3 Inductor Switch Node
22	LXN3	VN3 Inductor Switch Node
23	VN3	Feedback pin for VN3 and supply for VNEG3 rail
24	VNEG3	Negative supply output pin for panel source drivers. Discharge VNEG3 to Ground whenever the rail is disable.
25	VN_IN	VCOM OPA negative supply input
26	VCOM	Power for panel common-voltage driver. Discharge VCOM to ground whenever the rail is disable.
27,46,58,62	NC	No Connection
28	*(VCOM_EN)	VCOM enable pin when VCOMCTL[7]=1 & VCOM_EXT_CTL[4]=0 Pull this pin high to enable the VCOM
29	VPOS3	Positive supply output pin for panel source drivers. Discharge VPOS3 to Ground whenever the rail is disable.
30	VP3	Feedback pin for VP3 and supply for VPOS3 rail
31	LXP3	VP3 Inductor Switch Node
32	LXP3	VP3 Inductor Switch Node
33	COMP_P3	VP3 Compensation pin
34	TS	Thermistor input pin.
35	EN	Pull this pin high to power up all output rails.

Pin Description (Continued)

Pin No.	NAME	DESCRIPTION
36	EN_TS	Temperature ADC enable/disable control
37	VIN	Power supply input for PMIC control logic
38	VL	Internal 5V LDO output
39	*(A0)	I^2C Slave Address select pin (0x48H or 0x49H)
40	VL_PWR	Internal 5V LDO input
41	COMP_P1	VP1 Compensation pin
42	AGND	Analog ground for general analog circuitry
43	VPOS1	Positive supply output pin for panel source drivers. Discharge VPOS1 to Ground whenever the rail is disable.
44	VP1	Feedback pin for VP1 and supply for VPOS1 rail
45	LXP1	VP1 Inductor Switch Node
47	LXP2	VP2 Inductor Switch Node
48	LXP2	VP2 Inductor Switch Node
49	VP2	Feedback pin for VP2 and supply for VPOS2 rail
50	VPOS2	Positive supply output pin for panel source drivers. Discharge VPOS2 to Ground whenever the rail is disable.
51	COMP_P2	VP2 Compensation pin
52	VGH	VGH Feedback pin
53	VGH_DIS	VGH discharge control pin
54	DRVP	Driver output pin for positive charge pump VGH
55	VGH_D	Base voltage output pin for positive charge-pump VGH
56	VGH_IN	Input Supply pin for positive charge-pump VGH
57	DRVN	Driver output pin for negative charge pump VGL
59	VGL_IN	Input Supply pin for negative charge-pump VGL
60	VGL_D	Base voltage output pin for negative charge-pump VGL
61	VGL	VGL Feedback pin
63	GD	Gate Driver for true shutdown function
64	COMP_N2	VN2 Compensation pin
	EP(PGND)	Exposed Pad. Connect exposed pad to PGND(Power Ground of DC/DC Converter)

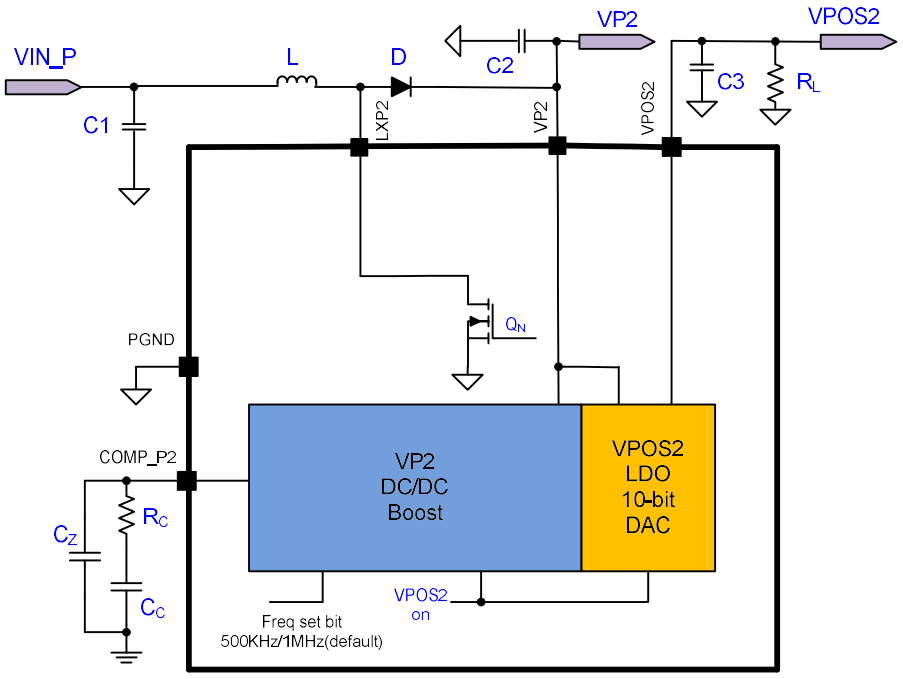
Power Rails Topology

(1) VP1 & VPOS1



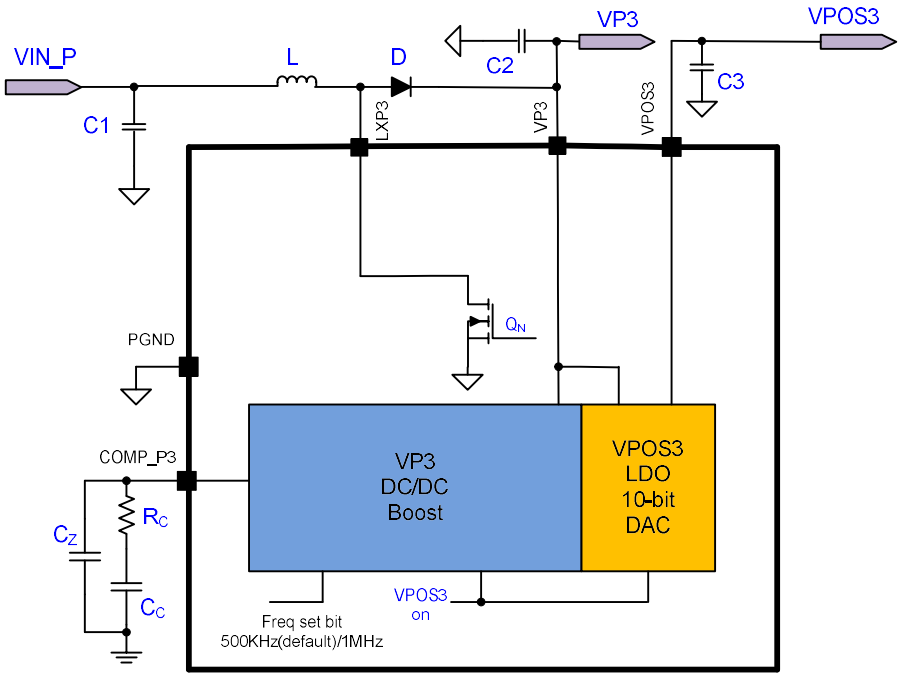
Design Parameter	VPOS1=6V/100mA, VIN=3.6V
C1	muRata, GRM21BR61A106K(10μF/10V/X5R, 0805)*2
C2	muRata, GRM21BR61C106K(10μF/16V/X5R, 0805)*1
C3	muRata, GRM21BR61C475K(4.7μF/16V/X5R, 0805)*1
L	Yuden, NRS5030T 100MMGJ(10μH/1.7A/70mΩ,5.0x5.0x3.0mm)
R_L	NC
R_C	47KΩ
C_C	470pF
C_Z	NC

(2) VP2 & VPOS2



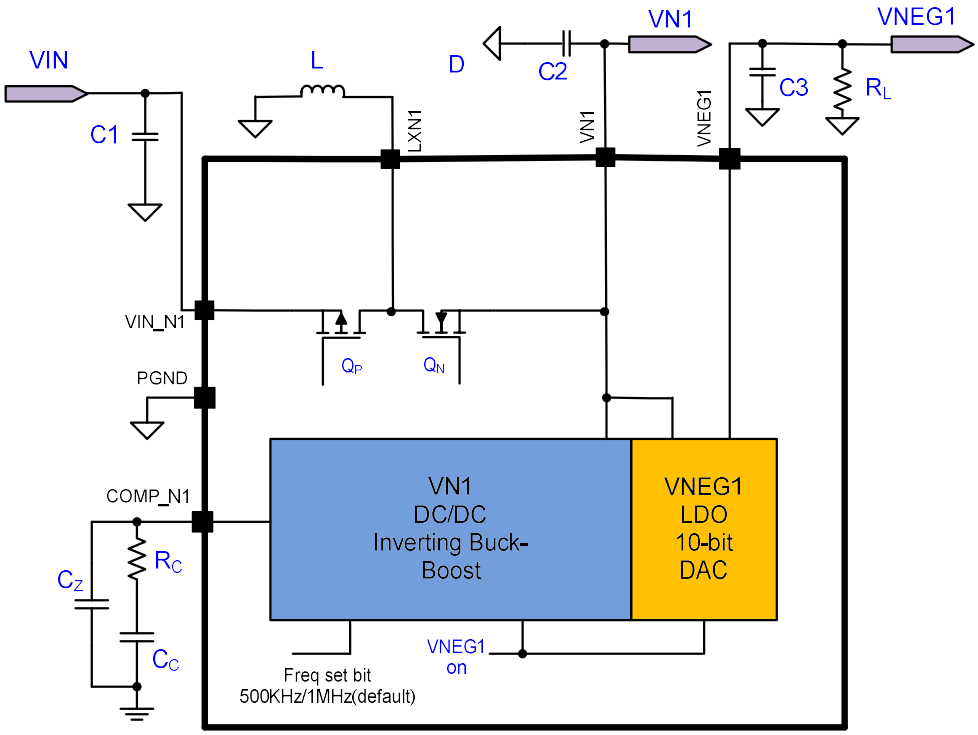
Design Parameter	VPOS2=12V/150mA, VIN=3.6V
C1	muRata, GRM21BR61A106K (10μF/10V/X5R, 0805)*2
C2	muRata, GRM31CR61E106K(10μF/25V/X5R, 1206)*1
C3	muRata, GRM31CR61E475K(4.7μF/25V/X5R, 1206)*1
L	Yuden, NRS5030T 4R7MMGJ(4.7μH/2.6A/35mΩ, 5.0x5.0x3.0mm)
D	CHENMKO, SMD26LGGP , 60V/2A SOD-123G
R_L	NC
R_C	51KΩ
C_C	330pF
C_Z	NC

(3) VP3 & VPOS3



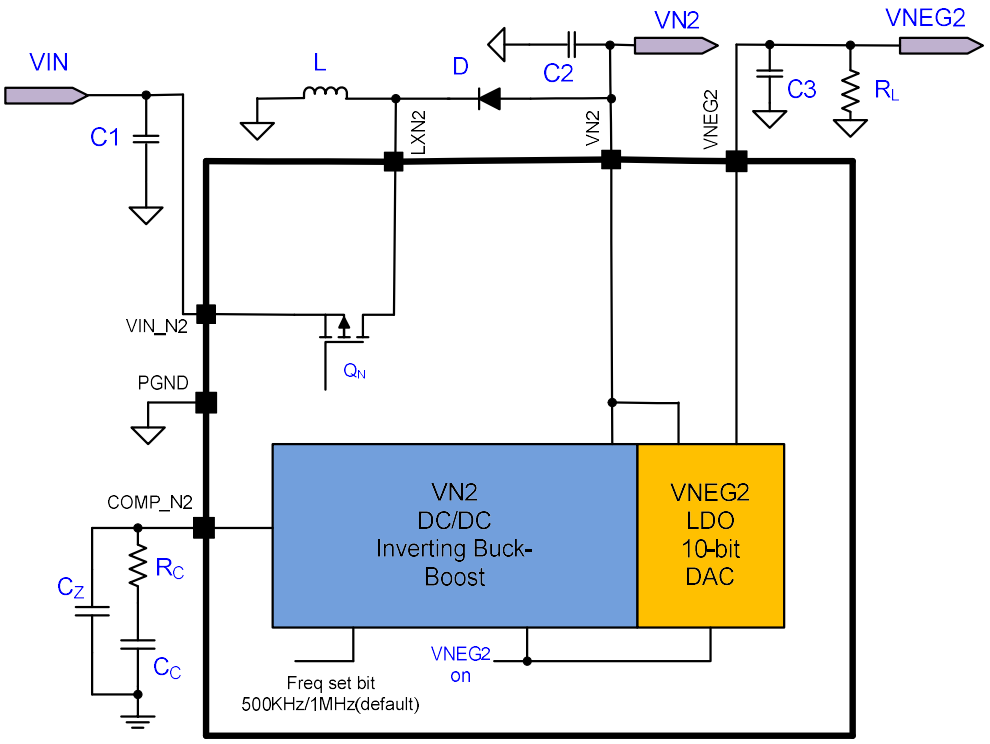
Design Parameter	VPOS3=24V/500mA, VIN=3.6V
C1	muRata, GRM21BR61A106K (10μF/10V/X5R, 0805)*2
C2	muRata, GRM319R6YA106MA12(10μF/35V/X5R, 1206)*2
C3	muRata, GRM319R6YA106MA12(10μF/35V/X5R, 1206)*2
L	ARLITECH, AMPI0624ED3R3MT (3.3μH/8A/39mΩ, 6.6x7.1x2.4mm)
D	CHENMKO, SMD26LGGP , 60V/2A SOD-123G
R_C	100KΩ
C_C	330pF
C_Z	NC

(4) VN1 & VNEG1



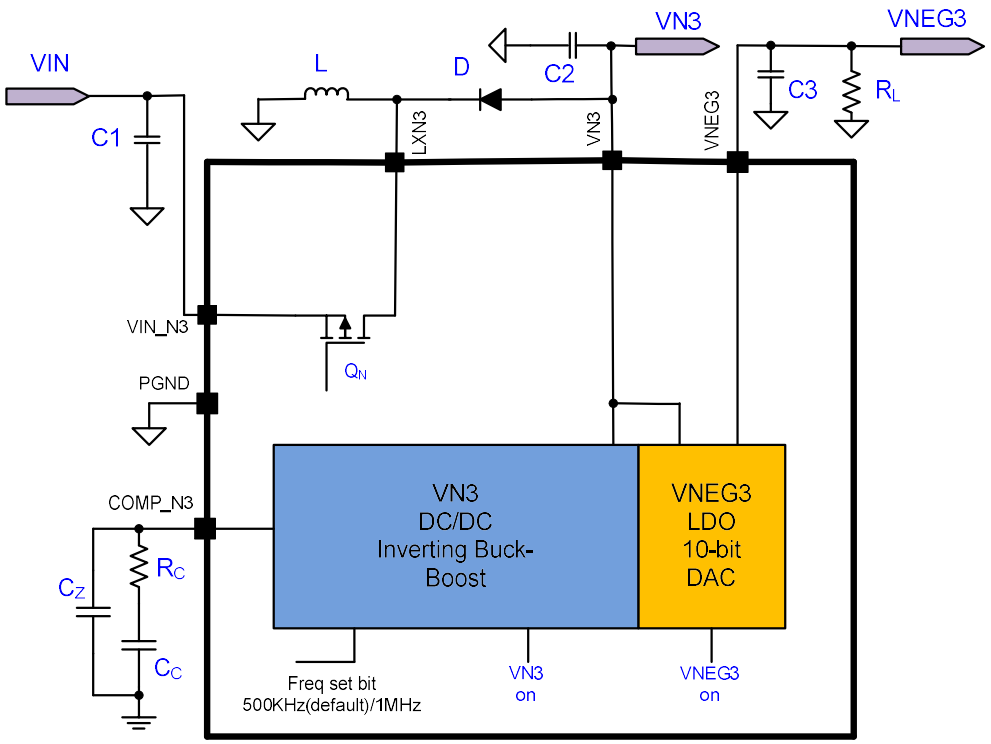
Design Parameter	VNEG1=-6V/100mA, VIN=3.6V
C1	muRata, GRM21BR61A106K (10μF/10V/X5R, 0805)*2
C2	muRata, GRM21BR61C106K(10μF/16V/X5R, 0805)*1
C3	muRata, GRM21BR61C475K(4.7μF/16V/X5R, 0805)*1
L	Yuden, NRS5030T 100MMGJ(10μH/1.7A/70mΩ,5.0x5.0x3.0mm)
R_L	NC
R_C	75KΩ
C_C	120pF
C_Z	NC

(5) VN2 & VNEG2



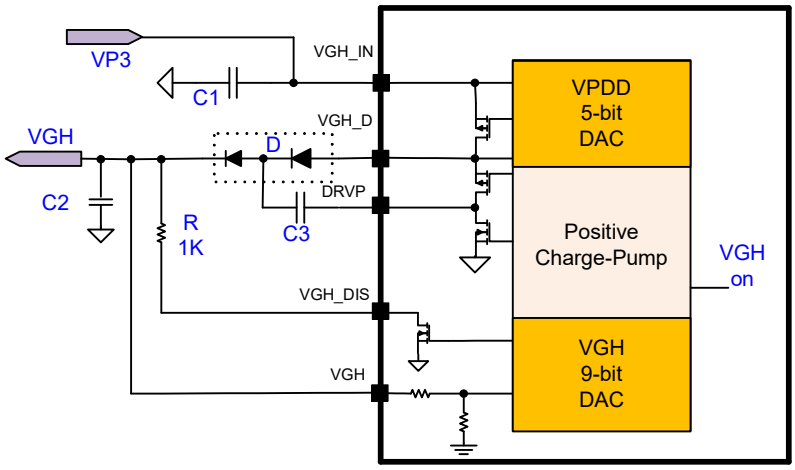
Design Parameter	VNEG2=-12V/150mA, VIN=3.6V
C1	muRata, GRM21BR61A106K (10μF/10V/X5R, 0805)*2
C2	muRata, GRM31CR61E106K(10μF/25V/X5R, 1206)*1
C3	muRata, GRM31CR61E475K(4.7μF/25V/X5R, 1206)*1
L	Yuden, NRS5030T 4R7MMGJ(4.7μH/2.6A/35mΩ, 5.0x5.0x3.0mm)
D	CHENMKO, SMD26LGGP , 60V/2A SOD-123G
R_L	NC
R_C	68KΩ
C_C	220pF
C_Z	NC

(6) VN3 & VNEG3



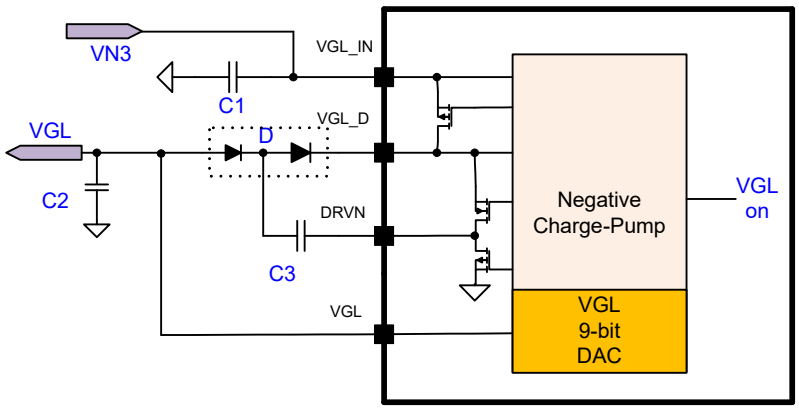
Design Parameter	VNEG3=-24V/500mA, VIN=3.6V
C1	muRata, GRM21BR61A106K (10μF/10V/X5R, 0805)*2
C2	muRata, GRM319R6YA106MA12(10μF/35V/X5R, 1206)*3
C3	muRata, GRM319R61H475MA12(4.7μF/50V/X5R, 1206)*2
L1	ARLITECH, AMPI0624ED3R3MT (3.3μH/8A/39mΩ, 6.6x7.1x2.4mm)
D	CHENMKO, SMD26LGGP , 60V/2A SOD-123G
R_C	68KΩ
C_C	330pF
C_Z	NC

(7) VGH



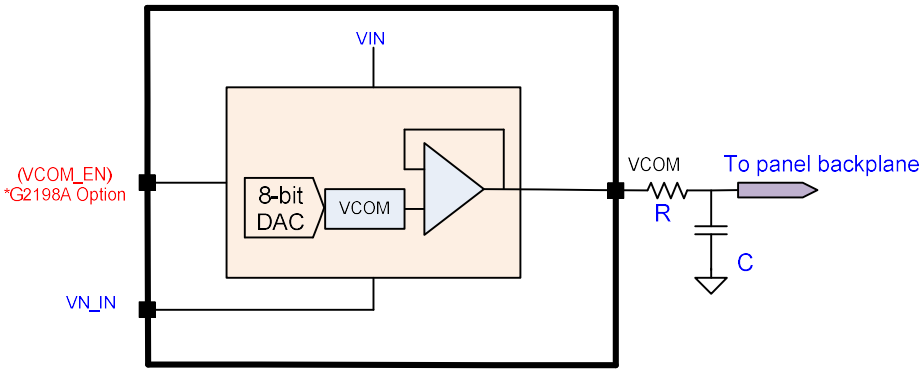
Design Parame-ter	VGHx=35V/20mA, VP3=24V
C1	muRata, GRM21BR61H225KA73(2.2μF/50V/X5R, 0805)*1
C2	muRata, GRM21BR61H225KA73(2.2μF/50V/X5R, 0805)*1
C3	muRata, GRM155R61H104KE19(0.1μF/50v/X5R,0402)*1
D	Dual small-signal diodes (SOT23),Fairchild MMBD4148SE/ BAV99
R	1KΩ

(8) VGL



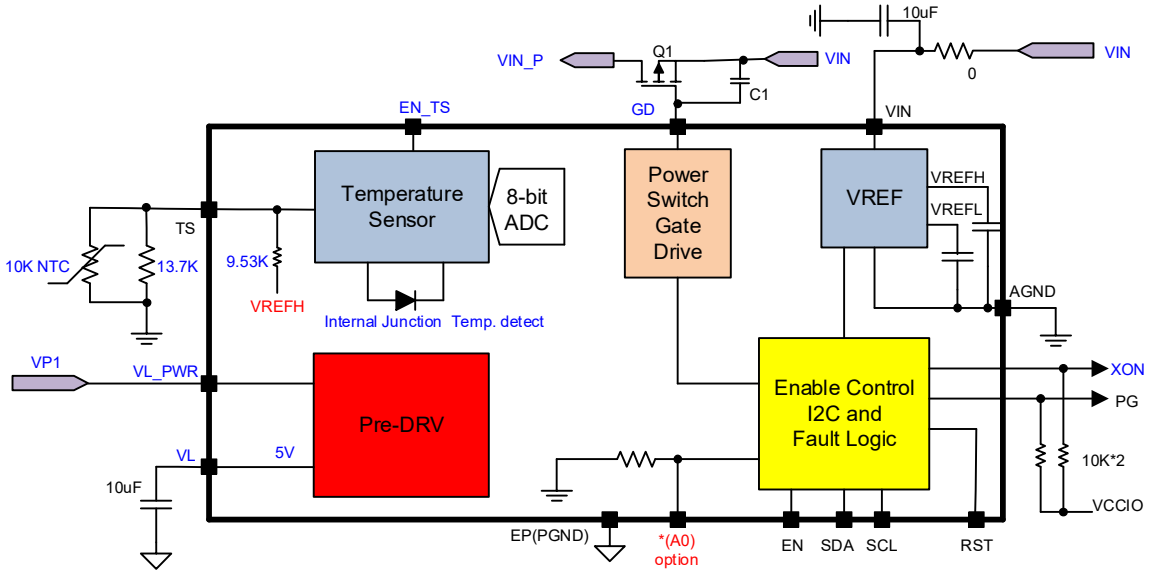
Design Parameter	VGH=-35V/20mA, VN3=-24V
C1	muRata, GRM21BR61H225KA73(2.2μF/50V/X5R, 0805)*1
C2	muRata, GRM319R61H475MA12(4.7μF/50V/X5R, 1206)*1
C3	muRata, GRM155R61H104KE19(0.1μF/50v/X5R,0402)*1
D	Dual small-signal diodes (SOT23),Fairchild MMBD4148SE/ BAV99

(9) VCOM



Design Parameter	DCVCOM=-1V/40mA, (0x16H, 3/7 LEVEL[4]=”0”)
C	muRata, ME05GRM155R61H105ME05 (1uF/50v/X5R,0402)*1
R	0Ω

(10) Control



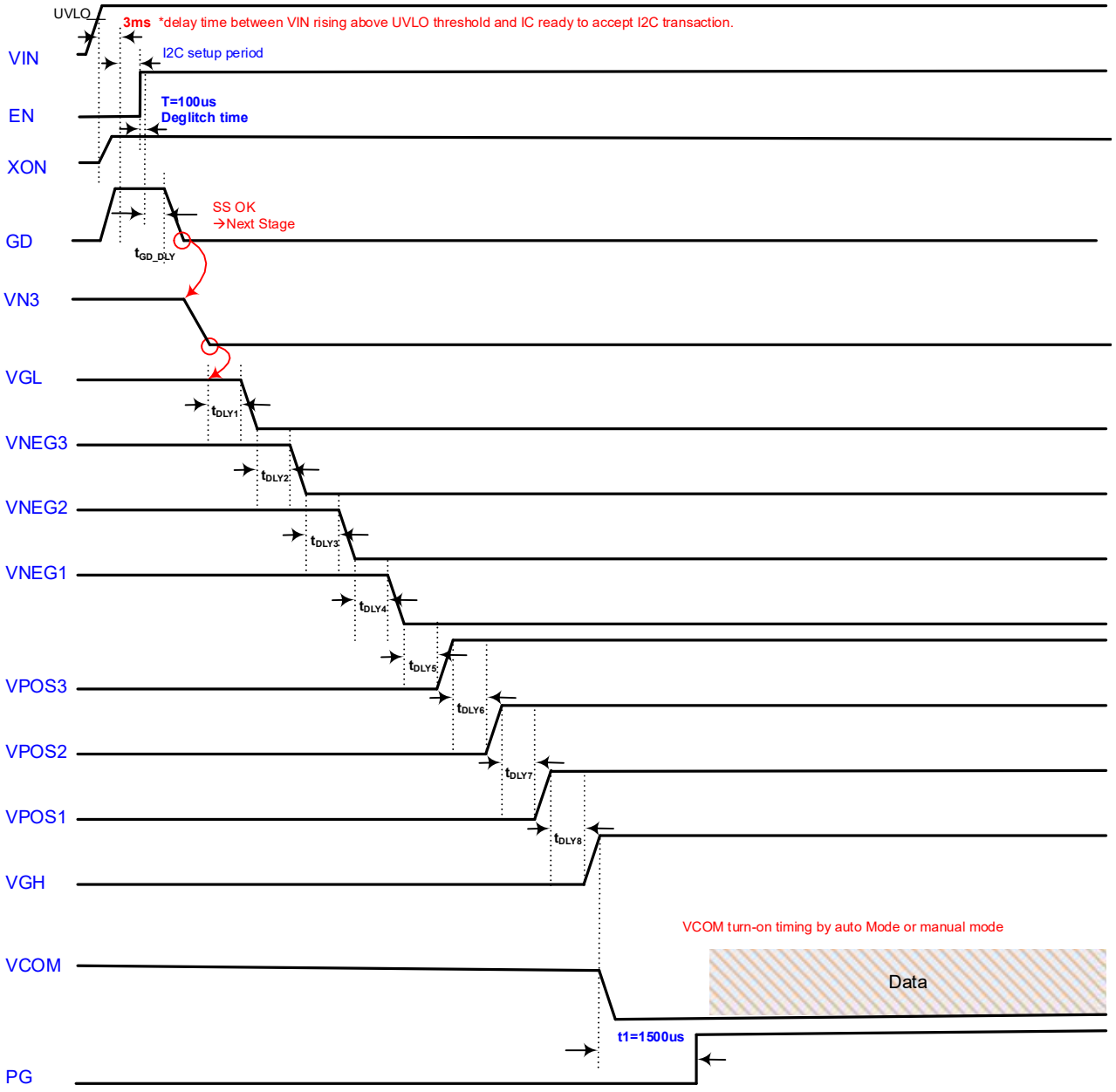
Design Parameter	
C1	47nF
Q1	FETek FKBB4115(40V/Ron=20mΩ@VGS=4.5V,P-MOS)

EN pin and 0x16h ON_OFF[4]

Hardware pin	ON_OFF[4]	Status
EN		
0	x	Sleep Mode
1	1	Normal Operation
1	0	Power Rails OFF (VPx,VNx,VPOSx,VNEGx,VGH, VGL,VCOM);

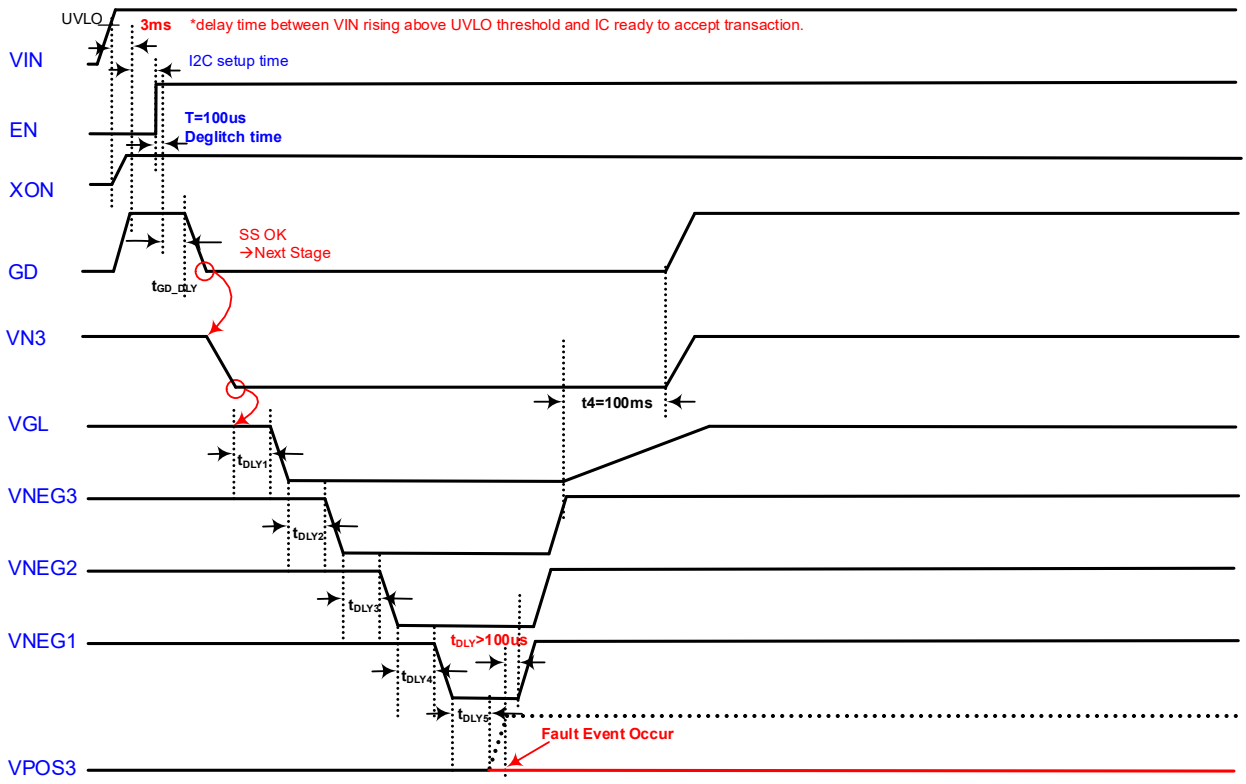
Power-up and Power-down Sequence

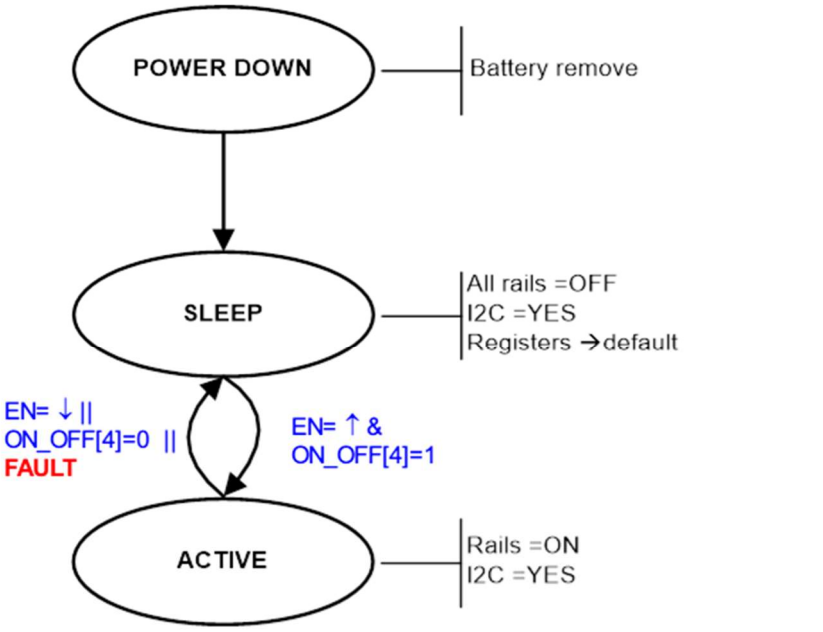
(A) Power-ON Sequence(7-Level Output)



1. Soft-start time(VPOSx/VNEGx) is setting by register 0x16 and 0x18 (**6ms**,8ms,10ms,12ms) or (**3ms**,4ms,5ms,6ms).
2. Discharge function only for VNEG3/2/1, VPOS3/2/1, VGH & VCOM. VGL are no discharge function.
3. 3-Level or 7-Level output mode is setting by register 0x16 bit5 (3/7 LEVEL[5]).
4. For manual mode, after the last rail power-on(VGH), VCOM starts ramping as EN_VCOM pull high. As EN_VCOM pull-low & VPx/VNx power ready, VCOM is shutdown.
5. t_{DLY1}~t_{DLY8} is programmable by register 0x13,0x14 (2-bit 0ms,1ms,**2ms**,4ms) and 0x16(soft-start time SS[7:6]).

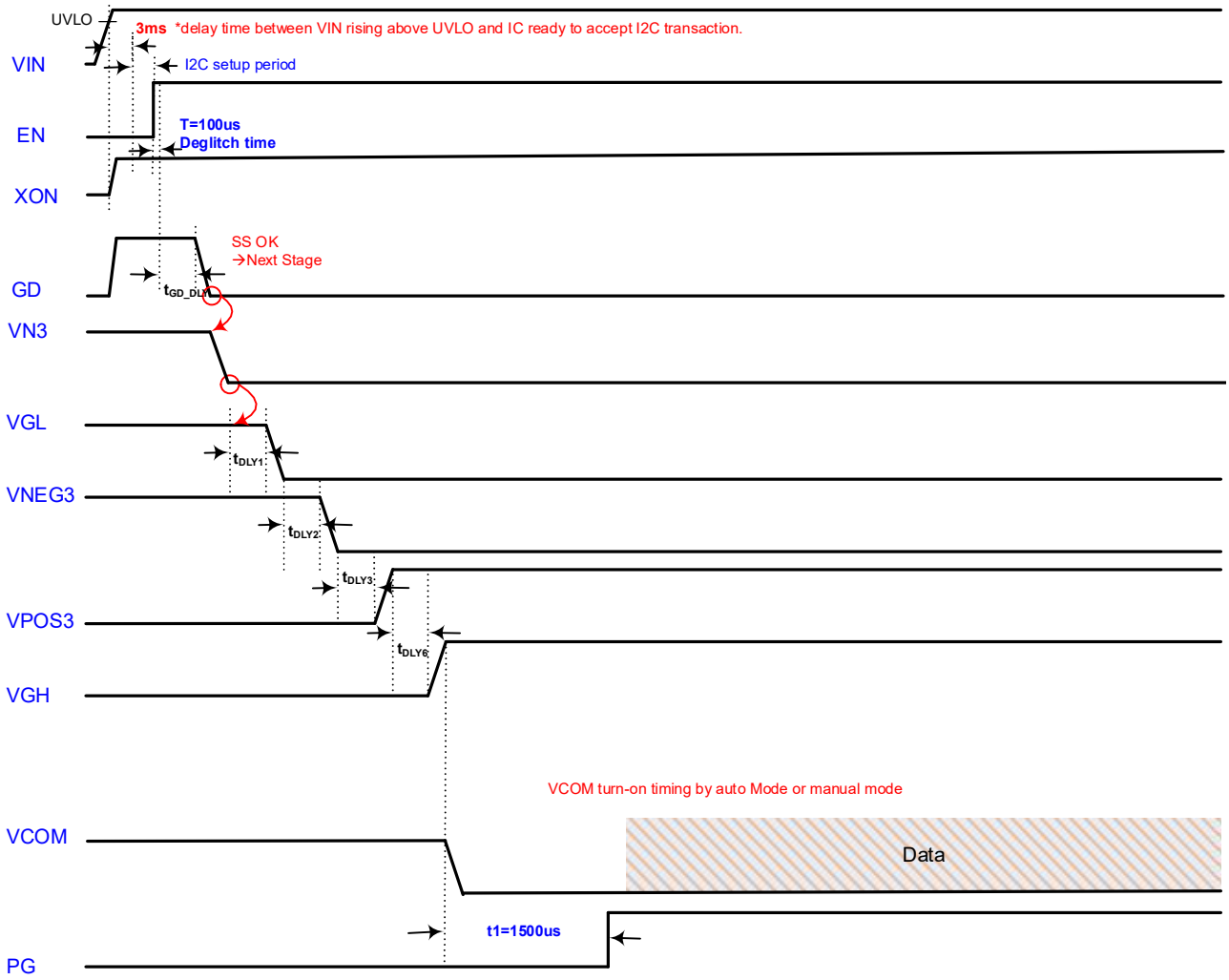
(B) Power-ON Sequence with Fault Event(7-Level Output, FLT_VPOS3[5]=1)





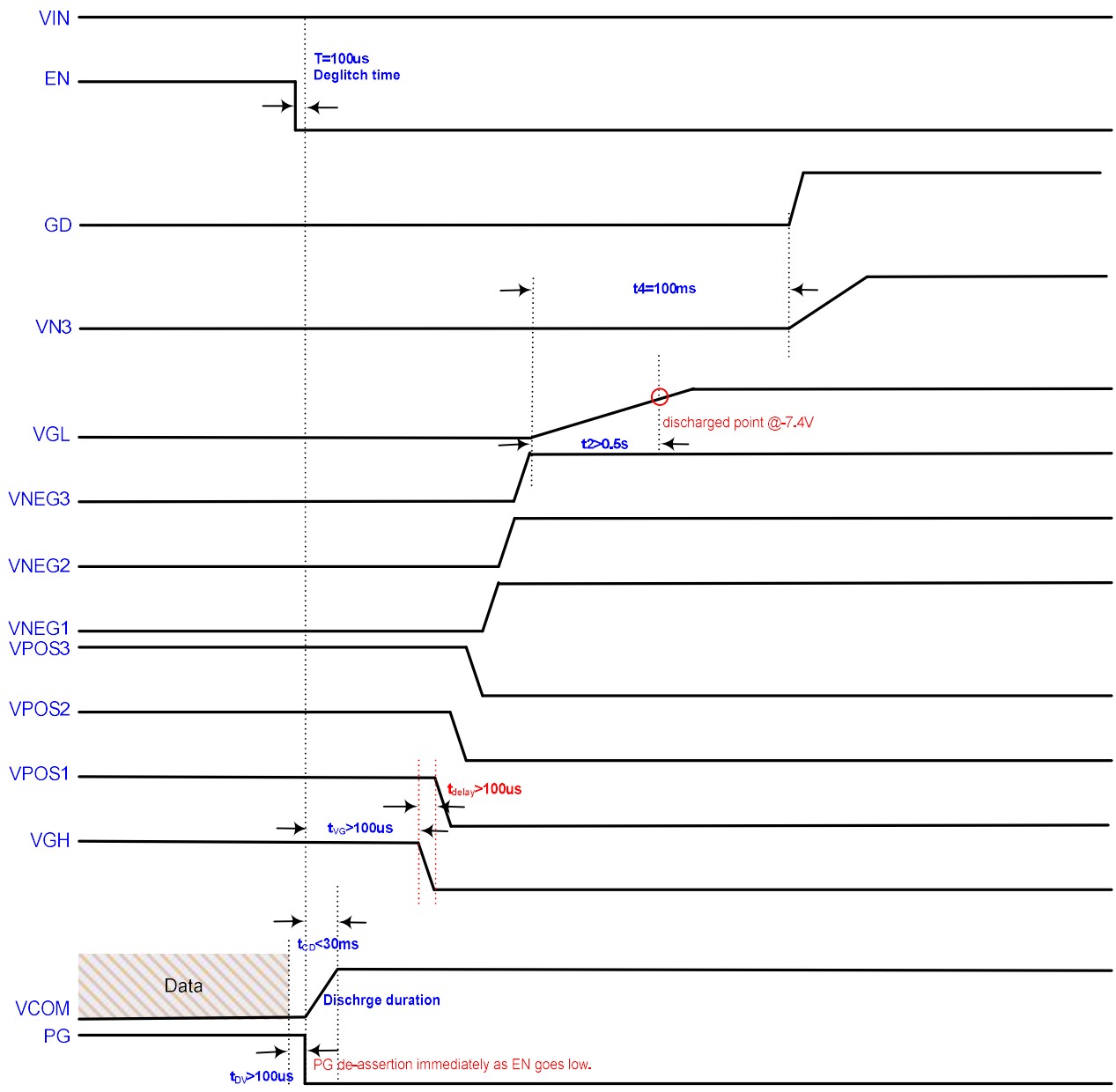
*G2198 if no PG (any Fault)→turn OFF all rails.

(C) Power-ON Sequence(3-Level Output)



0x16H	0x0DH	Function	Power Rail active	
3/7 LEVEL[5]	VCOM_3L_MODE[3]		DC/DC	Source Power
0	x	7_LEVEL DCVCOM	VP1/VN1 VP2/VN2 VP3/VN3	VPOS1/VNEG1 VPOS2/VNEG2 VPOS3/VNEG3
1	**0**	**3_LEVEL DCVCOM**	**VP3/VN3**	**VPOS3/VNEG3**

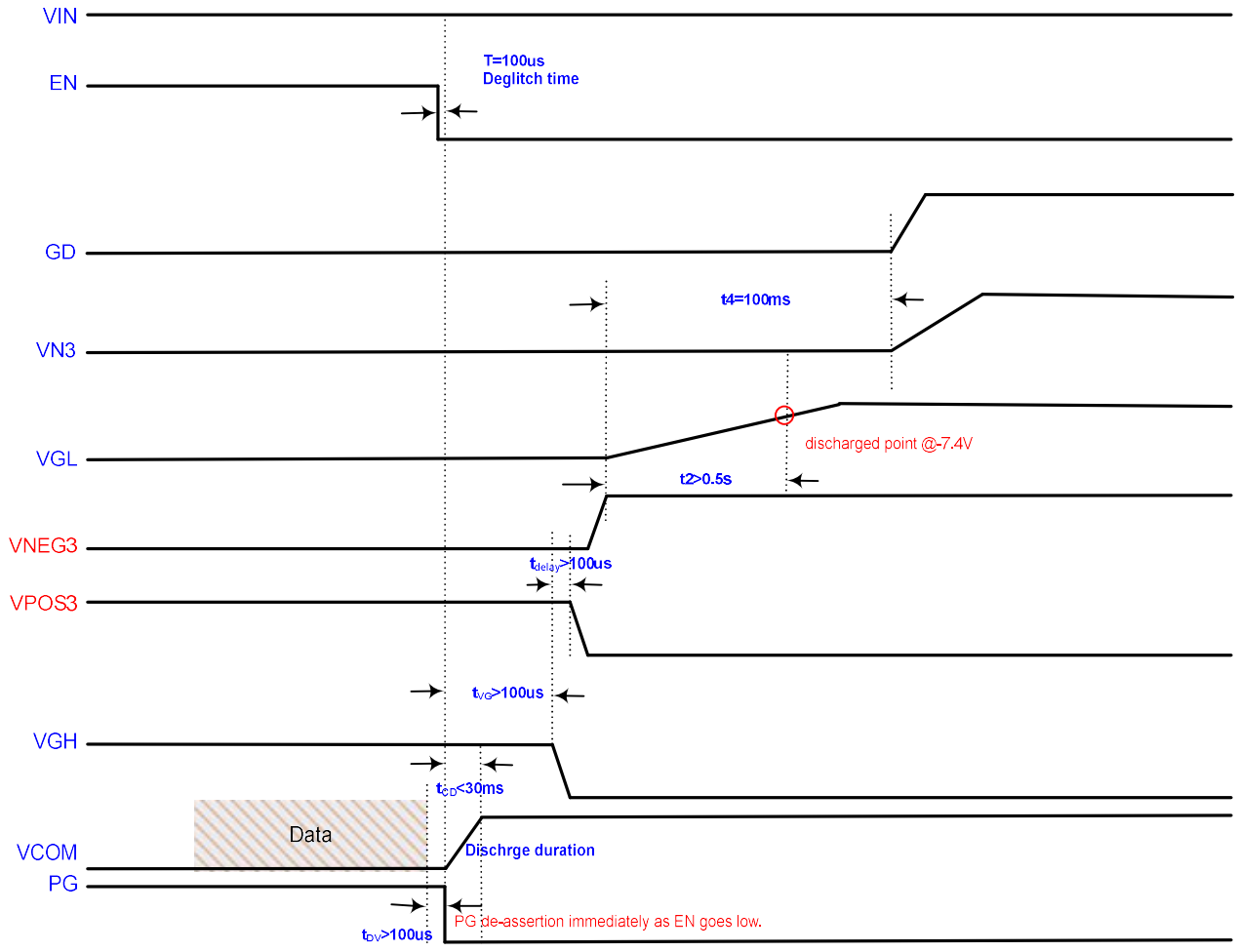
(D) Power-OFF Sequence (7-Level Output)



Normal Mode:

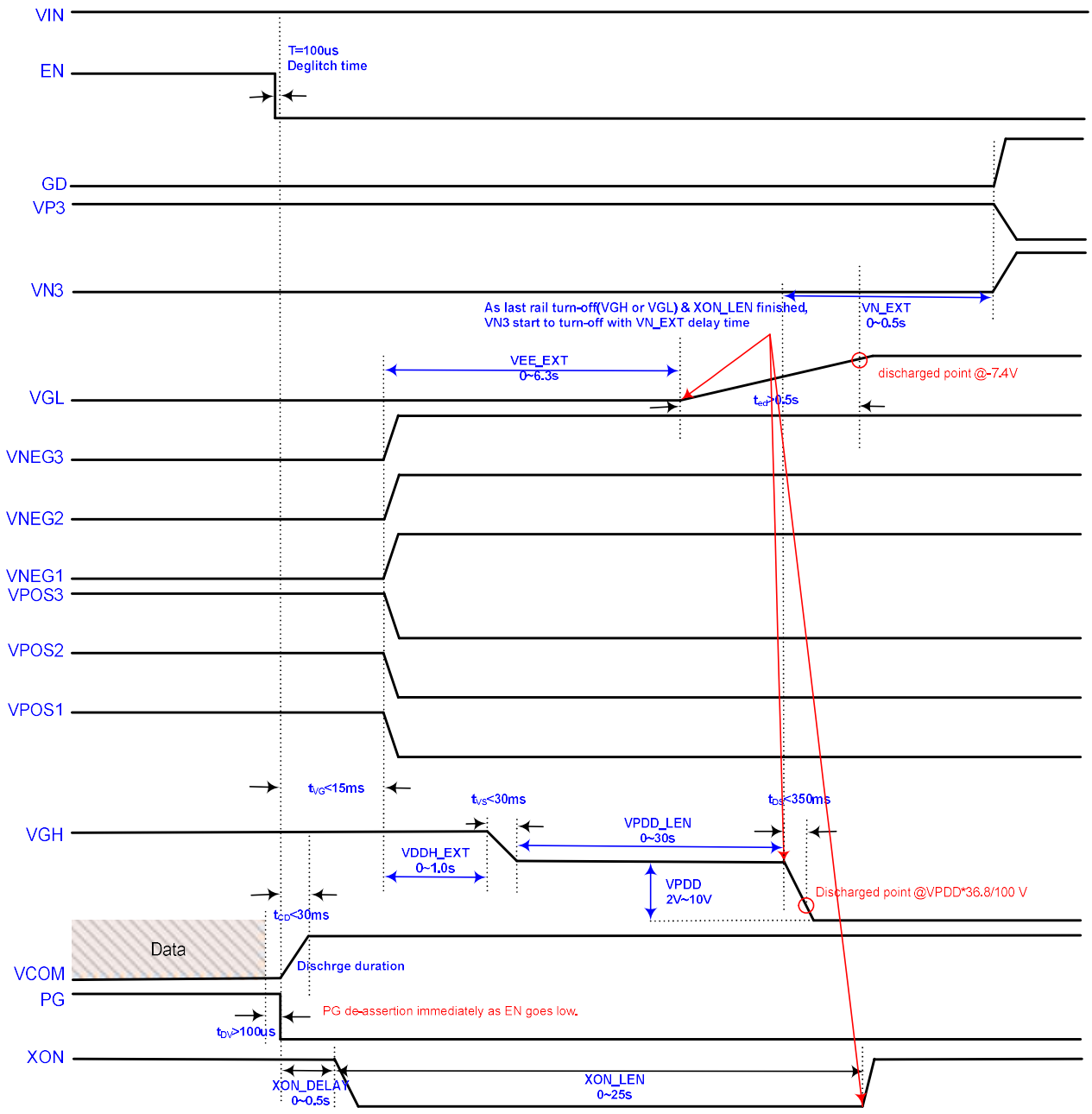
1. Supply voltage decay through pull-down resistors.
2. Normal mode off sequence is setting by 0x15 MODE[5] register.

(E) Power-OFF Sequence (3-Level Output Mode)



0x16H	0x0DH	Function	Power Rail active	
3/7 LEVEL[5]	VCOM_3L_MODE[3]		DC/DC	Source Power
0	x	7_LEVEL DCVCOM	VP1/VN1 VP2/VN2 VP3/VN3	VPOS1/VNEG1 VPOS2/VNEG2 VPOS3/VNEG3
1	**0**	**3_LEVEL DCVCOM**	**VP3/VN3**	**VPOS3/VNEG3**

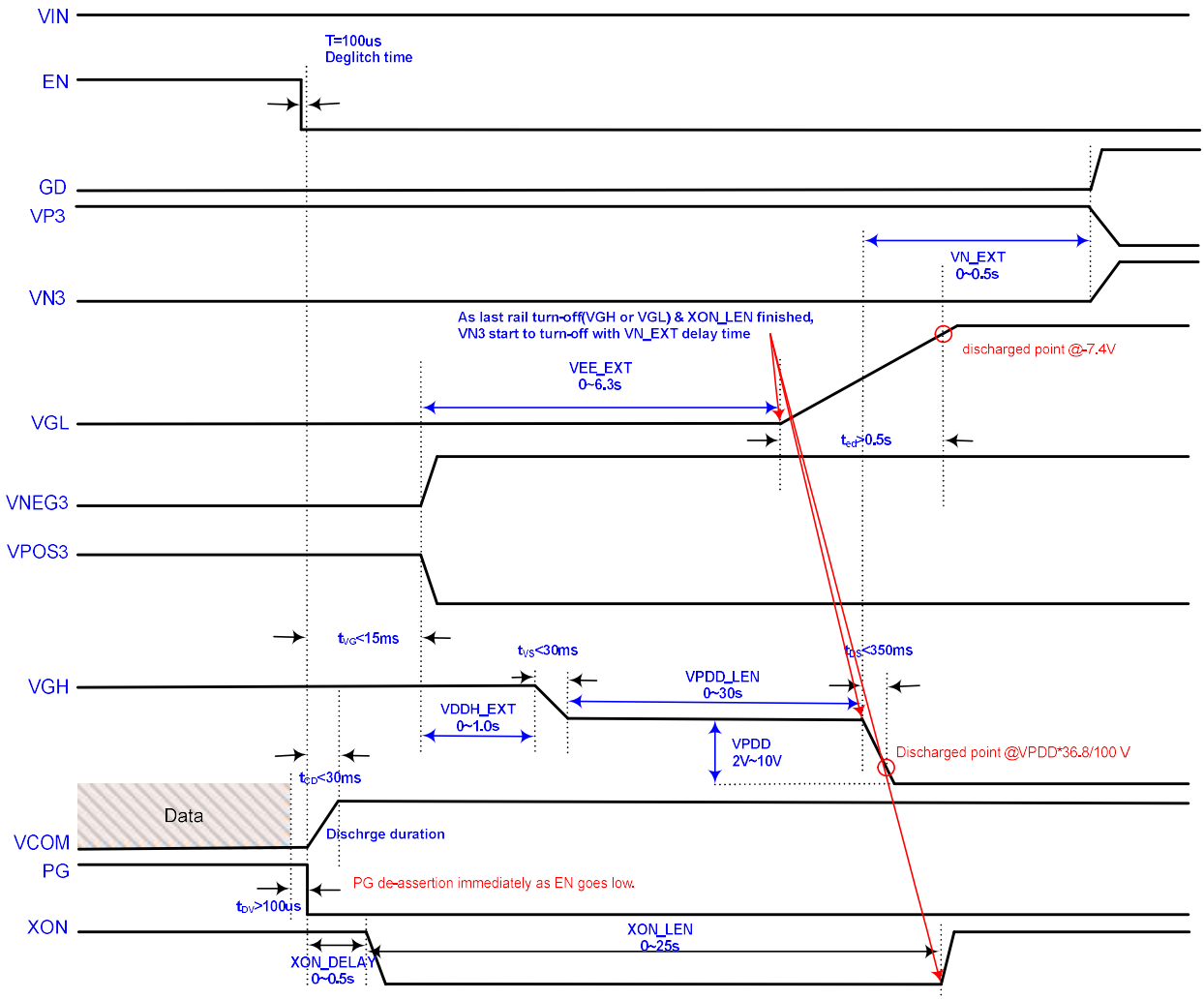
(F) Power-OFF Sequence (Post Drive Mode, 7-Level):



Post Drive Mode:

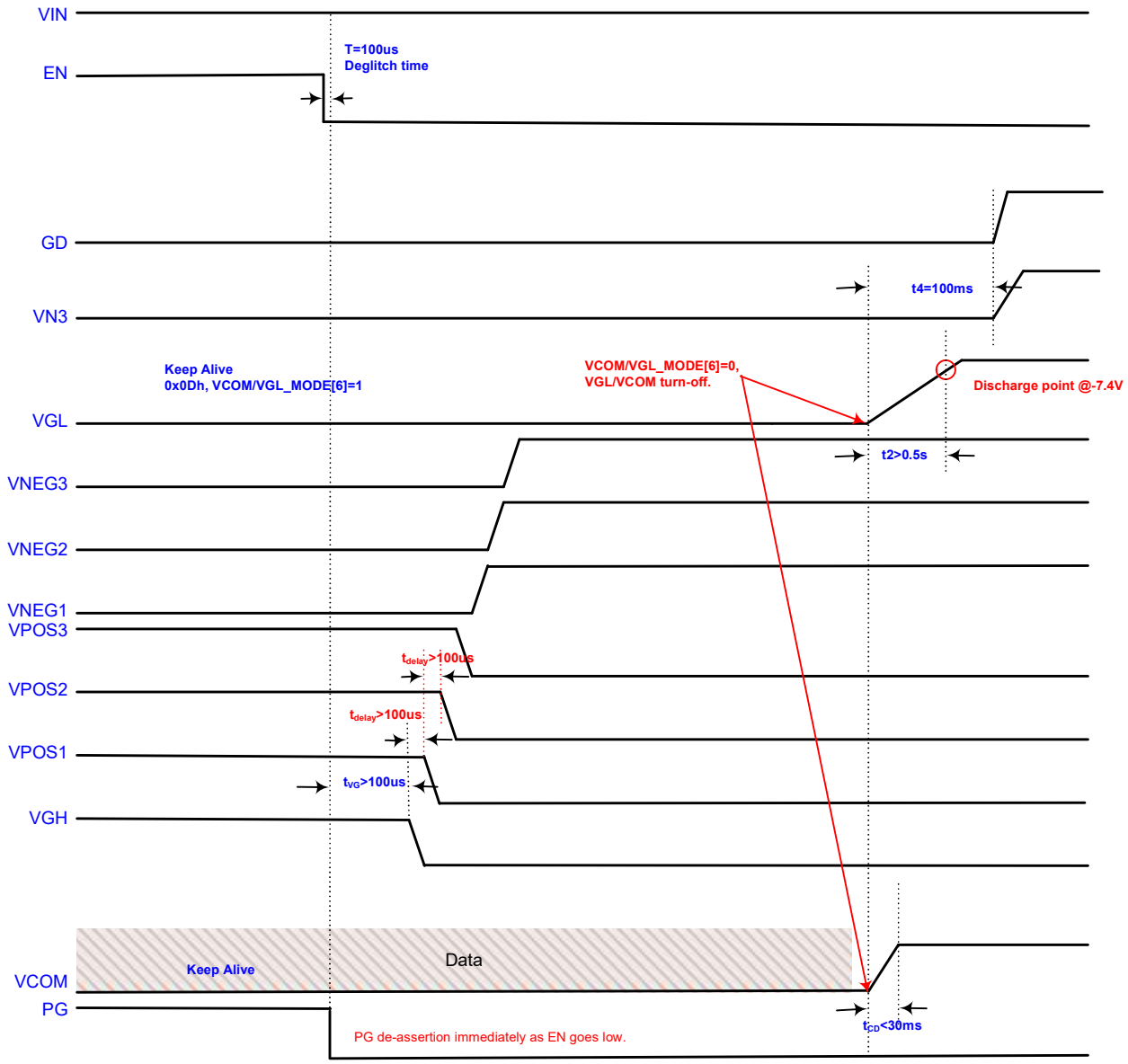
1. VGH has post drive mode (Night Mode).
2. The gate high voltage (VGH) can be extended beyond that required for the normal active update. The extension time is given by VDDH_EXT. VDDH_EXT starts after t_{VG} time where t_{VG} must be less than 15ms.
3. In addition, VGH is pulled to VPDD in less than 30ms(t_{VS}) when the PMIC powers down the standard VGH voltage. VPDD will be powered on for the time duration of VPDD_LEN. In addition, VGH powers down with RC decay of t_{DS} (<350ms).
4. The low gate voltage (VGL) can be extended beyond that which is required for the normal active update. The extension time is given by VEE_EXT.
5. VCOM will quickly be pulled to ground through a low resistance path (<30ms) after the active drive. A low resistance path of less than 1kΩ is desirable.
6. As last rail turn-off (VGL or VGH) & XON_LEN finished, VN3 start to turn-off with VN_EXT delay time.

(G)Power-OFF Sequence (Post Drive Mode, 3-Level):



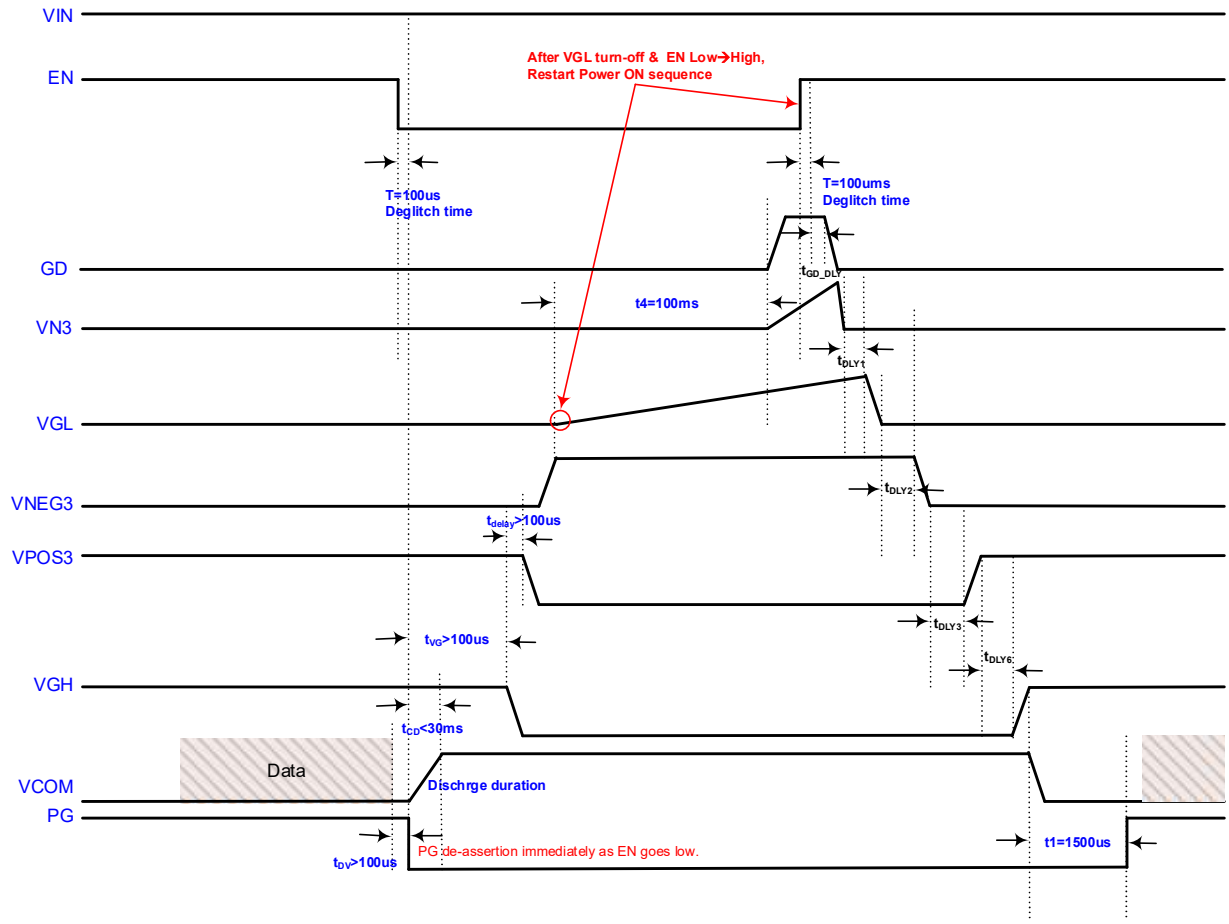
0x16H	0x0DH	Function	Power Rail active	
3/7 LEVEL[5]	VCOM_3L_MODE[3]		DC/DC	Source Power
0	x	7_LEVEL DCVCOM	VP1/VN1 VP2/VN2 VP3/VN3	VPOS1/VNEG1 VPOS2/VNEG2 VPOS3/VNEG3
1	**0**	**3_LEVEL DCVCOM**	**VP3/VN3**	**VPOS3/VNEG3**

(H) Power-OFF Sequence (7-Level Output Mode, VCOM/VGL Keep Alive)

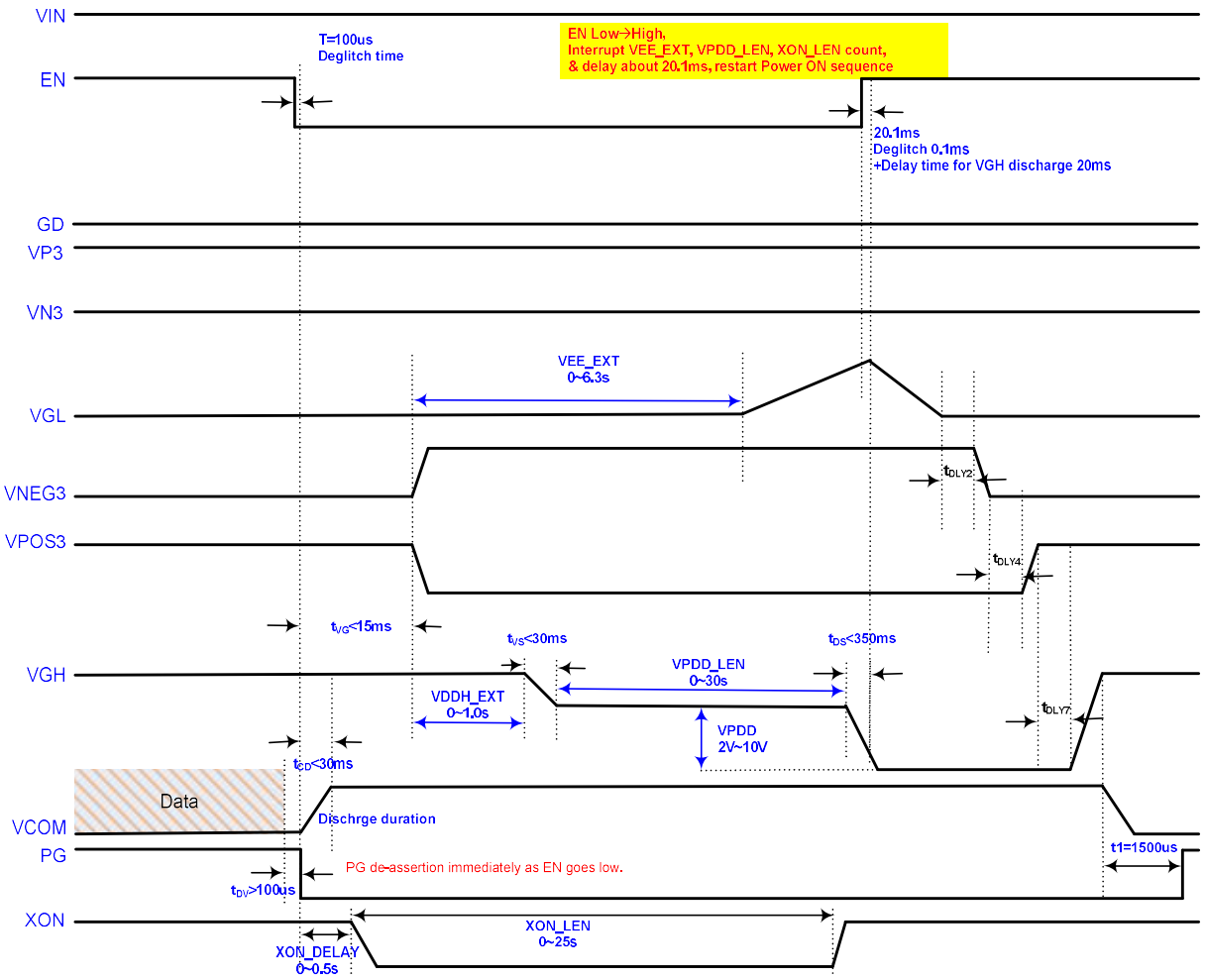


1. For VCOM/VGL_MODE[6] =”1” set by I²C (register 0x0D), VCOM and VGL continue power-on after EPD update.

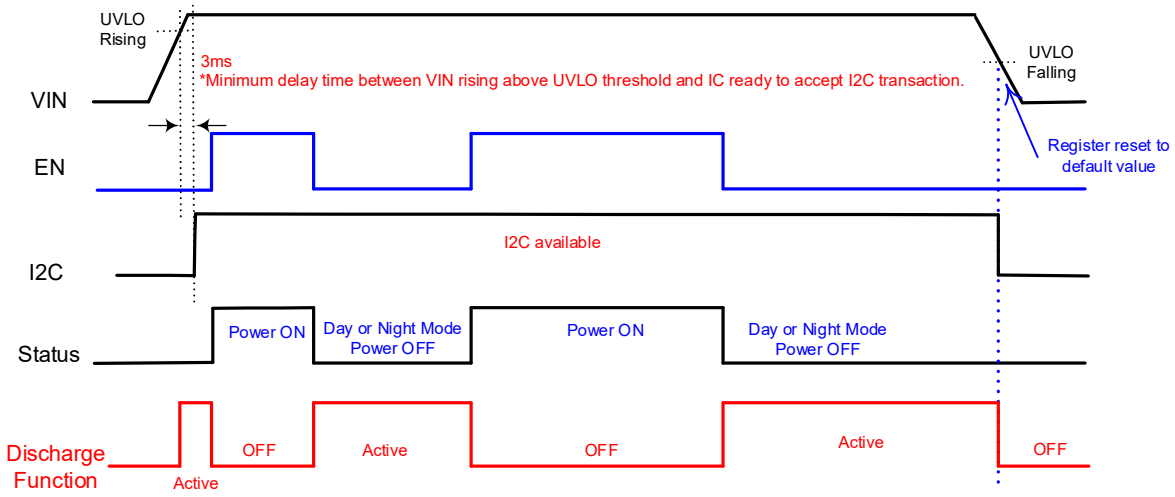
(I) Power-OFF to ON Sequence (3-Level Output)



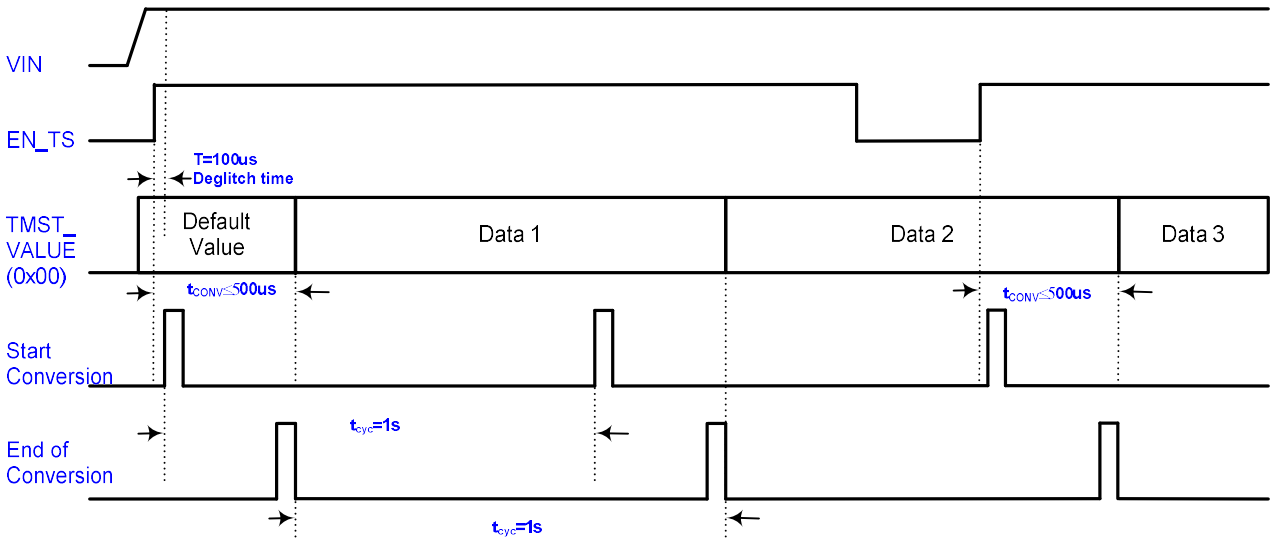
(J)Power-OFF to ON Sequence (Post Drive Mode, 3-Leve):



(K) EN vs. I²C



(L) EN _TS vs. Temperature Acquisition



G2198A I²C Command Set up Example with Post Drive Mode(PDD) for ACeP2

	EN=0 (Standby Mode, disable all power rails, allow to accept I2C register settings)			
PDD Mode (Night Mode)	**The following I2C command settings follow the register definition in the datasheet.**			
	ID(No include R/W Bit)	**Address**	**Data**	**Note**
VPOS1 Voltage	48	01	0590	Set VPOS1= +6V, enable discharge
VNEG1 Voltage	48	03	0590	Set VNEG1= -6V, enable discharge
VPOS2 Voltage	48	05	05D3	Set VPOS2= +12V, enable discharge
VNEG2 Voltage	48	07	05D3	Set VNEG2= -12V, enable discharge
VPOS3 Voltage	48	09	02CA	Set VPOS3= +24V, enable discharge, VP3 500KHz operating
VNEG3 Voltage	48	0B	02CA	Set VNEG3= -24V, enable discharge, VN3 500KHz operating
VCOM Voltage	48	0D	00	Set VCOM= -1V, enable discharge, VCOM control by default sequence
	48	0E	32	
VGH/VPDD Voltage	48	0F	13A8	Set VGH=+35V, VPDD=3V, VGL enable discharge(mode 1)
VGL/VEE_EXT Voltage	48	11	01A8	Set VGL=-35V, VEE_EXT=0s
Delay Time	48	13	FF	t_{DYL1}~t_{DYL4}=4ms
Delay Time	48	14	FF	t_{DYL5}~t_{DYL8}=4ms
Enable PDD, VDDH_EXT	48	15	A0	t_{DYL9}=4ms, enable PDD mode(Night Mode), VDDH_EXT=0s
Control Mode, VN_EXT	48	16	D0	7 level ,SS time=12ms, VGH discharge enable, VN_EXT=0s
VPDD_LEN	48	17	5F	VPDD_LEN=6s
XON_DELAY	48	18	14	XON_DELAY=50ms
XON_LEN	48	19	FF	XON_LEN=25.5s
VGL Discharge Threshold	48	1D	18	VGL discharge point=-7.4V
	EN=1(Active Mode, enable all power rails)			

Register Map:

Register	Address(Hex)	Name	Default Value	Description
0	0x00	TMST_VALUE	0001 1001	Thermistor value read by ADC
1	0x01	VPOS1_SETTING	0000 0101	Voltage settings for VPOS1(10-bit) & VPOS1 function setting
2	0x02		1001 0000	
3	0x03	VNEG1_SETTING	0000 0101	Voltage settings for VNEG1(10-bit) & VNEG1 function setting
4	0x04		1001 0000	
5	0x05	VPOS2_SETTING	0000 0101	Voltage settings for VPOS2(10-bit) & VPOS2 function setting
6	0x06		1101 0011	
7	0x07	VNEG2_SETTING	0000 0101	Voltage settings for VNEG2(10-bit) & VNEG2 function setting
8	0x08		1101 0011	
9	0x09	VPOS3_SETTING	0000 0010	Voltage settings for VPOS3(10-bit) & VPOS3 function setting
10	0x0A		1100 1010	
11	0x0B	VNEG3_SETTING	0000 0010	Voltage settings for VNEG3(10-bit) & VNEG3 function setting
12	0x0C		1100 1010	
13	0x0D	VCOM_SETTING	0000 1000	Voltage settings for VCOM(8-bit) & VCOM mode
14	0x0E		0011 0011	
15	0x0F	VGH & VPDD_SETTING	0001 0011	Voltage settings for VGH(9-bit) & VPDD(5-bit)
16	0x10		1010 1000	
17	0x11	VGL & VEE_EXT_SETTING	0000 0001	Voltage settings for VGL(9-bit) & VEE_EXT(7-bit)
18	0x12		1010 1000	
19	0x13	PWRON_DELAY1	1010 1010	Power on delay time set for VGL & VNEGx
20	0x14	PWRON_DELAY2	1010 1010	Power on delay time set for VPOSx & VGH
21	0x15	MODE & VDDH_EXT SETTING	1000 0000	Normal Mode or Post Drive Mode and VDDH_EXT delay setting for post drive discharge function
22	0x16	CONTROL_REG1 & VN_EXT	0001 0000	Soft-Start time, 3 level and 7-level output switch,ON/OFF control, Phase-Shift, VGH discharge function
				VN_EXT delay setting for post drive discharge function(2-bit)
23	0x17	VPDD_LEN	0000 0000	VPDD_LEN delay setting for post drive discharge function(8-bit)
24	0x18	XON_SETTING	0000 0000	XON delay time & LEN setting
25	0x19		0000 0000	
26	0x1A	Fault Flag1	0000 0000	Show error code and Power-Good signal
27	0x1B	Fault Flag2	0000 0000	Show error code
28	0x1C	Fault Flag2	0000 0000	Show error code & Revision ID
29	0x1D	VGL_DIS_TH	0001 1000	VGL discharge threshold

0x00h

Address-0x00h								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	TMST_VALUE[7:0]							
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	1	1	0	0	1

Field Name	BIT Definition
TMST_VALUE[7:0]	Temperature read-out
	1111 0110 : < -10°C
	1111 0110 : -10°C
	1111 0111 : -9°C
	……..
	1111 1110 : -2°C
	1111 1111 : -1°C
	0000 0000 : 0°C
	0000 0001 : 1°C
	0000 0010 : 2°C
	……..
	0001 1001 : 25°C
	……..
	0101 0101 : 85°C
	0101 0101 : > 85°C

0x01h & 0x02h

Address-0x01h								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	/VPOS1_DIS	TRACK1	VP1_FIXED_OUT		MODE_VP1	FREQ_VP1	VPOS1[9:8]	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	1	0	1
Address-0x02h								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VPOS1[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	0	0	1	0	0	0	0

Field Name	BIT Definition
/VPOS1_DIS[7]	**0: enable VPOS1 discharge function**
	1: disable VPOS1 discharge function
TRACK1[6]	VPOS1/VNEG1 Tracking function
	0: disable
	1: enable(Only for VPOS/VNEG are of opposite sign but same magnitude)
VP1_FIXED_OUT[5:4]	VP1 Fixed Output @ VPOS1[9:0]<6V
	00: 6.0V
	01: 5.5V
	10: 5.0V
	11: 4.5V
MODE_VP1[3]	VP1 DC/DC Operating Mode
	0: with PSM
	1: No PSM
FREQ_VP1[2]	VP1 Switching Frequency
	0: 500KHz
	1: 1MHz
VPOS1[9:0]	VPOS1 voltage adjustment
	VPOS1=VPOS1[9:0]*10mV+2V

0x03h & 0x04h

Address-0x03h								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	/VNEG1_DIS	Reserved			MODE_VN1	FREQ_VN1	VNEG1[9:8]	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	1	0	1
Address-0x04h								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VNEG1[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	0	0	1	0	0	0	0

Field Name	BIT Definition
/VNEG1_DIS[7]	**0: enable VNEG1 discharge function**
	1: disable VNEG1 discharge function
Reserved[6:4]	Reserved bit
MODE_VN1[3]	VN1 DC/DC Operating Mode
	0: with PSM
	1: No PSM
FREQ_VN1[2]	VN1 Switching Frequency
	0: 500KHz
	1: 1MHz
VNEG1[9:0]	VNEG1 voltage adjustment
	VNEG1=VNEG1[9:0]*-10mV-2.0V

0x05h & 0x06h

Address-0x05h								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	/VPOS2_DIS	TRACK2	Reserved		MODE_VP2	FREQ_VP2	VPOS2[9:8]	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	1	0	1
Address-0x06h								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VPOS2[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	0	1	0	0	1	1

Field Name	BIT Definition
/VPOS2_DIS[7]	**0: enable VPOS2 discharge function**
	1: disable VPOS2 discharge function
TRACK2[6]	VPOS2/VNEG2 Tracking function
	0: disable
	1: enable(Only for VPOS/VNEG are of opposite sign but same magnitude)
Reserved[5:4]	Reserved bit
MODE_VP2[3]	VP2 DC/DC Operating Mode
	0: with PSM
	1: No PSM
FREQ_VP2[2]	VP2 Switching Frequency
	0: 500KHz
	1: 1MHz
VPOS2[9:0]	VPOS2 voltage adjustment
	VPOS2=VPOS2[9:0]*15mV+5.0V

0x07h & 0x08h

Address-0x07h								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	/VNEG2_DIS	Reserved			MODE_VN2	FREQ_VN2	VNEG2[9:8]	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	1	0	1
Address-0x08h								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VNEG2[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	0	1	0	0	1	1

Field Name	BIT Definition
/VNEG2_DIS[7]	**0: enable VNEG2 discharge function**
	1: disable VNEG2 discharge function
Reserved[6:4]	Reserved bit
MODE_VN2[3]	VN2 DC/DC Operating Mode
	0: with PSM
	1: Noh PSM
FREQ_VN2[2]	VN2 Switching Frequency
	0: 500KHz
	1: 1MHz
VNEG2[9:0]	VNEG2 voltage adjustment
	VNEG2=VNEG2[9:0]*-15mV-5.0V

0x09h & 0x0Ah

Address-0x09h								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	/VPOS3_DIS	TRACK3	Reserved		MODE_VP3	FREQ_VP3	VPOS3[9:8]	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	1	0
Address-0x0Ah								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VPOS3[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	0	0	1	0	1	0

Field Name	BIT Definition
/VPOS3_DIS[7]	**0: enable VPOS3 discharge function**
	1: disable VPOS3 discharge function
TRACK3[6]	VPOS3/VNEG3 Tracking function
	0: disable
	1: enable(Only for VPOS/VNEG are of opposite sign but same magnitude)
Reserved[5:3]	Reserved bit
MODE_VP3[3]	VP3 DC/DC Operating Mode
	0: with PSM
	1: No PSM
FREQ_VP3[2]	VP3 Switching Frequency
	0: 500KHz
	1: 1MHz
VPOS3[9:0]	VPOS3 voltage adjustment
	VPOS3=VPOS3[9:0]*21mV+9.0V

0x0Bh & 0x0Ch

Address-0x0Bh								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	/VNEG3_DIS	VN3_SSCL	SSN3		MODE_VN3	FREQ_VN3	VNEG3[9:8]	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	1	0
Address-0x0Ch								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VNEG3[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	0	0	1	0	1	0

Field Name	BIT Definition
/VNEG3_DIS[7]	**0: enable VNEG3 discharge function**
	1: disable VNEG3 discharge function
VN3_SSCL	VN3 Current Limit of Soft-Start
	0: 3.5A
	1: 2.5A
SSN3[5:4]	VN3/VNEG3 soft-start time control with 0x0DH SS_CTLN3[1]
	00:6ms/3ms
	01:8ms/4ms
	10:10ms/5ms
	11:12ms/6ms
MODE_VN3[3]	VN3 DC/DC Operating Mode
	0: with PSM
	1: No PSM
FREQ_VN3[2]	VN3 Switching Frequency
	0: 500KHz
	1: 1MHz
VNEG3[9:0]	VNEG3 voltage adjustment
	VNEG3=VNEG3[9:0]*-21mV-9.0V

0x0Dh & 0x0Eh

Address-0x0Dh								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VCOMCTL	VCOM/VGL_MODE	/VCOM_DIS	VCOM_EXT_CTL	VCOM_3L_MODE	Re-served	SS_CTLN3	/SW_CTL_VCOM
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	1	0	0	0
Address-0x0Eh								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VCOM[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	1	1	0	0	1	1

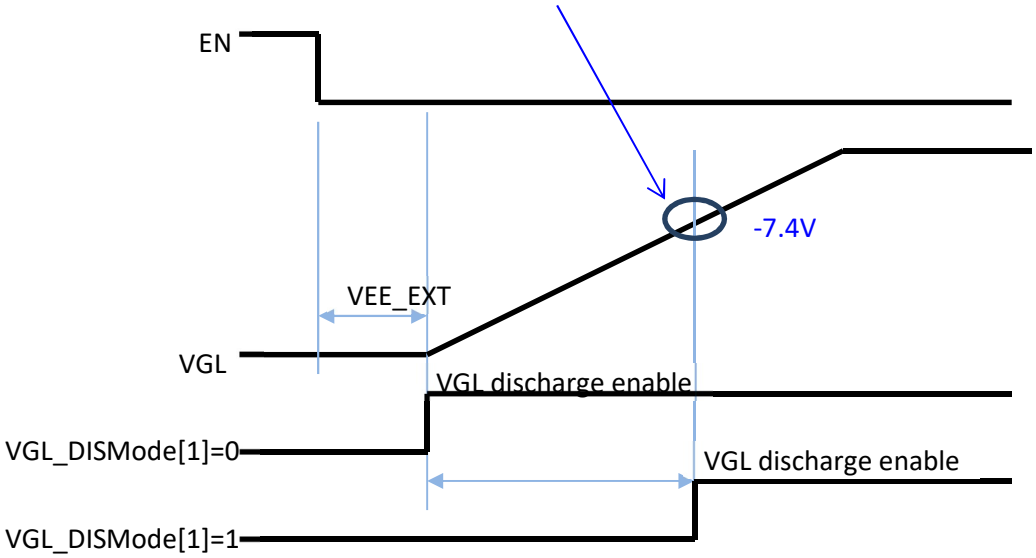
Field Name	BIT Definition
VCOMCTL[7]	**0: VCOM on/off will follow the default sequence**
	1: VCOM on/off is controlled by external Control by VCOM_EXT_CTL[4]
VCOM/VGL_MODE[6]	**0: normal power off sequence for VCOM/VGL**
	1: VCOM/VGL keep alive when power off after EPD update
/VCOM_DIS[5]	**0: enable VCOM discharge function**
	1: disable VCOM discharge function
VCOM_EXT_CTL[4]	**0: Control by external pin EN_VCOM**
	1: Control by Register SW_CTL_VCOM[0]
VCOM_3L_MODE[3]	0: 3 LEVEL source power from VPOS3/VNEG3
	1: 3 LEVEL source power from VPOS2/VNEG2
Reserved[2]	**Reserved Bit**
SS_CTLN3[1]	**0: VN3/VNEG3 SS Time=6,8,10,12 ms(Control by 0x0BH SSN3[5:4])**
	1: VN3/VNEG3 SS Time=3,4,5,6 ms(Control by 0x0BH SSN3[5:4])
/SW_CTL_VCOM[0]	**0: VCOM dsiable**
	1: VCOM enable
VCOM[7:0]	VCOM voltage adjustment
	VCOM=0V-VCOM[7:0]*19.6mV

0x0Fh & 0x10h

Address-0x0Fh								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VPDD[7:3]					/VGL_DIS	VGL_DISMode	VGH[8]
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	1	0	0	1	1
Address-0x10h								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VGH[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	0	1	0	1	0	0	0

Field Name	BIT Definition
VPDD[7:3]	VPDD voltage setting for post drive discharge function
	VPDD=VPDD[7:3]*500mV+2.0V
Reserved[2:1]	**Reserved bit**
/VGL_DIS[2]	**0: enable VGL discharge function**
	1: disable VGL discharge function
VGL_DISMode[1]	0: Discharge Mode 0
	1:Discharge Mode 1
VGH[8:0]	VGH voltage adjustment
	VGH=VGH[8:0]*59mV+10V

/VGL_DIS[2]=0→enable VGL discharge function
/VGL_DIS[2]=1, default→disable VGL discharge function



0x11h & 0x12h

Address-0x11h								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VEE_EXT[7:1]							VGL[8]
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	1
Address-0x12h								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VGL[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	0	1	0	1	0	0	0

Field Name	BIT Definition
VEE_EXT[7:1]	VEE_EXT delay setting for post drive discharge function(0~6.3s)
	VEE_EXT=VEE_EXT[7:1]*50ms
VGL[8:0]	VGL voltage adjustment
	VGL=VGL[8:0]*-59mV-10V

0x13h

Address-0x13h								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	t_{DLY1}		t_{DLY2}		t_{DLY3}		t_{DLY4}	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	0	1	0	1	0	1	0

Field Name	BIT Definition
t_{DLY1}[7:6]	Delay time set from VN3 to VGL
	00: 0ms
	01: 1ms
	10: 2ms
	11: 4ms
t_{DLY2}[5:4]	Delay time set from VGL to VNEG3
	00: 0ms
	01: 1ms
	10: 2ms
	11: 4ms
t_{DLY3}[3:2]	Delay time set from VNEG3 to VNEG2
	00: 0ms
	01: 1ms
	10: 2ms
	11: 4ms
t_{DLY4}[1:0]	Delay time set from VNEG2 to VNEG1
	00: 0ms
	01: 1ms
	10: 2ms
	11: 4ms

0x14h

Address-0x14h								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	t_{DLY5}		t_{DLY6}		t_{DLY7}		t_{DLY8}	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	0	1	0	1	0	1	0

Field Name	BIT Definition
t_{DLY5}[7:6]	Delay time set from VNEG1 to VPOS3
	00: 0ms
	01: 1ms
	10: 2ms
	11: 4ms
t_{DLY6}[5:4]	Delay time set from VPOS3 to VPOS2
	00: 0ms
	01: 1ms
	10: 2ms
	11: 4ms
t_{DLY7}[3:2]	Delay time set from VPOS2 to VPOS1
	00: 0ms
	01: 1ms
	10: 2ms
	11: 4ms
t_{DLY8}[1:0]	Delay time set from VPOS1 to VGH
	00: 0ms
	01: 1ms
	10: 2ms
	11: 4ms

0x15h

Address-0x15h								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	t_{GD_DLY}		MODE	VDDH_EXT[4:0]				
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	0	0	0	0	0	0	0

Field Name	BIT Definition
t_{GD_DLY}[7:6]	Delay time set for true shutdown MOS turn on
	00: 0ms
	01: 2ms
	10: 4ms
	11: 6ms
MODE[5]	**0: normal mode power off sequence**
	1: post drive discharge mode power off sequence
VDDH_EXT[4:0]	VDDH_EXT delay setting for post drive discharge function(0~1s)
	VDDH_EXT=VDDH_EXT[4:0]*50ms

0x16h

Address-0x16h								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	SS		3/7_LEVEL	ON_OFF	PHASE-SHIFT	/VGH_DIS	VN_EXT	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	1	0	0	0	0

Field Name	BIT Definition
SS[7:6]	PMIC soft-start time(VPOSx/VGH/VGL) control with 0x18H SS_CTL[0]
	00: 6ms/3ms
	01: 8ms/4ms
	10: 10ms/5ms
	11: 12ms/6ms
3/7 LEVEL[5]	**0: 7-Level output**
	1: 3-Level output
ON_OFF[4]	0: turn off all power rails(VN3,VPOSx,VNEGx,VGH1,VGH2,VGL)
	1: turn on all power rails(VN3,VPOSx,VNEGx,VGH1,VGH2,VGL)
PHASE-SHIFT[3]	**0: disable Phase-Shift (VPx/VNx)**
	1: enable Phase-Shift (VPx/VNx)
/VGH_DIS[2]	**0: enable VGH discharge function**
	1: disable VGH discharge function
VN_EXT[1:0]	VN_EXT delay setting for post drive discharge function(0~500ms)
	00: 0ms
	01: 250ms
	10: 500ms
	11: Reserved

0x17h

Address-0x17h								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VPDD_LEN[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Field Name	BIT Definition
VPDD_LEN[7:0]	VPDD_LEN delay setting(0~30s)
	VPDD_LEN follow RFQ reguest as below

Index	Time(ms)	Index	Time(ms)	Index	Time(ms)	Index	Time(ms)
0	0	64	3820	128	8850	192	16230
1	50	65	3890	129	8950	193	16380
2	110	66	3960	130	9040	194	16530
3	160	67	4030	131	9130	195	16680
4	210	68	4090	132	9230	196	16830
5	270	69	4160	133	9320	197	16980
6	320	70	4230	134	9420	198	17140
7	380	71	4300	135	9510	199	17290
8	430	72	4370	136	9610	200	17450
9	490	73	4440	137	9710	201	17610
10	540	74	4510	138	9810	202	17770
11	600	75	4580	139	9900	203	17930
12	650	76	4650	140	10000	204	18100
13	710	77	4720	141	10100	205	18260
14	760	78	4800	142	10200	206	18430
15	820	79	4870	143	10300	207	18600
16	870	80	4940	144	10400	208	18770
17	930	81	5010	145	10510	209	18940
18	990	82	5080	146	10610	210	19120
19	1040	83	5160	147	10710	211	19290
20	1100	84	5230	148	10820	212	19470
21	1160	85	5310	149	10920	213	19650
22	1210	86	5380	150	11030	214	19830
23	1270	87	5450	151	11130	215	20020
24	1330	88	5530	152	11240	216	20210
25	1390	89	5600	153	11350	217	20390

Index	Time(ms)	Index	Time(ms)	Index	Time(ms)	Index	Time(ms)
26	1440	90	5680	154	11460	218	20590
27	1500	91	5760	155	11570	219	20780
28	1560	92	5830	156	11680	220	20980
29	1620	93	5910	157	11790	221	21170
30	1680	94	5990	158	11900	222	21370
31	1740	95	6060	159	12010	223	21580
32	1800	96	6140	160	12120	224	21780
33	1860	97	6220	161	12240	225	21990
34	1920	98	6300	162	12350	226	22200
35	1980	99	6380	163	12470	227	22420
36	2040	100	6460	164	12580	228	22640
37	2100	101	6540	165	12700	229	22860
38	2160	102	6620	166	12820	230	23080
39	2220	103	6700	167	12940	231	23300
40	2280	104	6780	168	13060	232	23530
41	2340	105	6860	169	13180	233	23770
42	2400	106	6940	170	13300	234	24000
43	2460	107	7020	171	13420	235	24240
44	2530	108	7110	172	13540	236	24490
45	2590	109	7190	173	13670	237	24730
46	2650	110	7270	174	13790	238	24990
47	2710	111	7360	175	13920	239	25240
48	2780	112	7440	176	14050	240	25500
49	2840	113	7520	177	14170	241	25760
50	2900	114	7610	178	14300	242	26030
51	2970	115	7700	179	14430	243	26300
52	3030	116	7780	180	14570	244	26580
53	3100	117	7870	181	14700	245	26860
54	3160	118	7960	182	14830	246	27150
55	3230	119	8040	183	14970	247	27440
56	3290	120	8130	184	15100	248	27740
57	3360	121	8220	185	15240	249	28050
58	3420	122	8310	186	15380	250	28360
59	3490	123	8400	187	15520	251	28670
60	3550	124	8490	188	15660	252	28990
61	3620	125	8580	189	15800	253	29320
62	3690	126	8670	190	15940	254	29660
63	3750	127	8760	191	16090	255	30000

0x18h & 0x19h

Address-0x18h								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	XON_DELAY[7:1]							SS_CTL
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Address-0x19h								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	XON_LEN[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Field Name	BIT Definition
XON_DELAY[7:1]	XON_DELAY setting for post drive discharge function(0~0.5s)
	XON_DELAY=XON_DELAY[7:1]*5ms
SS_CTL[0]	**0: SS Time=6,8,10,12mS(Control by 0x16H SS[7:6])**
	1: SS Time=3,4,5,6mS(Control by 0x16H SS[7:6])
XON_LEN[7:0]	XON_LEN setting for post drive discharge function(0~25s)
	XON_LEN=XON_LEN[7:0]*100ms

0x1Ah

Address-0x1Ah								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	PG	TSD	FLT_VP1	FLT_VP2	FLT_VP3	FLT_VN1	FLT_VN2	FLT_VN3
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0

Field Name	BIT Definition
PG[7]	**0: VPOS1/2/3, VNEG1/2/3, VGH,VGL are not in regulation or turn off**
	1: VPOS1/2/3, VNEG1/2/3, VGH, VGL are in regulation
TSD[6]	**0: no fault event**
	1: Thermal shutdown
FLT_VP1[5]	**0: no fault event**
	1: UVP or SCP
FLT_VP2[4]	**0: no fault event**
	1: UVP or SCP
FLT_VP3[3]	**0: no fault event**
	1: UVP or SCP
FLT_VN1[2]	**0: no fault event**
	1: UVP or SCP
FLT_VN2[1]	**0: no fault event**
	1: UVP or SCP
FLT_VN3[0]	**0: no fault event**
	1: UVP or SCP

0x1Bh

Address-0x1Bh								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	FLT_VPOS1	FLT_VPOS2	FLT_VPOS3	FLT_VNEG1	FLT_VNEG2	FLT_VNEG3	FLT_VGH1	Reserved
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0

Field Name	BIT Definition
FLT_VPOS1[7]	**0: no fault event**
	1: UVP or SCP
FLT_VPOS2[6]	**0: no fault event**
	1: UVP or SCP
FLT_VPOS3[5]	**0: no fault event**
	1: UVP or SCP
FLT_VNEG1[4]	**0: no fault event**
	1: UVP or SCP
FLT_VNEG2[3]	**0: no fault event**
	1: UVP or SCP
FLT_VNEG3[2]	**0: no fault event**
	1: UVP or SCP
FLT_VGH[1]	**0: no fault event**
	1: UVP or SCP
Reserved	**Reserved bit**

0x1Ch

Address-0x1Ch								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	FLT_VGL	FLT_VCOM	REVID[5:0]					
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0

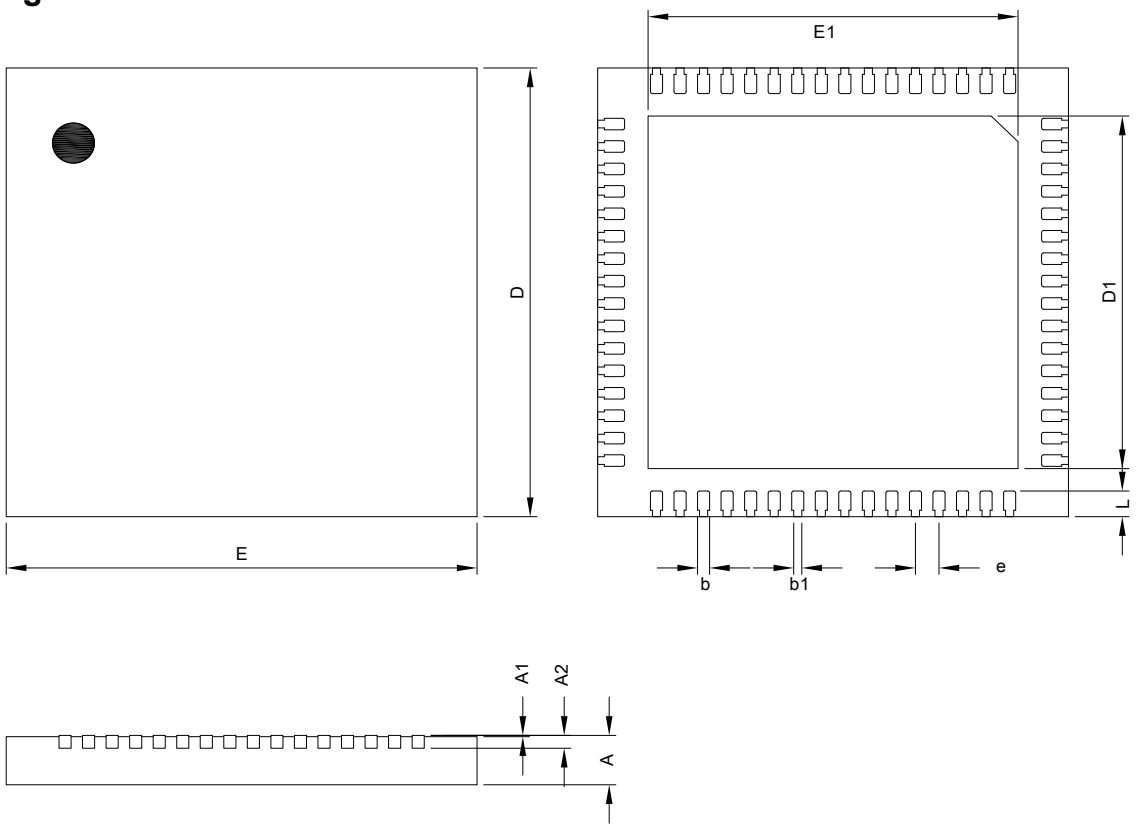
Field Name	BIT Definition
FLT_VGL[7]	**0: no fault event**
	1: UVP or SCP
FLT_VCOM[6]	**0: no fault event**
	1:SCP
REVID[5:0]	**TBD**

0x1Dh

Address-0x1Dh								
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VGL_DIS_TH[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	1	1	0	0	0

Field Name	BIT Definition
VGL_DIS_TH[7:0]	VGL Discharge Threshold
	Threshold=VGL_DIS_TH[7:0]*-0.1V-5.0V

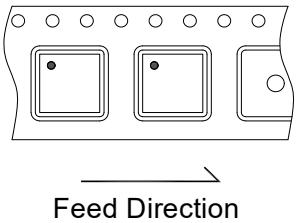
Package Information



TQFN7X7-64 Package

Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.0276	0.0295	0.0315
A1	0.00	- - -	0.05	0.0000	- - -	0.0020
A2		0.20 REF			0.0079 REF	
D	6.95	7.00	7.05	0.2736	0.2756	0.2776
E	6.95	7.00	7.05	0.2736	0.2756	0.2776
D1	5.45	5.50	5.55	0.2146	0.2165	0.2185
E1	5.45	5.50	5.55	0.2146	0.2165	0.2185
b	0.13	0.18	0.23	0.0051	0.0071	0.0091
b1	0.07	0.12	0.17	0.0028	0.0047	0.0067
e		0.35 BSC			0.0138 BSC	
L	0.35	0.40	0.45	0.0138	0.0157	0.0177

Taping Specification



Feed Direction

PACKAGE	Q'TY/REEL
TQFN7X7-64	3,000ea