

Low Cost Integrated Switch-Mode One-Cell Li-Ion Charger With Full USB Compliance and USB-OTG Support

Features

- 4.2V ~ 6.2V Input Voltage Operation.
- Integrated switched mode Li-ion charger with dynamic power path function.
- USB charger with Auto Power Source Detection witch is compliant to USB Battery Charging Revision 1.2.
- Built-In Thermal Shutdown Function.
- OTG Mode Operation for USB OTG with Adjustable output 4.5-5.5V @1.5A
- Power Bank Mode Operation with 5.2V output.
- Hiccup Mode Over-current Protection in OTG mode.
- Power key function embedded.
- Shipping Mode function embedded.
- WLCSP4x5-20 Package (0.5mm pitch)

General Description

The G2230A provides switch-mode Li-ion charger with dynamic power path control. The device supports USB input sources, including standard USB host port and USB charging port, and detects the input source through D+/D- detection following the USB battery charging revision 1.2. In addition, the G2230A detects non-standard 2A/1A adapters. The G2230A also supports USB OTG operation by supplying default 5V on the DCIN with a programmable current limit (1.5A/2.0A). The G2230A supports Power Bank Mode operation by supplying 5.2V on the PMID pin. Meanwhile, the G2230A includes Power key function to manage the power on/off control through PWRON signal.

Applications

Tablet PC

Ordering Information

ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE (Green)
G2230ABZ1U	2230A	-40°C~+85°C	WLCSP4x5-20

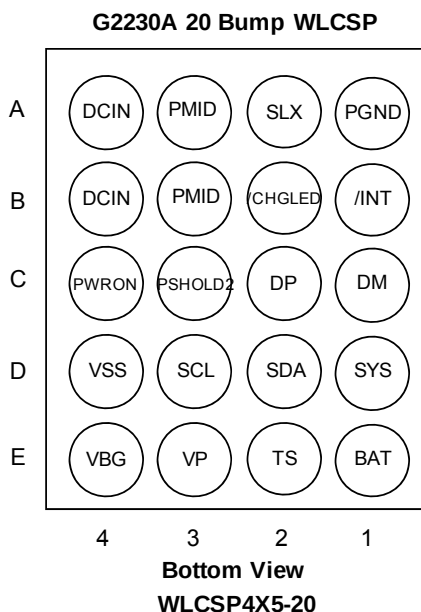
Note: BZ: WLCSP4X5-20

1: Bonding code

U: Tape & Reel

Green : Lead Free / Halogen Free

Pin Configuration



Absolute Maximum Ratings

DCIN	-0.3V to +20V
PMID, PVCCSW, SYS, BAT	-0.3V to +6.3V
SLX	-0.3V to +6.3V
VP	-0.3V to +6.3V
TS, SCL, SDA, DP, DM, /INT, /CHGLED, PWRON, PSHOLD2	-0.3V to +6.3V
Thermal Resistance Junction to Ambient, (θ_{JA})	
WLCSP4x5-20	TBD
Continuous Power Dissipation ($T_A=+25^\circ\text{C}$)	
WLCSP4x5-20	TBD

Operating Ambient Temperature	-40°C to +85°C
Storage Temperature range	-55°C to +150°C
Reflow Temperature (Soldering, 10sec)	260°C
ESD Susceptibility (HBM) (DCIN, BAT, DP, DM, /CHGLED, PWRON)	.8KV
ESD(HBM)	.4KV
ESD(MM)	.300V

Recommended Operation Conditions

DCIN	2.8V to +5.5V
BAT	2.5V to +5.5V
Operating Ambient Temperature	-40°C to 85°C
Operating Junction Temperature	+150°C

- Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
- Device is ESD sensitive. Handling precaution recommended. The Human Body model is a 100pF capacitor discharged through a 1.5K Ω resistor into each pin.

Electrical characteristics

(DCIN=SYS=5V, $T_A=25^\circ\text{C}$.)

The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
DCIN Input						
DCIN Operation Range			4.2	---	6.2	V
DCIN Under Voltage Lockout Threshold	V_{DCUV}	DCIN rising	---	3.8	4.1	V
DCIN Under Voltage Lockout Hysteresis	ΔV_{DCUV}		---	400	---	mV
DCIN Over Voltage Threshold	V_{DCOV}	DCIN rising	6.15	6.4	6.65	V
DCIN Over Voltage Hysteresis	ΔV_{DCOV}	DCIN falling	---	300	---	mV
DCIN supply current	I_{SUPDC}	$I_{SYS}=I_{BAT}=0\text{mA}$, /ENCH=1'b0 ($V_{BAT}>V_{BATREG}$)	---	1.35	---	mA
		$I_{SYS}=I_{BAT}=0\text{mA}$, /ENCH=1'b1 ($V_{BAT}>V_{BATREG}$)	---	1.25	---	mA
DCIN suspend current	I_{INSUS}	DCIN=5V, INSUS=1'b1	---	---	300	μA
DCIN automatic shutdown threshold	ΔV_{ASDN1}	DCIN-BAT, DCIN rising	---	200	300	mV
DCIN automatic shutdown hysteresis	$\Delta V_{ASDN1HS}$	DCIN-BAT, DCIN falling	10	50	---	mV
DCIN to PMID ON Resistance	R_{ON_IN}	DCIN=5V	---	48	---	m Ω
DCIN Current Limit Accuracy	$\%I_{IN_LIMIT}$		-10	---	10	%
PMID to DCIN reverse current blocking	I_{INREV}		---	1	---	μA
PMID Regulation voltage	V_{PMID}		---	5.2	---	V
SYS Output						
Minimum SYS Regulation Voltage Accuracy	V_{SYS_MIN}	BAT< V_{SYS_MIN}	-100	---	100	mV
SYS Regulation Voltage under no-battery condition	V_{SYS_NOBAT}	A4.VSETA<2>=1'b0	4.35	4.4	4.45	V
		A4.VSETA<2>=1'b1	4.55	4.6	4.65	V
SYS Regulation voltage in DPPM mode	ΔV_{SYS_DPPM}	BAT< V_{SYS_MIN} $V_{DPPM}=V_{SYS_MIN}-\Delta V_{SYS_DPPM}$	---	200	---	mV
BAT to SYS ON Resistance	R_{ON_BAT}	BAT=4.2V, $I_{SYS}=1\text{A}$	---	25	---	m Ω
Battery Condition						
Battery Depletion Threshold	V_{BAT_DPL}	BAT falling	---	2.4	---	V
Battery Depletion rising hysteresis	$V_{BAT_DPL_HYS}$	BAT rising	---	200	---	mV

Electrical Characteristics (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Battery Charger						
BAT Supply Current at battery supplement mode	I_{SUPBAT}	DCIN=VBUS=0V, BAT=4.2V, $I_{SYS}=0A$	---	---	15	μA
BAT Regulation voltage	$V_{BATREG1}$	Loading=50mA, VSETA=3'b000	4.06	4.1	4.13	V
	$V_{BATREG2}$	Loading=50mA, VSETA=3'b001	4.11	4.15	4.18	V
	$V_{BATREG3}$	Loading=50mA, VSETA=3'b010	4.16	4.2	4.23	V
	$V_{BATREG4}$	Loading=50mA, VSETA=3'b011	4.21	4.25	4.28	V
	$V_{BATREG5}$	Loading=50mA, VSETA=3'b100	4.26	4.3	4.33	V
	$V_{BATREG6}$	Loading=50mA, VSETA=3'b101	4.31	4.35	4.38	V
	$V_{BATREG7}$	Loading=50mA, VSETA=3'b110	4.46	4.4	4.43	V
	$V_{BATREG8}$	Loading=50mA, VSETA=3'b111	4.41	4.45	4.48	V
BAT Re-Charge Threshold	$\%V_{RECHG}$	Battery re-charge threshold $=\%V_{RECHG} * V_{BATREGX}$	---	97.5	---	%
BAT Fast-Charge Threshold	$V_{FASTCHG}$	BAT Rising, A4[0]=1 (Pre-charge to fast charge)	2.9	3.0	3.1	V
BAT Fast-Charge Hysteresis	$\Delta V_{FASTCHG}$	BAT Falling, A4[0]=1 (Fast charge to pre-charge)	---	200	---	mV
BAT Pre-Charge Hysteresis	ΔV_{PRECHG}	BAT Rising, (Trickle charge to pre-charge)	---	200	---	mV
BAT Pre-Charge Threshold	V_{PRECHG}	BAT Falling, (Pre-charge to trickle charge)	1.9	2.0	2.1	V
Fast Charge Current Accuracy	$\%I_{CHG}$	BAT=3.8V, $I_{CHG}=1024mA$	-10	---	10	%
Pre-Charge Current Accuracy	$\%I_{PRECHG}$	BAT=2.6V, $I_{CHG}=256mA$	-20	---	20	%
Trickle Charge Current	I_{TRICHG}	BAT=2.0V,		96		mA
Termination Current Ratio	$\%I_{TERM}$	BAT=4.2V, $\%I_{TERM}=I_{TERM}/I_{CHG}$	5	10	15	%
Charger Soft-Start Time	t_{SSCHG}		---	1.0	---	mS
PWM						
Switching Frequency	F_{OSC_CHG}		1.3	1.5	1.7	MHz
PVCCSW to SLX ON Resistance	R_{ON_P}	PMID=5V	---	65	---	m Ω
SLX to Ground ON Resistance	R_{ON_N}	PMID=5V	---	65	---	m Ω
Protection						
Thermal Regulation	THM_{REG}	THRREG A7[6:5]=11	---	120	---	$^{\circ}C$
Thermal Shutdown Temperature	THM_{SD}		---	155	---	$^{\circ}C$
Thermal Shutdown Hysteresis	ΔTHM_{SD}		---	20	---	$^{\circ}C$
SYS Output Short Circuit Detection at DCIN or VBUS Power up	V_{SYS_SCP1}		1.1	1.2	1.3	V
SYS Output Short Circuit Detection Threshold at BAT Supplement Mode	V_{SYS_SCP2}	BAT-VSYS	---	300	---	mV
Time						
Fast Charge Safety Time	t_{FCHG}	CHG_TIMER[1:0]=10	---	12	---	hrs.
Pre-charge to Fast Charge Timer Ratio	$\%t_{PCHG}$	Pre-charge safety timer $t_{PCHG}=\%t_{PCHG} * t_{FCHG}$	---	1/8	---	
Safety Timer Accuracy	$\%t_{CHG}$		-15	---	15	%
DCIN PGOOD Deglitch Time	t_{VINPG}	Time measure from DCIN: 0->5V 1 μ S rise-time to PG_STAT Bit=H	---	1.875	---	mS
DCIN Over Voltage Blanking Time	t_{VINOV}		---	50	---	μ S
Pre-Charge to Fast Charge Deglitch Time	t_{PF}		---	30	---	mS
Fast Charge to Pre-Charge Deglitch Time	t_{FP}		---	30	---	mS
Termination Deglitch Time	t_{TERMI}		---	30	---	mS
Recharge Deglitch Time	t_{RECHG}		---	120	---	mS

Electrical Characteristics (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Input power loss to PWM modulator Turn-Off Deglitch Time	t_{NO_VIN}		---	30	---	mS
No battery detection checking time	$t_{nobatchk}$			3.85		mS
Pack Temperature Fault Detection Deglitch Time	t_{TS}		---	30	---	mS
SYS Output short Circuit Deglitch Time at Battery Supplement Mode	t_{SYS_SCP}		---	250	---	μ S
SYS Output Short circuit Recovery Time at Battery Supplement Mode	$t_{SYS_SCP_R}$		---	64	---	mS
Thermistor Monitor						
VP regulation voltage	V_{VP}	VSYS=5V	2.94	3.0	3.06	V
VP Under Voltage Lockout Threshold	V_{VPUV}		---	1.2	---	V
NTC-R Installation Detection Threshold at TS	V_{NO_NTC-R}	As Percentage to VP	---	97	---	%
Cold Temperature Trip Point with JEITA function disabled	V_{COLD}	NTC=100K, ENJEITA=0	---	See Table	---	% of VP
		NTC=10K, ENJEITA=0	---	See Table	---	
Cool Temperature Trip Point with JEITA function disabled	V_{COOL}	NTC=100K, ENJEITA=0	---	See Table	---	% of VP
		NTC=10K, ENJEITA=0	---	See Table	---	
Warm Temperature Trip Point with JEITA function disabled	V_{WARM}	NTC=100K, ENJEITA=0	---	See Table	---	% of VP
		NTC=10K, ENJEITA=0	---	See Table	---	
Hot Temperature Trip Point with JEITA function disabled	V_{HOT}	NTC=100K, ENJEITA=0	---	See Table	---	% of VP
		NTC=10K, ENJEITA=0	---	See Table	---	
Cold Temperature Trip Point(0°C) with JEITA function enabled	V_{COLD}	NTC=100K, ENJEITA=1	83	84	85	% of VP
		NTC=10K, ENJEITA=1	76	77	78	
Cool Temperature Trip Point(10°C) with JEITA function enabled	V_{COOL}	NTC=100K, ENJEITA=1	74	75	76	% of VP
		NTC=10K, ENJEITA=1	68	69	70	
Warm Temperature Trip Point(45°C) with JEITA function enabled	V_{WARM}	NTC=100K, ENJEITA=1	37	38	39	% of VP
		NTC=10K, ENJEITA=1	38	39	40	
Hot Temperature Trip Point(60°C) with JEITA function enabled	V_{HOT}	NTC=100K, ENJEITA=1	24	25	26	% of VP
		NTC=10K, ENJEITA=1	28	29	30	
Temperature Trip Point Hysteresis			---	1	---	% of VP
Logic I/O						
Internal Pull Low Resistance (PWRON)	R_{pull_low}		---	200	---	k Ω
Open-Drain Output Low Voltage (/INT, /CHGLED)	V_{ODLOW}	$I_{SINK}=5mA$, VSYS=3.7V	---	---	100	mV
Open-Drain Output Leakage Current	I_{LK_OD}	$V_{OD}=5V$	---	---	1	μ A
SMBus Interface						
Logic Input High Voltage		SCL, SDA	1.3	---	---	V
Logic Input Low Voltage		SCL, SDA	---	---	0.4	V
Logic Input Current		Logic inputs forced to VCC or GND	-2	---	2	μ A
SMBus Input Capacitance		SCL, SDA	---	5	---	pF
SMBus Clock Frequency			---	---	3.5	MHz
SCL Clock Low Time	t_{LOW}	t_{LOW} , 10% to 10% points	1.3	---	---	μ S
SCL Clock High Time	t_{HIGH}	t_{HIGH} , 90% to 90% points	0.6	---	---	μ S
SMBus Start-Condition Setup Time			0.6	---	---	μ S
SMBus Repeated Start-Condition Setup Time	$t_{SU:STA}$	90% to 90% points	0.6	---	---	μ S
SMBus Start-Condition Hold Time	$t_{HD:STA}$	10% of SDA to 90% of SCL	0.6	---	---	μ S
SMBus Stop-Condition Setup Time	$t_{SD:STO}$	90% of SCL to 10% of SDA	0.6	---	---	μ S

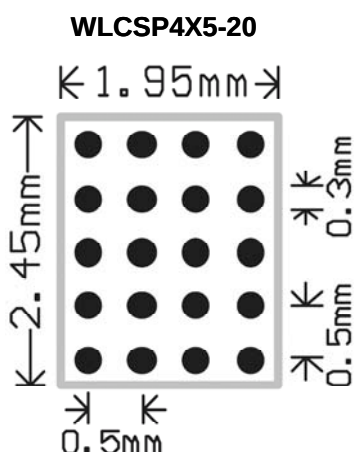
Electrical Characteristics (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
SMBus Data Valid to SCL Rising-Edge Time	$t_{SU: DAT}$	10% or 90% of SDA to 10% of SCL	100	---	---	nS
SMBus Data-Hold Time	$t_{HD: DAT}$		300	---	---	nS
SCL Falling Edge to SMBus Data-Valid Time		Master clocking in data	---	---	1	μ S
Boost Mode Operation						
Battery current in boost mode	I_{Q_BOOST}	$V_{BAT}=4.2V$, boost mode, $I_{VDCIN}=0A$	---	1	---	mA
Battery voltage exiting boost mode	V_{BOOST_BAT}	BAT falling, A4[0]=1	2.8	---	---	V
Boost Mode Operation (OTG)						
DCIN Regulation Voltage	$V_{DCINOTG}$	$V_{BOOST_BAT} < BAT < 4.5V$ $I(VDCIN)=0$, A6[7:4]=0111 (4.998V)	---	5	---	V
OTG mode output current	I_{OTG}	A6[3]=0	1	---	---	A
		A6[3]=1	1.5	---	---	A
PMID Short Circuit Threshold	V_{PMID_SCP}		---	1.212	---	V
DCIN Short Circuit Threshold	V_{DCIN_SCP}		---	1.212	---	V
OTG over-voltage threshold	V_{OTG_OVP}	Rising threshold	---	6.4	---	V
OTG over-voltage hysteresis	$V_{OTG_OVP_HYS}$	Falling threshold	---	300	---	mV
OTG over-voltage threshold recovery time	t_{OVP}		---	30	---	mS
LSFET cycle by cycle current limit	I_{LIM_OTG}		---	4.6	---	A
HSFET under current falling threshold	I_{ZCP_OTG}		---	100	---	mA
OTG mode output current limit	I_{Q1_OCP}	A6[3]=0	---	1.5	---	A
		A6[3]=1	---	2	---	A
OTG mode over-current protection off cycle time	$t_{OTG_OCP_OFF}$		---	32	---	mS
OTG mode over-current protection on cycle time	$t_{OTG_OCP_ON}$		---	0.8	---	mS
Boost Mode Operation (Power Bank)						
PMID Regulation Voltage	$V_{PMIDPWRBNK}$	$V_{BOOST_BAT} < BAT < 4.5V$, $I(VPMID)=0$	---	5.2	---	V
PMID Short Circuit Threshold	V_{PMID_SCP}		---	1.212	---	V
Auto Power Source Detection						
DP DCD Current Source	I_{DP_SRC}		7	10	13	μ A
DM Pull Down Resistance	R_{DM_DWN}		14.25	19.5	24.8	k Ω
DP DCD Detect Voltage	V_{DP_DCD}	SDP/CDP/DCP	0.8	0.825	0.85	V
DP Source Voltage	V_{DP_SRC}	$I_{DP_SRC}=250\mu A$	0.5	0.6	0.7	V
DM Source Voltage	V_{DM_SRC}	$I_{DM_SRC}=250\mu A$				
DP Sink Current	I_{DP_SINK}		50	100	150	μ A
DM Sink Current	I_{DM_SINK}					
DP & DM Data Detect Voltage	V_{DAT_REF}		0.25	0.325	0.4	V
Data Contact Detect Debounce Time	T_{DCD_DBNC}		15	30	45	mS
DCD Time Out	T_{DCD_TO}		300	430	700	mS
DP Voltage Source ON Time	T_{VDPSRC_ON}		50	84	100	mS
DM Voltage Source ON Time	T_{VDMSRC_ON}					
DP,DM Detect Debounce Time	T_{DET_DBNC}		15	30	45	mS
Charging timer with 150mA USB host in default mode	$t_{SDP_DEFAULT}$		---	---	45	mins.

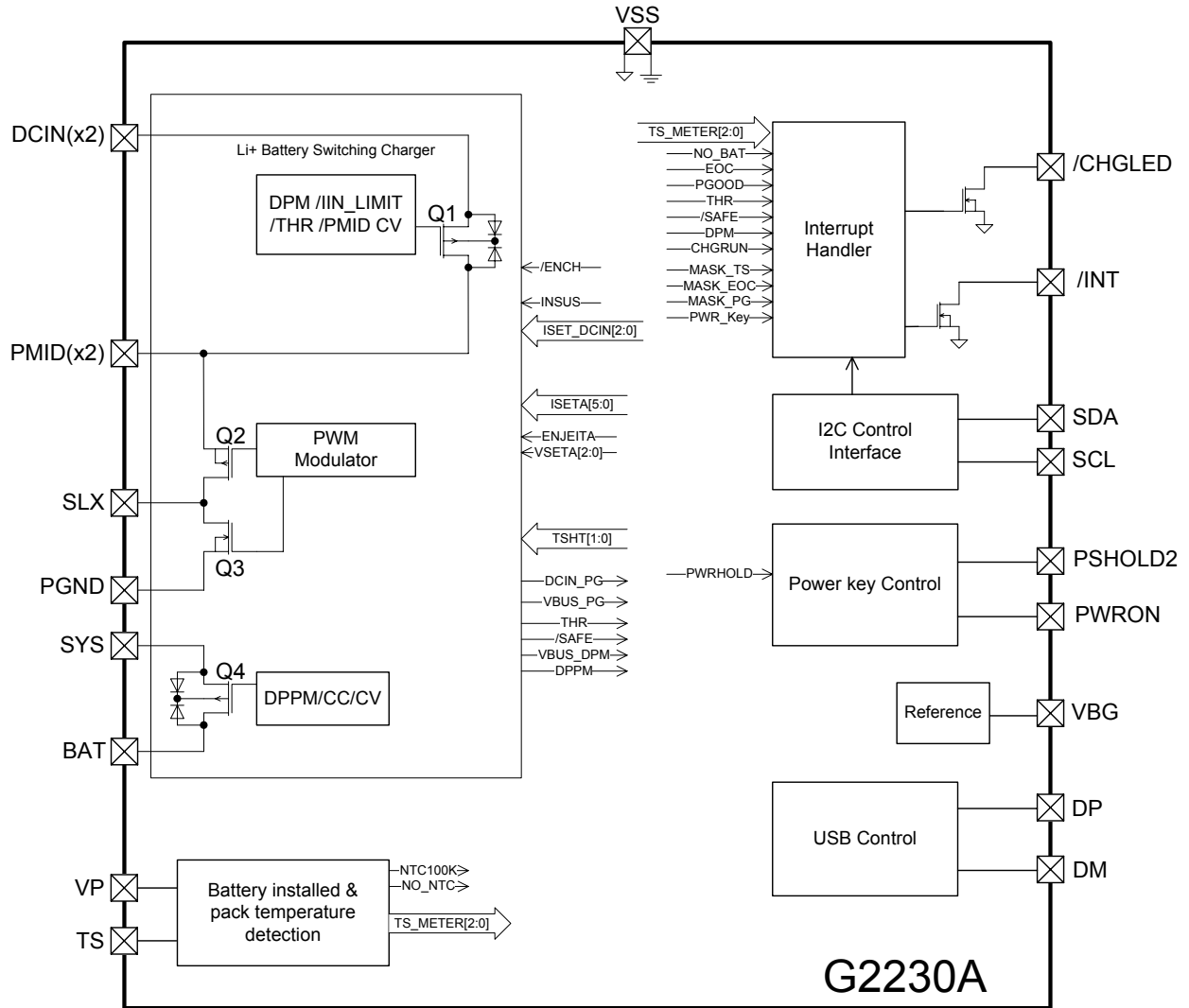
Pin Description

Pin No	Pin Name	Function
A1	PGND	Power ground of Switching Charger.
A2	SLX	Inductor switch node of Switching Charger. Connect the inductor between SLX and SYS.
A3	PMID	Power Output of DCIN and power input of Switching Charger. Bypass with at least a 10uF ceramic capacitor.
A4	DCIN	Adapter Power or USB Power Input. Bypass with a 4.7uF or greater capacitor.
B1	/INT	Interrupt Indicator with open drain output. If any toggle of events of battery installed, end of charging, DCIN power good, thermal regulation, safety timer expired, DCIN DPM, power source detection happen, the output /INT goes low.
B2	/CHGLED	Indicator of Charger status with open drain output.
B3	PMID	Power Output of DCIN and power input of Switching Charger. Bypass with at least a 10uF ceramic capacitor.
B4	DCIN	Adapter Power or USB Power Input. Bypass with a 4.7uF or greater capacitor.
C1	DM	USB input for D-.
C2	DP	USB Input for D+.
C3	PSHOLD2	PSHOLD2 is a push-pull pin which high level=V(SYS).
C4	PWRON	External switch-on control (ON button).
D1	SYS	System Supply output. Bypass with a 10uF or greater ceramic capacitor. SYS connects to BAT though an internal 20mΩ system load switch when DCIN is invalid, or when the VSYS load is greater than the input current limit.
D2	SDA	Data Input PIN of I2C interface.
D3	SCL	Clock Input PIN of I2C interface.
D4	VSS	All chip digital and analog ground.
E1	BAT	Battery Connection. Connect to a single-cell Li+ battery.
E2	TS	Battery Temperature Sense.
E3	VP	Power Output 3.0V buffer for battery temperature sense. Bypass with a 0.1uF or greater ceramic capacitor.
E4	VBG	1.21v reference voltage output. Bypass this pin to ground with a 1uF ceramic capacitor.

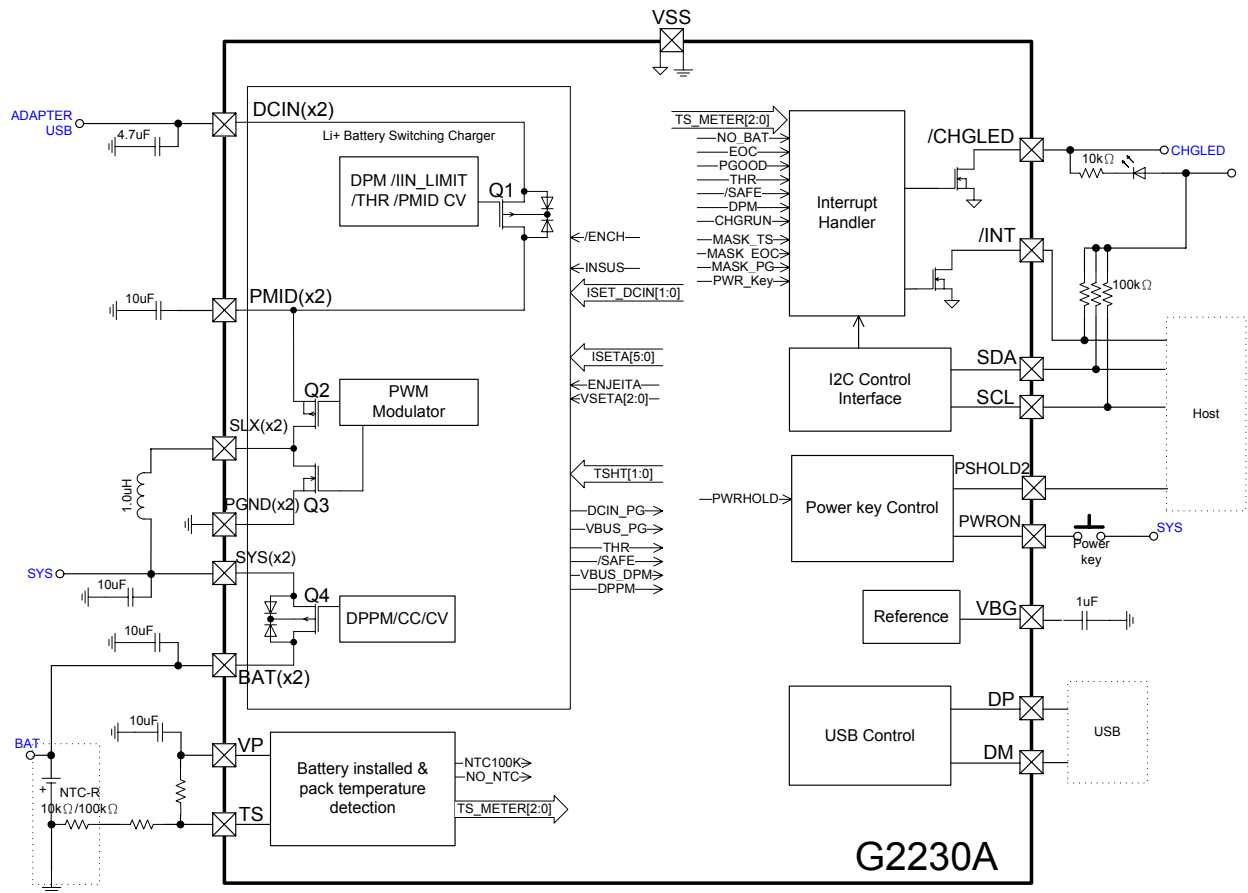
Minimum Footprint PCB Layout Section



Block Diagram



Application circuit

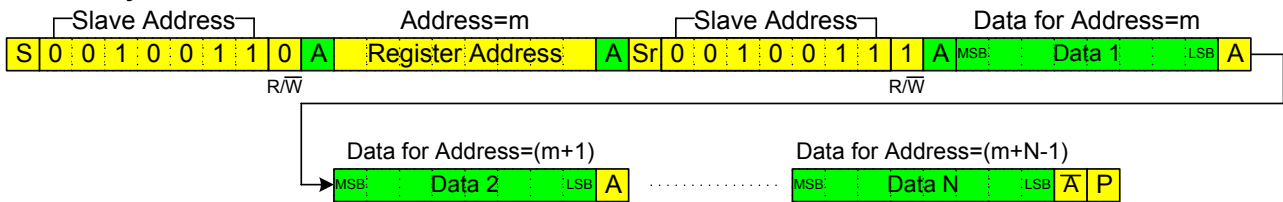


I2C Interface

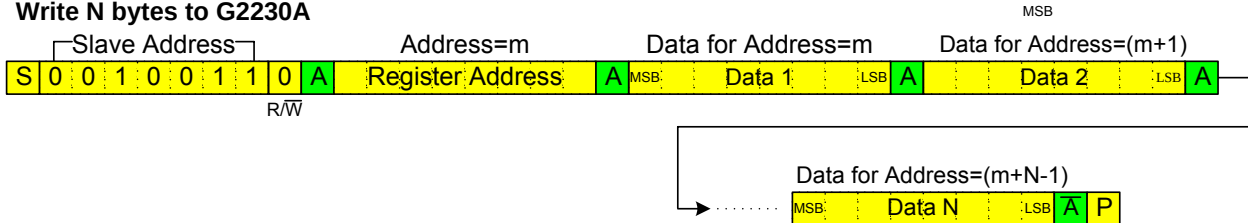
G2230A I2C slave address=7'b0010011. The write or read bit stream ($N \geq 1$) is shown below:

- Driven by Master
- S Start
- Driven by G2230A
- P Stop
- Sr Repeat Start

Read N bytes from G2230A



Write N bytes to G2230A



I2C Register Map

Address	Byte Name		Data							
			b7	b6	b5	b4	b3	b2	b1	b0
00h	A0	Meaning	CHGRST	reserved	VP_ON	ENSHIP	ENOTGI2C	/ENCHIN	ENPWRBNK	INSUS
		Default	0	0	0	0	0	0	0	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
01h	A1	Meaning	ENDPM	VINDPM<3:0>			ISET_DCIN<2:0>			
		Default	1	1	0	0	See Table Below			
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
02h	A2	Meaning	VSYSMIN<2:0>			VS2B<1:0>		reserved	VBLOW<1:0>	
		Default	1	0	1	1	0	0	1	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
03h	A3	Meaning	ISETA<5:0>						reserved	ICHGDONE
		Default	0	0	1	0	0	0	0	1
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
04h	A4	Meaning	IPRECHG<3:0>			VSETA<2:0>				VBATFC
		Default	0	0	0	1	0	1	0	1
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
05h	A5	Meaning	EN_TIMER	TIMER<1:0>		TMR2X_EN	CHGSTEN	CVCOMP<2:0>		
		Default	1	1	0	1	0	0	0	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
06h	A6	Meaning	OTGV<3:0>				I_OTG	ENTS_BOOST	reserved	reserved
		Default	0	1	1	1	1	1	0	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
07h	A7	Meaning	/ENTHR	THRREG<1:0>		CHG_2DET	CHG_1DET	EN_ILIMADJ	ENJEITA	ICHG50PCT
		Default	0	1	1	0	0	0	0	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
08h	A8	Meaning	TSCD<1:0>		TSCL<1:0>		TSWM<1:0>		TSHT<1:0>	
		Default	0	1	1	0	1	0	0	1
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
09h	A9	Meaning	/NTCDET	TSSEL	TIME_IT<1:0>		TIME_LP<1:0>		TDSIPPING<1:0>	
		Default	0	1	0	0	0	0	1	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0Ah	A10	Meaning	INT	CHGRUN	INLIMIT	THR	TS_METER<2:0>			DCDET
		Default	0	0	0	0	1	1	1	0
		Read/Write	R/W	R	R	R	R	R	R	R
0Bh	A11	Meaning	reserved	MASK_CHGRUN	MASK_INLIMIT	MASK_THR	MASK_TS	reserved	reserved	MASK_DCDET
		Default	0	1	1	0	0	0	0	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0Ch	A12	Meaning	DCIN_PG	BATLOW	NOBAT	EOC	CHGDONE	/SAFE	BST_FAULT	reserved
		Default	0	1	1	0	0	0	0	0
		Read/Write	R	R	R	R	R	R	R	R/W
0Dh	A13	Meaning	MASK_DCIN_PG	MASK_BATLOW	MASK_NOBAT	MASK_EOC	MASK_CHGDONE	MASK_SAFE	MASK_BST_FAULT	reserved
		Default	0	1	0	0	0	0	0	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0Eh	A14	Meaning	OTG_OC	PWRON_IT	PWRON_LP	reserved	reserved	reserved	reserved	reserved
		Default	0	0	0	0	0	0	0	0
		Read/Write	R	R	R	R/W	R/W	R/W	R/W	R/W
0Fh	A15	Meaning	MASK_OTG_OC	MASK_PWRON_IT	MASK_PWRON_LP	reserved	reserved	reserved	reserved	reserved
		Default	1	0	0	0	0	0	0	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
10h	A16	Meaning	CHGTYPIN<2:0>			DPM	INCC	DPPM	THSD	NTC100K
		Default	0	0	0	0	0	0	0	1
		Read/Write	R	R	R	R	R	R	R	R
11h	A17	Meaning	reserved	reserved	VER<5:0>					
		Default	0	0	0	0	0	1	0	1
		Read/Write	R/W	R/W	R	R	R	R	R	R

When A7.EN_ILIMADJ=1'b1, ISET_DCIN<2:0> default value depends on A16.CHGTYP<2:0> which is used to record the charger type.

Otherwise, ISET_DCIN<2:0> default value is 3'b001 (0.45A)

CHGTYP<2:0>	Power source Type	ISET_DCIN<2:0> default value
000	Stand Downstream Port (SDP)	001 (0.45A)
001	Reserved	111 (3.0A)
010	Reserved	111 (3.0A)
011	Reserved	111 (3.0A)
100	Reserved	111 (3.0A)
101	Reserved	111 (3.0A)
110	Charging Downstream Port (CDP)	100 (1.5A)
111	Dedicated Charging Port (DCP)	111 (3.0A)

I2C Register Group

Group A (Main Setting): A0,
 Group B (Charging Function Setting): A1, A2, A3, A4, A5, A7
 Group C (NTC-R Function Setting): A8, A9<7:6>
 Group C (Power Key and Shipping Mode Timer Setting): A9<5:0>
 Group D (OTG and Power Bank Mode Function Setting): A6 (and A4<0>)
 Group E (Status Read and /INT Mask): A10, A11, A12, A13, A14, A15, A16, A17.

DCIN UV reset: Group B. (except A2<1:0>, A4<0> and A7<4:2>)

SYS UV reset: All registers.

I2C Register Function Table

Byte Name	Data Bit	Data Name	Function Description																										
A0	b7	CHGRST	Reset condition of the registers Group B when BAT goes under BAT _{DET} (3.4V).																										
			<table><tr><td>VSYS<2.3V</td><td>DCIN<DCIN_{UV} & VBUS<VBUS_{UV}</td><td>BAT<BAT_{DET}</td><td>CHGRST</td><td>Condition of registers Group B</td></tr><tr><td>TRUE</td><td>X</td><td>X</td><td>X</td><td>Reset</td></tr><tr><td rowspan="5">FALSE</td><td>TRUE</td><td>X</td><td>X</td><td>Reset</td></tr><tr><td rowspan="4">FALSE</td><td rowspan="2">TRUE</td><td>1</td><td>Reset</td></tr><tr><td>0</td><td>NO Reset</td></tr><tr><td rowspan="2">FALSE</td><td>1</td><td>NO Reset</td></tr><tr><td>0</td><td>NO Reset</td></tr></table>	VSYS<2.3V	DCIN<DCIN _{UV} & VBUS<VBUS _{UV}	BAT<BAT _{DET}	CHGRST	Condition of registers Group B	TRUE	X	X	X	Reset	FALSE	TRUE	X	X	Reset	FALSE	TRUE	1	Reset	0	NO Reset	FALSE	1	NO Reset	0	NO Reset
			VSYS<2.3V	DCIN<DCIN _{UV} & VBUS<VBUS _{UV}	BAT<BAT _{DET}	CHGRST	Condition of registers Group B																						
			TRUE	X	X	X	Reset																						
			FALSE	TRUE	X	X	Reset																						
				FALSE	TRUE	1	Reset																						
						0	NO Reset																						
					FALSE	1	NO Reset																						
0	NO Reset																												
VP_ON	b5	VP_ON	VP_ON is used to tell G2230A that PMU is enabled. The bandgap and VP circuits will be turned on and the NTC-R temperature monitor will be activated.																										
			<table><tr><td>VP_ON</td><td>PMU status</td></tr><tr><td>0</td><td>OFF</td></tr><tr><td>1</td><td>ON</td></tr></table>	VP_ON	PMU status	0	OFF	1	ON																				
			VP_ON	PMU status																									
			0	OFF																									
1	ON																												
ENSHIP	b4	ENSHIP	ENSHIP is used to enable shipping mode. G2230A can enter shipping mode when DCIN does not exist and ENSHIP=1.																										
			ENOTGI2C	b3	ENOTGI2C	ENOTGI2C is used to set the switching charger operating in OTG mode, and delivering power to DCIN from BAT. ENOTGI2C would over-ride Charge Enable Function in /ENCHIN.																							
<table><tr><td>ENOTGI2C</td><td>OTG Mode</td></tr><tr><td>0</td><td>NO</td></tr><tr><td>1</td><td>YES</td></tr></table>	ENOTGI2C	OTG Mode				0	NO	1	YES																				
ENOTGI2C	OTG Mode																												
0	NO																												
1	YES																												
/ENCHIN	b2	/ENCHIN	Charge Enable Signal.																										
			<table><tr><td>/ENCHIN</td><td>Charge Status</td></tr><tr><td>0</td><td>Enable</td></tr><tr><td>1</td><td>Disable</td></tr></table>	/ENCHIN	Charge Status	0	Enable	1	Disable																				
			/ENCHIN	Charge Status																									
0	Enable																												
1	Disable																												
ENPWRBNK	b1	ENPWRBNK	ENPWRBNK is used to set the switching charger operating in power bank mode, and delivering power to PMID from BAT. The Q1 MOS (DCIN-PMID) is off.																										
			<table><tr><td>ENPWRBNK</td><td>Power Bank Mode</td></tr><tr><td>0</td><td>NO</td></tr><tr><td>1</td><td>YES</td></tr></table>	ENPWRBNK	Power Bank Mode	0	NO	1	YES																				
			ENPWRBNK	Power Bank Mode																									
0	NO																												
1	YES																												
INSUS	b0	INSUS	DCIN Suspend Control Input																										
			<table><tr><td>INSUS</td><td>DCIN Status</td></tr><tr><td>0</td><td>No Suspend</td></tr><tr><td>1</td><td>Suspend</td></tr></table>	INSUS	DCIN Status	0	No Suspend	1	Suspend																				
			INSUS	DCIN Status																									
0	No Suspend																												
1	Suspend																												

A1	b7	ENDPM	Enable DCIN DPM function <table><tr><td>ENDPM</td><td>DCIN DPM function</td></tr><tr><td>0</td><td>Disable</td></tr><tr><td>1</td><td>Enable</td></tr></table>	ENDPM	DCIN DPM function	0	Disable	1	Enable																																		
ENDPM	DCIN DPM function																																										
0	Disable																																										
1	Enable																																										
A1	b6~b3	VINDPM<3:0>	Setting DCIN DPM voltage. $V_{DCIN_DPM} = 3.88V + VINDPM<3:0>*80mV$ <table><tr><td>VINDPM<3:0></td><td>V_{DCIN_DPM}</td><td>VINDPM<3:0></td><td>V_{DCIN_DPM}</td><td>VINDPM<3:0></td><td>V_{DCIN_DPM}</td><td>VINDPM<3:0></td><td>V_{DCIN_DPM}</td></tr><tr><td>0000</td><td>3.88V</td><td>0100</td><td>4.2V</td><td>1000</td><td>4.52V</td><td>1100</td><td>4.84V</td></tr><tr><td>0001</td><td>3.96V</td><td>0101</td><td>4.28V</td><td>1001</td><td>4.6V</td><td>1101</td><td>4.92V</td></tr><tr><td>0010</td><td>4.04V</td><td>0110</td><td>4.36V</td><td>1010</td><td>4.68V</td><td>1110</td><td>5.0V</td></tr><tr><td>0011</td><td>4.12V</td><td>0111</td><td>4.44V</td><td>1011</td><td>4.76V</td><td>1111</td><td>5.08V</td></tr></table>	VINDPM<3:0>	V_{DCIN_DPM}	VINDPM<3:0>	V_{DCIN_DPM}	VINDPM<3:0>	V_{DCIN_DPM}	VINDPM<3:0>	V_{DCIN_DPM}	0000	3.88V	0100	4.2V	1000	4.52V	1100	4.84V	0001	3.96V	0101	4.28V	1001	4.6V	1101	4.92V	0010	4.04V	0110	4.36V	1010	4.68V	1110	5.0V	0011	4.12V	0111	4.44V	1011	4.76V	1111	5.08V
VINDPM<3:0>	V_{DCIN_DPM}	VINDPM<3:0>	V_{DCIN_DPM}	VINDPM<3:0>	V_{DCIN_DPM}	VINDPM<3:0>	V_{DCIN_DPM}																																				
0000	3.88V	0100	4.2V	1000	4.52V	1100	4.84V																																				
0001	3.96V	0101	4.28V	1001	4.6V	1101	4.92V																																				
0010	4.04V	0110	4.36V	1010	4.68V	1110	5.0V																																				
0011	4.12V	0111	4.44V	1011	4.76V	1111	5.08V																																				
A1	b2~b0	ISSET_DCIN<2:0>	Setting DCIN Current Limit Threshold. The actual input current limit is the lower of I2C and setting of ILIM pin. <table><tr><td>ISSET_DCIN<2:0></td><td>DCIN Current limit</td><td>ISSET_DCIN<2:0></td><td>DCIN Current limit</td></tr><tr><td>000</td><td>150mA</td><td>100</td><td>1.5A</td></tr><tr><td>001</td><td>450mA</td><td>101</td><td>2A</td></tr><tr><td>010</td><td>850mA</td><td>110</td><td>2.5A</td></tr><tr><td>011</td><td>1A</td><td>111</td><td>3A</td></tr></table>	ISSET_DCIN<2:0>	DCIN Current limit	ISSET_DCIN<2:0>	DCIN Current limit	000	150mA	100	1.5A	001	450mA	101	2A	010	850mA	110	2.5A	011	1A	111	3A																				
ISSET_DCIN<2:0>	DCIN Current limit	ISSET_DCIN<2:0>	DCIN Current limit																																								
000	150mA	100	1.5A																																								
001	450mA	101	2A																																								
010	850mA	110	2.5A																																								
011	1A	111	3A																																								
A2	b7~b5	VSYS_MIN<2:0>	Minimum System Voltage Limit <table><tr><td>VSYS_MIN<2:0></td><td>System Voltage limit</td><td>VSYS_MIN<2:0></td><td>System Voltage limit</td></tr><tr><td>000</td><td>3.1V</td><td>100</td><td>3.5V</td></tr><tr><td>001</td><td>3.2V</td><td>101</td><td>3.6V</td></tr><tr><td>010</td><td>3.3V</td><td>110</td><td>3.7V</td></tr><tr><td>011</td><td>3.4V</td><td>111</td><td>3.8V</td></tr></table>	VSYS_MIN<2:0>	System Voltage limit	VSYS_MIN<2:0>	System Voltage limit	000	3.1V	100	3.5V	001	3.2V	101	3.6V	010	3.3V	110	3.7V	011	3.4V	111	3.8V																				
VSYS_MIN<2:0>	System Voltage limit	VSYS_MIN<2:0>	System Voltage limit																																								
000	3.1V	100	3.5V																																								
001	3.2V	101	3.6V																																								
010	3.3V	110	3.7V																																								
011	3.4V	111	3.8V																																								
A2	b4~b3	VS2B<1:0>	VS2B<1:0> is used to set the SYS to BAT voltage. $V_{SYS}=V_{BAT}+V_{S2B}$ when $V_{BAT}+V_{S2B} >V_{SYSMIN}$. <table><tr><td>VS2B<1:0></td><td>V_{S2B}</td></tr><tr><td>00</td><td>60mV</td></tr><tr><td>01</td><td>120mV</td></tr><tr><td>10</td><td>180mV</td></tr><tr><td>11</td><td>240mV</td></tr></table>	VS2B<1:0>	V_{S2B}	00	60mV	01	120mV	10	180mV	11	240mV																														
VS2B<1:0>	V_{S2B}																																										
00	60mV																																										
01	120mV																																										
10	180mV																																										
11	240mV																																										
A2	b1~b0	VBLOW<1:0>	Setting the BAT _{LOW} threshold. <table><tr><td>VBLOW<1:0></td><td>BAT_{LOW}</td></tr><tr><td>00</td><td>3.2</td></tr><tr><td>01</td><td>3.3</td></tr><tr><td>10</td><td>3.4</td></tr><tr><td>11</td><td>3.5</td></tr></table>	VBLOW<1:0>	BAT _{LOW}	00	3.2	01	3.3	10	3.4	11	3.5																														
VBLOW<1:0>	BAT _{LOW}																																										
00	3.2																																										
01	3.3																																										
10	3.4																																										
11	3.5																																										
A3	b7~b2	ISSETA<5:0>	ISSETA<5:0> is used to set the battery charge current level. The termination current limit is 10% of the programmed value. ICHG=512mA+ISSETA<5:0>*64mA, (512~4544mA), Default=1024mA (001000) ITERM=10%*ICHG																																								
A3	b0	ICHGDONE	Setting the termination current ratio. <table><tr><td>ICHGDONE</td><td>Termination Current Ratio</td></tr><tr><td>0</td><td>5%</td></tr><tr><td>1</td><td>10%</td></tr></table>	ICHGDONE	Termination Current Ratio	0	5%	1	10%																																		
ICHGDONE	Termination Current Ratio																																										
0	5%																																										
1	10%																																										

A4	b7~b4	IPRECHG <3:0>	Setting the pre-charge current limit. $I_{PRECHG} = 128mA + IPRECHG<3:0>*128mA$ <table><tr><td>IPRECHG <3:0></td><td>I_{PRECHG}</td><td>IPRECHG <3:0></td><td>I_{PRECHG}</td><td>IPRECHG <3:0></td><td>I_{PRECHG}</td><td>IPRECHG <3:0></td><td>I_{PRECHG}</td></tr><tr><td>0000</td><td>128mA</td><td>0100</td><td>640mA</td><td>1000</td><td>1152mA</td><td>1100</td><td>1664mA</td></tr><tr><td>0001</td><td>256mA</td><td>0101</td><td>768mA</td><td>1001</td><td>1280mA</td><td>1101</td><td>1792mA</td></tr><tr><td>0010</td><td>384mA</td><td>0110</td><td>896mA</td><td>1010</td><td>1408mA</td><td>1110</td><td>1920mA</td></tr><tr><td>0011</td><td>512mA</td><td>0111</td><td>1024mA</td><td>1011</td><td>1536mA</td><td>1111</td><td>2048mA</td></tr></table>	IPRECHG <3:0>	I_{PRECHG}	IPRECHG <3:0>	I_{PRECHG}	IPRECHG <3:0>	I_{PRECHG}	IPRECHG <3:0>	I_{PRECHG}	0000	128mA	0100	640mA	1000	1152mA	1100	1664mA	0001	256mA	0101	768mA	1001	1280mA	1101	1792mA	0010	384mA	0110	896mA	1010	1408mA	1110	1920mA	0011	512mA	0111	1024mA	1011	1536mA	1111	2048mA
IPRECHG <3:0>	I_{PRECHG}	IPRECHG <3:0>	I_{PRECHG}	IPRECHG <3:0>	I_{PRECHG}	IPRECHG <3:0>	I_{PRECHG}																																				
0000	128mA	0100	640mA	1000	1152mA	1100	1664mA																																				
0001	256mA	0101	768mA	1001	1280mA	1101	1792mA																																				
0010	384mA	0110	896mA	1010	1408mA	1110	1920mA																																				
0011	512mA	0111	1024mA	1011	1536mA	1111	2048mA																																				
A4	b3~b1	VSETA<2:0>	VSETA<2:0> is used to set the battery charge voltage level. <table><tr><td>VSETA<2:0></td><td>BAT_{REG}</td><td>VSETA<2:0></td><td>BAT_{REG}</td></tr><tr><td>000</td><td>4.1V</td><td>100</td><td>4.3V</td></tr><tr><td>001</td><td>4.15V</td><td>101</td><td>4.35V</td></tr><tr><td>010</td><td>4.2V</td><td>110</td><td>4.4V</td></tr><tr><td>011</td><td>4.25V</td><td>111</td><td>4.45V</td></tr></table>	VSETA<2:0>	BAT _{REG}	VSETA<2:0>	BAT _{REG}	000	4.1V	100	4.3V	001	4.15V	101	4.35V	010	4.2V	110	4.4V	011	4.25V	111	4.45V																				
VSETA<2:0>	BAT _{REG}	VSETA<2:0>	BAT _{REG}																																								
000	4.1V	100	4.3V																																								
001	4.15V	101	4.35V																																								
010	4.2V	110	4.4V																																								
011	4.25V	111	4.45V																																								
A4	b0	VBATFC	Setting the battery voltage threshold from pre-charge to fast charge. <table><tr><td>BATLOWV</td><td>Pre-charge to Fast charge threshold</td></tr><tr><td>0</td><td>2.8V</td></tr><tr><td>1</td><td>3.0V</td></tr></table>	BATLOWV	Pre-charge to Fast charge threshold	0	2.8V	1	3.0V																																		
BATLOWV	Pre-charge to Fast charge threshold																																										
0	2.8V																																										
1	3.0V																																										
A5	b7	EN_TIMER	Enable timers. <table><tr><td>EN_TIMER</td><td>Timers</td></tr><tr><td>0</td><td>Disable</td></tr><tr><td>1</td><td>Enable</td></tr></table>	EN_TIMER	Timers	0	Disable	1	Enable																																		
EN_TIMER	Timers																																										
0	Disable																																										
1	Enable																																										
A5	b6~b5	TIMER <1:0>	Setting Charger Safety Timer. Fast charge safety time $T_{FASTCHG}=T_{SAFE}$. Pre-Charge safety time $T_{PRECHG}=T_{SAFE}/8$. (2X during VINDPM, IINDPM, JEITA, Thermal regulation) <table><tr><td>TIMER<1:0></td><td>T_{SAFE}</td></tr><tr><td>00</td><td>5 hrs.</td></tr><tr><td>01</td><td>8 hrs.</td></tr><tr><td>10</td><td>12 hrs.</td></tr><tr><td>11</td><td>20 hrs.</td></tr></table>	TIMER<1:0>	T_{SAFE}	00	5 hrs.	01	8 hrs.	10	12 hrs.	11	20 hrs.																														
TIMER<1:0>	T_{SAFE}																																										
00	5 hrs.																																										
01	8 hrs.																																										
10	12 hrs.																																										
11	20 hrs.																																										
A5	b4	TMR2X_EN	Enable 2X extended safety timer during DPM and thermal regulation. <table><tr><td>TMR2X_EN</td><td>2X T_{SAFE}</td></tr><tr><td>0</td><td>Disable</td></tr><tr><td>1</td><td>Enable</td></tr></table>	TMR2X_EN	2X T_{SAFE}	0	Disable	1	Enable																																		
TMR2X_EN	2X T_{SAFE}																																										
0	Disable																																										
1	Enable																																										
A5	b3	CHGSTEN	CHGSTEN is used to set indication method of /CHGLED PIN. The /CHGLED pin status are based on the charger state shown below: <table><tr><td rowspan="2">Charger State</td><td>CHGSTEN=1'b1</td><td>CHGSTEN=1'b0</td></tr><tr><td>/CHGLED Status</td><td>/CHGLED Status</td></tr><tr><td>Charging Done</td><td rowspan="4">Hi-Z</td><td rowspan="4">Hi-Z</td></tr><tr><td>Recharging after Termination</td></tr><tr><td>IC Disabled or No valid VIN power</td></tr><tr><td>Battery Not Installed</td></tr><tr><td>Charging</td><td>Flash at 0.5Hz (50% Duty)</td><td>Low</td></tr><tr><td>Safety Timer Expired</td><td rowspan="3">Flash at 4Hz (50% Duty)</td><td rowspan="3">Flash at 4Hz (50% Duty)</td></tr><tr><td>Battery Pack too cold or too hot</td></tr><tr><td>Charger in Thermal Shutdown</td></tr><tr><td>Charger in Thermal Regulation</td><td></td><td></td></tr></table>	Charger State	CHGSTEN=1'b1	CHGSTEN=1'b0	/CHGLED Status	/CHGLED Status	Charging Done	Hi-Z	Hi-Z	Recharging after Termination	IC Disabled or No valid VIN power	Battery Not Installed	Charging	Flash at 0.5Hz (50% Duty)	Low	Safety Timer Expired	Flash at 4Hz (50% Duty)	Flash at 4Hz (50% Duty)	Battery Pack too cold or too hot	Charger in Thermal Shutdown	Charger in Thermal Regulation																				
Charger State	CHGSTEN=1'b1	CHGSTEN=1'b0																																									
	/CHGLED Status	/CHGLED Status																																									
Charging Done	Hi-Z	Hi-Z																																									
Recharging after Termination																																											
IC Disabled or No valid VIN power																																											
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Charging	Flash at 0.5Hz (50% Duty)	Low																																									
Safety Timer Expired	Flash at 4Hz (50% Duty)	Flash at 4Hz (50% Duty)																																									
Battery Pack too cold or too hot																																											
Charger in Thermal Shutdown																																											
Charger in Thermal Regulation																																											

A5	b2~b0	CVCOMP<2:0>	CVCOMP<2:0> is used to set the battery charge voltage compensation level. BAT_{TARGET}=BAT_{REG}+BAT_{COMP} <table><tr><th>CVCOMP<2:0></th><th>BAT_{COMP}</th><th>CVCOMP<2:0></th><th>BAT_{COMP}</th></tr><tr><td>000</td><td>0mV</td><td>100</td><td>20mV</td></tr><tr><td>001</td><td>5mV</td><td>101</td><td>25mV</td></tr><tr><td>010</td><td>10mV</td><td>110</td><td>30mV</td></tr><tr><td>011</td><td>15mV</td><td>111</td><td>40mV</td></tr></table>	CVCOMP<2:0>	BAT _{COMP}	CVCOMP<2:0>	BAT _{COMP}	000	0mV	100	20mV	001	5mV	101	25mV	010	10mV	110	30mV	011	15mV	111	40mV																				
CVCOMP<2:0>	BAT _{COMP}	CVCOMP<2:0>	BAT _{COMP}																																								
000	0mV	100	20mV																																								
001	5mV	101	25mV																																								
010	10mV	110	30mV																																								
011	15mV	111	40mV																																								
A6	b7~b4	OTGV<3:0>	Setting the OTG voltage. V_{OTG} = 4.55V + OTGV<3:0>*64mV <table><tr><th>OTGV<3:0></th><th>V_{OTG}</th><th>OTGV<3:0></th><th>V_{OTG}</th><th>OTGV<3:0></th><th>V_{OTG}</th><th>OTGV<3:0></th><th>V_{OTG}</th></tr><tr><td>0000</td><td>4.55V</td><td>0100</td><td>4.806V</td><td>1000</td><td>5.062V</td><td>1100</td><td>5.318V</td></tr><tr><td>0001</td><td>4.614V</td><td>0101</td><td>4.87V</td><td>1001</td><td>5.126V</td><td>1101</td><td>5.382V</td></tr><tr><td>0010</td><td>4.678V</td><td>0110</td><td>4.934V</td><td>1010</td><td>5.19V</td><td>1110</td><td>5.446V</td></tr><tr><td>0011</td><td>4.742V</td><td>0111</td><td>4.998V</td><td>1011</td><td>5.254V</td><td>1111</td><td>5.51V</td></tr></table>	OTGV<3:0>	V _{OTG}	OTGV<3:0>	V _{OTG}	OTGV<3:0>	V _{OTG}	OTGV<3:0>	V _{OTG}	0000	4.55V	0100	4.806V	1000	5.062V	1100	5.318V	0001	4.614V	0101	4.87V	1001	5.126V	1101	5.382V	0010	4.678V	0110	4.934V	1010	5.19V	1110	5.446V	0011	4.742V	0111	4.998V	1011	5.254V	1111	5.51V
OTGV<3:0>	V _{OTG}	OTGV<3:0>	V _{OTG}	OTGV<3:0>	V _{OTG}	OTGV<3:0>	V _{OTG}																																				
0000	4.55V	0100	4.806V	1000	5.062V	1100	5.318V																																				
0001	4.614V	0101	4.87V	1001	5.126V	1101	5.382V																																				
0010	4.678V	0110	4.934V	1010	5.19V	1110	5.446V																																				
0011	4.742V	0111	4.998V	1011	5.254V	1111	5.51V																																				
A6	b3	I_OTG	Setting the output current in OTG mode. <table><tr><th>I_OTG</th><th>OTG Output Current</th></tr><tr><td>0</td><td>1.0A</td></tr><tr><td>1</td><td>1.5A</td></tr></table>	I_OTG	OTG Output Current	0	1.0A	1	1.5A																																		
I_OTG	OTG Output Current																																										
0	1.0A																																										
1	1.5A																																										
A6	b2	ENTS_BOOST	Enable boost mode thermal protection function. <table><tr><th>ENTS_BOOST</th><th>Boost mode thermal protection</th></tr><tr><td>0</td><td>Disable</td></tr><tr><td>1</td><td>Enable</td></tr></table>	ENTS_BOOST	Boost mode thermal protection	0	Disable	1	Enable																																		
ENTS_BOOST	Boost mode thermal protection																																										
0	Disable																																										
1	Enable																																										
A7	b7	/ENTHR	Enable thermal regulation function. <table><tr><th>/ENTHR</th><th>Thermal regulation function</th></tr><tr><td>0</td><td>Enable</td></tr><tr><td>1</td><td>Disable</td></tr></table>	/ENTHR	Thermal regulation function	0	Enable	1	Disable																																		
/ENTHR	Thermal regulation function																																										
0	Enable																																										
1	Disable																																										
A7	b6~b5	THRREG<1:0>	Thermal Regulation Threshold <table><tr><th>THRREG<1:0></th><th>Thermal Regulation Threshold</th></tr><tr><td>00</td><td>60°C</td></tr><tr><td>01</td><td>80°C</td></tr><tr><td>10</td><td>100°C</td></tr><tr><td>11</td><td>120°C</td></tr></table>	THRREG<1:0>	Thermal Regulation Threshold	00	60°C	01	80°C	10	100°C	11	120°C																														
THRREG<1:0>	Thermal Regulation Threshold																																										
00	60°C																																										
01	80°C																																										
10	100°C																																										
11	120°C																																										
A7	b4	CHG_2DET	CHG_2DET is used to enable the secondary detection of charger type. <table><tr><th>CHG_2DET</th><th>Secondary Detection</th></tr><tr><td>0</td><td>Disable</td></tr><tr><td>1</td><td>Enable</td></tr></table>	CHG_2DET	Secondary Detection	0	Disable	1	Enable																																		
CHG_2DET	Secondary Detection																																										
0	Disable																																										
1	Enable																																										
A7	b3	CHG_1DET	CHG_1DET is used to enable the primary detection of charger type. <table><tr><th>CHG_1DET</th><th>Primary Detection</th></tr><tr><td>0</td><td>Disable</td></tr><tr><td>1</td><td>Enable</td></tr></table>	CHG_1DET	Primary Detection	0	Disable	1	Enable																																		
CHG_1DET	Primary Detection																																										
0	Disable																																										
1	Enable																																										
A7	b2	EN_ILIMADJ	EN_ILIMADJ is used to enable the function which automatically adjusts A1.ISET_DCIN value according to the USB detection result. When EN_ILIMADJ=1'b1, A1. ISET_DCIN will be set to corresponding value after USB detection completed. <table><tr><th>EN_ILIMADJ</th><th>A1.ISET_DCIN</th></tr><tr><td>0</td><td>Keep value.</td></tr><tr><td>1</td><td>Adjusted to corresponding value automatically.</td></tr></table>	EN_ILIMADJ	A1.ISET_DCIN	0	Keep value.	1	Adjusted to corresponding value automatically.																																		
EN_ILIMADJ	A1.ISET_DCIN																																										
0	Keep value.																																										
1	Adjusted to corresponding value automatically.																																										

A7	b1	ENJEITA	ENJEITA is used to enable the JEITA function. When ENJEITA=1'b1, A8.TSHT<1:0>, A8.TSWM<1:0>, A8.TSCL<1:0>, A8.TSCD<1:0> are set to 8'b1110,1001 and cannot be changed by user. <table><tr><th rowspan="2">ENJEITA</th><th colspan="5">Charging condition</th></tr><tr><th>T<TSCD</th><th>TSCD<T<TSCL</th><th>TSCL<T<TSWM</th><th>TSWM<T<TSHT</th><th>T>TSHT</th></tr><tr><td>0</td><td>Stop Chg.</td><td>BAT_{REG} I_{CHG}</td><td>BAT_{REG} I_{CHG}</td><td>BAT_{REG} I_{CHG}</td><td>Stop Chg.</td></tr><tr><td>1</td><td>T<0°C Stop Chg.</td><td>0°C<T<10°C BAT_{REG}-0.15V I_{CHG}X0.5</td><td>15°C<T<45°C BAT_{REG} I_{CHG}</td><td>45°C<T<60°C BAT_{REG}-0.15V I_{CHG}X0.5</td><td>T>60°C Stop Chg.</td></tr></table>	ENJEITA	Charging condition					T<TSCD	TSCD<T<TSCL	TSCL<T<TSWM	TSWM<T<TSHT	T>TSHT	0	Stop Chg.	BAT _{REG} I _{CHG}	BAT _{REG} I _{CHG}	BAT _{REG} I _{CHG}	Stop Chg.	1	T<0°C Stop Chg.	0°C<T<10°C BAT _{REG} -0.15V I _{CHG} X0.5	15°C<T<45°C BAT _{REG} I _{CHG}	45°C<T<60°C BAT _{REG} -0.15V I _{CHG} X0.5	T>60°C Stop Chg.
ENJEITA	Charging condition																									
	T<TSCD	TSCD<T<TSCL	TSCL<T<TSWM	TSWM<T<TSHT	T>TSHT																					
0	Stop Chg.	BAT _{REG} I _{CHG}	BAT _{REG} I _{CHG}	BAT _{REG} I _{CHG}	Stop Chg.																					
1	T<0°C Stop Chg.	0°C<T<10°C BAT _{REG} -0.15V I _{CHG} X0.5	15°C<T<45°C BAT _{REG} I _{CHG}	45°C<T<60°C BAT _{REG} -0.15V I _{CHG} X0.5	T>60°C Stop Chg.																					
A7	b0	ICHG50PCT	Setting the battery charge current level to 50% of full scale. <table><tr><th>ICHG50PCT</th><th>ICHG</th></tr><tr><td>0</td><td>ICHG=A3<7:2> programmed</td></tr><tr><td>1</td><td>ICHG=50%*A3<7:2> programmed</td></tr></table>	ICHG50PCT	ICHG	0	ICHG=A3<7:2> programmed	1	ICHG=50%*A3<7:2> programmed																	
ICHG50PCT	ICHG																									
0	ICHG=A3<7:2> programmed																									
1	ICHG=50%*A3<7:2> programmed																									
A8	b7~b6	TSCD<1:0>	Set TS/VP ratio to monitor battery pack temperature for COLD boundary when A7.ENJEITA=1'b0. When A7.ENJEITA=1'b1, TSCD<1:0> is set to 2'b11. <table><tr><th rowspan="2">TSCD<1:0></th><th rowspan="2">Battery Pack Temp.</th><th colspan="2">TS/VP Ratio</th></tr><tr><th>10k NTC-R</th><th>100k NTC-R</th></tr><tr><td>00</td><td>-15°C</td><td>87%</td><td>93%</td></tr><tr><td>01</td><td>-10°C</td><td>84%</td><td>90%</td></tr><tr><td>10</td><td>-5°C</td><td>81%</td><td>87%</td></tr><tr><td>11</td><td>0°C</td><td>77%</td><td>84%</td></tr></table>	TSCD<1:0>	Battery Pack Temp.	TS/VP Ratio		10k NTC-R	100k NTC-R	00	-15°C	87%	93%	01	-10°C	84%	90%	10	-5°C	81%	87%	11	0°C	77%	84%	
TSCD<1:0>	Battery Pack Temp.	TS/VP Ratio																								
		10k NTC-R	100k NTC-R																							
00	-15°C	87%	93%																							
01	-10°C	84%	90%																							
10	-5°C	81%	87%																							
11	0°C	77%	84%																							
A8	b5~b4	TSCL<1:0>	Set TS/VP ratio to monitor battery pack temperature for COOL boundary when A7.ENJEITA=1'b0. When A7.ENJEITA=1'b1, TSCL<1:0> is set to 2'b10. <table><tr><th rowspan="2">TSCL<1:0></th><th rowspan="2">Battery Pack Temp.</th><th colspan="2">TS/VP Ratio</th></tr><tr><th>10k NTC-R</th><th>100k NTC-R</th></tr><tr><td>00</td><td>0°C</td><td>77%</td><td>84%</td></tr><tr><td>01</td><td>5°C</td><td>73%</td><td>80%</td></tr><tr><td>10</td><td>10°C</td><td>69%</td><td>75%</td></tr><tr><td>11</td><td>15°C</td><td>65%</td><td>70%</td></tr></table>	TSCL<1:0>	Battery Pack Temp.	TS/VP Ratio		10k NTC-R	100k NTC-R	00	0°C	77%	84%	01	5°C	73%	80%	10	10°C	69%	75%	11	15°C	65%	70%	
TSCL<1:0>	Battery Pack Temp.	TS/VP Ratio																								
		10k NTC-R	100k NTC-R																							
00	0°C	77%	84%																							
01	5°C	73%	80%																							
10	10°C	69%	75%																							
11	15°C	65%	70%																							
A8	b3~b2	TSWM<1:0>	Set TS/VP ratio to monitor battery pack temperature for WARM boundary when A7.ENJEITA=1'b0. When A7.ENJEITA=1'b1, TSWM<1:0> is set to 2'b10. <table><tr><th rowspan="2">TSWM<1:0></th><th rowspan="2">Battery Pack Temp.</th><th colspan="2">TS/VP Ratio</th></tr><tr><th>10k NTC-R</th><th>100k NTC-R</th></tr><tr><td>00</td><td>35°C</td><td>47%</td><td>48%</td></tr><tr><td>01</td><td>40°C</td><td>43%</td><td>43%</td></tr><tr><td>10</td><td>45°C</td><td>39%</td><td>38%</td></tr><tr><td>11</td><td>50°C</td><td>35%</td><td>33%</td></tr></table>	TSWM<1:0>	Battery Pack Temp.	TS/VP Ratio		10k NTC-R	100k NTC-R	00	35°C	47%	48%	01	40°C	43%	43%	10	45°C	39%	38%	11	50°C	35%	33%	
TSWM<1:0>	Battery Pack Temp.	TS/VP Ratio																								
		10k NTC-R	100k NTC-R																							
00	35°C	47%	48%																							
01	40°C	43%	43%																							
10	45°C	39%	38%																							
11	50°C	35%	33%																							
A8	b1~b0	TSHT<1:0>	Set TS/VP ratio to monitor battery pack temperature for HOT boundary when A7.ENJEITA=1'b0. When A7.ENJEITA=1'b1, TSHT<1:0> is set to 2'b01. <table><tr><th rowspan="2">TSHT<1:0></th><th rowspan="2">Battery Pack Temp.</th><th colspan="2">TS/VP Ratio</th></tr><tr><th>10k NTC-R</th><th>100k NTC-R</th></tr><tr><td>00</td><td>55°C</td><td>32%</td><td>29%</td></tr><tr><td>01</td><td>60°C</td><td>29%</td><td>25%</td></tr><tr><td>10</td><td>65°C</td><td>26%</td><td>22%</td></tr><tr><td>11</td><td>70°C</td><td>23%</td><td>19%</td></tr></table>	TSHT<1:0>	Battery Pack Temp.	TS/VP Ratio		10k NTC-R	100k NTC-R	00	55°C	32%	29%	01	60°C	29%	25%	10	65°C	26%	22%	11	70°C	23%	19%	
TSHT<1:0>	Battery Pack Temp.	TS/VP Ratio																								
		10k NTC-R	100k NTC-R																							
00	55°C	32%	29%																							
01	60°C	29%	25%																							
10	65°C	26%	22%																							
11	70°C	23%	19%																							

A9	b7	/NTCDET	/NTCDET bit is used to disable the auto battery NTC-R type detection. The TS/VP threshold of Battery pack temperature monitor is auto adjusted by the NTC-R type detection result if the /NTCDET bit is 1'b0. Otherwise, the TS/VP threshold is decided by the register bit A9.TSSEL. <table><tr><td>/NTCDET</td><td>Auto NTC-R Type Detection</td></tr><tr><td>0</td><td>Enable</td></tr><tr><td>1</td><td>Disable</td></tr></table>	/NTCDET	Auto NTC-R Type Detection	0	Enable	1	Disable				
/NTCDET	Auto NTC-R Type Detection												
0	Enable												
1	Disable												
A9	b6	TSSEL	TSSEL is used to choose the set the TS/VP ratio when the register bit A9./NTCDET=1'b1. <table><tr><td>TSSEL</td><td>TS/VP ratio</td></tr><tr><td>0</td><td>10K set</td></tr><tr><td>1</td><td>100K set</td></tr></table>	TSSEL	TS/VP ratio	0	10K set	1	100K set				
TSSEL	TS/VP ratio												
0	10K set												
1	100K set												
A9	b5~b4	TIME_IT <1:0>	TIME_IT<1:0> is used to defined the PWRON rising-edge de-bouncing delay time $T_{dbPWRONF}$. When PWRON is toggled high with duration longer than $T_{dbPWRONF}$, the register A14.PWRON_IT is 1'b1. <table><tr><td>TIME_IT<1:0></td><td>$T_{dbPWRONF}$</td></tr><tr><td>00</td><td>128mS</td></tr><tr><td>01</td><td>1.0S</td></tr><tr><td>10</td><td>1.5S</td></tr><tr><td>11</td><td>2.0S</td></tr></table>	TIME_IT<1:0>	$T_{dbPWRONF}$	00	128mS	01	1.0S	10	1.5S	11	2.0S
TIME_IT<1:0>	$T_{dbPWRONF}$												
00	128mS												
01	1.0S												
10	1.5S												
11	2.0S												
A9	b3~b2	TIME_LP <1:0>	TIME_LP<1:0> is used to defined the PWRON long-press delay time $T_{dPWRONLP}$. When PWRON is toggled high with duration > $T_{dPWRONLP}$, the register A14.PWRON_LP is 1'b1. <table><tr><td>TIME_LP<1:0></td><td>$T_{dPWRONLP}$</td></tr><tr><td>00</td><td>1.0S</td></tr><tr><td>01</td><td>1.5S</td></tr><tr><td>10</td><td>2.0S</td></tr><tr><td>11</td><td>2.5S</td></tr></table>	TIME_LP<1:0>	$T_{dPWRONLP}$	00	1.0S	01	1.5S	10	2.0S	11	2.5S
TIME_LP<1:0>	$T_{dPWRONLP}$												
00	1.0S												
01	1.5S												
10	2.0S												
11	2.5S												
A9	b1~b0	TD_SHIPPING <1:0>	TD_SHIPPING<1:0> is used to defined the delay time $T_{dSHIPPING}$. G2230A enter shipping $T_{dSHIPPING}$ delay after A0.ENSHIP=1'b1 and DCINPG is invalid. <table><tr><td>TD_SHIPPING<1:0></td><td>$T_{dSHIPPING}$</td></tr><tr><td>00</td><td>1.0S</td></tr><tr><td>01</td><td>2.0S</td></tr><tr><td>10</td><td>4.0S</td></tr><tr><td>11</td><td>8.0S</td></tr></table>	TD_SHIPPING<1:0>	$T_{dSHIPPING}$	00	1.0S	01	2.0S	10	4.0S	11	8.0S
TD_SHIPPING<1:0>	$T_{dSHIPPING}$												
00	1.0S												
01	2.0S												
10	4.0S												
11	8.0S												
A10	b7	INT	INT is used to control the output status of /INT pin. When interrupt events happen, /INT pin goes low and the bit A10.INT is set to 1'b1. After Micro-processor write the bit to be 1'b0, /INT pin goes to high-Z state. <table><tr><td>INT</td><td>/INT Pin Status</td></tr><tr><td>0</td><td>Hi-Z</td></tr><tr><td>1</td><td>Low</td></tr></table>	INT	/INT Pin Status	0	Hi-Z	1	Low				
INT	/INT Pin Status												
0	Hi-Z												
1	Low												
A10	b6	CHGRUN	CHGRUN is used to record the Auto Power Source Detection Status. <table><tr><td>CHGRUN</td><td>APSD Status</td></tr><tr><td>0</td><td>Not running</td></tr><tr><td>1</td><td>Running</td></tr></table>	CHGRUN	APSD Status	0	Not running	1	Running				
CHGRUN	APSD Status												
0	Not running												
1	Running												
A10	b5	INLIMIT	INLIMIT is used to record DCIN Status. <table><tr><td>INLIMIT</td><td>DCIN Status</td></tr><tr><td>0</td><td>Normal</td></tr><tr><td>1</td><td>DCIN DPM or DCIN current limit</td></tr></table>	INLIMIT	DCIN Status	0	Normal	1	DCIN DPM or DCIN current limit				
INLIMIT	DCIN Status												
0	Normal												
1	DCIN DPM or DCIN current limit												
A10	b4	THR	THR show the status of thermal regulation on charger <table><tr><td>THR</td><td>Thermal Regulation Happen</td></tr><tr><td>0</td><td>NO</td></tr><tr><td>1</td><td>YES</td></tr></table>	THR	Thermal Regulation Happen	0	NO	1	YES				
THR	Thermal Regulation Happen												
0	NO												
1	YES												

A10	b3~b1	TS_METER <2:0>	Record the battery temperature by detecting the TS pin voltage. <table><tr><td>TS_METER<2:0></td><td>Battery Temp.</td></tr><tr><td>110</td><td>$T \leq T_{COLD}$</td></tr><tr><td>100</td><td>$T_{COLD} < T \leq T_{COOL}$</td></tr><tr><td>000</td><td>$T_{COOL} < T \leq T_{WARM}$</td></tr><tr><td>001</td><td>$T_{WARM} < T \leq T_{HOT}$</td></tr><tr><td>011</td><td>$T_{HOT} < T$</td></tr><tr><td>010</td><td>NTC not existed</td></tr><tr><td>111</td><td>No battery installed</td></tr></table>	TS_METER<2:0>	Battery Temp.	110	$T \leq T_{COLD}$	100	$T_{COLD} < T \leq T_{COOL}$	000	$T_{COOL} < T \leq T_{WARM}$	001	$T_{WARM} < T \leq T_{HOT}$	011	$T_{HOT} < T$	010	NTC not existed	111	No battery installed
TS_METER<2:0>	Battery Temp.																		
110	$T \leq T_{COLD}$																		
100	$T_{COLD} < T \leq T_{COOL}$																		
000	$T_{COOL} < T \leq T_{WARM}$																		
001	$T_{WARM} < T \leq T_{HOT}$																		
011	$T_{HOT} < T$																		
010	NTC not existed																		
111	No battery installed																		
A10	b0	DCDET	DCDET is used to record the power status of DCIN. <table><tr><td>DCDET</td><td>DCIN>DCIN_{UV}</td></tr><tr><td>0</td><td>NO</td></tr><tr><td>1</td><td>YES</td></tr></table>	DCDET	DCIN>DCIN _{UV}	0	NO	1	YES										
DCDET	DCIN>DCIN _{UV}																		
0	NO																		
1	YES																		
A11	b6	MASK_CHGRUN	By writing 1'b1 to MASK_CHGRUN to disable asserting /INT low when the Auto Power Source Detection status is changed.																
A11	b5	MASK_INLIMIT	By writing 1'b1 to MASK_INLIMIT to disable asserting /INT low when the DCIN Status is changed.																
A11	b4	MASK_THR	By writing 1'b1 to MASK_THR to disable asserting /INT low when the event of thermal regulation occurs or not.																
A11	b3	MASK_TS	By writing 1'b1 to MASK_TS to disable asserting /INT low when battery temp. status is changed.																
A11	b0	MASK_DCDET	By writing 1'b1 to MASK_DCDET to disable asserting /INT low when the event of DCIN detection crossing occurs or not.																
A12	b7	DCIN_PG	DCIN power status <table><tr><td>DCIN_PG</td><td>DCIN Status</td></tr><tr><td>0</td><td>Not Power Good $DCIN < \text{Max}[V_{DCUV}, (V_{BAT} + \Delta V_{ASDN1})]$ or $DCIN > V_{DCOV}$</td></tr><tr><td>1</td><td>Power Good $\text{Max}[V_{DCUV}, (V_{BAT} + \Delta V_{ASDN1})] < DCIN < V_{DCOV}$</td></tr></table>	DCIN_PG	DCIN Status	0	Not Power Good $DCIN < \text{Max}[V_{DCUV}, (V_{BAT} + \Delta V_{ASDN1})]$ or $DCIN > V_{DCOV}$	1	Power Good $\text{Max}[V_{DCUV}, (V_{BAT} + \Delta V_{ASDN1})] < DCIN < V_{DCOV}$										
DCIN_PG	DCIN Status																		
0	Not Power Good $DCIN < \text{Max}[V_{DCUV}, (V_{BAT} + \Delta V_{ASDN1})]$ or $DCIN > V_{DCOV}$																		
1	Power Good $\text{Max}[V_{DCUV}, (V_{BAT} + \Delta V_{ASDN1})] < DCIN < V_{DCOV}$																		
A12	b6	BATLOW	BATLOW is used to record the power status of BAT. <table><tr><td>BATLOW</td><td>BAT<BAT_{LOW}</td></tr><tr><td>0</td><td>NO</td></tr><tr><td>1</td><td>YES</td></tr></table>	BATLOW	BAT<BAT _{LOW}	0	NO	1	YES										
BATLOW	BAT<BAT _{LOW}																		
0	NO																		
1	YES																		
A12	b5	NOBAT	NOBAT is used to indicate whether the battery is installed. <table><tr><td>NOBAT</td><td>Battery installed</td></tr><tr><td>0</td><td>YES</td></tr><tr><td>1</td><td>NO</td></tr></table>	NOBAT	Battery installed	0	YES	1	NO										
NOBAT	Battery installed																		
0	YES																		
1	NO																		
A12	b4	EOC	EOC show the charger status. <table><tr><td>EOC</td><td>Charger Status</td></tr><tr><td>0</td><td>During Charging</td></tr><tr><td>1</td><td>Charging Done or Recharging after Termination</td></tr></table>	EOC	Charger Status	0	During Charging	1	Charging Done or Recharging after Termination										
EOC	Charger Status																		
0	During Charging																		
1	Charging Done or Recharging after Termination																		
A12	b3	CHGDONE	CHGDONE show the charger status. CHGDONE is reset by recharging. <table><tr><td>CHGDONE</td><td>Charger Status</td></tr><tr><td>0</td><td>During Charging or No Battery</td></tr><tr><td>1</td><td>Charging Done</td></tr></table>	CHGDONE	Charger Status	0	During Charging or No Battery	1	Charging Done										
CHGDONE	Charger Status																		
0	During Charging or No Battery																		
1	Charging Done																		

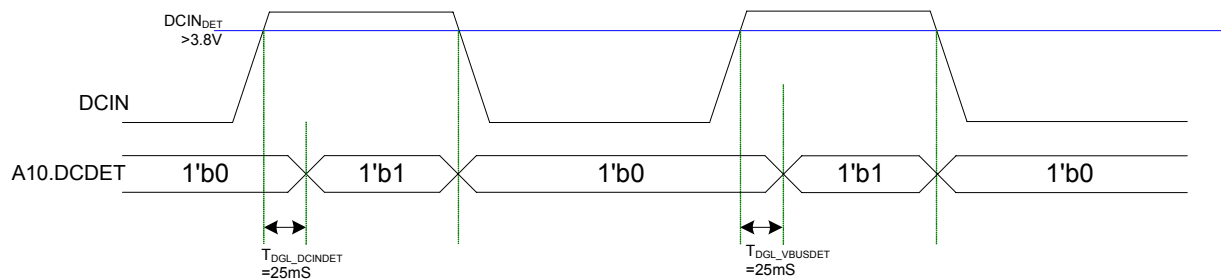
A12	b2	/SAFE	/SAFE show the status of Safety Timer.<table><tr><td>/SAFE</td><td>Safety Timer Status</td></tr><tr><td>0</td><td>No Expired</td></tr><tr><td>1</td><td>Expired</td></tr></table>	/SAFE	Safety Timer Status	0	No Expired	1	Expired
/SAFE	Safety Timer Status								
0	No Expired								
1	Expired								
A12	b1	BST_FAULT	BST_FAULT is used to indicate any fault conditions that G2230A stops switching.<table><tr><td>BST_FAULT</td><td>Boost Function Status</td></tr><tr><td>0</td><td>Normal</td></tr><tr><td>1</td><td>Stop switching (DCIN OVP in OTG mode, BAT<V_{BOOST BAT}, or Battery too hot unless A6.ENTS BOOST set to 0)</td></tr></table>	BST_FAULT	Boost Function Status	0	Normal	1	Stop switching (DCIN OVP in OTG mode, BAT<V _{BOOST BAT} , or Battery too hot unless A6.ENTS BOOST set to 0)
BST_FAULT	Boost Function Status								
0	Normal								
1	Stop switching (DCIN OVP in OTG mode, BAT<V _{BOOST BAT} , or Battery too hot unless A6.ENTS BOOST set to 0)								
A13	b7	MASK_DCIN_PG	By writing 1'b1 to MASK_DCIN_PG to disable asserting /INT low when the event of DCIN power good occurs or not.						
A13	b6	MASK_BATLOW	By writing 1'b1 to MASK_BATLOW to disable asserting /INT low when the event of low battery occurs or not.						
A13	b5	MASK_NOBAT	By writing 1'b1 to MASK_NOBAT to disable asserting /INT low when the event of no battery occurs or not.						
A13	b4	MASK_EOC	By writing 1'b1 to MASK_EOC to disable asserting /INT low when the event of end of charging occurs or not.						
A13	b3	MASK_CHGDONE	By writing 1'b1 to MASK_CHGDONE to disable asserting /INT low when the event of charge done occurs or not.						
A13	b2	MASK_SAFE	By writing 1'b1 to MASK_SAFE to disable asserting /INT low when the event of safety timer is expired occurs or not.						
A13	b1	MASK_BST_FAULT	By writing 1'b1 to MASK_BST_FAULT to disable asserting /INT low when any boost function faults occurs or not.						
A14	B7	OTG_OC	OTG_OC is used to indicate whether OTG is in OC protect (hiccup mode).<table><tr><td>OTG_OC</td><td>OTG is in OC protect (hiccup mode)</td></tr><tr><td>0</td><td>NO</td></tr><tr><td>1</td><td>YES</td></tr></table>	OTG_OC	OTG is in OC protect (hiccup mode)	0	NO	1	YES
OTG_OC	OTG is in OC protect (hiccup mode)								
0	NO								
1	YES								
A14	b6	PWRON_IT	PWRON_IT is used to record the PWRON rising status. PWRON_IT is reset to 0 when DCIN plug-in/out or A10.INT is reset to 0.<table><tr><td>PWRON_IT</td><td>T>T_{dbPWRONF}</td></tr><tr><td>0</td><td>NO</td></tr><tr><td>1</td><td>YES</td></tr></table>	PWRON_IT	T>T _{dbPWRONF}	0	NO	1	YES
PWRON_IT	T>T _{dbPWRONF}								
0	NO								
1	YES								
A14	b5	PWRON_LP	PWRON_LP is used to record the PWRON long press status. PWRON_LP is reset to 0 when DCIN plug-in/out or A10.INT is reset to 0..<table><tr><td>PWRON_LP</td><td>T>T_{dPWRONLP}</td></tr><tr><td>0</td><td>NO</td></tr><tr><td>1</td><td>YES</td></tr></table>	PWRON_LP	T>T _{dPWRONLP}	0	NO	1	YES
PWRON_LP	T>T _{dPWRONLP}								
0	NO								
1	YES								
A15	B7	MASK_OTG_OC	By writing 1'b1 to MASK_OTG_OC to disable asserting /INT low when OTG enters or leaves hiccup mode.						
A15	b6	MASK_PWRON_IT	By writing 1'b1 to MASK_PWRON_IT to disable asserting /INT low when the event of PWRON rising with duration longer than T _{dbPWRONF} occurs.						
A15	b5	MASK_PWRON_LP	By writing 1'b1 to MASK_PWRON_LP to disable asserting /INT low when the event of PWRON rising with duration longer than T _{dPWRONLP} occurs.						

A16	b7~b5	CHGTYPIN <2:0>	CHG_TYP<2:0> is used to record the charger type. <table><tr><td>CHGTYP<2:0></td><td>Power source Type</td></tr><tr><td>000</td><td>Stand Downstream Port (SDP) (0.45A)</td></tr><tr><td>001</td><td>Reserved</td></tr><tr><td>010</td><td>Reserved</td></tr><tr><td>011</td><td>Reserved</td></tr><tr><td>100</td><td>Reserved</td></tr><tr><td>101</td><td>Reserved</td></tr><tr><td>110</td><td>Charging Downstream Port (CDP) (1.5A)</td></tr><tr><td>111</td><td>Dedicated Charging Port (DCP) (3A)</td></tr></table>	CHGTYP<2:0>	Power source Type	000	Stand Downstream Port (SDP) (0.45A)	001	Reserved	010	Reserved	011	Reserved	100	Reserved	101	Reserved	110	Charging Downstream Port (CDP) (1.5A)	111	Dedicated Charging Port (DCP) (3A)
CHGTYP<2:0>	Power source Type																				
000	Stand Downstream Port (SDP) (0.45A)																				
001	Reserved																				
010	Reserved																				
011	Reserved																				
100	Reserved																				
101	Reserved																				
110	Charging Downstream Port (CDP) (1.5A)																				
111	Dedicated Charging Port (DCP) (3A)																				
A16	b4	DPM	DPM is used to record the DCIN DPM mode status <table><tr><td>DPM</td><td>DPM Status</td></tr><tr><td>0</td><td>Not in DCIN DPM Mode</td></tr><tr><td>1</td><td>In DCIN DPM Mode</td></tr></table>	DPM	DPM Status	0	Not in DCIN DPM Mode	1	In DCIN DPM Mode												
DPM	DPM Status																				
0	Not in DCIN DPM Mode																				
1	In DCIN DPM Mode																				
A16	b3	INCC	INCC is used to record the DCIN current limit status <table><tr><td>INCC</td><td>DCIN Current Limit Status</td></tr><tr><td>0</td><td>Not in DCIN current limit</td></tr><tr><td>1</td><td>In DCIN current limit</td></tr></table>	INCC	DCIN Current Limit Status	0	Not in DCIN current limit	1	In DCIN current limit												
INCC	DCIN Current Limit Status																				
0	Not in DCIN current limit																				
1	In DCIN current limit																				
A16	b2	DPPM	DPPM is used to record the SYS DPPM mode status <table><tr><td>DPPM</td><td>SYS DPPM Status</td></tr><tr><td>0</td><td>Not in SYS DPPM Mode</td></tr><tr><td>1</td><td>In SYS DPPM Mode</td></tr></table>	DPPM	SYS DPPM Status	0	Not in SYS DPPM Mode	1	In SYS DPPM Mode												
DPPM	SYS DPPM Status																				
0	Not in SYS DPPM Mode																				
1	In SYS DPPM Mode																				
A16	b1	THSD	THSD is used to record if the thermal shutdown occurs. <table><tr><td>THSD</td><td>Thermal Shutdown occurs</td></tr><tr><td>0</td><td>NO</td></tr><tr><td>1</td><td>YES</td></tr></table>	THSD	Thermal Shutdown occurs	0	NO	1	YES												
THSD	Thermal Shutdown occurs																				
0	NO																				
1	YES																				
A16	b0	NTC100K	NTC100K is used to record the resistance of the NTC thermistor. <table><tr><td>NTC100K</td><td>NTC Thermistor</td></tr><tr><td>0</td><td>10KΩ</td></tr><tr><td>1</td><td>100KΩ</td></tr></table>	NTC100K	NTC Thermistor	0	10KΩ	1	100KΩ												
NTC100K	NTC Thermistor																				
0	10KΩ																				
1	100KΩ																				
A17	b5~b0	VER<5:0>	VER<5:0> is the version code of G2230A <table><tr><td>VER<5:0></td><td>Version of G2230A</td></tr><tr><td>000101</td><td>CC</td></tr><tr><td>-</td><td>-</td></tr></table>	VER<5:0>	Version of G2230A	000101	CC	-	-												
VER<5:0>	Version of G2230A																				
000101	CC																				
-	-																				

Function Description

DCIN Power Detection

When DCIN is plugged in, and the voltage is higher than the detection threshold voltage, 3.8v(typ.), the register bit A10.DCDET is changed from 1'b0 to 1'b1. DCDET signal is asserted with deglitch time $T_{DGL_DCINDET}$ after DCIN voltage reaching its threshold voltage to eliminate any chattering on the input.



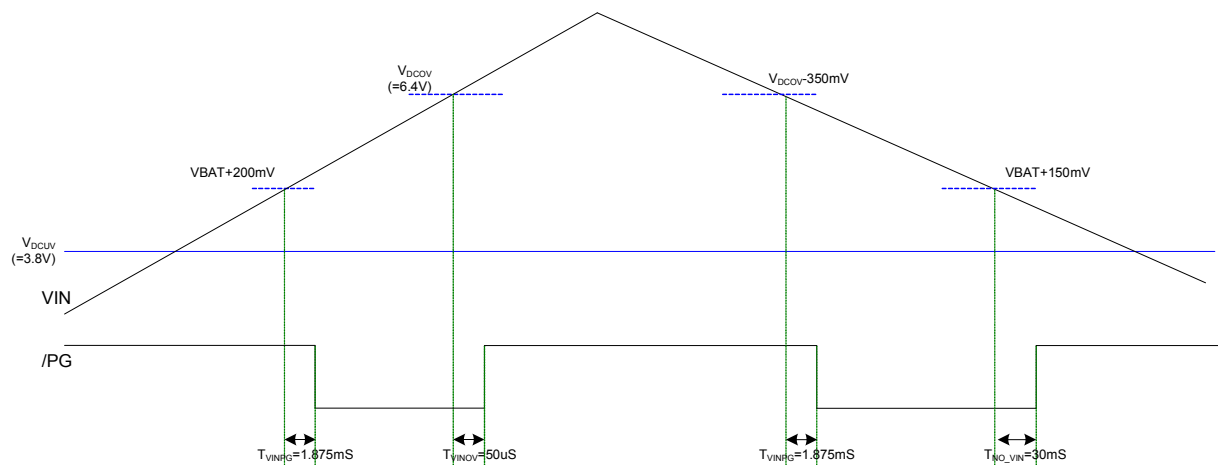
DCIN Power Good (DCIN_PG)

The register bit A12.DCIN_PG is used to indicate the DCIN voltage meets below conditions:

- ◆ $V_{DCIN} > V_{DCUV}$
- ◆ $V_{DCIN} > V_{BAT} + \Delta V_{ASDN1}$
- ◆ $V_{DCIN} < V_{DCOV}$

The condition of $V_{DCIN} > V_{BAT} + \Delta V_{ASDN1}$ is asserted with deglitch time T_{VINPG} ($=1.875mS$). After the condition is asserted, deglitch time T_{NO_VIN} ($=30mS$) is inserted.

VIN over voltage condition is asserted with deglitch time T_{VINOV} ($=50uS$). After the condition is asserted, deglitch time T_{VINPG} ($=1.875mS$) is inserted.



DCIN Over-Voltage Protection (OVP)

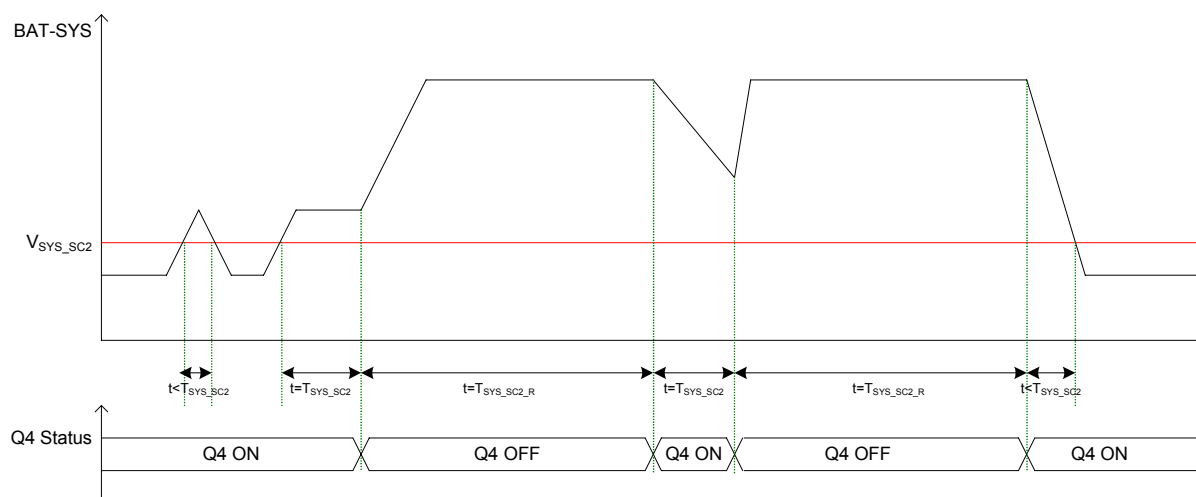
The G2230A Li-ion charger accepts DCIN input voltage up to 12V without damage. When $DCIN > V_{DCOV}$ for a period longer than T_{VINOV} , the Q1 FET that connects DCIN to PMID is OFF and the battery charging is stopped. When in DCIN OVP mode, the SYS output is connected to battery through Q4 FET is fully ON. Once the OVP function is removed, the safety timer is reset and a new charge cycle will be indicated by the /CHGLED output.

VIN Under-Voltage Lockout (UVLO)

The G2230A Li-ion charger remains in power down mode when the input voltage $DCIN$ is below the under-voltage threshold V_{DCUV} . In power down mode, the Q1 FET that connects $DCIN$ to $PMID$ is OFF, and the Q4 FET that connects BAT to SYS is ON. The V_{SYS_SCP2} circuit is active and monitors for overload conditions on SYS .

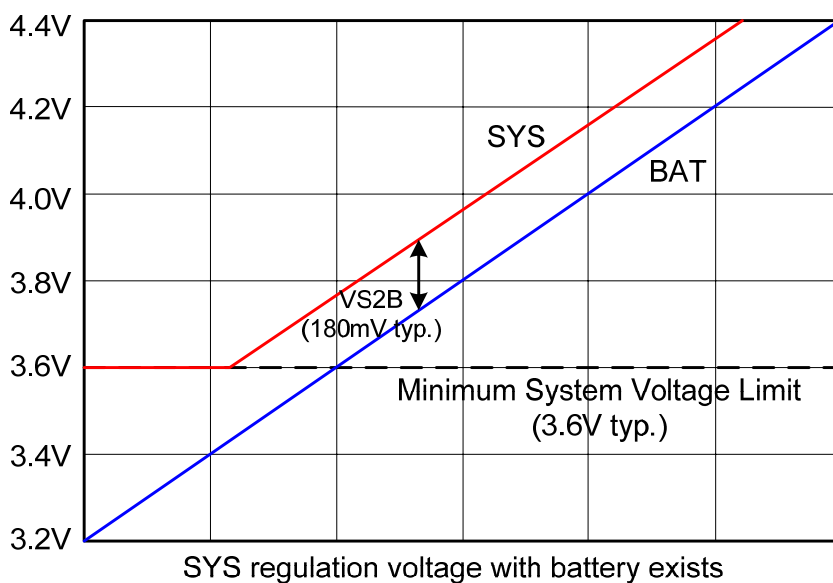
BAT to SYS Short Circuit Protection (SCP)

The V_{SYS_SC2} circuit is used for overload condition on SYS . When $(BAT-SYS) > V_{SYS_SC2}$ for a period longer than t_{SYS_SCP} , the Q4 FET that connects BAT to SYS is turned OFF and the internal recovery timer is start. After the time $t_{SYS_SCP_R}$ of the recovery timer is reached, the Q4 FET is turned ON for a period t_{SYS_SCP} to see if the overload condition is removed.



SYS voltage regulation

The PWM modulator regulates the SYS voltage depending on the BAT condition. Under no-battery condition, the SYS voltage is fixed at V_{SYS_NOBAT} . With battery exists, the SYS voltage is regulated at V_{SYS_MIN} if the BAT voltage is smaller than V_{SYS_MIN} . As the BAT voltage rises above V_{SYS_MIN} , the voltage difference between SYS and BAT is always regulated at V_{S2B} set by register A2.VS2B<1:0>.



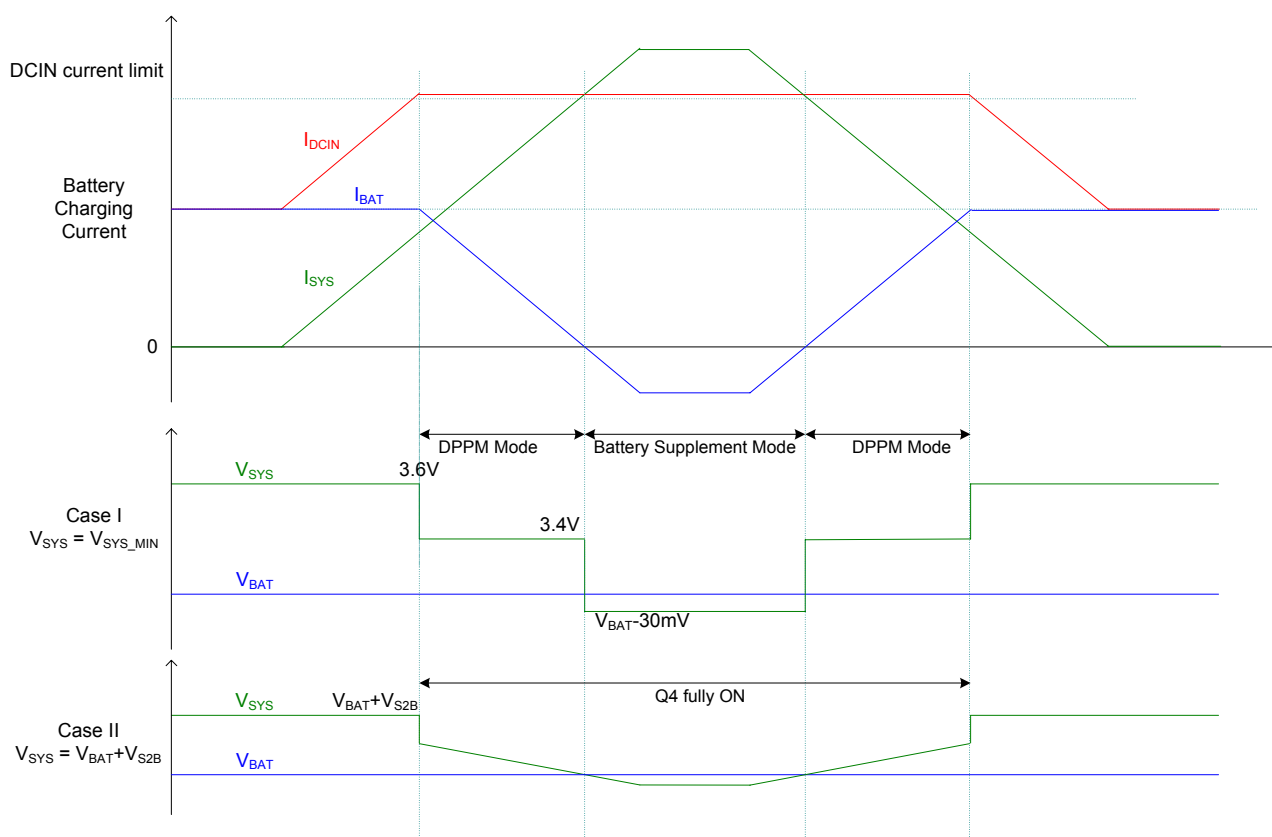
Dynamic Power Path Management

VIN-DPM mode is utilized in G2230A Li-ion charger for preventing it from crashing poorly designed or incorrectly configured DCIN power source. If DCIN voltage falls below V_{IN_DPM} (4.36V typ.), the input current limit is reduced to prevent the DCIN voltage falling further. When in VIN-DPM mode, the register A16.DPM is 1'b1.

DPPM mode is utilized in G2230A Li-ion charger to maintain SYS voltage in the increasing SYS output current. When the sum of the battery charging current and the SYS output current exceeds DCIN input current limit, the SYS voltage falls. The battery charging current is reduced to prevent the SYS voltage falling further. In DPPM mode, the battery charging termination detection is halted and the register A16.DPPM is 1'b1.

In DPPM mode, if the battery charging current is reduced to zero and the SYS output current increases beyond the DCIN input current limit, the battery supplements the SYS load. In Battery Supplement Mode, the battery charging termination detection is halted, and the register A17.BATSUP is 1'b1.

If the SYS load keeps increasing until $(BAT-SYS) > V_{SYS_SC2}$, the BAT to SYS short circuit protection is active.



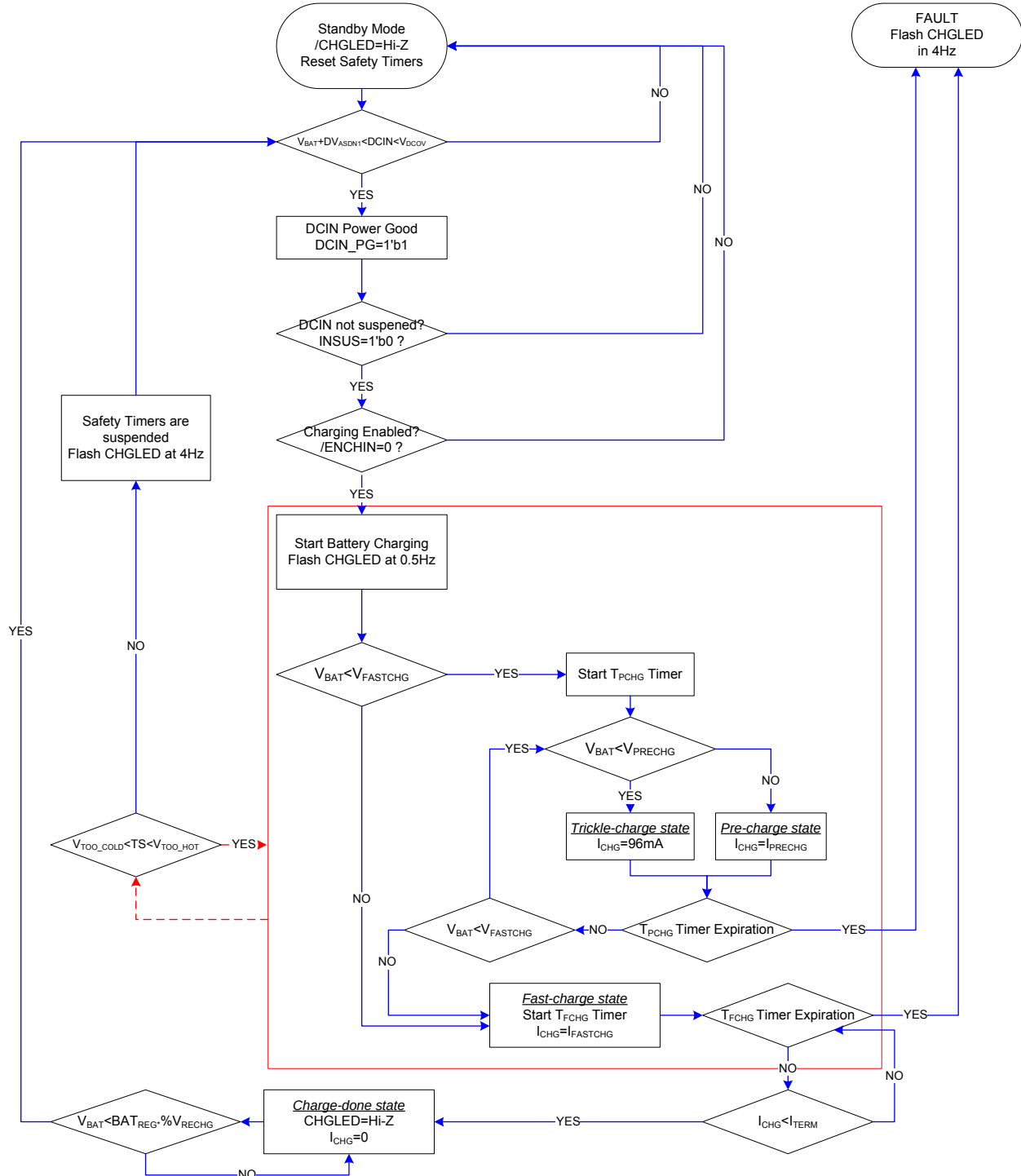
VIN Suspend Mode or VIN not Connected

When no input source is connected to DCIN or in VIN suspend mode by setting register A0.INSUS=1'b1, SYS is powered strictly from battery. During this mode, the Q4 FET that connects BAT to SYS is fully on, and the SYS voltage is not regulated, but the SYS short circuit protection is active.

Battery Charging

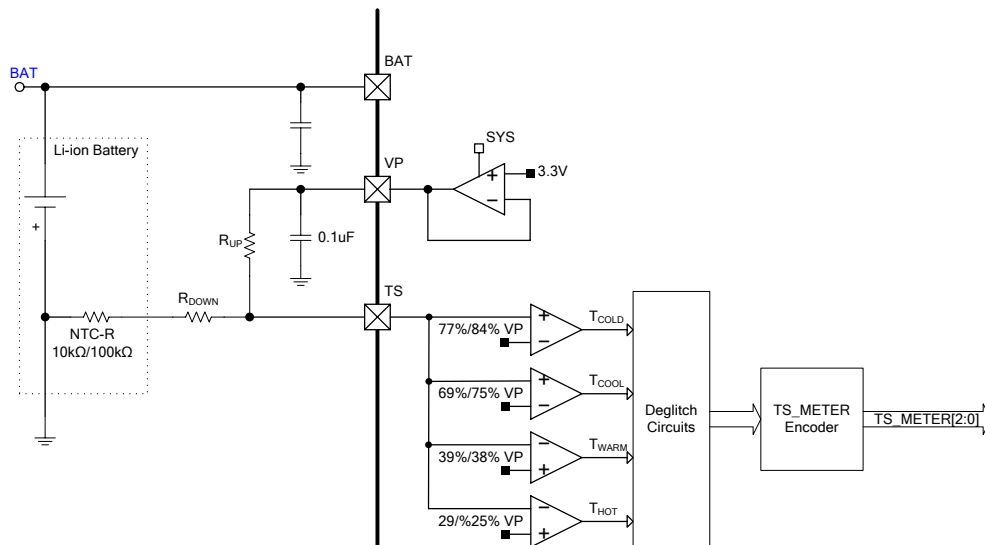
Once the DCIN power good is sustained, set /ENCH low to initiate battery charging. The battery is charged in four phases: trickle charge, pre-charge, constant current fast charge, and a constant voltage regulation. The battery charging flow chart is as below:

Battery Charging Flowchart



Battery Pack Temperature Monitoring

When G2230A detects the presence of the battery or PWRON is toggled low to pull /PMUON pin to low, the G2230A detects battery NTC-R is presented or not by detecting the voltage level of TS pin. If the voltage of TS pin is lower than 97% of VP with duration longer than t_{NO_NTC} (30ms typ.), the battery NTC-R is presented.



After the G2230A battery NTC-R detection is finished, the TS input voltage connects to the NTC thermistor in the battery pack to monitor the battery temperature and prevent over temperature condition. During charging with the voltage at TS is outside of the operating range (V_{COLD} to V_{HOT}), charging is suspended and the safety timer maintain their values but suspend counting.

The G2230A provides standard JEITA function when A7.ENJEITA=1'b1. Once the voltage at TS is inside the range (V_{COLD} to V_{COOL} and V_{WARM} to V_{HOT}), the charge current and voltage are reduced (-150mV, $I_{chg}=50\%$). The temperature thresholds and corresponding TS/VP ratios are as below (Table A):

NTC Thermistor	$T_{COLD}=0^{\circ}C$	$T_{COOL}=10^{\circ}C$	$T_{WARM}=45^{\circ}C$	$T_{HOT}=60^{\circ}C$
10K	TS/VP=77%	TS/VP=69%	TS/VP=39%	TS/VP=29%
100K	TS/VP=84%	TS/VP=75%	TS/VP=38%	TS/VP=25%

When A7.ENJEITA=1'b0, the V_{COOL} , V_{WARM} , V_{HOT} threshold can be set through I2C and the charge current and voltage will not be reduced automatically. The temperature thresholds and corresponding TS/VP ratios are as below (Table B):

NTC Thermistor	T_{COLD}	T_{COOL}	T_{WARM}	T_{HOT}
10K	Defined by A8.TSCD<1:0>	Defined by A8.TSCL<1:0>	Defined by A8.TSWM<1:0>	Defined by A8.TSHT<1:0>
100K	Defined by A8.TSCD<1:0>	Defined by A8.TSCL<1:0>	Defined by A8.TSWM<1:0>	Defined by A8.TSHT<1:0>

The G2230A supports 100k and 10k NTC thermistor, and the suggested R_{UP} and R_{DOWN} resistor values are as below:

NTC Thermistor	$R_{UP}(\Omega)$	$R_{DOWN}(\Omega)$
10K	8K	0.2K
100K	70K	1K

Choosing R_{UP} and R_{DOWN} resistors in other cases:

Follow the steps to calculate the R_{UP} and R_{DOWN} resistor values when NTC thermistor is not 10K/100K cases:

1. Get the resistance over temperature data of the NTC thermistor.
2. Choose one set of the TS/VP ratio by setting A9.TSSEL. (Remember to disable NTC-R type detection by setting A9.NTCDET to 1'b1)
3. The TS/VP ratio $= \frac{R_{NTC} + R_{DOWN}}{R_{NTC} + R_{DOWN} + R_{UP}}$.
4. Define two temperatures for two TS/VP ratio (see Table A or Table B in pg.24) and find out the R_{NTC} value from the data in step 1.
5. Use the equation in step 3 to calculate R_{UP} and R_{DOWN} .
6. After choosing the R_{UP} and R_{DOWN} , use the equation in step 3 to calculate other TS/VP ratio for different temperatures with corresponding R_{NTC} .
7. Set A8.TSHT<1:0>, A8.TSWM<1:0>, A8.TSCL<1:0> and A8.TSCD<1:0> to the TS/VP ratio needed.
8. Iterate and fit the temperature by repeating step 2-6.

Examples:

1. Get the resistance over temperature data of the NTC thermistor.
2. Choose the 10K NTC-R ratios by setting A9.TSSEL=1'b0.
3. The TS/VP ratio $= \frac{R_{NTC} + R_{DOWN}}{R_{NTC} + R_{DOWN} + R_{UP}}$.
4. Define $T_{COLD} = -5^{\circ}\text{C}$ and set TSCD<1:0>=2'b01 which TS/VP ratio is 84%. Define $T_{HOT} = 65^{\circ}\text{C}$ and from A8.TSHT the TS/VP ratio is selectable between 32%, 29%, 26%, 23%. Here choose 29% for example. From the data in step 1, the R_{NTC} are 300k Ω and 5k Ω respectively.
5. Use the equation in step 3, the R_{UP} and R_{DOWN} equals 61k Ω and 20k Ω respectively.
6. Define $T_{WARM} = 40^{\circ}\text{C}$ and $T_{COOL} = 15^{\circ}\text{C}$, where the R_{NTC} are 20k Ω and 100k Ω from data in step 1. Use the equation and get the TS/VP ratio are 40% and 66% respectively.
7. From A8.TSCL and A8.TSWM, set the A8.TSCL=2'b11(65%) and A8.TSWM=2'b10(39%).
8. Done.

Battery Detection

The battery detection function is active once the battery charging is initiate. G2230A detects the existance of the battery with two phases, Charge-Done phase and Re-Charge phase. The Charge-Done phase is triggered by the charge termination signal I_{TERM} . At the same time, a detection timer is started and a small current is introduced to pull down the BAT voltage. If the BAT voltage does NOT reach the re-charge level ($BAT_{REG} * \%V_{RECHG}$) within the time $T_{nobatchk}$ of the timer, the battery is presented and the register A12.NOBAT is set to 1'b0. The Re-Charge phase, on the other hand, is triggered by the re-charge signal. The detection timer is started and the new charging period will charge up the BAT voltage. If the charge current does NOT reach the termination level within the time $T_{nobatchk}$ of the timer, the battery is presented and the register A12.NOBAT is set to 1'b0. The register A12.NOBAT is set to 1'b1 only if both the two phases determine that the battery is not exist. To detect the absence of the battery correctly, the capacitance at the BAT pin without battery must be smaller than 75uF.

Thermal Regulation Loop and Thermal Shutdown

The G2230A contain a thermal regulation loop that monitors the die temperature. If the temperature heat up, the thermal regulation loop reduces the DCIN input current to maintain the die temperature less than THM_{REG} (120 $^{\circ}\text{C}$ typ.). The battery termination detection is disabled when thermal regulation loop is active.

Despite the operation of the thermal loop, the die temperature continues to rise above THM_{SD} (155 $^{\circ}\text{C}$ typ.) in some cases, the FET Q1 connects DCIN to PMID is turned OFF, and G2230A charger enters Battery Supplement Mode to ensure that the battery powers the load on SYS.

Safety Timer

The G2230A charger contains an internal safety timer for the trickle charge, pre-charge, fast-charge phases to prevent potential damage to the battery and the system. The timer value of the fast-charge phase is programmed by the register TIMER[3:0] through I²C control, and the timer value of trickle charge and pre-charge is 1/8 of the fast-charge timer value. See details in the Register Function Table. When the temperature of the battery pack monitored by the NTC thermistor through TS pin is out of the operating range (0°C<T<60°C), the safety timer maintains the timer value but suspends the counting. Once the temperature is back in the operating range, the safety timer resumes from the timer value maintained previously. If the register A5.TMR2X_EN is set to 1'b1, the safety timer counts at half clock rate when the following conditions occurs:

- ◆ DCIN DPM
- ◆ DCIN current limit
- ◆ JEITA function expired.
- ◆ Thermal regulation
- ◆ Register A7.ICHG50PCT is set to 1'b1

Once the safety timer is expired, the G2230A latches off the charging progress, and the latch can be reset by these conditions shown below:

- ◆ Remove DCIN
- ◆ Remove Battery
- ◆ Write /ENCHIN=1'b1 or INSUS=1'b0 through I²C interface

/CHGLED Indicator

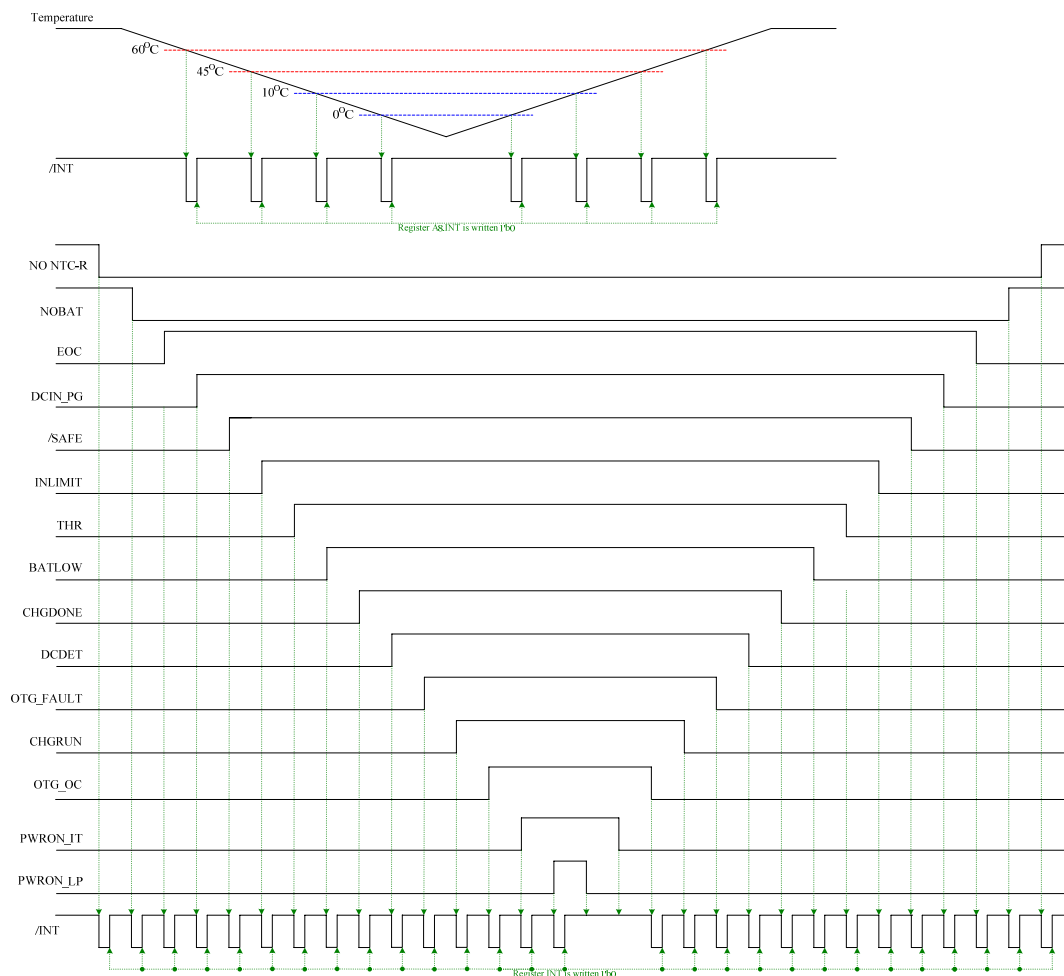
The open-drain CHGLED output indicates various charger operations, and the indication method is controlled by the register CHGSTEN through I²C interface.

Charger State	CHGLED Status	
	CHGSTEN=1'b1	CHGSTEN=1'b0
Charging Done	Hi-Z	Hi-Z
Recharging after Termination		
IC Disabled or No valid VIN power		
Battery Not Installed		
Charging	Flash at 0.5Hz	Low
Safety Timer Expired	Flash at 4Hz	Flash at 4Hz
Battery Pack too cold or too hot		
Charger in Thermal Shutdown		
Charger in Thermal Regulation		

/INT, Interrupt Signal

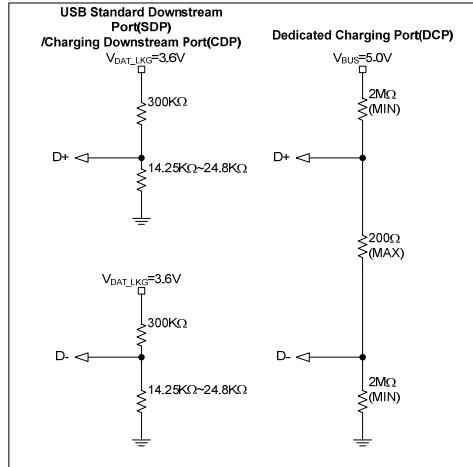
The G2230A indicates interrupt signal to external processor by /INT open-drain output. /INT is toggled low and INT bit is set to 1'b1 when these conditions shown below happen. After /INT is toggled low in these conditions, /INT is toggled high by written INT bit 1'b0 through I²C interface.

/INT Toggle Low	Event Appear	Event Disappear
JEITA Temperature Limit	YES	YES
NTC-R Not Installed (TS > 97% VP)	YES	YES
Battery Not Installed (NOBAT)	YES	YES
End of Charging (EOC)	YES	YES
DCIN Power Good (DCIN_PG)	YES	YES
Safety Timer Expired (/SAFE)	YES	YES
VIN DPM or VIN current limit is active (INLIMIT)	YES	YES
Thermal Regulation is active (THR)	YES	YES
Low Battery (BATLOW)	YES	YES
Charging Done (CHGDONE)	YES	YES
VIN is valid (DCDET)	YES	YES
BOOST fault situations (BST_FAULT)	YES	YES
Auto Power Source Detection is active (CHGRUN)	YES	YES
OTG is in OC protect (hiccup mode) (OTG_OC)	YES	YES
PWRON falling-edge de-bouncing (PWRON_IT)	YES	NO
PWRON long press (PWRON_LP)	YES	NO



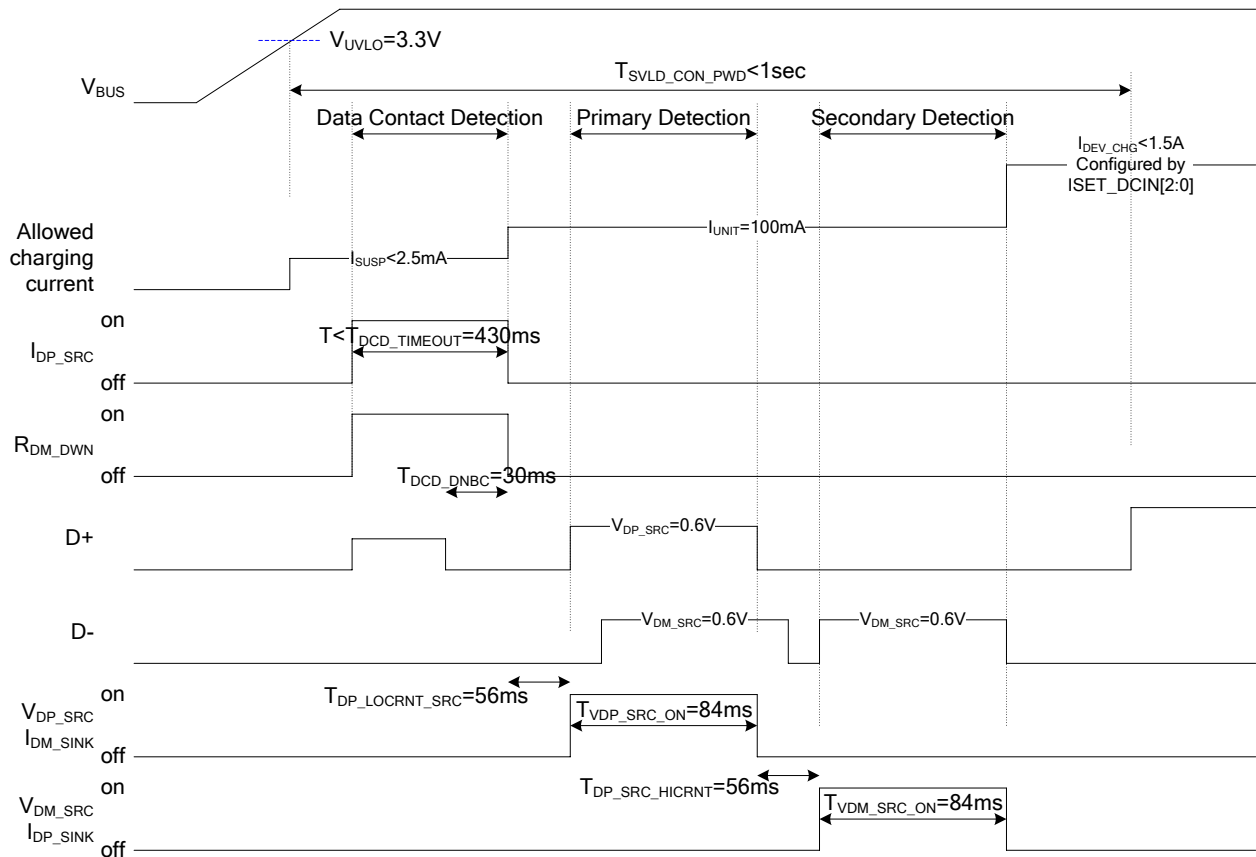
USB Charger Detection

The G2230A has USB charger detection circuit compliant with USB Battery Charging Revision 1.2. The USB charger detection circuit detects USB standard downstream port (SDP), USB charging downstream port (CDP) and dedicated charging port (DCP) to control the Li-ion battery charger. The downstream port topology is shown below:

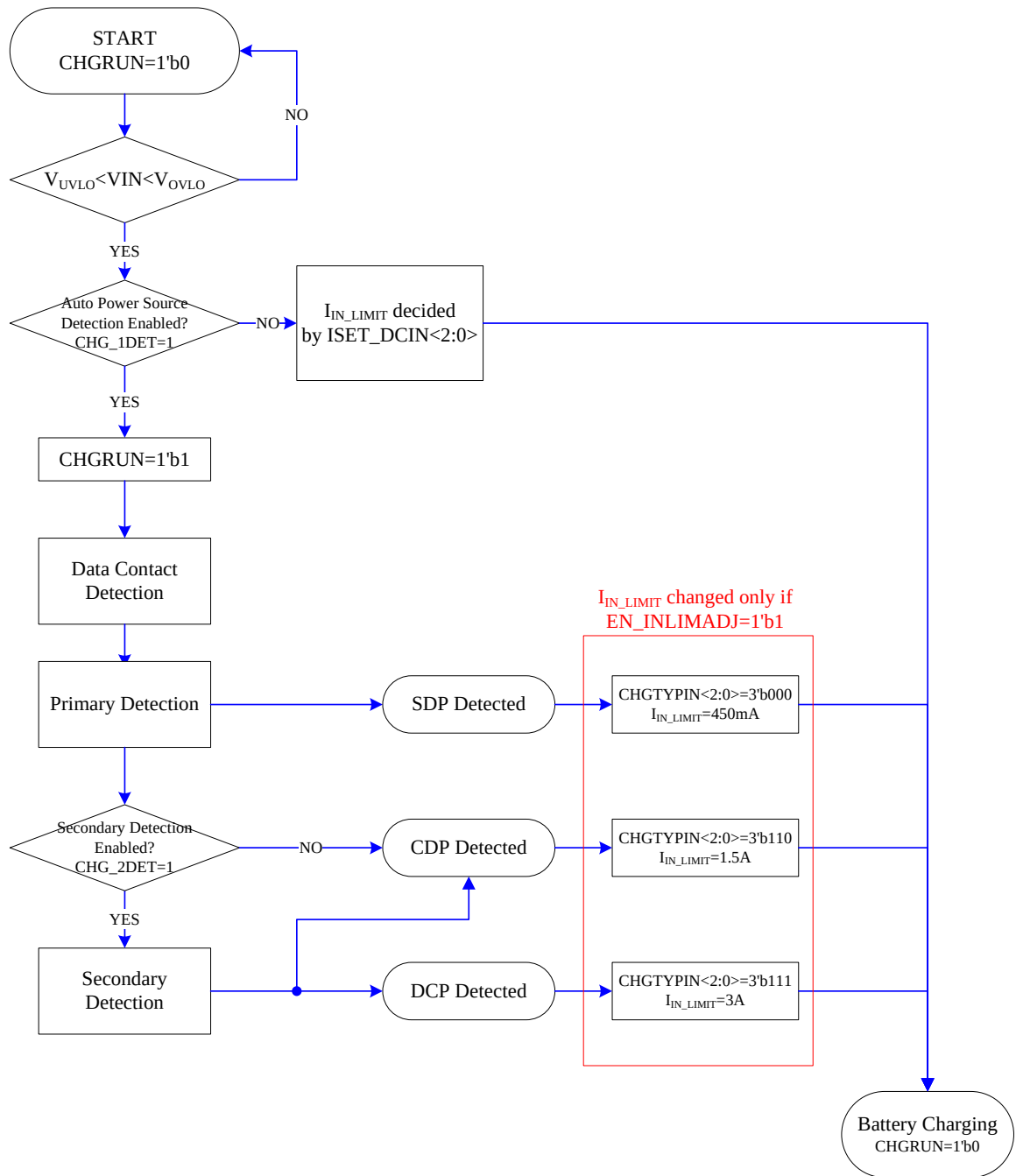


After VIN exceeds VIN_{UVLO}, USB detection sequence starts with three phases: Data Contact Detection (DCD), Primary Detection, and Secondary Detection. See the flow chart and the timing sequence of CDP detection in details.

Auto Power Source Detection Timing of CDP



Auto Power Source Detection Flowchart



Boost Mode Operation (OTG or Power Bank Mode)

The G2230A supports boost operation mode which converts the battery voltage (2.6V to 4.5V) to DCIN (5V) in OTG Mode or to PMID (5.2V) in Power Bank Mode. The Boost Mode is activated under either of the following cases:

Case 1 (OTG Mode): A0.ENOTGI2C is set to 1'b1.

Case 2 (Power Bank Mode): A0.ENPWRBNK is set to 1'b1 and $DCIN < (BAT + \Delta V_{ASDN1})$.

G2230A leaves Boost Mode if both of the two cases are invalid. Note that Case 2 (Power Bank Mode) overrides Case 1 (OTG Mode).

In Boost Mode, G2230A will stop charging and the converter is transformed into a boost converter. The boost converter starts to switch after 30ms delay from all the following conditions are valid:

- ◆ BAT voltage is larger than VBATFC threshold (set by A4.VBATFC).
- ◆ DCIN is less than DCIN automatic shutdown threshold ($=BAT + \Delta V_{ASDN1}$).
- ◆ The battery temperature is within the operating range (V_{COLD} to V_{HOT}) unless A6.ENTS_BOOST is set to 1'b0 to disable this thermal protection function.

The boost converter stops switching (but still in Boost Mode) if one of the following conditions is valid:

- ◆ BAT voltage falls below VBATFC threshold (set by A4.VBATFC).
- ◆ DCIN over-voltage. ($DCIN > V_{DCOV}$) (for OTG Mode)
- ◆ The battery temperature is without the operating range (V_{COLD} to V_{HOT}) unless A6.ENTS_BOOST is set to 1'b0 to disable this thermal protection function.

OTG Mode Operation for DCIN

When A0.ENOTGI2C=1'b1 and A0.ENPWRBNK=1'b0, G2230A is in OTG Mode. The FET Q1 connects DCIN to PMID and FET Q4 connects BAT to SYS are fully turned on. The converter boosts the voltage from BAT to DCIN and delivers current to support other USB OTG devices connects to the USB connector.

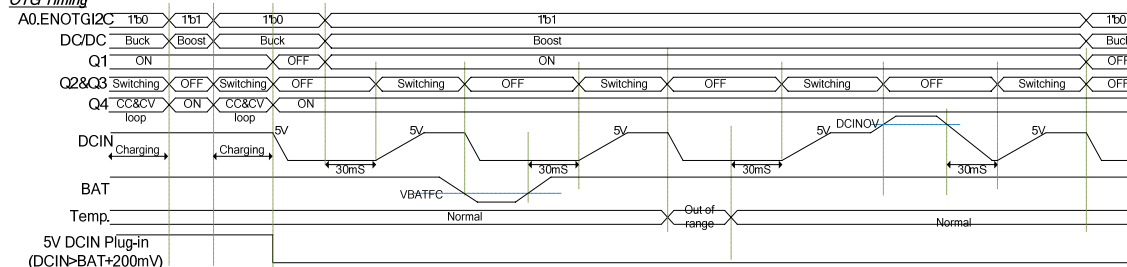
Over-Current Protection in OTG Mode

G2230A monitors the currents of the FET Q1 connects DCIN to PMID for over-current protection in OTG Mode. During over-current condition, G2230A operates in hiccup mode by turning off FET Q1 for $t_{OTG_OCP_OFF}$ (32ms typ.) and turning on FET Q1 for $t_{OTG_OCP_ON}$ (0.8ms typ.) to restart. If the over-current condition is removes, G2230A goes back to normal OTG Mode operation.

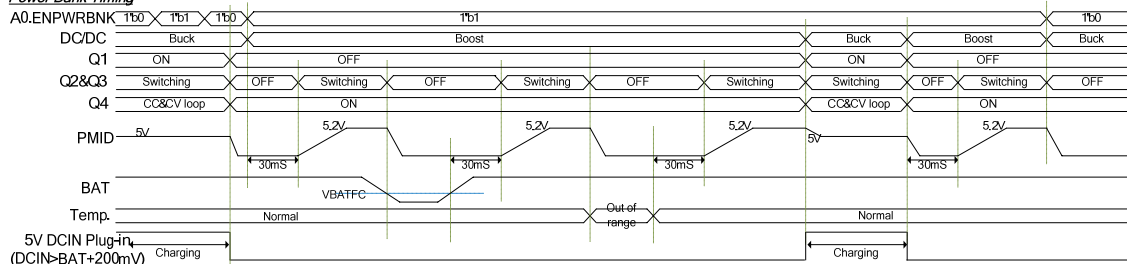
Power Bank Mode Operation for PMID

When A0.ENPWRBNK=1'b1 and $DCIN < (BAT + \Delta V_{ASDN1})$, G2230A is in Power Bank Mode. The FET Q1 connects DCIN to PMID is turned off and FET Q4 connects BAT to SYS are fully turned on. The converter boosts the voltage from BAT to PMID (5.2V).

OTG Timing



Power Bank Timing



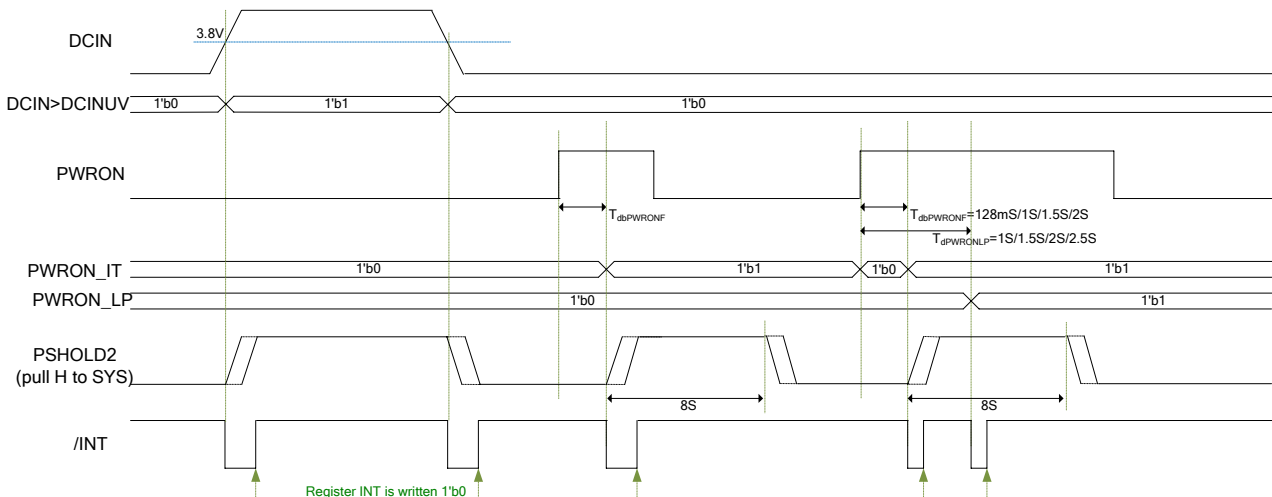
PSHOLD2 Power ON/OFF Initiation

The following conditions are available to pull the PSHOLD2 pin high to SYS voltage:

- DCIN > DCINUV
- PWRON high-level pressed with duration longer than $T_{dbPWRONF}$ or $T_{dbPWRONLP}$

When the PSHOLD2 pin is pulled high by PWRON high-level pressed, it will be pulled low again after 8S delay even if the short press or long press events triggered again within 8S.

DCIN Plug-in, PWRON Key-pressed Start-up Timing



Shipping Mode

In order to extend the battery life during shipping or storage, G2230A can turn off FET Q4 so that the SYS voltage drops to zero to minimize the current consumed from the battery.

To enter shipping mode, set the register A0.ENSHIP to 1'b1. Once the DCINPG is invalid, the FET Q4 will be turned off and G2230A enters shipping mode after $T_{dSHIPPING}$ delay

The following conditions are available to exit shipping mode and turn FET Q4 back on:

- DCIN plug-in
- PWRON low-level pressed

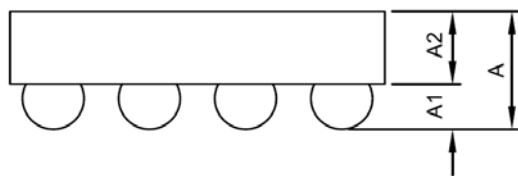
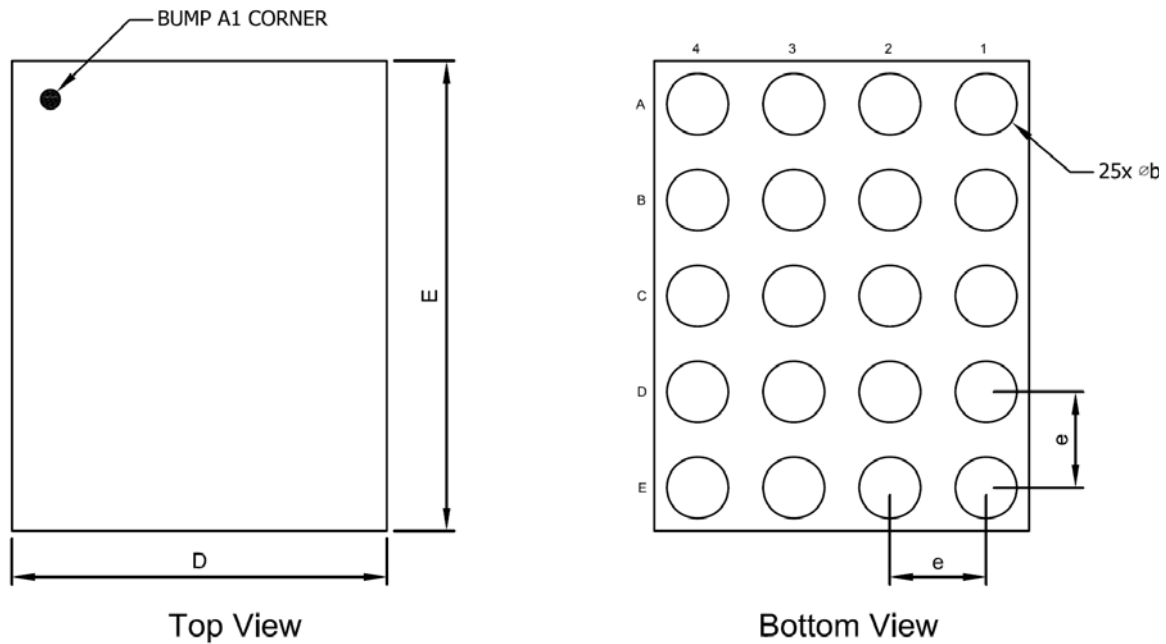
Fault Protection

Operating Mode	Function	Error Description	Condition	Behavior	Reset requirement	After reset
Charging	DCIN	DCIN-OVP	1. DCIN > 6.4V 2. Deglitch time : 50uS	1. MOS Q1 turn off 2. Stop charging mode 3. MOS Q4 full turn on	1. DCIN < 6.06V (DCOV-350mV) 2. Deglitch time : 1.875mS	1. Auto restart charge mode 2. Safety timer reset
		DCIN_PG	DCIN_PG=0 when: 1. DCIN < 3.4V (DCIN_UV) (falling) 2. DCIN < 3.7V (DCIN_BAD) (falling) 3. DCIN < VBAT+150mV (falling) Deglitch time : 30mS (falling)	1. MOS Q1 turn off 2. Stop charging mode 3. MOS Q4 full turn on	DCIN_PG=1 when: 1. DCIN > 3.8V (DCIN_UV) (rising) 2. DCIN > 4.5V (DCIN_BAD) (rising) 3. DCIN > BAT+200mV (rising) Deglitch time : 1.875mS (rising)	1. Auto restart charge mode 2. Safety timer reset
	PMID	PMID-SCP	PMID < 1.2V	DCIN current limit=100mA	PMID > 1.2V	DCIN current limit= ISET_DCIN
	SYS	SYS-SCP	1. (VBAT-VSYS) > Vsys_scp2=300mV 2. Deglitch time : 250uS(Tsys_scp)	1. MOS Q4 turn off 2. VSYS_SCP timer will start 3. After 64mS(Tsys_scp_r) Q4 will turn on and check Vsys_scp2 again, VSYS_SCP timer will reset	1. VSYS_SCP will auto check & recover 2. (VBAT-VSYS) < Vsys_scp2=300mV 3. Deglitch time : 64mS(Tsys_scp_r)	
	Thermal	NO NTC	TS voltage > 97% VP	A10 TS_METER detect as 010 (NTC not existed)	1. Install NTC-R	Start NTC-R detection
		VP short	VP voltage under 1.2V	A10 TS_METER detect as 010 (VP short)	1. Remove VP short	Start NTC-R detection
		Thermal regulation	IC die temp over 120	Reduce DCIN Q1 current to make die under 120 degree	IC die temp under 120 degree	Q1 current recover
		Thermal SD	IC die temp over 155	1. Turn off Q1 MOS and stop charging 2. Full turn on Q4 MOS to keep VSYS	IC die temp under 135 degree	Turn on Q1 MOS and start charging mode
Battery Supply	SYS	SYS-SCP	1. (VBAT-VSYS) > Vsys_scp2=300mV 2. Deglitch time : 250uS(Tsys_scp)	1. MOS Q4 turned off 2. VSYS_SCP timer will start 3. After 64mS(Tsys_scp_r) Q4 will turn on and check Vsys_scp2 again, VSYS_SCP timer will reset	1. VSYS_SCP will auto check & recover 2. (VBAT-VSYS) < Vsys_scp2=300mV 3. Deglitch time : 64mS(Tsys_scp_r)	MOS Q4 turned on

Fault Protection (Continued)

OTG	DCIN	OC	DCIN output current > 1.5A or 2A (A6 bit3)	MOS Q1 in hiccup operation : 1. MOS Q1 turn off 30mS(tOTG_OCP_OFF) 2. MOS Q1 turn on 0.8mS(tOTG_OCP_ON)	DCIN output current (Q1) < 1.5A or 2A	Operation in normal OTG mode
		DCIN_SCP	DCIN < 1.2V	Stop switching (but DC/DC still in boost mode)	DCIN > 1.2V	Operation in normal OTG mode
		DCIN-OVP	1. DCIN > 6.4V 2. Deglitch time : 50uS	Stop switching (but DC/DC still in boost mode) BOOST_FAULT=1'b1	1. DCIN < 6.06V (DCOV-350mV) 2. DCIN < BAT+200mV 3. Deglitch time : 30mS	Restart OTG boosting
	PMID	PMID_SCP	DCIN < 1.2V	Stop switching (but DC/DC still in boost mode)	PMID > 1.2V	Operation in normal OTG mode
	BAT	VBATtoo LOW	VBAT < 2.8V or 3.0V (A4. VBATFC)	Stop switching (but DC/DC still in boost mode) BOOST_FAULT=1'b1	1. VBAT > VBATFC2. DCIN < BAT+200mV3. Deglitch time : 30mS	Restart OTG boosting
	Thermal	Thermal SD	IC die temp over 155	1. Turn off Q1 MOS 2. Stop switching (but DC/DC still in boost mode)	IC die temp under 135 degree	Turn on Q1 MOS and start OTG boost.
Power Bank	DCIN	DCIN Plug-in	DCIN > BAT+200mV	1. Leave Power Bank mode. 2. Start Charging mode.	1. DCIN plug-out (DCIN < BAT+200mV) 2. ENPWRBNK=1'b1 3. Deglitch time : 30mS	Start Power Bank mode.
	PMID	PMID_SCP	DCIN < 1.2V	Stop switching (but DC/DC still in boost mode)	PMID > 1.2V	Operation in normal Power Bank mode
	BAT	VBAT too LOW	VBAT < 2.8V or 3.0V (A4. VBATFC)	Stop switching (but DC/DC still in boost mode) BOOST_FAULT=1'b1	1. VBAT > VBATFC 2. DCIN < BAT+200mV 3. Deglitch time : 30mS	Restart Power Bank boosting
	Thermal	Thermal SD	IC die temp over 155	Stop switching (but DC/DC still in boost mode)	IC die temp under 135 degree	Restart Power Bank boosting

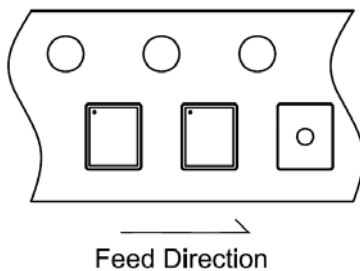
Package Information



WLCSP4X5-20 Package

Symble	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.540	0.600	0.660	0.0212	0.0236	0.0260
A1	0.210	0.235	0.260	0.0083	0.0093	0.0102
A2	0.330	0.365	0.400	0.0130	0.0144	0.0157
D	1.950	1.970	2.000	0.0768	0.0776	0.0787
E	2.450	2.470	2.500	0.0965	0.0972	0.0984
b	0.300	0.320	0.340	0.0118	0.0126	0.0134
e	0.50 BSC			0.0197 BSC		

Taping Specification



PACKAGE	Q'TY/REEL
WLCSP4X5-20	3,000 ea

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