

DDR Termination Regulator

Features

- VIN Input Voltage Range: 2.5V to 5.5V
- VLDOIN Voltage Range: 1.0V to 3.5V
- Support DDR I (1.25 V_{TT}), DDR II (0.9 V_{TT}), DDR III (0.75 V_{TT}), DDR IIIL (0.675V_{TT}) and DDR IV (0.6 V_{TT}) Requirements
- Stable with Output Ceramic Capacitor
- PGOOD to Monitor Output Regulation
- EN Input for Shutdown Function (S3 Mode)
- Remote Sensing (VOSNS)
- ±25mV Accuracy for VTT Refers to VTTREF
- ±10mA Buffered Reference (VTTREF)
- Built-In Soft-Start and UVLO
- Over Current Protection
- Thermal Shutdown Protection
- TDFN3X3-10 (Thermal Pad) Package

Applications

- DDR I/II/III/IIIL/IV Memory Termination
- SSTL_3, SSTL_2, SSTL_18, SSTL_15
- HSTL Termination
- Notebook/Desktop/Server
- Telecom/Datacom, GSM Base Station, LCD-TV/PDP-TV, Copier/Printer, Set-Top Box

Ordering Information

ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE (Green)
G2985RE1D	2985	-40°C~85°C	TDFN3X3-10

Note: RE: TDFN3X3-10

1: Bonding code

D: Tape & Reel

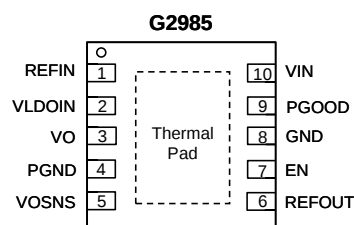
Green : Lead Free / Halogen Free.

General Description

The G2985 is a linear regulator designed to meet the JEDEC SSTL (Series Stub Termination Logic) specifications in DDR I/II/III/IIIL/IV –SDRAM systems. It is designed for the system which has low input voltage, low cost, low noise and space consideration.

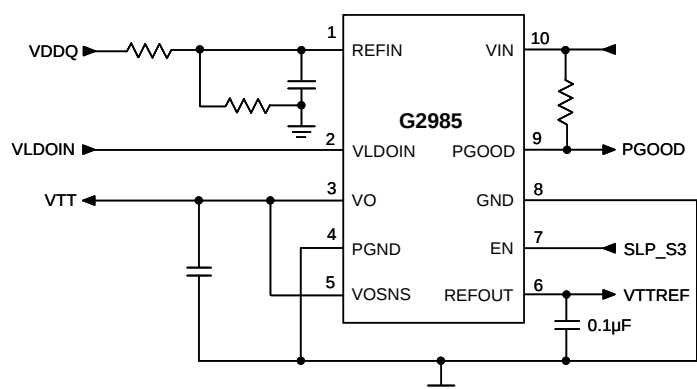
The G2985 provides accurate and fast response with amperage source/sink ability in load transient to track reference voltage with typically 20μF output capacitor. The terminated voltage can be generated by two external resistors or programmed by forcing REFIN pin at a desired voltage. Also the G2985 provides an open-drain PGOOD flag which monitors the output regulation and an EN signal to discharge VTT during STR (S3) mode.

Pin Configuration



Note: Recommend connecting the Thermal Pad to the Ground for excellent power dissipation.

Typical Application



Absolute Maximum Ratings ⁽¹⁾

Supply Voltage Range

VIN, VLDOIN, VOSNS, REFIN, EN -0.3V to +6.5V
PGND, GND -0.3V to 0.3V

Output Voltage Range

VO -0.3V to VLDOIN+0.3V
REFOUT, PGOOD -0.3V to +6.5V
Thermal Resistance of Junction to Ambient (θ_{JA})*
TDFN3X3-10. 98°C/W
Continuous Power Dissipation ($T_A = +25^\circ\text{C}$)*
TDFN3X3-10. 1.3W
Thermal Resistance Junction to Case, (θ_{JC})
TDFN3X3-10. 30°C/W
Maximum Junction Temperature, T_J 160°C
Storage Temperature Range, T_{STG} . . -55°C to +160°C
Reflow Temperature (soldering, 10sec) 260°C

Recommend Operating Range ⁽¹⁾

VIN 2.5V to 5.5V
VLDOIN 1V to min(3.5V, VIN-1V)
VOSNS, VO -0.1V to min(3.5V, VIN-1V)
EN -0.1V to 3.5V
REFIN. 0.5V to 1.8V
PGOOD -0.1V to 5.5V
REFOUT. -0.1V to 1.8V
PGND, GND -0.1V to 0.1V

Operating Ambient Temperature Range

T_A -40°C to 85°C

* Measured on 1in² of 1oz PCB.

Note:

⁽¹⁾ All voltage values are with respect to the network ground terminal unless otherwise noted.

Electrical Characteristics

Specifications with standard typeface are for $T_A=25^\circ\text{C}$, $V_{VIN}=5\text{V}$, $V_{VLDOIN}=1.5\text{V}$, $V_{REFIN}=0.75\text{V}$, and $V_{EN}=V_{VIN}$. Unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
VIN supply current	I_{VIN}	$V_{VIN}=5\text{V}$, no load, $V_{EN}=5\text{V}$	---	0.7	1	mA
VIN standby current	I_{VINSTB}	$V_{VIN}=5\text{V}$, no load, $V_{EN}=0\text{V}$, $V_{REFIN}>0.4\text{V}$	---	200	400	μA
VIN shutdown current	I_{VINSN}	$V_{VIN}=5\text{V}$, no load, $V_{EN}=0\text{V}$, $V_{REFIN}=0\text{V}$	---	65	130	μA
VLDOIN supply current	I_{VLDOIN}	$V_{VIN}=5\text{V}$, no load	---	1	100	μA
VLDOIN standby current	$I_{VLDOINSTB}$	$V_{VIN}=5\text{V}$, no load, $V_{EN}=0\text{V}$, $V_{REFIN}>0.4\text{V}$	---	0.1	50	μA
VLDOIN shutdown current	$I_{VLDOINSN}$	$V_{VIN}=5\text{V}$, no load, $V_{EN}=0\text{V}$, $V_{REFIN}=0\text{V}$	---	0.1	50	μA
REFIN input current	I_{REFIN}	$V_{EN}=5\text{V}$	---	---	1	μA
VOSNS input current	I_{VOSNS}	$V_{VIN}=5\text{V}$, no load, $V_{EN}=5\text{V}$	---	---	1	μA
VTT output voltage	V_{VTT}	DDR I	---	1.25	---	V
		DDR II	---	0.9	---	
		DDR III	---	0.75	---	
		DDR IIIL	---	0.675	---	
		DDR IV	---	0.6	---	
VTT output voltage tolerance refer to REOUT	V_{VTTOS}	$I_{VTT}=0$	-15	---	15	mV
VTT output voltage tolerance refer to REFOUT	ΔV_{VTT}	$ I_{VTT} <2\text{A}$	-25	---	25	mV
VTT source current limit	$I_{VOCLSRC}$	$V_{TT}=\text{REFIN} * 0.90$, PGOOD=Hi	3	4	---	A
		$V_{TT}=0$	1.5	2.4	---	
VTT sink current limit	$I_{VOCLSNK}$	$V_{TT}=\text{REFIN} * 1.1$, PGOOD=Hi	3	4	---	A
		$V_{TT}=V_{VIN}$	1.5	2.4	---	
VO discharge current	$I_{DISCHARGE}$	$V_{REFIN}=0\text{V}$, $V_{VTT}=0.3\text{V}$, $V_{EN}=0\text{V}$	---	18	25	Ω

Electrical Characteristics (continued)

Specifications with standard typeface are for $T_A=25^{\circ}\text{C}$, $V_{\text{VIN}}=5\text{V}$, $V_{\text{VLDOIN}}=1.5\text{V}$, $V_{\text{REFIN}}=0.75\text{V}$, and $V_{\text{EN}}=V_{\text{VIN}}$. Unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
PGOOD threshold	V_{PGTH}	PGOOD lower threshold refer to REFOUT	-23.5	-20	-17	%
		PGOOD upper threshold refer to REFOUT	17	20	23.5	
		PGOOD hysteresis	---	5	---	
PGOOD startup delay	$T_{\text{PGSTUPDLY}}$	VOSNS is within 15% of REFOUT	---	2	---	ms
PGOOD bad delay	T_{PGBADDLY}	VOSNS is outside 20% of REFOUT	---	10	---	μs
PGOOD output low voltage	V_{PGOODLOW}	$I_{\text{SINK}}=4\text{mA}$	---	---	0.4	V
PGOOD leakage current	I_{PGOODLK}	VOSNS is inside of PGOOD window	---	---	1	μA
REFIN UVLO threshold	$V_{\text{REFINUULO}}$	REFIN rising	0.36	0.39	0.42	V
		Hysteresis	---	20	---	mV
REFOUT output voltage	V_{REFOUT}	DDR I	---	1.25	---	V
		DDR II	---	0.9	---	
		DDR III	---	0.75	---	
		DDR IIIL	---	0.675	---	
		DDR IV	---	0.6	---	
REFOUT output voltage tolerance refer to REFIN	ΔV_{REFOUT}	$-10\text{mA} < I_{\text{REFOUT}} < 10\text{mA}$	-15	---	15	mV
REFOUT source current limit	$I_{\text{REFOUTSRCL}}$	$V_{\text{REFOUT}}=0\text{V}$	10	40	---	mA
REFOUT sink current limit	$I_{\text{REFOUTSNCL}}$	$V_{\text{REFOUT}}=V_{\text{IN}}$	10	40	---	mA
VIN UVLO threshold	V_{VINUVLO}	VIN rising	2.2	2.3	2.375	V
		Hysteresis	---	50	---	mV
EN input voltage threshold	V_{ENTH}	Enable rising	1.7	---	---	V
		Enable falling	---	---	0.3	
		Hysteresis	---	0.5	---	
Logic input leakage current	I_{ENLEAK}		-1	---	1	μA
Thermal Shutdown	T_{SD}		---	150	---	$^{\circ}\text{C}$
Thermal Shutdown Hysteresis	T_{SDHYS}		---	25	---	$^{\circ}\text{C}$

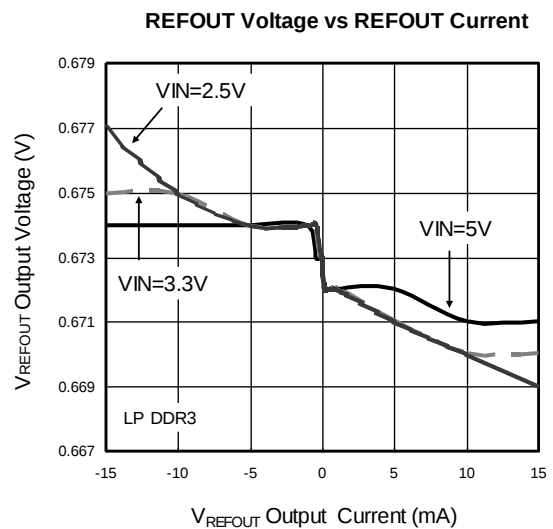
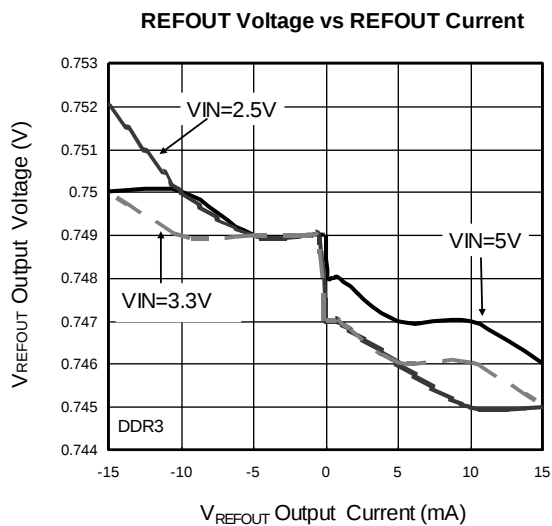
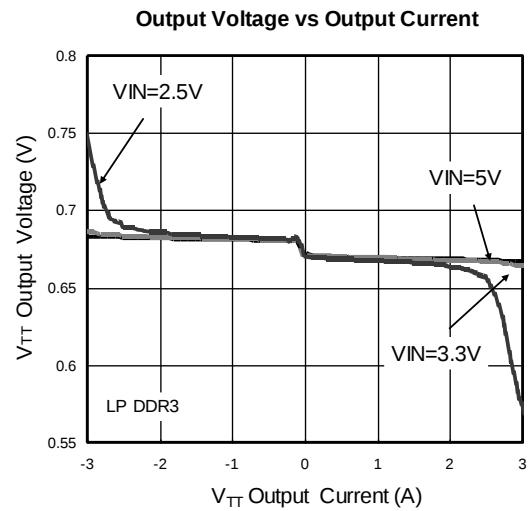
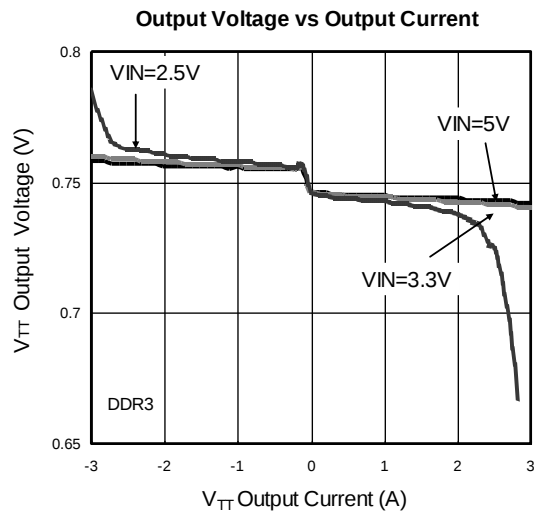
Electrical Characteristics

Specifications with standard typeface are for $T_A=25^{\circ}\text{C}$, $V_{\text{VIN}}=3.3\text{V}$, $V_{\text{VLDOIN}}=1.5\text{V}$, $V_{\text{REFIN}}=0.75\text{V}$, and $V_{\text{EN}}=V_{\text{VIN}}$. Unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
VIN supply current	I_{VIN}	$V_{\text{VIN}}=3.3\text{V}$, no load, $V_{\text{EN}}=3.3\text{V}$	---	0.7	1	mA
VIN standby current	I_{VINSTB}	$V_{\text{VIN}}=3.3\text{V}$, no load, $V_{\text{EN}}=0\text{V}$, $V_{\text{REFIN}}>0.4\text{V}$	---	200	400	μA
VIN shutdown current	I_{VINSN}	$V_{\text{VIN}}=3.3\text{V}$, no load, $V_{\text{EN}}=0\text{V}$, $V_{\text{REFIN}}=0\text{V}$	---	65	80	μA
VLDOIN supply current	I_{VLDOIN}	$V_{\text{VIN}}=3.3\text{V}$, no load	---	1	50	μA
VLDOIN standby current	$I_{\text{VLDOINSTB}}$	$V_{\text{VIN}}=3.3\text{V}$, no load, $V_{\text{EN}}=0\text{V}$, $V_{\text{REFIN}}>0.4\text{V}$	---	0.1	50	μA
VLDOIN shutdown current	I_{VLDOINSN}	$V_{\text{VIN}}=3.3\text{V}$, no load, $V_{\text{EN}}=0\text{V}$, $V_{\text{REFIN}}=0\text{V}$	---	0.1	50	μA
REFIN input current	I_{REFIN}	$V_{\text{EN}}=3.3\text{V}$	---	---	1	μA
VOSNS input current	I_{VOSNS}	$V_{\text{VIN}}=3.3\text{V}$, no load, $V_{\text{EN}}=3.3\text{V}$	---	---	1	μA
VTT output voltage	V_{VTT}	DDR I	---	1.25	---	V
		DDR II	---	0.9	---	
		DDR III	---	0.75	---	
		DDR IIIL	---	0.675	---	
		DDR IV	---	0.6	---	
VTT output voltage tolerance refer to REOUT	V_{VTTOS}	$I_{\text{VTT}}=0$	-15	---	15	mV
VTT output voltage tolerance refer to REFOUT	ΔV_{VTT}	$ I_{\text{VTT}} <2\text{A}$	-25	---	25	mV
VTT source current limit	I_{VOCLSRC}	VTT=REFIN *0.90, PGOOD=Hi	3	4	---	A
		VTT=0	1.5	2.4	---	
VTT sink current limit	I_{VOCLSNK}	VTT=REFIN *1.1, PGOOD=Hi	3	4	---	A
		VTT= V_{VIN}	1.5	2.4	---	
VO discharge current	$I_{\text{DISCHARGE}}$	$V_{\text{REFIN}}=0\text{V}$, $V_{\text{VTT}}=0.3\text{V}$, $V_{\text{EN}}=0\text{V}$	---	18	25	Ω
PGOOD threshold	V_{PGTH}	PGOOD lower threshold refer to REFOUT	-23.5	-20	-17	%
		PGOOD upper threshold refer to REFOUT	17	20	23.5	
		PGOOD hysteresis	---	5	---	
PGOOD startup delay	$T_{\text{PGSTUPDLY}}$	VOSNS is within 15% of REFOUT	---	2	---	ms
PGOOD bad delay	T_{PGBADDLY}	VOSNS is outside 20% of REFOUT	---	10	---	μs
PGOOD output low voltage	V_{PGOODLOW}	$I_{\text{SINK}}=4\text{mA}$	---	---	0.4	V
PGOOD leakage current	I_{PGOODLK}	VOSNS is inside of PGOOD window	---	---	1	μA
REFIN UVLO threshold	$V_{\text{REFINUULO}}$	REFIN rising	0.36	0.39	0.42	V
		Hysteresis	---	20	---	mV
REFOUT output voltage	V_{REFOUT}	DDR I	---	1.25	---	V
		DDR II	---	0.9	---	
		DDR III	---	0.75	---	
		DDR IIIL	---	0.675	---	
		DDR IV	---	0.6	---	
REFOUT output voltage tolerance refer to REFIN	ΔV_{REFOUT}	$-10\text{mA} < I_{\text{REFOUT}} < 10\text{mA}$	-15	---	15	mV
REFOUT source current limit	$I_{\text{REFOUTSRCL}}$	$V_{\text{REFOUT}}=0\text{V}$	10	40	---	mA
REFOUT sink current limit	$I_{\text{REFOUTSNCL}}$	$V_{\text{REFOUT}}=V_{\text{IN}}$	10	40	---	mA
VIN UVLO threshold	V_{VINUULO}	VIN rising	2.2	2.3	2.375	V
		Hysteresis	---	50	---	mV
EN input voltage threshold	V_{ENTH}	Enable rising	1.7	---	---	V
		Enable falling	---	---	0.3	
		Hysteresis	---	0.5	---	
Logic input leakage current	I_{ENLEAK}		-1	---	1	μA
Thermal Shutdown	T_{SD}		---	150	---	$^{\circ}\text{C}$
Thermal Shutdown Hysteresis	T_{SDHYS}		---	25	---	$^{\circ}\text{C}$

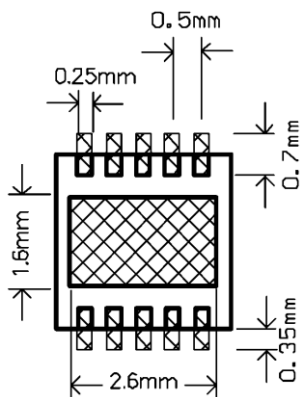
Electrical Characteristics

$C_{VLDIOIN}=20\mu\text{F/MLCC/X5R}$, $C_{VIN}=4.7\mu\text{F/MLCC/X7R}$, $C_{REFOUT}=0.1\mu\text{F/MLCC/X7R}$, $C_{VTT}=20\mu\text{F/X5R/MLCC}$, $T_A=25^\circ\text{C}$
unless otherwise noted.

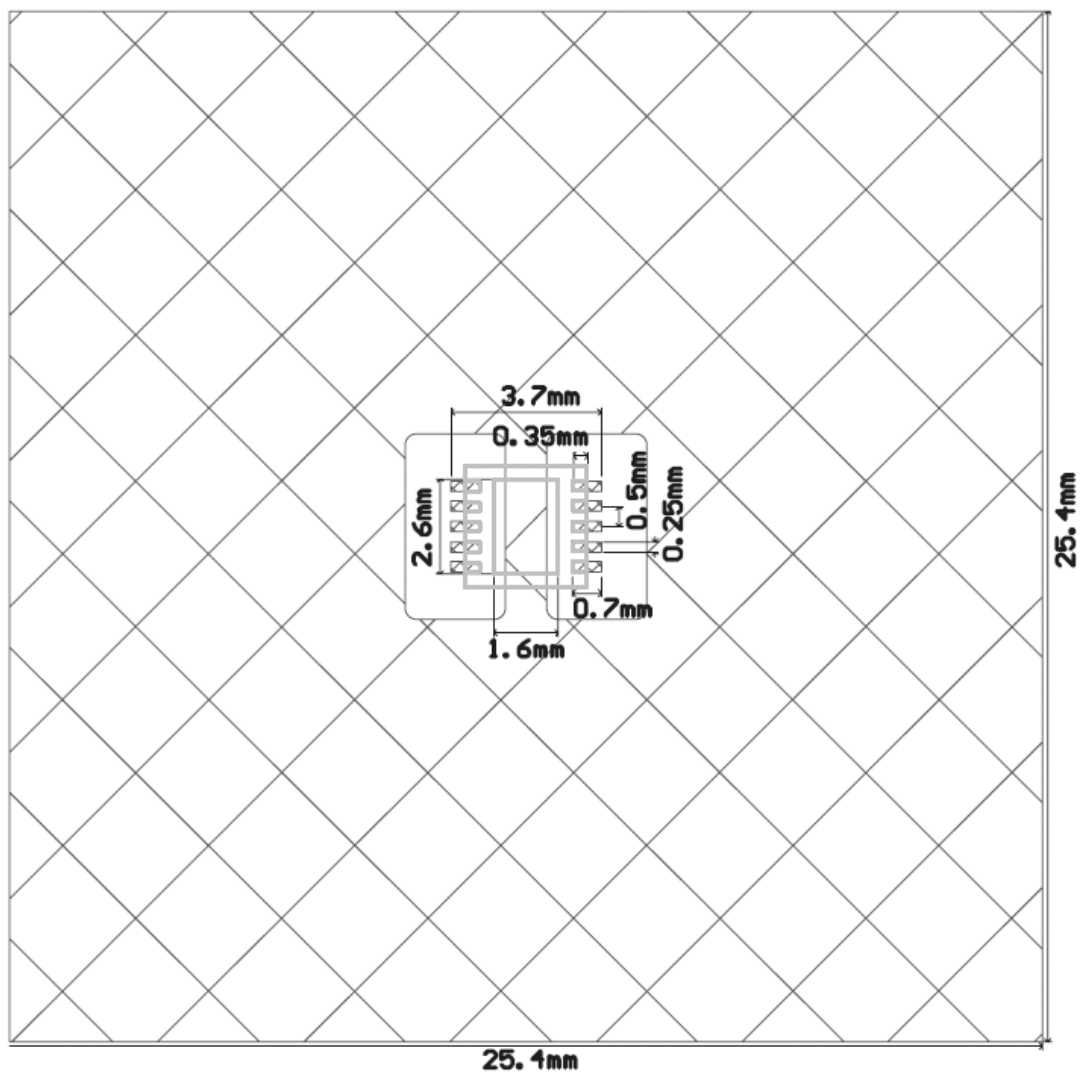


Minimum Footprint PCB Layout Section

TDFN3X3-10



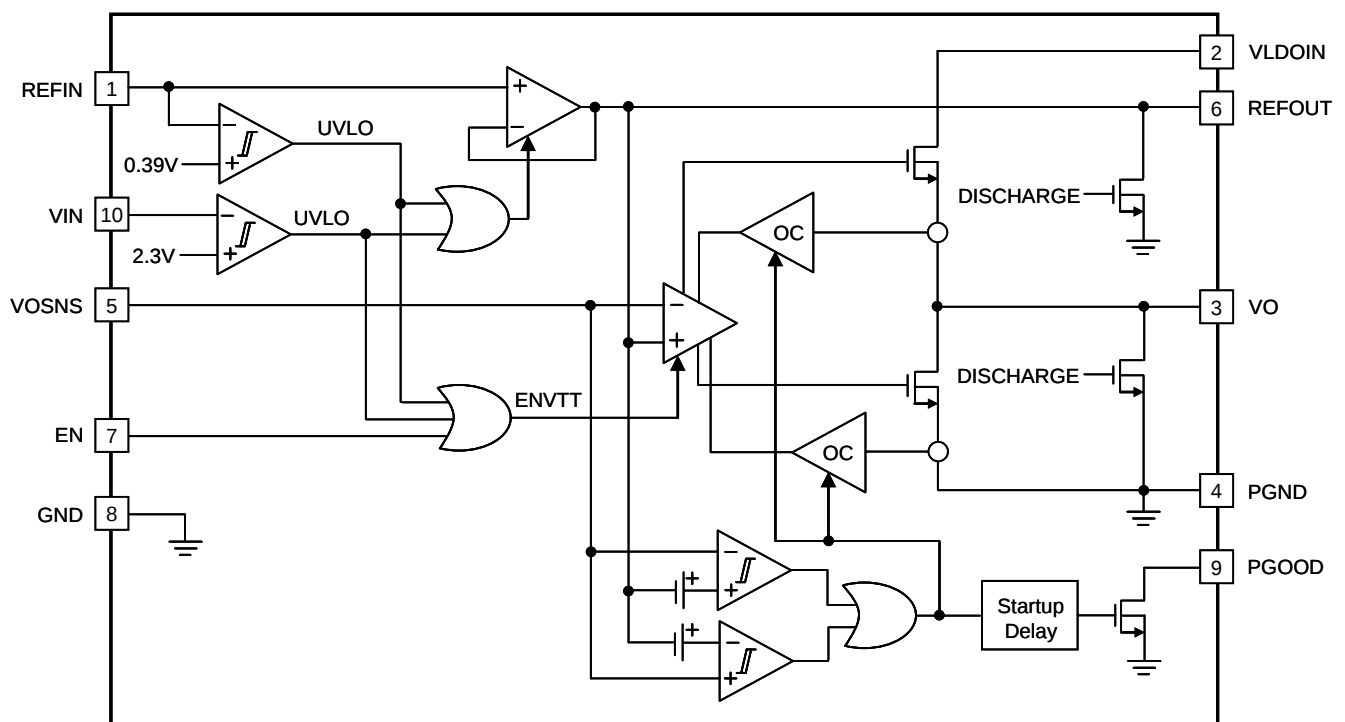
1in² of 1oz PCB Layout Section.



Pin Description

PIN	NAME	DESCRIPTIONS
1	REFIN	Terminator reference input voltage, 1.25V for DDR I, 0.9V for DDR II, 0.75V for DDR III, 0.675V for DDR IIIL, 0.6V for DDR IV.
2	VLDOIN	Terminator power pin
3	VO	Terminator output pin
4	PGND	Terminator power ground pin
5	VOSNS	Voltage sense input pin, connect to remote termination
6	REFOUT	Terminator reference output pin
7	EN	ON/OFF function for SLP_S3 mode.
8	GND	Ground
9	PGOOD	PGOOD open-drain output
10	VIN	Internal circuit power pin, at least 2.5V
Thermal Pad		Recommend connecting the Thermal Pad to the GND for excellent power dissipation.

Block Diagram



Description

VIN, VLDOIN

VIN and VLDOIN are two independent input supply pins for the G2985. VIN is used to supply all the internal analog circuits. VLDOIN is only used to supply the output stage to create the regulated V_{TT} . To keep the regulation successfully, VIN should be equal to or larger than VLDOIN+1V. Using a higher VLDOIN voltage will produce a larger sourcing capability from V_{TT} . But the internal power loss will also increase and then the heat increases. If the junction temperature exceeds the thermal shutdown threshold than the G2985 will enter the shutdown state that is the same as manual shutdown, where V_{TT} is tri-state and V_{REF} remains active.

REFIN

When REFIN is configured for standard DDR termination applications, REFIN can be set by an external equivalent ratio voltage divider connected to the memory supply bus (VDDQ). Then, the G2985 generates REFOUT voltage by reference to REFIN. The REFIN voltage is supported from 0.5 V to 2.5 V for many types of DDR application.

REFOUT

REFOUT generates the V_{TT} reference voltage. It has 10mA source and sink ability. REFOUT becomes active when REFIN voltage rises to 0.390 V and VIN is above the UVLO threshold. In contrast, it becomes deactivated and discharges to GND through an internal 10-k Ω MOSFET when REFIN is less than 0.375 V. REFOUT are independent of the EN pin state.

For better performance, using an output bypass capacitor close this pin is more helpful for the noise. A ceramic capacitor in the range of 0.1 μ F to 0.01 μ F is recommended.

VOSNS

The VOSNS pin is the feedback sensing pin of the operation amplifier which regulates the V_{TT} voltage. In most motherboard applications, the termination resistors will connect V_{TT} in a long plane. If using the re-remote sensing pin – VOSNS to the middle of the bus, the significant long-trace IR drop resulting in a termination voltage which is lower at one end than the other can be avoided. This will provide a better distribution across the entire termination bus. If the remote load regulation is not used, the VOSNS pin must still be connected to V_{TT} for correct regulation. Care should be taken when a long VOSNS trace is implemented in close proximity to the memory. Noise pickup in the VOSNS trace can cause problems with precise regulation of V_{TT} . A small 0.1 μ F ceramic capacitor placed next to the VOSNS pin can help to filter any high frequency signals and preventing errors.

VO

VO is the regulated output that is used to terminate the bus resistors of DDR-SDRAM. It can precisely track the REFOUT voltage with large sinking and sourcing current capability. The maximum continuous current sourcing from VO is a function of VLDOIN. Using a higher VLDOIN will increase the source current but it also increase the internal power dissipation and reduce the efficiency. Although the G2985 can deliver the larger current, care should be taken for the thermal dissipation when larger current is required. Thus, an over current function is embedded for preventing overloading and short is occurred. Also, when the temperature exceeds the junction temperature, the thermal shutdown protection is activated. That will drive the VO output into tri-state until the temperature returns below the hysteric trigger point.

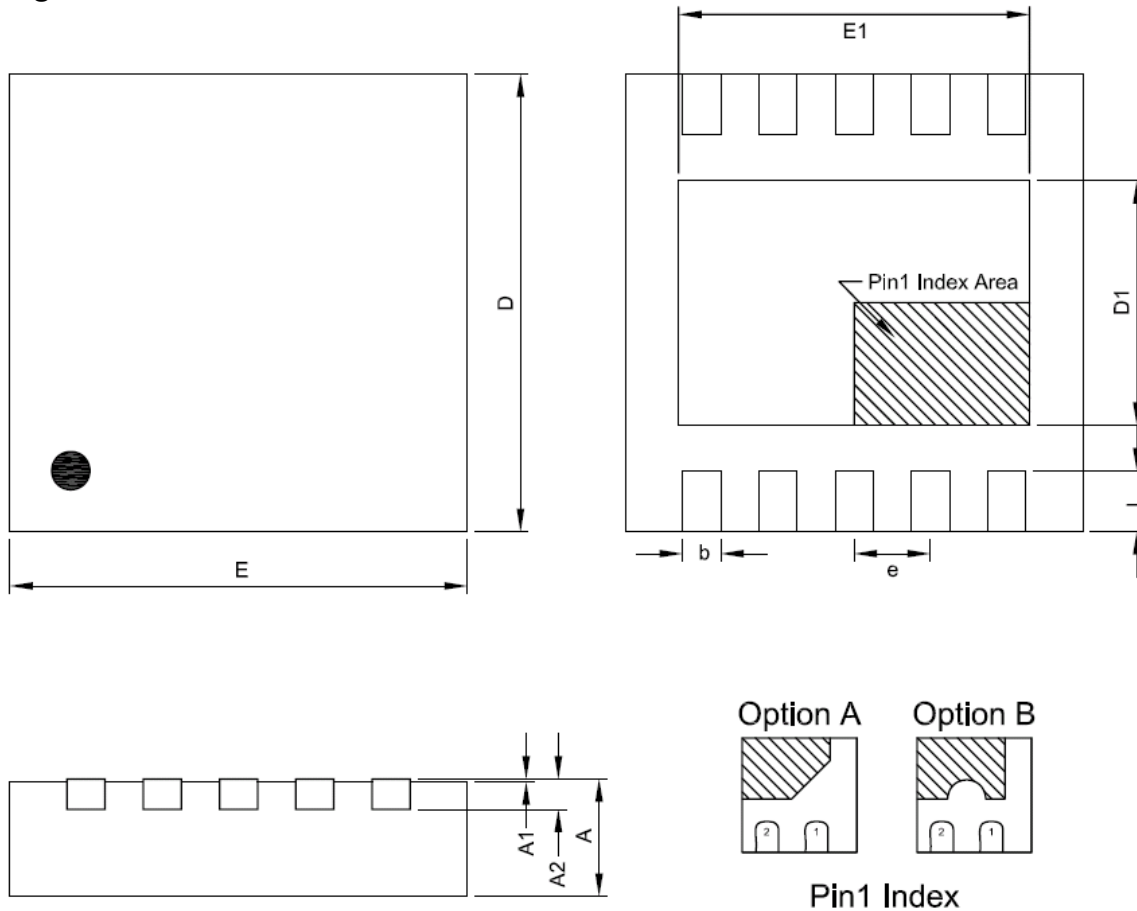
Capacitors

The G2985 does not require the capacitors for input stability, but it is recommended for improving the performance during large load transition to prevent the input power rail from dropping, especially for VLDOIN. The input capacitor for VLDOIN should be as close as possible. The typical recommended value is 50 μ F for AL electrolytic capacitors, 10 μ F with X5R for the ceramic capacitors. To prevent the excessive noise coupling into this device, an additional 0.1 μ F ceramic capacitor can be placed on the VIN power rail for the better performance.

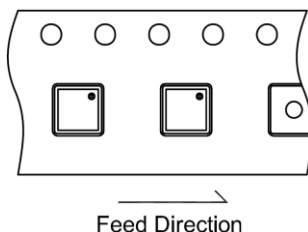
The output capacitor of the G2985 is suggested to use the capacitors with low ESR. Using the capacitors with low ESR (as ceramic, OS-CON, tantalum) will have the better transition performance which is with smaller voltage drop when the peak current occurring at the transition. As a general recommendation the output capacitor should be above 20 μ F with the low ESR for SSTL applications with DDR-SDRAM.

S3 and Pseudo-S5 Support

The G2985 provides S3 and pseudo-S5 support by EN and REFIN voltage level. Both REFOUT and VO are on when EN = high. While REFIN is above 0.390V but EN = low, REFOUT is maintained but VO is turned off and discharged via an internal discharge MOSFET. When REFIN voltage is less than 0.375V and EN = low, G2985 enters pseudo-S5 state. Both VO and REFOUT are turned off and discharged to GND through internal MOSFETs.

Package Information

TDFN3X3-10 Package

Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.0276	0.0295	0.0315
A1	0.00	---	0.05	0.0000	---	0.0020
A2	0.20 REF			0.0079 REF		
D	2.95	3.00	3.05	0.1161	0.1181	0.1201
E	2.95	3.00	3.05	0.1161	0.1181	0.1201
D1	1.50	1.60	1.75	0.0591	0.0630	0.0689
E1	2.20	2.60	2.70	0.0866	0.1024	0.1063
b	0.18	0.25	0.30	0.0071	0.0098	0.0118
e	0.50 BSC			0.0197 BSC		
L	0.30	0.40	0.50	0.0118	0.0157	0.0197

Taping Specification


PACKAGE	Q'TY/REEL
TDFN3X3-10	3,000 ea

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