G2992B

2A DDR Bus Termination Regulator

Features

- **V_{CNTL} Supply Voltage: 3V to 5.5V**
- **Termination Supply Voltage: 1.2V to 3.6V**
- **Support DDR I(1.25V_{TT}), DDR II (0.9 V_{TT}), and DDR III(0.75V_{TT}) Requirements**
- **Requires Only 20µF Ceramic Output Capacitor**
- **Low Output Offset**
- **2A Source and Sink Current**
- **Low External Component Count**
- **No Inductor Required**
- **Thermal Shutdown Protection**
- **Over Current Protection**
- **Suspend to RAM (STR) Function with High-impedance Output**
- **SOT-23-5, SOP-8 and MSOP-8 (FD) Package**

Applications

- **DDR-SDRAM Termination Voltage**
- **DDR I / DDR II / DDRIII Termination Voltage**
- **SSTL-18**
- **SSTL-2**
- **SSTL-3**

General Description

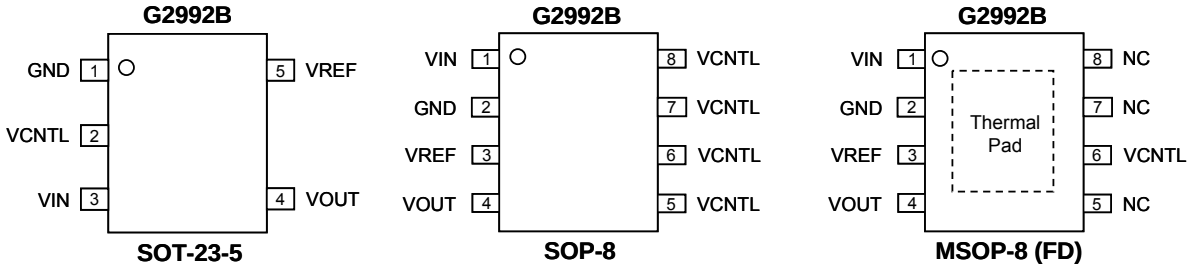
The G2992B is a linear regulator designed to meet the JEDEC SSTL-18, SSTL-2 and SSTL-3 (Series Stub Termination Logic) specifications for termination of DDR I/ II/ III -SDRAM. It contains a high-speed operational amplifier that provides excellent response to the load transients. This device can deliver 2A continuous current in the application such as required for DDR I/ II/ III SDRAM termination. The G2992B can easily provide the accurate V_{TT} voltage with two external resistors generating reference voltage. The quiescent current is as low as 750µA @ V_{CNTL} = 3.3V. So the power consumption can meet the low power consumption applications. The G2992B also has a shutdown function by setting V_{REF} smaller than 0.2V, that provides Suspend to RAM (STR) functionality. When in the shutdown mode, the V_{TT} output (on V_{OUT} pin) will be tri-state providing a high impendence. A power saving advantage can be obtained in this mode through lowering the quiescent current to 50µA @ V_{CNTL} = 3.3V.

Ordering Information

ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE (Green)
G2992BT11U	292Bx	-40°C to +125°C	SOT-23-5
G2992BP11U	G2992B	-40°C to +125°C	SOP-8
G2992BF51U	G2992B	-40°C to +125°C	MSOP-8 (FD)

Note: T1: SOT-23-5 P1: SOP-8 F5: MSOP-8 (FD)
1: Bonding Code
U: Tape & Reel

Pin Configuration



Note: Recommend connecting the Thermal Pad to the Ground for excellent power dissipation.

Absolute Maximum Ratings (1)

Supply Voltage

V_{CNTL}, V_{IN}, V_{REF} to GND . . . . . .-0.3V to +7V

Output Voltage Range

V_{OUT} . . . . . -0.3V to V_{IN}+0.3V

Thermal Resistance Junction to Ambient, (θ_{JA})

SOT-23-5 . . . . . .240°C/W(2)

SOP-8 . . . . . 160°C/W(2)

MSOP-8 (FD) . . . . . 132°C/W(3)

Continuous Power Dissipation (T_A = +25°C)

SOT-23-5. . . . . 0.55W(2)

SOP-8 . . . . . .0.8W(2)

MSOP-8 (FD) . . . . 0.9W(3)

Thermal Resistance Junction to Case, (θ_{Jc})

SOT-23-5 . . . . . .60°C/W

SOP-8 . . . . . 31°C/W

MSOP-8 (FD) . . . . . 40°C/W

Maximum Junction Temperature, T_J . . . . . .150°C

Storage Temperature Range, T_{STG} . . . . -65°C to+150°C

Reflow Temperature (soldering, 10sec) . . . . . .260°C

Electrostatic Discharge, V_{ESD}

Human body mode . . . . . .2000V(4)

Recommend Operation Range (5)

Operating Ambient Temperature Range

T_A . . . . . -40°C to +125°C

V_{CNTL} to GND. . . . . 3V to 5.5V

V_{IN} to GND. . . . . .1.2V to 3.6V

V_{REF} to GND . . . . . 0.65V to 1.25V

Note:

(1) : Absolute maximum rating indicates limits beyond which damage to the device may occurs.

(2) : Please refer to Minimum Footprint PCB Layout Section.

(3) : Please refer to 1in² of 1oz PCB Layout Section.

(4) : Human body model : C = 100pF, R = 1500Ω, 3 positive pulses plus 3 negative pulses.

(5) : V_{IN} and V_{REF} mustn't be higher than V_{CNTL}.

Electrical Characteristics

Specifications with standard typeface are for T_A=25°C, V_{IN}=2.5V, V_{CNTL}=3.3V, V_{REF}=1.25V, C_{OUT}=20µF.

The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Output Offset Voltage	V_{OS}		-20	0	20	mV
VTT output voltage	V_{TT}	(DDR I/DDR II/DDR III)	---	1.25/0.9/0.75	---	V
VTT Output Voltage Load Regulation (DDR I/DDR II/DDR III)	ΔV_{TT}	I_{VTT}=0, V_{REF}=½V_{IN}	-20	---	20	mV
		$\|I_{VTT}\|$<1A,V_{REF}=½V_{IN}	-30	---	30	
		$\|I_{VTT}\|$<2A, V_{REF} =½V_{IN}	-40	---	40	
Input Voltage Range (DDR I/DDR II)	V_{IN}		1.6	2.5/1.8	3.6	V
Input Voltage Range (DDR III)			1.2	1.5	3.6	
Control Voltage Range (DDR I/DDR II)	V_{CNTL}		3	3.3	5.5	V
Control Voltage Range (DDR III)			3	3.3	5.5	V
Quiescent Current	I_{CNTL}	I_{OUT}=0A	---	1.3	2	mA
Quiescent Current in Shutdown	I_{SD}	V_{REF}<0.2V	---	50	90	µA
Current Limit	I_{LIMIT}		2	---	---	A
Thermal Shutdown Temperature	T_{TS}	3.3V≦V_{CNTL}≦5.5V	---	160	---	°C
Thermal Shutdown Hysteresis	T_{HYS}		---	20	---	°C
Shutdown High Trigger Level Output	V_{IH}	Output active	0.55	---	---	V
Shutdown Low Trigger Level Output	V_{IL}	Output disable	---	---	0.2	V

Electrical Characteristics

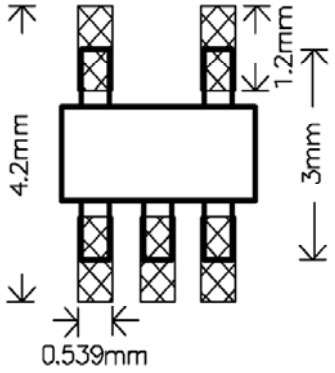
Specifications with standard typeface are for T_A=25°C, V_{IN}=1.5V, V_{CNTL}=3.3V, V_{REF}=0.75V, C_{OUT}=20µF.

The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified.

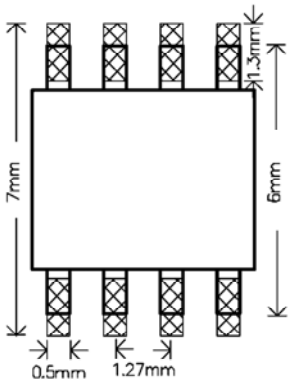
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Output Offset Voltage	V_{OS}		-20	0	20	mV
VTT output voltage	V_{TT}	(DDR I/DDR II/DDR III)	---	1.25/0.9/0.75	---	V
VTT Output Voltage Load Regulation (DDR I/DDR II/DDR III)	ΔV_{TT}	I_{VTT}=0, V_{REF}=½V_{IN}	-20	---	20	mV
		$\|I_{VTT}\|$<1A,V_{REF}=½V_{IN}	-30	---	30	
		$\|I_{VTT}\|$<2A, V_{REF} =½V_{IN}	-40	---	40	
Input Voltage Range (DDR I/DDR II)	V_{IN}		1.6	2.5/1.8	3.6	V
Input Voltage Range (DDR III)			1.2	1.5	3.6	
Control Voltage Range (DDR I/DDR II)	V_{CNTL}		3	3.3	5.5	V
Control Voltage Range (DDR III)			---	3.3	---	V
Quiescent Current	I_{CNTL}	I_{OUT}=0A	---	1.3	2	mA
Quiescent Current in Shutdown	I_{SD}	V_{REF}<0.2V	---	50	90	µA
Current Limit	I_{LIMIT}		2	---	---	A
Thermal Shutdown Temperature	T_{TS}	3.3V≦V_{CNTL}≦5.5V	---	160	---	°C
Thermal Shutdown Hysteresis	T_{HYS}		---	20	---	°C
Shutdown High Trigger Level Output	V_{IH}	Output active	0.55	---	---	V
Shutdown Low Trigger Level Output	V_{IL}	Output disable	---	---	0.2	V

Minimum Footprint PCB Layout Section

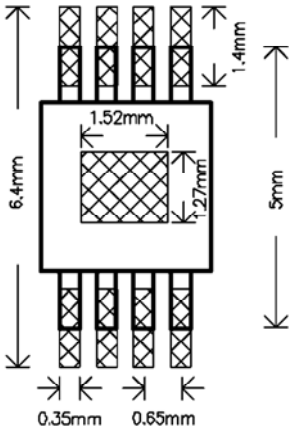
SOT-23-5



SOP-8



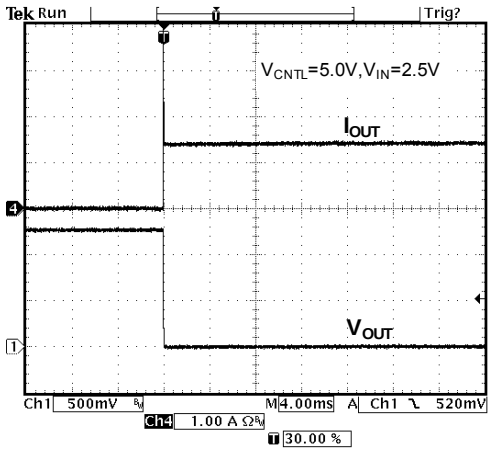
MSOP-8 (FD)



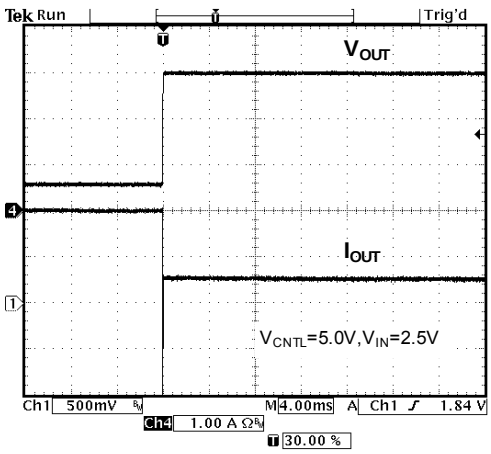
Typical Performance Characteristics

C_{CNTL}=1μF/MLCC/X5R, C_{IN}=22μF/MLCC/X5R, C_{SS}=1μF/MLCC/X5R, C_{OUT}=20μF/X5R/MLCC unless otherwise noted.

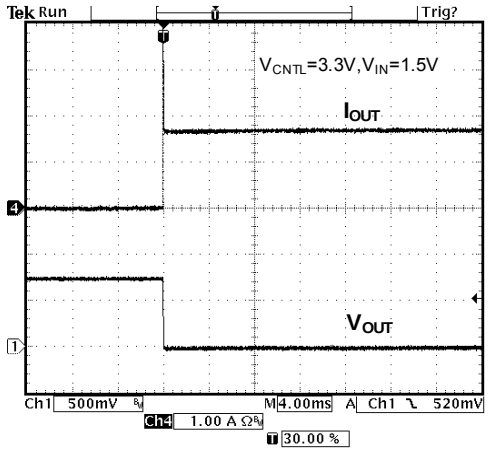
V_{OUT} is Shorted to GND



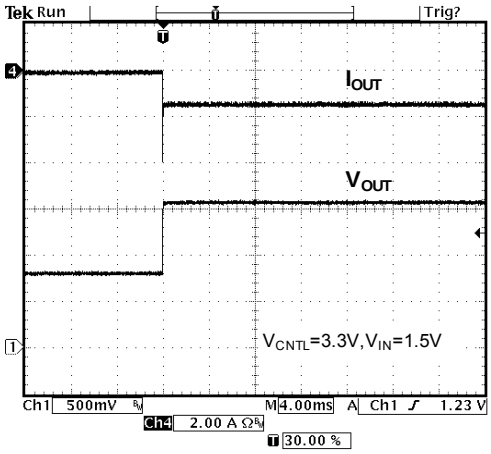
V_{OUT} is Shorted to V_{IN} (2.5V)



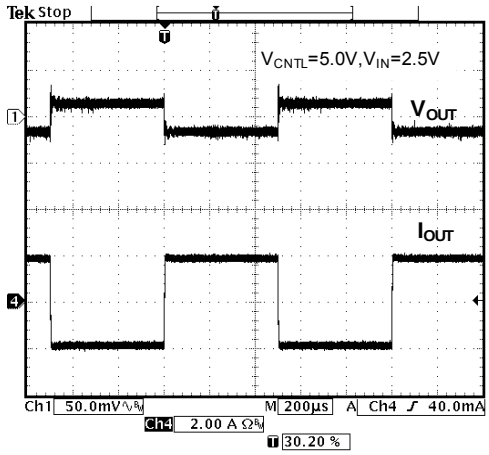
V_{OUT} is Shorted to GND



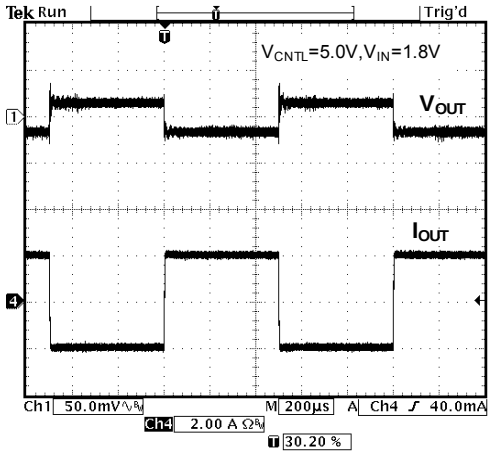
V_{OUT} is Shorted to V_{IN} (1.5V)



V_{OUT} Load Transient Response

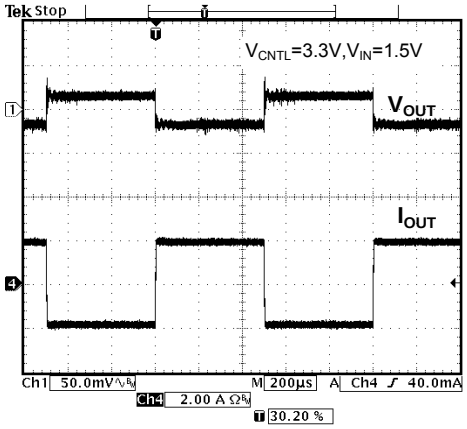


V_{OUT} Load Transient

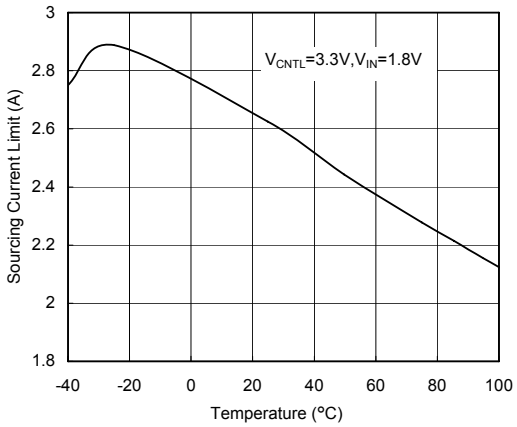


Typical Performance Characteristics (continued)

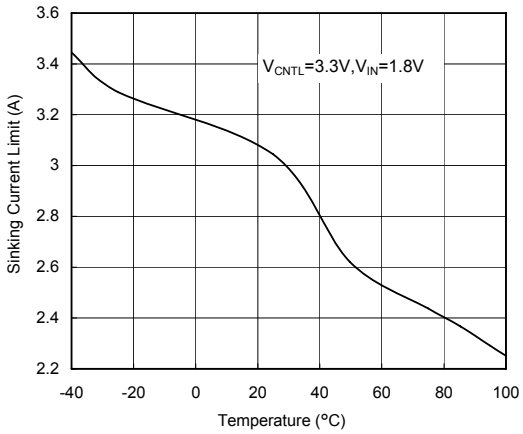
V_{OUT} Load Transient Response



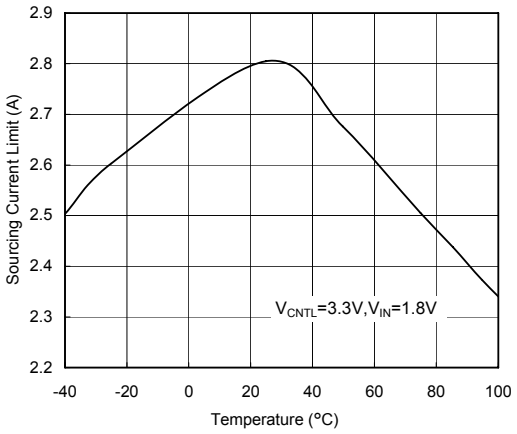
Sourcing Current Limit vs. Temperature



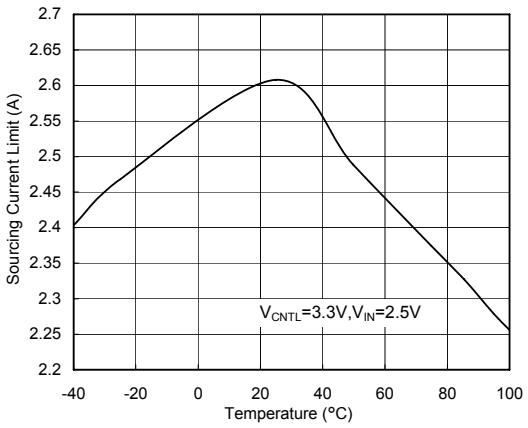
Sinking Current Limit vs. Temperature



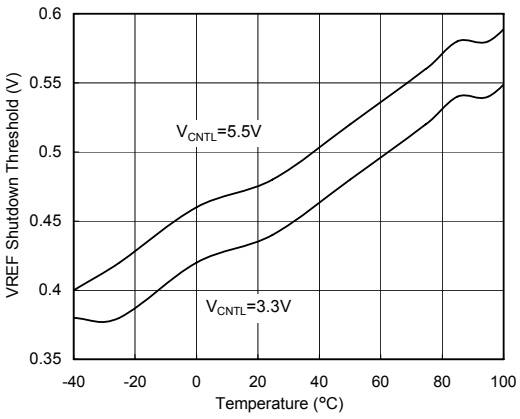
Sourcing Current Limit vs. Temperature



Sourcing Current Limit vs Temperature

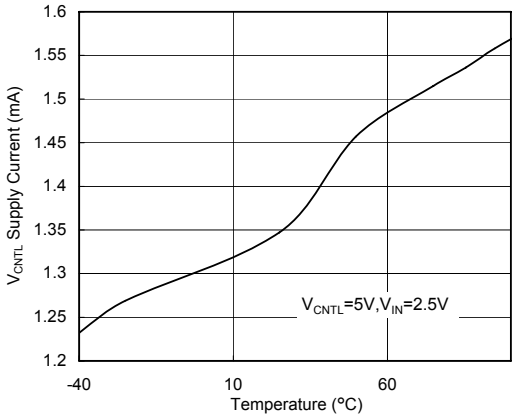


V_{REF} Shutdown Threshold vs Temperature

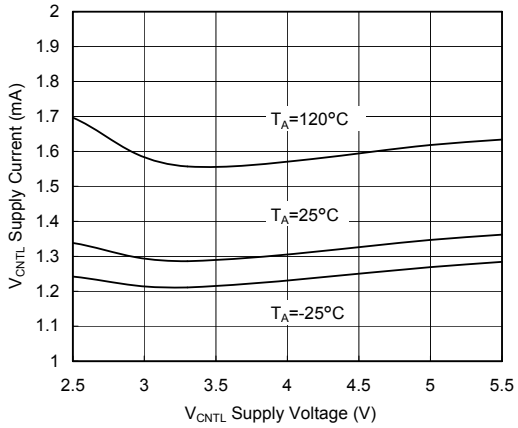


Typical Performance Characteristics (continued)

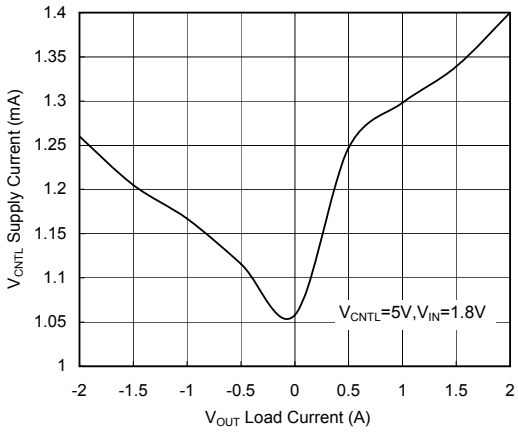
V_{CNTL} Supply Current vs. Temperature



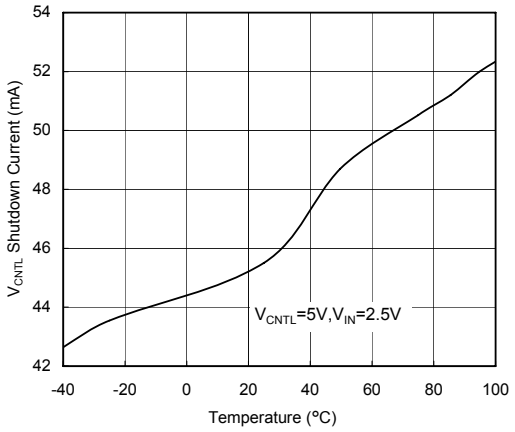
V_{CNTL} Supply Current vs. V_{CNTL} Supply



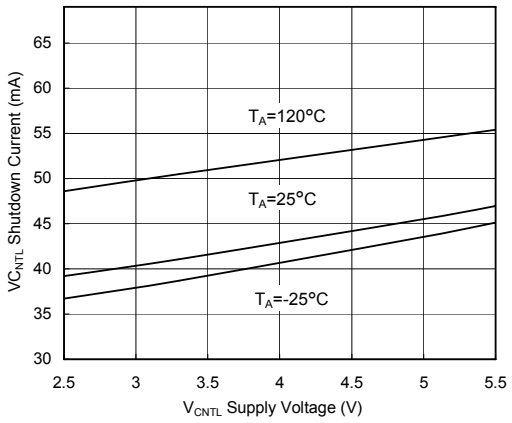
V_{CNTL} Supply Current vs. V_{OUT} Load



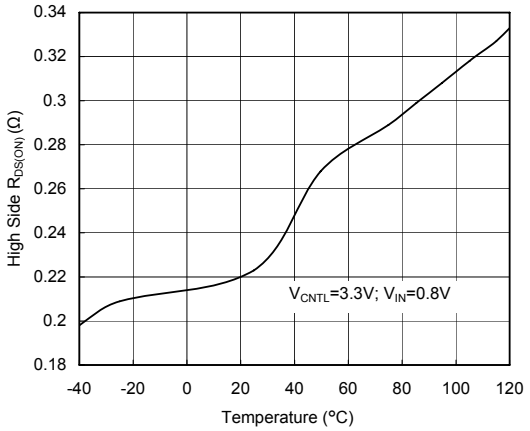
V_{CNTL} Shutdown Current vs. Temperature



V_{CNTL} Shutdown Current vs. V_{CNTL} Supply

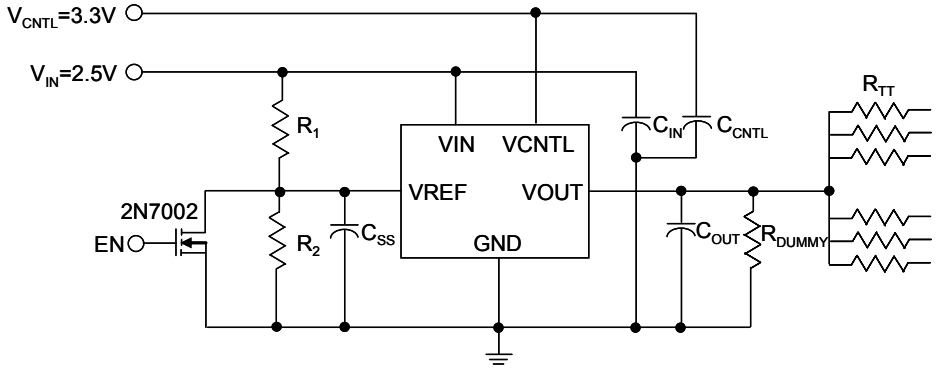


High Side $R_{DS(ON)}$ vs. Temperature

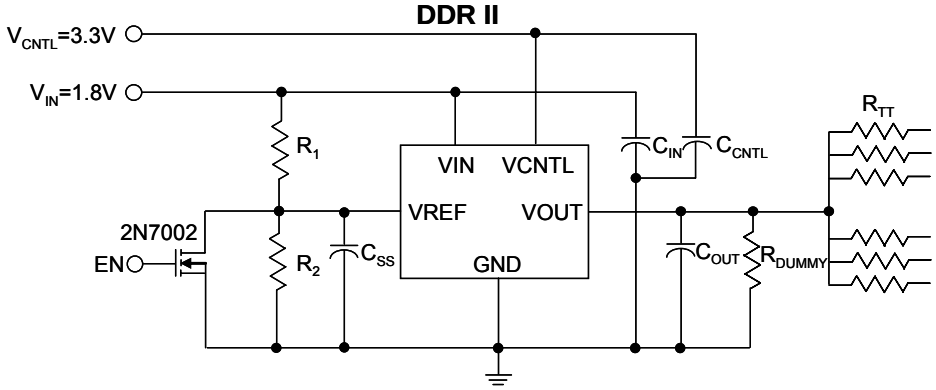


Typical Application Circuit

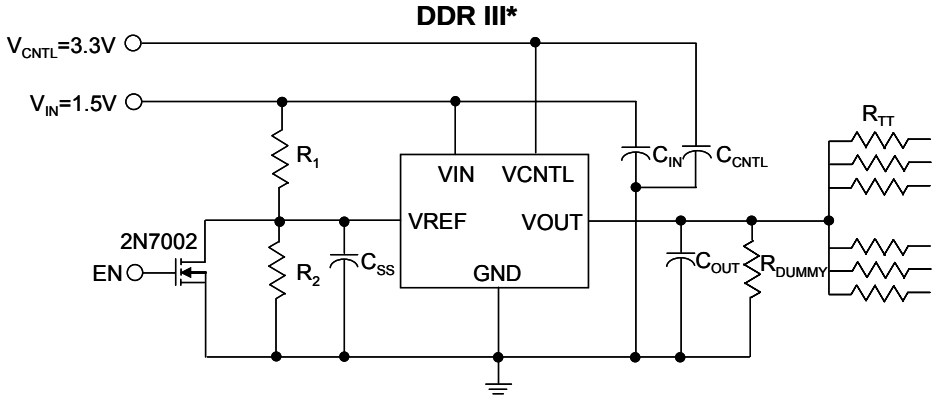
DDR I



DDR II



DDR III*

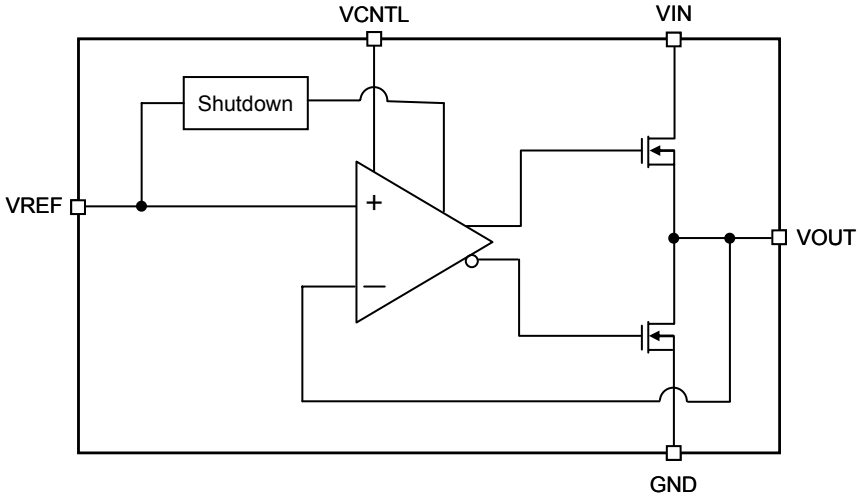


* Recommended V_{CTRL} =3.3V

Pin Description

PIN			NAME	FUNCTION
SOT-23-5	SOP-8	MSOP-8 (FD)		
1	2	2	GND	Ground
2	5,6,7,8	6	VCNTL	Internal circuit power pin.
3	1	1	VIN	Terminator power pin.
4	4	4	VOUT	Terminator output pin (V_{TT} voltage supplied)
5	3	3	VREF	Terminator reference input voltage, 1.25V for DDR I, 0.9V for DDR II, 0.75V for DDR III. Below 0.2V, the chip will be shutdown.
---	---	5,7,8	NC	No Connection
---	---	Thermal Pad		Recommend connecting the Thermal Pad to the GND for excellent power dissipation.

Block Diagram



Application Information

Output Capacitor

For stable operation, total capacitance of the V_{TT} output terminal can be equal or greater than 20μF. The output capacitor should be located near V_{TT} output terminal as close as possible to minimize the effect of ESR and ESL.

Power on sequence

For safely operation, The G2992B must keep V_{CNTL} voltage larger than V_{IN}, this condition is due to the internal parasitic diodes between V_{IN} to V_{CNTL}. The G2992B will consume large current when V_{IN} voltage is larger than V_{CNTL}.

Consideration of the V_{REF} Voltage

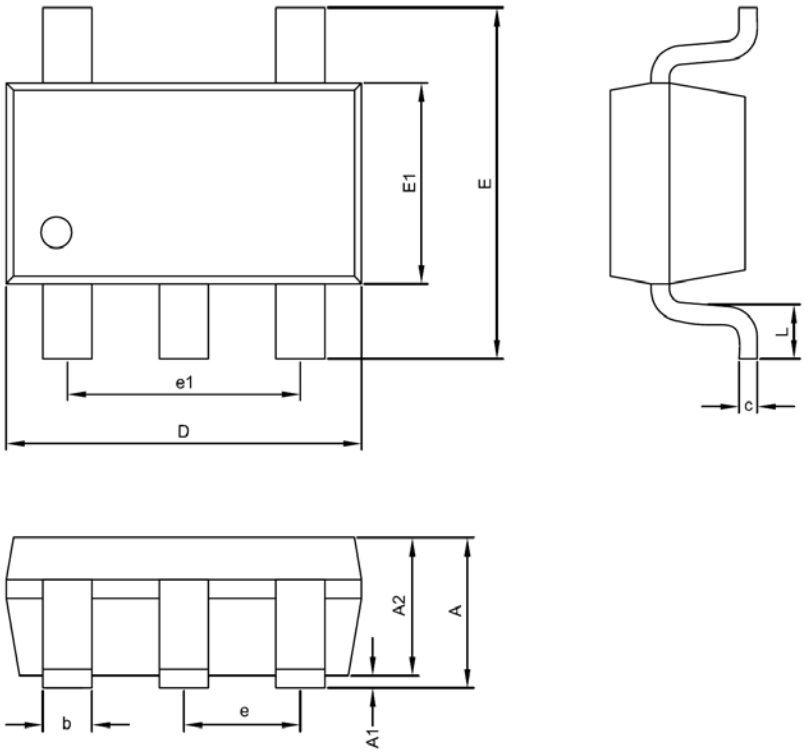
The V_{REF} voltage is applied by a buffered mid-rail voltage which is generated by a resistor divider between V_{IN} and GND. Using a capacitor tapped to the voltage divider can form a low-pass filter. It can increase both the soft-start interval and the noise immunity.

Input Capacitor

Adding a capacitance close to V_{IN} pin can improve the V_{TT} performance when fast load- transient. In general, 1/2 C_{OUT} is recommended for the V_{IN} capacitance. Separating the V_{IN} and V_{CNTL} pins will get better transient performance.

A ceramic capacitance with a value between 1.0μF and 4.7μF close to the V_{CNTL} pin is recommended to stabilize the V_{CNTL} voltage.

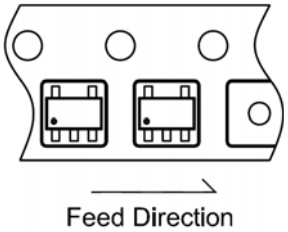
Package Information



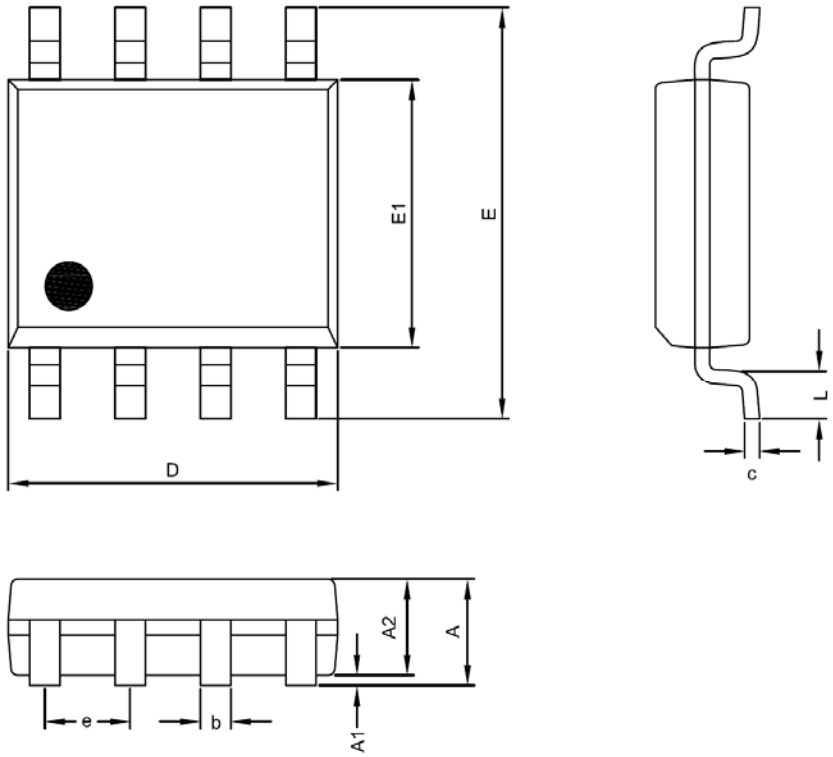
SOT-23-5 Package

Symble	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00	1.10	1.45	0.039	0.043	0.057
A1	0.00	- - -	0.15	0.000	- - -	0.006
A2	1.00	1.10	1.30	0.039	0.043	0.051
D	2.70	2.90	3.10	0.106	0.114	0.122
E	2.60	2.80	3.00	0.102	0.110	0.118
E1	1.50	1.60	1.70	0.059	0.063	0.067
c	0.08	0.15	0.25	0.003	0.006	0.010
b	0.30	0.40	0.50	0.012	0.016	0.020
e	0.95 BSC			0.037 BSC		
e1	1.90 BSC			0.075 BSC		
L	0.30	0.45	0.60	0.012	0.018	0.024

Taping Specification



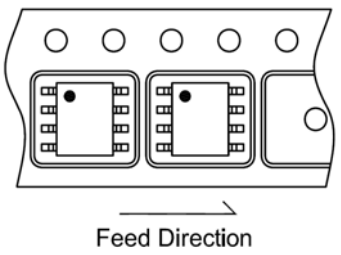
PACKAGE	Q'TY/REEL
SOT-23-5	3,000 ea



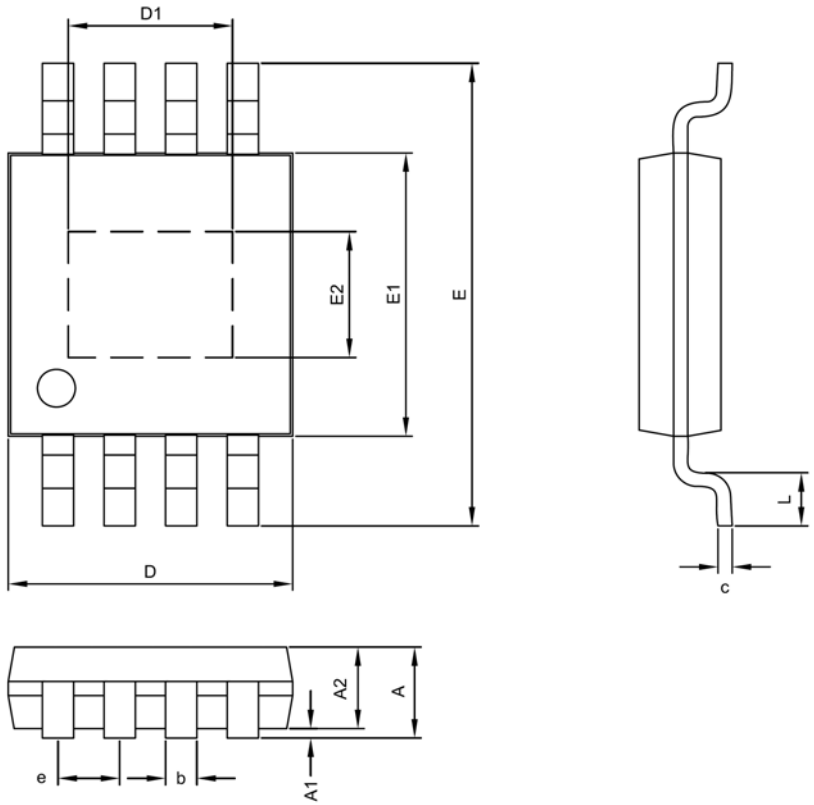
SOP-8 Package

Symble	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.35	1.55	1.75	0.053	0.061	0.069
A1	0.00	- - -	0.25	0.000	- - -	0.010
A2	1.15	1.35	1.50	0.045	0.053	0.059
D	4.80	4.90	5.00	0.189	0.192	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.153	0.157
c	0.19	0.23	0.27	0.007	0.009	0.011
b	0.33	0.43	0.53	0.013	0.017	0.021
e	1.27 BSC			0.050 BSC		
L	0.40	0.7	1.00	0.016	0.028	0.039

Taping Specification



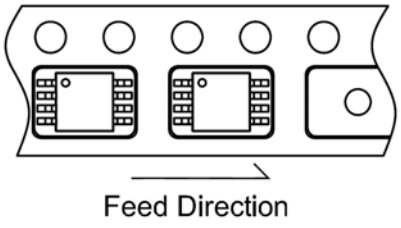
PACKAGE	Q'TY/REEL
SOP-8	2,500 ea



MSOP-8 (FD) Package

Symble	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.81	0.95	1.10	0.032	0.037	0.043
A1	0.00	- - -	0.15	0.000	- - -	0.006
A2	0.76	0.86	0.96	0.030	0.034	0.038
D	2.85	3.00	3.15	0.112	0.118	0.124
D1	1.40	1.90	2.10	0.055	0.074	0.083
E	4.75	4.90	5.05	0.187	0.193	0.199
E1	2.85	3.00	3.15	0.112	0.118	0.124
E2	1.35	1.60	1.75	0.053	0.063	0.069
c	0.13	0.15	0.23	0.005	0.006	0.009
b	0.28	0.30	0.38	0.011	0.012	0.015
e	0.65 TYP.			0.026 TYP.		
L	0.4	0.53	0.8	0.016	0.021	0.031

Taping Specification



PACKAGE	Q'TY/REEL
MSOP-8 (FD)	3,000 ea