G5193

High Efficiency, 3A Output, Synchronous Step Down

Features

- **Two 45mΩ (typical) MOSFETs for high efficiency at 3A loads**
- **300kHz to 2MHz Switching Frequency**
- **0.827V±1% Voltage Reference Over Temperature**
- **Synchronizes to External Clock**
- **Adjustable Soft Start**
- **UV and OV Power Good Output**
- **Low Operating and Shutdown Quiescent Current**
- **Safe Start-up into Pre-Biased Output**
- **Cycle by Cycle Current Limit, Thermal and Frequency Fold Back Protection**
- **Thermally Enhanced 3mm × 3mm 16-pin QFN**

Applications

- **Low-Voltage, High-Density Power Systems**
- **Point of Load Regulation for High Performance DSPs, FPGAs, ASICs and Microprocessors**
- **Broadband, Networking and Optical Communication Infrastructure**

General Description

The G5193 device is a full featured 5.5V, 3A synchronous step down current mode converter with two integrated MOSFETs.

The G5193 enables small designs by integrating the MOSFETs, implementing current mode control to reduce external component count, reducing inductor size by enabling up to 2MHz switching frequency, and minimizing the IC footprint with a small 3mm x 3mm thermally enhanced QFN package.

The G5193 provides accurate regulation for a variety of loads with an accurate ±1% Voltage Reference (VREF) over temperature.

Efficiency is maximized through the integrated 45mΩ MOSFETs and 350μA typical supply current. Using the enable pin, shutdown supply current is reduced to 2μA by entering a shutdown mode.

Under voltage lockout is internally set at 2.6V, but can be increased by programming the threshold with a resistor network on the enable pin. The output voltage startup ramp is controlled by the soft start pin. An open drain power good signal indicates the output is within 93% to 107% of its nominal voltage.

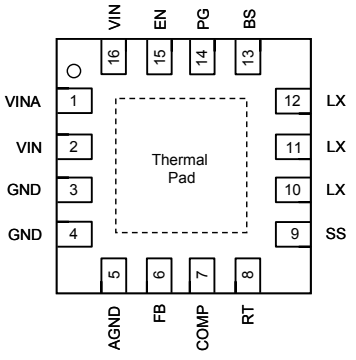
Frequency fold back and thermal shutdown protects the device during an over-current condition.

Ordering Information

ORDER NUMBER	Marking	TEMP. RANGE	PACKAGE (Green)
G5193R41U	5193	-40°C to +85°C	TQFN3X3-16
G5193R41D	5193	-40°C to +85°C	TQFN3X3-16

Note: R4: TQFN3X3-16
1: Bonding Code
U & D: Tape & Reel

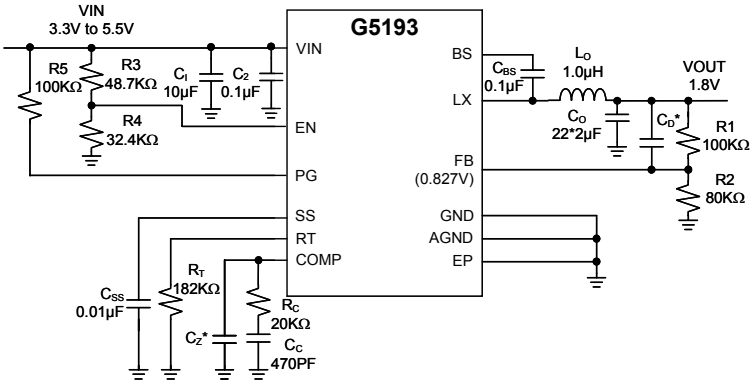
Pin Configuration



G5193 TQFN3X3-16

Note: Recommend connecting the Thermal Pad to the Ground for excellent power dissipation.

Typical Application Circuit



∗ Option

∗ VINA must connect to VIN

Absolute Maximum Ratings

VIN Power Input Voltage . . . . . -0.3V to +6.5V
EN, FB, COMP, PG, SS, RT, LX Pin Input/Output Voltage. . . . . .-0.3V to +6.5V
'BS - LX ' Voltage . . . . . -0.3V to +6.5V
LX Pin 10ns Transient . . . . . -2V to +8V
Thermal Resistance Junction to Ambient, (θ_{JA})*
TQFN3X3-16. . . . . 125°C/W
Continuous Power Dissipation (T_A = +25°C)*
TQFN3X3-16. . . . . .1080mW
Thermal Resistance Junction to Case, (θ_{Jc})
TQFN3X3-16. . . . . 39°C/W
Operation Temperature . . . . . .-40°C to +85°C
Storage Temperature . . . . . -55°C to +150°C
ESD Susceptibility (HBM) 2kV
ESD Susceptibility (MM) 200V

Operation Conditions

Power supply voltage. . . . . .2.95V to +5.5V
EN,SS PIN input voltage . . . . . .0 to VIN
Operating ambient temperature (T_A) . . .-20°C to +85°C

* Please refer to Minimum Footprint PCB Layout Section.

1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Device are ESD sensitive. Handling precaution recommended. The Human Body model is a 100pF capacitor discharged through a 1.5KΩ resistor into each pin.

Electrical Characteristics

(VIN=5V, T_A=25°C)

The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified.

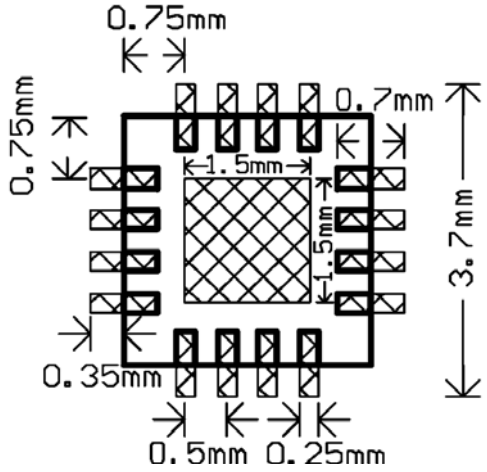
PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SUPPLY VOLTAGE (VIN PIN)						
VIN Operating input Voltage	V_{VIN}		2.95	---	5.5	V
Internal under voltage lockout threshold	$V_{UVLO(H2L)}$	hys. 20mV	---	2.6	2.8	V
Shutdown supply current	I_{SHDN}	EN = 0V, 25°C, 2.95V ≤ VIN ≤5.5V	---	2	5	μA
Quiescent current	I_Q	FB = 0.9V, VIN = 5V, Temp.=25°C, RT = 400kΩ	---	350	500	μA
ENABLE AND UVLO (EN PIN)						
EN Operating input Voltage	V_{EN}		0	---	VINA	V
Enable threshold	$V_{EN\_UVE\_R}$	Rising	1.16	1.25	1.37	V
	$V_{EN\_UVE\_F}$	Falling	---	1.18	---	V
Input current	I_{IN1}	Enable threshold +50mV	---	-3.2	---	μA
	I_{IN2}	Enable threshold –50mV	---	-0.65	---	μA
VOLTAGE REFERENCE (FB PIN)						
Voltage Reference	V_{FB}	2.95V ≤ VIN ≤ 5.5V	0.819	0.827	0.835	V
MOSFET						
High side switch resistance	R_{ON_HS}	BS-LX=5.0V	---	45	81	mΩ
		BS-LX=2.95V	---	64	110	
Low side switch resistance	R_{ON_LS}	VIN=5.0V	---	42	81	mΩ
		VIN=2.95V	---	59	110	
ERROR AMPLIFIER						
Input current	I_{ERROR}		---	7	---	nA
Error amplifier transconductance (gm)	GM_1	VCC=3.3V	---	225	---	μmhos
Error amplifier source/sink	I_{ERROR_MAX}	V(COMP)=0.827V, 100mV overdrive	---	±28	---	μA
COMP to ILX gm	GM_{COMP}		---	10	---	A/V

Electrical Characteristics (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CURRENT LIMIT						
Current limit threshold	I_{LIMIT}		4.5	6.4	---	A
Thermal Shutdown						
Thermal Shutdown Temperature	T_{TSD}	hys. 25deg.	---	160	---	°C
TIMING RESISTOR (RT PIN)						
Switching frequency range	F_{RANGE}		300	---	2000	KHz
Switching frequency	F_{500K}	Rt = 400kΩ	400	500	600	KHz
LX (LX PIN)						
Minimum off width	$TOFF_{MIN}$		---	60	---	nS
LX Current sensing delay width	LX_{MIN}		---	60	---	nS
Rise/Fall Time	$LX_{TR/TF}$		---	1.5	---	V/nS
BOOT (BS PIN)						
BOOT Charge Resistance	R_{BS}		---	15	---	Ω
BS-LX UVLO	$VUVE_{BS}$		---	2.1	---	V
Soft Start (SS PIN)						
Charge Current	I_{SS}	V(SS) = 0.4V	---	2	---	µA
SS to reference crossover	V_{SS}	98% nominal	---	0.9	---	V
SS discharge Current (overload)	I_{SSDIS1}	V(SS) = 0.4V	---	20	---	µA
SS discharge Current (UVLO,EN,THSD)	I_{SSDIS2}	V(SS) = 0.4V	---	1.25	---	mA
POWER GOOD (PG PIN)						
FB threshold	VPG_{LF}	FB falling (Fault)	---	91	---	% Vref
	VPG_{LR}	FB rising (Good)	---	93	---	% Vref
	VPG_{HR}	FB rising (Fault)	---	107	---	% Vref
	VPG_{HF}	FB falling (Good)	---	105	---	% Vref
Hysteresis		FB falling	---	2	---	% Vref
Output high leakage	IPG_{LEAK}	FB = VREF, V(PG) = 5.5V	---	2	---	nA
On resistance	R_{PG}		---	15	---	Ω
Output low		I(PG) = 3.5mA	---	0.3	---	V
Minimum VIN for valid output		V(PG) < 0.5V at 100A	---	1.2	1.6	V

Minimum Footprint PCB Layout Section

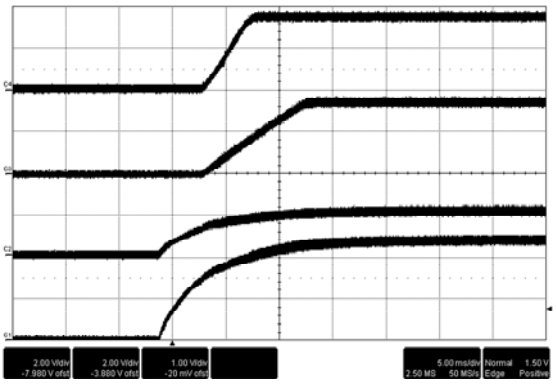
TQFN3X3-16



Typical Performance Characteristics

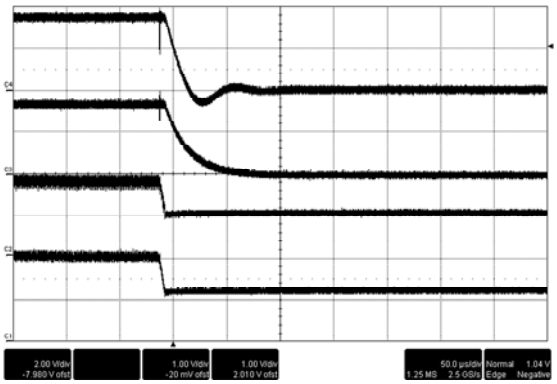
Condition: VIN=5V, VOUT=1.8V, Ci=10uF//0.1µF, Co=22µF*2, L=1µH, Css=10nF

Power ON



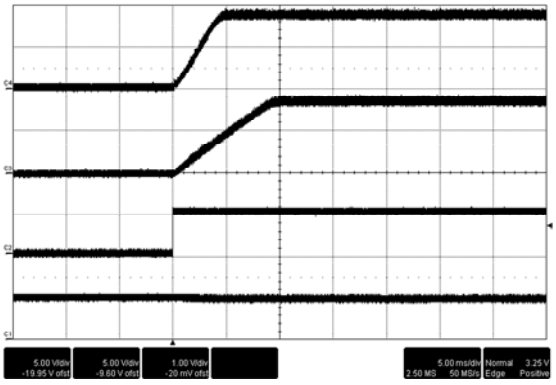
CH1:VIN(2V/div), CH2:EN(2V/div), CH3:SS(1V/div), CH4:VOUT(1V/div)

Power OFF



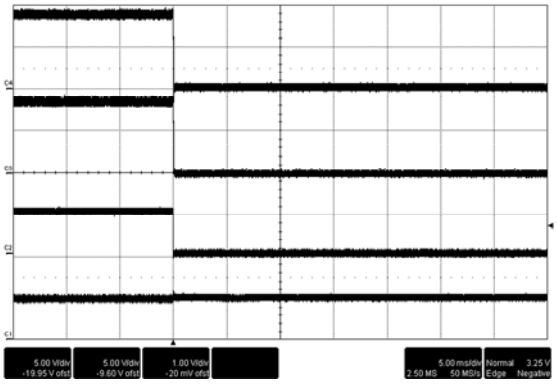
CH1:VIN(2V/div), CH2:EN(2V/div), CH3:SS(1V/div), CH4:VOUT(1V/div)

EN ON



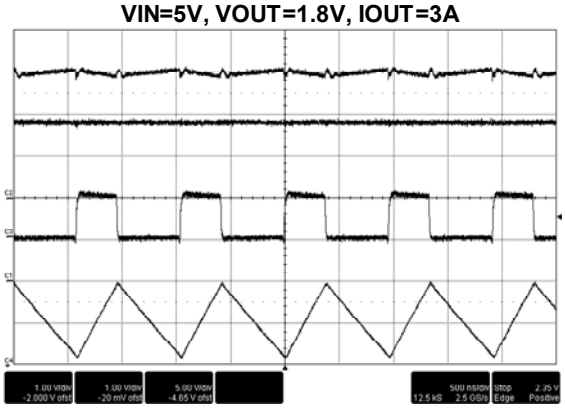
CH1:VIN(2V/div), CH2:EN(2V/div), CH3:SS(1V/div), CH4:VOUT(1V/div)

EN OFF



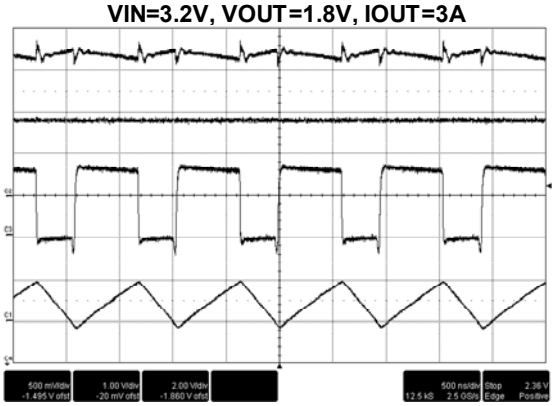
CH1:VIN(2V/div), CH2:EN(2V/div), CH3:SS(1V/div), CH4:VOUT(1V/div)

Steady State Waveforms
VIN=5V, VOUT=1.8V, IOUT=3A



CH1:VIN(1V/div), CH2:VOUT(1V/div), CH3:LX(2V/div), CH4:IL(500mA/div)

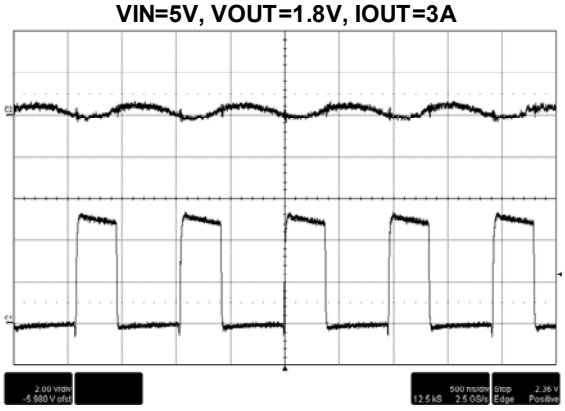
Steady State Waveforms
VIN=3.2V, VOUT=1.8V, IOUT=3A



CH1:VIN(500mV/div), CH2:VOUT(1V/div), CH3:LX(2V/div), CH4:IL(500mA/div)

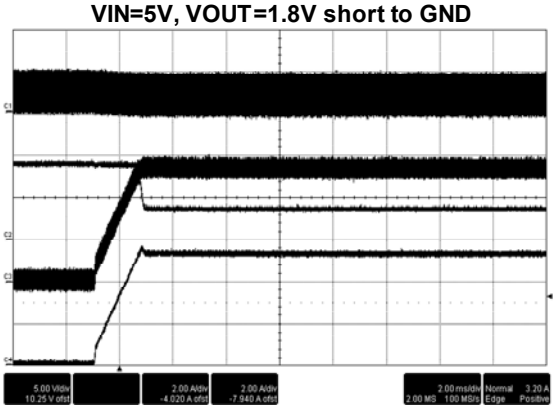
Typical Performance Characteristics (continued)

Output Voltage Ripple
VIN=5V, VOUT=1.8V, IOUT=3A



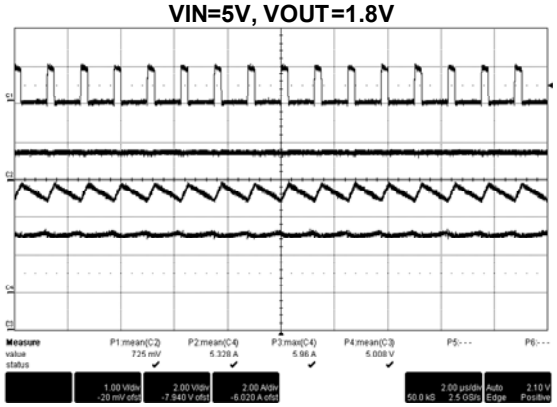
CH1:VIN(2V/div), CH2:VOUT(20mV/div)

Output Short Protection Test Waveforms
VIN=5V, VOUT=1.8V short to GND



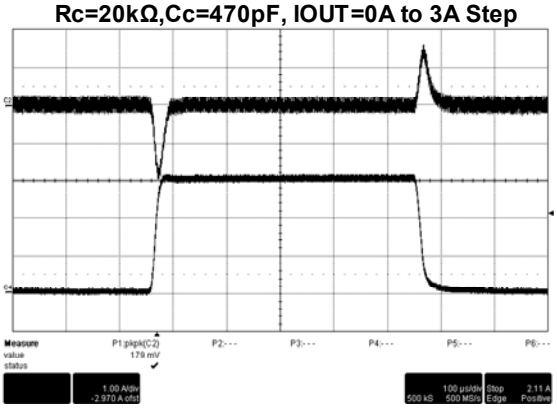
CH1:LX(5V/div), CH2:VOUT(1V/div), CH3:IL(2A/div), CH4:IOUT(2A/div)

Current Limit Protection Test Waveforms
VIN=5V, VOUT=1.8V



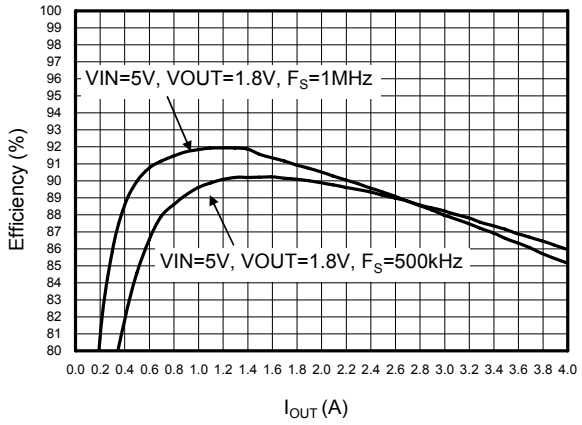
CH1:LX(5V/div), CH2:VOUT(1V/div), CH3:VIN(2V/div), CH4:IL(2A/div)

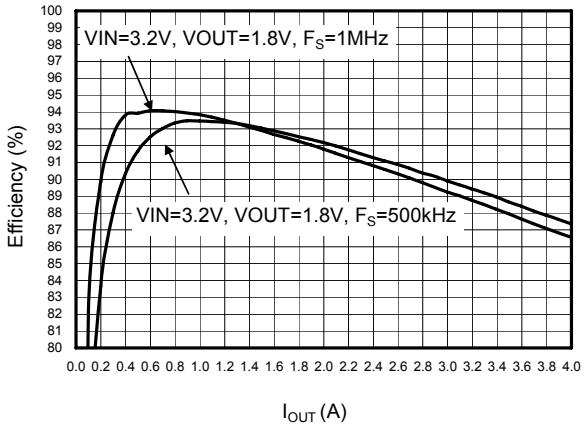
Load Transient Waveform
VIN=3.3V, VOUT=1.8V, L=1μH, C_{OUT}=22μF*2
Rc=20kΩ,Cc=470pF, IOUT=0A to 3A Step

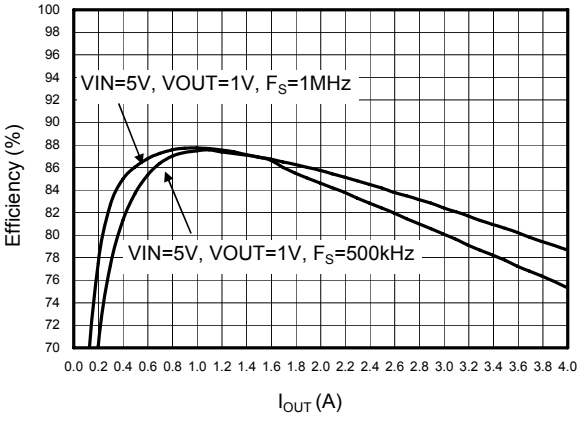


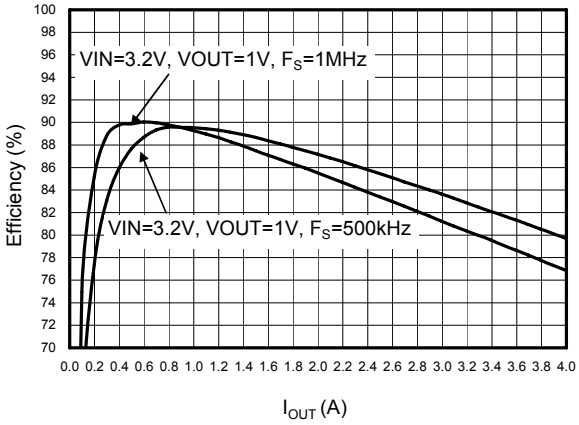
CH2:VOUT(50mV/div), CH4:IOUT(1A/div)

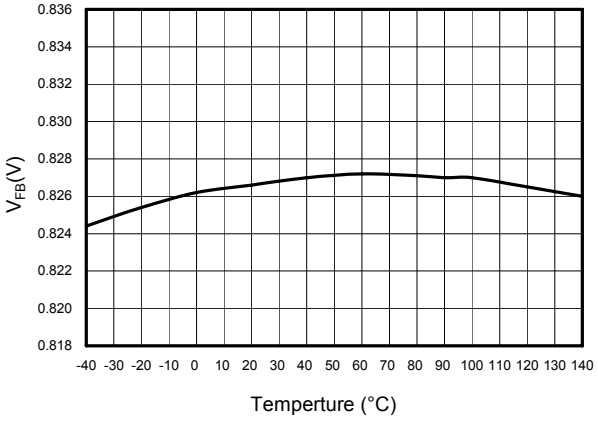
Typical Performance Characteristics (continued)











Pin Description

PIN NO.	SYMBOL	DESCRIPT
1	VINA	Input supply Analog voltage 2.95V to 5.5V (VINA must connect to VIN)
2,16	VIN	Input supply voltage 2.95V to 5.5V
3,4	GND	Power Ground. This pin should be electrically connected directly to the power pad under the IC.
5	AGND	Analog Ground should be electrically connected to GND close to the device.
6	FB	Inverting node of the transconductance (gm) error amplifier.
7	COMP	Error amplifier output, and input to the output switch current comparator. Connect frequency compensation components to this pin.
8	RT	Resistor Timing input pin.
9	SS	Soft-start. An external capacitor connected to this pin sets the output voltage rise time.
10,11,12	LX	The source of the internal high side power MOSFET, and drain of the internal low side (synchronous) rectifier MOSFET.
13	BS	A bootstrap capacitor is required between BOOT and PH. If the voltage on this capacitor is below the minimum required by the BOOT UVLO, the output is forced to switch off until the capacitor is refreshed.
14	PG	An open drain output, asserts low if output voltage is low due to thermal shutdown, over-current, over/under-voltage or EN shut down.
15	EN	Enable pin, internal pull-up current source. Pull below 1.2V to disable. Float to enable. Can be used to set the on/off threshold (adjust UVLO) with two additional resistors.
PGND	EP	Exposed PAD should be soldered to PCB and connected to GND

Block Diagram

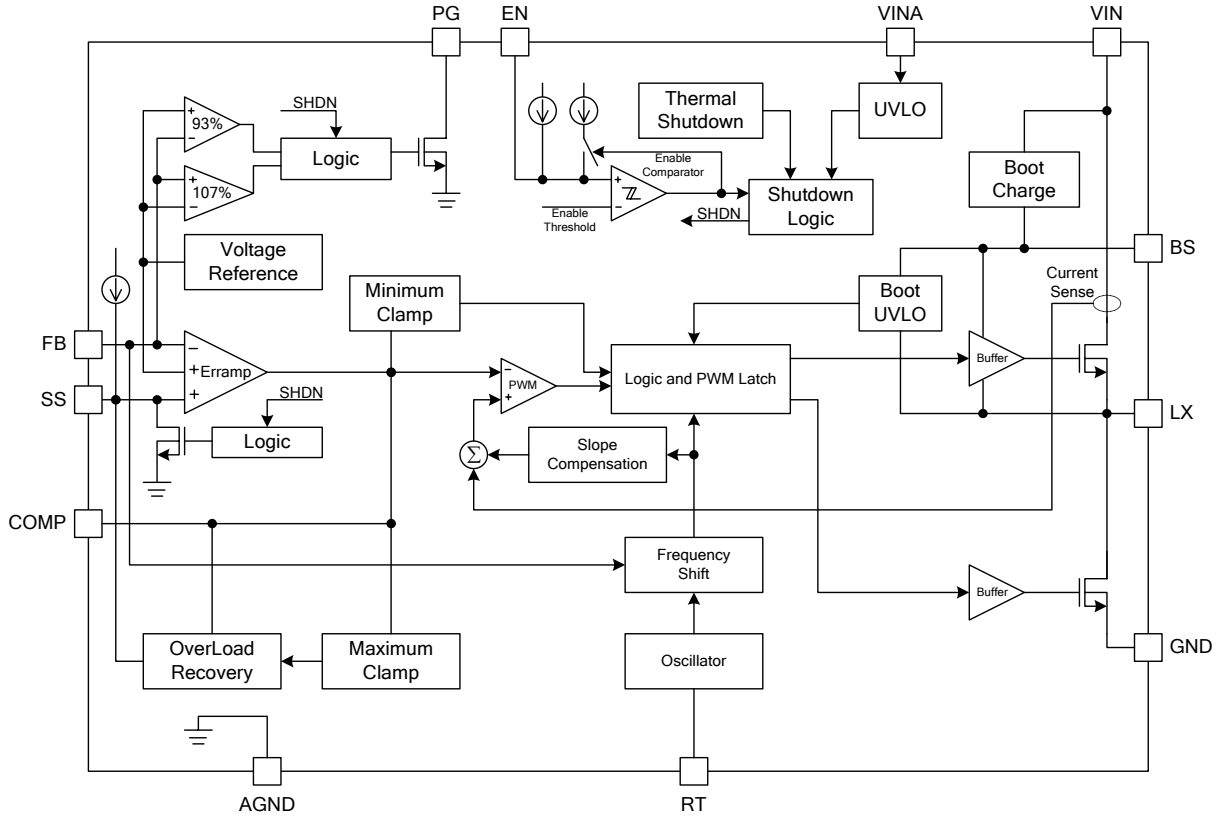


Fig. Block Diagram of G5193

Application Information

OVERVIEW

The G5193 is a 5.5V, 3A, synchronous step-down (buck) converter with two integrated n-channel MOSFETs. To improve performance during line and load transients the device implements a constant frequency, peak current mode control which reduces output capacitance and simplifies external frequency compensation design.

The wide switching frequency of 300kHz to 2000kHz allows for efficiency and size optimization when selecting the output filter components. The switching frequency is adjusted using a resistor to ground on the RT pin.

The G5193 has a typical default start up voltage of 2.6V. The EN pin has an internal pull-up current source that can be used to adjust the input voltage under voltage lockout (UVLO) with two external resistors. In addition, the pull up current provides a default condition when the EN pin is floating for the device to operate. The total operating current for the G5193 is 350μA when not switching and under no load. When the device is disabled, the supply current is less than 2μA.

The integrated 45 mΩ MOSFETs allow for high efficiency power supply designs with continuous output currents up to 3 amperes.

The G5193 reduces the external component count by integrating the boot recharge diode. The bias voltage for the integrated high side MOSFET is supplied by a capacitor on the BS to LX pin. The boot capacitor voltage is monitored by an UVLO circuit and turns off the high side MOSFET when the voltage falls below a preset threshold. This BOOT circuit allows the G5193 to operate approaching 100%. The output voltage can be stepped down to as low as the 0.827V reference.

The G5193 has a power good comparator (PG) with 2% hysteresis.

The G5193 minimizes excessive output overvoltage transients by taking advantage of the overvoltage power good comparator. When the regulated output voltage is greater than 109% of the nominal voltage, the overvoltage comparator is activated, and the high side MOSFET is turned off and masked from turning on until the output voltage is lower than 105%.

The SS (soft start) pin is used to minimize inrush currents or provide power supply sequencing during power up. A small value capacitor should be coupled to the pin for slow start. The SS pin is discharged before the output power up to ensure a repeatable restart after an over-temperature fault, UVLO fault or disabled condition.

The use of a frequency foldback circuit reduces the switching frequency during startup and over current fault conditions to help limit the inductor current.

FIXED FREQUENCY PWM CONTROL

The G5193 uses an adjustable fixed frequency, peak current mode control. The output voltage is compared through external resistors on the FB pin to an internal voltage reference by an error amplifier which drives the COMP pin. An internal oscillator initiates the turn on of the high side power switch. The error amplifier output is compared to the high side power switch current. When the power switch current reaches the COMP voltage level the high side power switch is turned off and the low side power switch is turned on.

The COMP pin voltage increases and decreases as the output current increases and decreases. The device implements a current limit by clamping the COMP pin voltage to a maximum level and also implements a minimum clamp for improved transient response performance.

SLOPE COMPENSATION AND OUTPUT CURRENT

The G5193 adds a compensating ramp to the switch current signal. This slope compensation prevents sub-harmonic oscillations as duty cycle increases. The available peak inductor current remains constant over the full duty cycle range.

BOOTSTRAP VOLTAGE (BS) AND LOW DROPOUT OPERATION

The G5193 has an integrated boot regulator and requires a small ceramic capacitor between the BS pin and LX pin to provide the gate drive voltage for the high side MOSFET. The value of the ceramic capacitor should be 0.1μF. A ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 10V or higher is recommended because of the stable characteristics over temperature and voltage.

To improve drop out, the G5193 is designed to operate at 100% duty cycle as long as the BS to LX pin voltage is greater than 2.5V. The high side MOSFET is turned off using an UVLO circuit, allowing for the low side MOSFET to conduct when the voltage from BS to LX drops below 2.5V. Since the supply current sourced from the BS pin is very low, the high side MOSFET can remain on for more switching cycles than are required to refresh the capacitor, thus the effective duty cycle of the switching regulator is very high.

ERROR AMPLIFIER

The G5193 has a transconductance amplifier. The error amplifier compares the FB voltage to the lower of the SS pin voltage or the internal 0.827V voltage reference. The transconductance of the error amplifier is 225μA/V during normal operation.

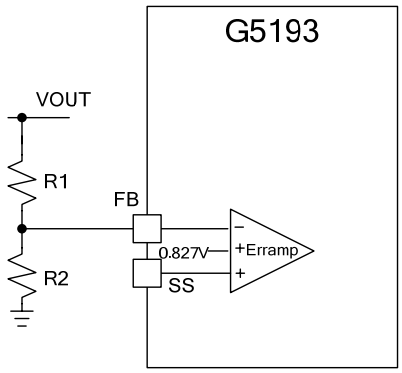
VOLTAGE REFERENCE

The voltage reference system produces a precise ±1% voltage reference over temperature by scaling the output of a temperature stable bandgap circuit. The bandgap and scaling circuits produce 0.827V at the non-inverting input of the error amplifier.

ADJUSTING THE OUTPUT VOLTAGE

The output voltage is set with a resistor divider from the output node to the FB pin. It is recommended to use divider resistors with 1% tolerance or better. Start with a 100kΩ for the R1 resistor and use the Equation 1 to calculate R2. To improve efficiency at very light loads consider using larger value resistors. If the values are too high the regulator is more susceptible to noise and voltage errors from the FB input current are noticeable.

$R2=R1*(0.827/ (V_{OUT}-0.827))$ ---- (Eq.1)



Voltage Divider Circuit

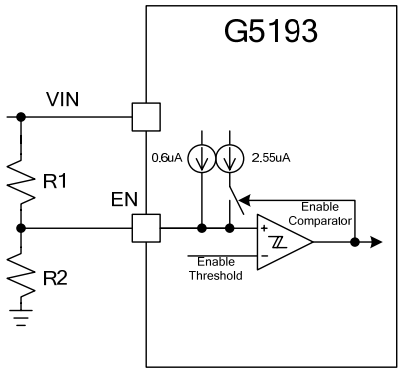
ENABLE AND ADJUSTING UNDER-VOLTAGE LOCKOUT

The G5193 is disabled when the VIN pin voltage falls below 2.6V. If an application requires a higher under-voltage lockout (UVLO), use the EN pin as shown below figure to adjust the input voltage UVLO by using two external resistors. It is recommended to use the enable resistors to set the UVLO falling threshold (VSTOP) above 2.7V. The rising threshold (VSTART) should be set to provide enough hysteresis to allow for any input supply variations. The EN pin has an internal pull-up current source that provides the default condition of the G5193 operating when the EN pin floats.

Once the EN pin voltage exceeds 1.25V, an additional 2.55μA of hysteresis is added. When the EN pin is pulled below 1.18V, the 2.55μA is removed. This additional current facilitates input voltage hysteresis.

$R1=(0.944*V_{START} - V_{STOP}) / (2.584*10^{-6})$ ----(Eq.2)

$R2=(1.18*R1) / (V_{STOP} -1.18 + R1*3.15*10^{-6})$ ----(Eq.3)



Adjustable Under Voltage Lock Out

SOFT START PIN

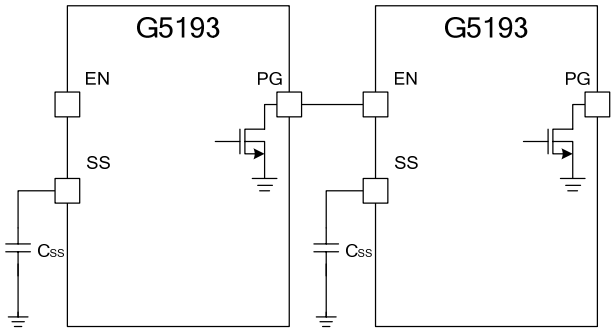
The G5193 regulates to the lower of the SS pin and the internal reference voltage. A capacitor on the SS pin to ground implements a soft start time. The G5193 has an internal pull-up current source of 2μA which charges the external slow start capacitor. Equation 4 calculates the required slow start capacitor value where Tss is the desired slow start time in ms, Iss is the internal slow start charging current of 2μA, and Vref is the internal voltage reference of 0.827V.

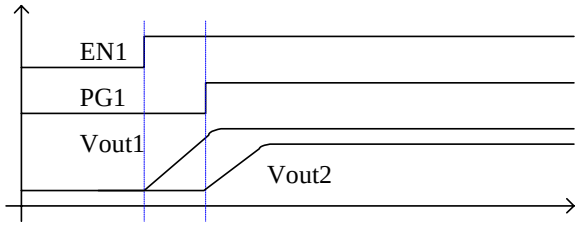
$$C_{SS(nF)} = (T_{SS(mS)} * I_{SS(\mu A)}) / Vref(V) \text{ ---- (Eq.4)}$$

If during normal operation, the VIN goes below the UVLO, EN pin pulled below 1.2V, or a thermal shutdown event occurs, the G5193 stops switching and the SS is discharged to 0 volts before reinitiating a powering up sequence.

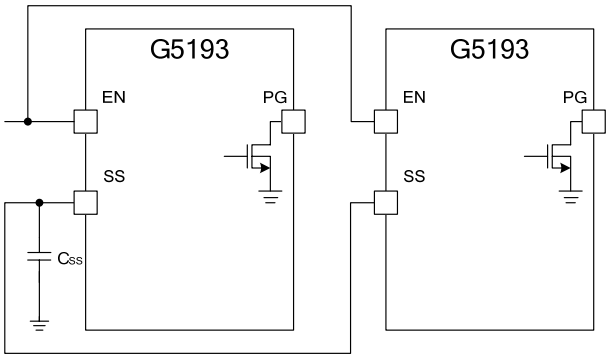
SEQUENCING

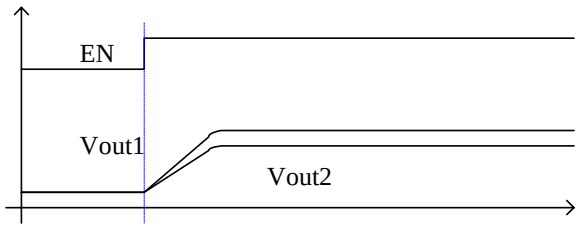
Many of the common power supply sequencing methods can be implemented using the SS, EN and PG pins. The sequential method can be implemented using an open drain or collector output of a power on reset pin of another device. Below figure shows the sequential method. The power good is coupled to the EN pin on the G5193 which enables the second power supply once the primary supply reaches regulation.





Ratiometric start up can be accomplished by connecting the SS pins together. The regulator outputs ramp up and reach regulation at the same time. When calculating the slow start time the pull up current source must be doubled in Equation 4. The ratiometric method is illustrated below figure.





CONSTANT SWITCHING FREQUENCY and TIMING RESISTOR

The switching frequency of the G5193 is adjustable over a wide range from 300kHz to 2000kHz by placing a maximum of 1000kΩ and minimum of 85kΩ, respectively, on the RT pin. An internal amplifier holds this pin at a fixed voltage when using an external resistor to ground to set the switching frequency. The RT is typically 0.5V. To determine the timing resistance for a given switching frequency, use the curve in Figures TBD and TBD, or Equation 5.

$$RT_{(K\Omega)} = 311890 / (F_{SW(KHz)})^{1.0793} \quad \text{---- (Eq.5)}$$

$$(F_{SW(KHz)} = 133870 / RT_{(K\Omega)})^{0.9393} \quad \text{---- (Eq.6)}$$

To reduce the solution size one would typically set the switching frequency as high as possible, but tradeoffs of the efficiency, maximum input voltage and minimum controllable on time should be considered.

OVERCURRENT PROTECTION

The G5193 implements a cycle by cycle current limit. During each switching cycle the high side switch current is compared to the voltage on the COMP pin. When the instantaneous switch current intersects the COMP voltage, the high side switch is turned off. During overcurrent conditions that pull the output voltage low, the error amplifier responds by driving the COMP pin high, increasing the switch current. The error amplifier output is clamped internally. This clamp functions as a switch current limit.

FREQUENCY SHIFT

To operate at high switching frequencies and provide protection during overcurrent conditions, the G5193 implements a frequency shift. If frequency shift was not implemented, during an overcurrent condition the low side MOSFET may not be turned off long enough to reduce the current in the inductor, causing a current runaway. With frequency shift, during an overcurrent condition the switching frequency is reduced from 100%, then 75%, then 50%, then 25% as the voltage decreases from 0.827 to 0 volts on FB pin to allow the low side MOSFET to be off long enough to decrease the current in the inductor. During start-up, the switching frequency increases as the voltage on FB increases from 0 to 0.827 volts.

REVERSE OVERCURRENT PROTECTION

The G5193 implements low side current protection by detecting the voltage across the low side MOSFET. When the converter sinks current through its low side FET, the control circuit turns off the low side MOSFET if the reverse current is more than 1.4A. By implementing this additional protection scheme, the converter is able to protect itself from excessive current during power cycling and start-up into pre-biased outputs.

POWER GOOD (PG PIN)

The PG pin output is an open drain MOSFET. The output is pulled low when the FB voltage enters the fault condition by falling below 91% or rising above 107% of the nominal internal reference voltage. There is a 2% hysteresis on the threshold voltage, so when the FB voltage rises to the good condition above 93% or falls below 105% of the internal voltage reference the PG output MOSFET is turned off. It is recommended to use a pull-up resistor between the values of 1kΩ and 100kΩ to a voltage source that is 5.5V or less. The PG is in a valid state once the VIN input voltage is greater than 1.2V.

OVERVOLTAGE TRANSIENT PROTECTION

The G5193 incorporates an overvoltage transient protection (OVTP) circuit to minimize voltage overshoot when recovering from output fault conditions or strong unload transients. The OVTP feature minimizes the output overshoot by implementing a circuit to compare the FB pin voltage to the OVTP threshold which is 109% of the internal voltage reference. If the FB pin voltage is greater than the OVTP threshold, the high side MOSFET is disabled preventing current from flowing to the output and minimizing output overshoot. When the FB voltage drops lower than the OVTP threshold the high side MOSFET is allowed to turn on the next clock cycle.

THERMAL SHUTDOWN

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 160°C. The thermal shutdown forces the device to stop switching when the junction temperature exceeds the thermal trip threshold. Once the die temperature decreases below 135°C, the device reinitiates the power up sequence by discharging the SS pin to 0 volts. The thermal shutdown hysteresis is 25°C.

SMALL SIGNAL MODEL FOR LOOP RESPONSE

Figure-3A shows an equivalent model for the G5193 control loop which can be modeled in a circuit simulation program to check frequency response and dynamic load response. The error amplifier is a trans-conductance amplifier with a gm of 225 μA/V. The error amplifier can be modeled using an ideal voltage controlled current source. The resistor Ro and capacitor Co model the open loop gain and frequency response of the amplifier. The 1mV AC voltage source between the nodes a and b effectively breaks the control loop for the frequency response measurements. Plotting a/c shows the small signal response of the frequency compensation. Plotting a/b shows the small signal response of the overall loop. The dynamic loop response can be checked by replacing the RL with a current source with the appropriate load step amplitude and step rate in a time domain analysis.

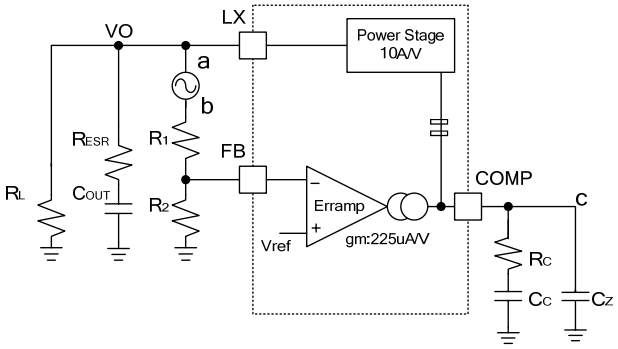


Figure-3A : Small Signal Model for Loop Response

SIMPLE SMALL SIGNAL MODEL FOR PEAK CURRENT MODE CONTROL

Figure-3A of the above is a simple small signal model that can be used to understand how to design the frequency compensation. The G5193 power stage can be approximated to a voltage controlled current source (duty cycle modulator) supplying current to the output capacitor and load resistor. The control to output transfer function is shown in Equation 7 and consists of a dc gain, one dominant pole and one ESR zero. The quotient of the change in switch current and the change in COMP pin voltage (node c in figure-3A) is the power stage trans-conductance. The gm for the G5193 is 10.0 A/V. The low frequency gain of the power stage frequency response is the product of the trans-conductance and the load resistance as shown in Equation 8. As the load current increases and decreases, the low frequency gain decreases and increases, respectively. This variation with load may seem problematic at first glance, but the dominant pole moves with load current [see Equation 9]. The combined effect is highlighted by the dashed line in the right half of figure-3B. As the load current decreases, the gain increases and the pole frequency lowers, keeping the 0dB crossover frequency the same for the varying load conditions which makes it easier to design the frequency compensation.

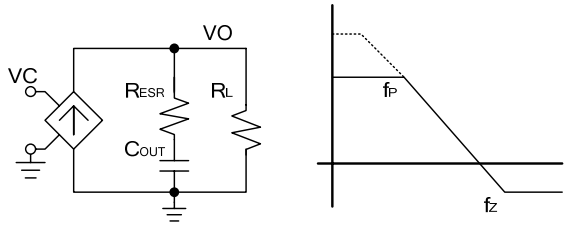


Figure 3B : Simple Small Signal Model and Frequency Response for Peak Current Mode Control

$$\frac{vo}{vc} = Adc \times \frac{\left(1+\frac{s}{2\pi \times fz}\right)}{\left(1+\frac{s}{2\pi \times fp}\right)} \quad \text{---- (Eq.7)}$$

$$Adc = gm_{ps} \times R_L \quad \text{---- (Eq.8)}$$

$$fp = \frac{1}{C_{OUT} \times R_L \times 2\pi} \quad \text{---- (Eq.9)}$$

$$fz = \frac{1}{C_{OUT} \times R_{ESR} \times 2\pi} \quad \text{---- (Eq.10)}$$

SMALL SIGNAL MODEL FOR FREQUENCY COMPENSATION

The G5193 uses a trans-conductance amplifier for the error amplifier and readily supports two of the commonly used frequency compensation circuits. The compensation circuits are shown in Figure 3C. The Type 2 circuits are most likely implemented in high bandwidth power supply designs using low ESR output capacitors. In Type 2, one additional high frequency pole is added to attenuate high frequency noise.

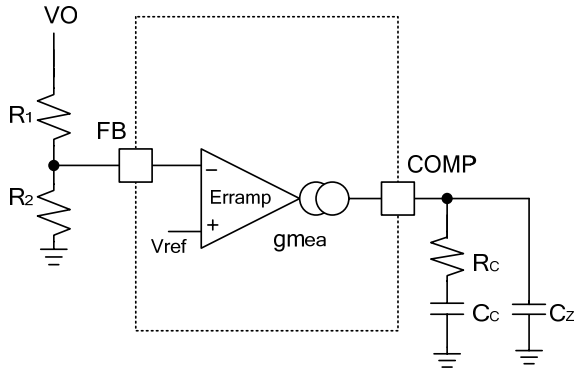


Figure 3C : Types of Frequency Compensation

The design guidelines for G5193 loop compensation are as follows:

1. The modulator pole (fpmod) and the esr zero(fzmod) must be calculated using Equation 11 and Equation 12. Derating the output capacitor (COUT) may be needed if the output voltage is a high percentage of the capacitor rating. Use the capacitor manufacturer information to derate the capacitor value. Use Equation 13 and Equation 14 to estimate a starting point for the crossover frequency, fc. Equation 13 is the geometric mean of the modulator pole and the esr zero and Equation 14 is the mean of modulator pole and the switching frequency. Use the lower value of Equation 13 or Equation 14 as the maximum crossover frequency (fc).

$$fp\,mod = \frac{loutmax}{2\pi \times Vout \times Cout} \quad \text{---- (Eq.11)}$$

$$fz\,mod = \frac{1}{2\pi \times Resr \times Cout} \quad \text{---- (Eq.12)}$$

$$f_C = \sqrt{fp\,mod \times fz\,mod} \quad \text{---- (Eq.13)}$$

$$f_C = \sqrt{fp\,mod \times \frac{fsw}{2}} \quad \text{---- (Eq.14)}$$

2. R_C can be determined by

$$R_C = \frac{2\pi \times fc \times Vo \times C_{OUT}}{gm_{ea} \times Vref \times gm_{ps}} \quad \text{---- (Eq.15)}$$

Where is the gm_{ea} amplifier gain (225 μA/V), gm_{ps} is the power stage gain (10 A/V).

3. Place a compensation zero at the dominant pole :

$$fp = \frac{1}{C_{OUT} \times R_L \times 2\pi}$$

C_C can be determined by :

$$C_C = \frac{R_L \text{ X } C_{OUT}}{R_C} \quad \text{---- (Eq.16)}$$

4. Cz is optional. It can be used to cancel the zero from Cout's ESR.

$$C_Z = \frac{R_{ESR} \text{ X } C_{OUT}}{R_C} \quad \text{---- (Eq.17)}$$

Layout Guide

Layout is a critical portion of good power supply design. There are several signal paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance.

1. Care should be taken to minimize the loop area formed by the bypass capacitor connections and the VIN pins. The AGND pins and GND pin should be tied directly to the power pad under the IC. The power pad should be connected to any internal PCB ground planes using multiple vias directly under the IC. Additional vias can be used to connect the top side ground area to the internal planes near the input and output capacitors.

2. The top side ground area along with any additional internal ground planes must provide adequate heat dissipating area for operation at full rated load.

3. Locate the input bypass capacitor as close to the IC as possible. The LX pin should be routed to the output inductor. Since the LX connection is the switching node, the output inductor should be located very close to the LX pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling.

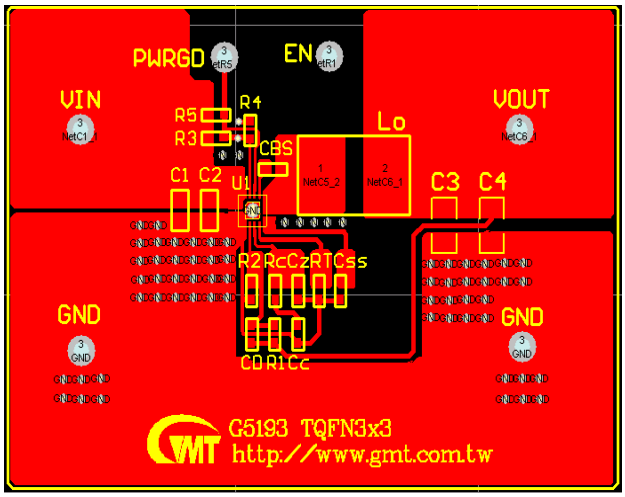
4. The boot capacitor must also be located close to the device. The sensitive analog ground connections for the feedback voltage divider, compensation components, slow start capacitor and frequency set resistor should be connected to a separate analog ground trace as shown.

5. The RT pin is particularly sensitive to noise so the RT resistor should be located as close as possible to the IC and routed with minimal lengths of trace. The additional external components can be placed approximately as shown.

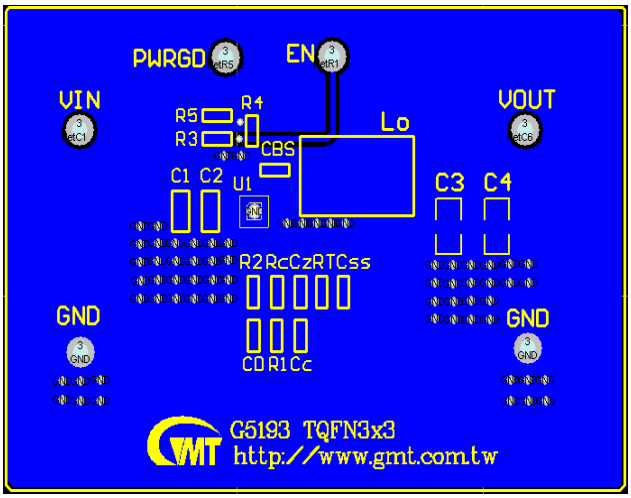
It may be possible to obtain acceptable performance with alternate PCB layouts, however this layout has been shown to produce good results and is meant as a guideline.

EVB PCB Layout

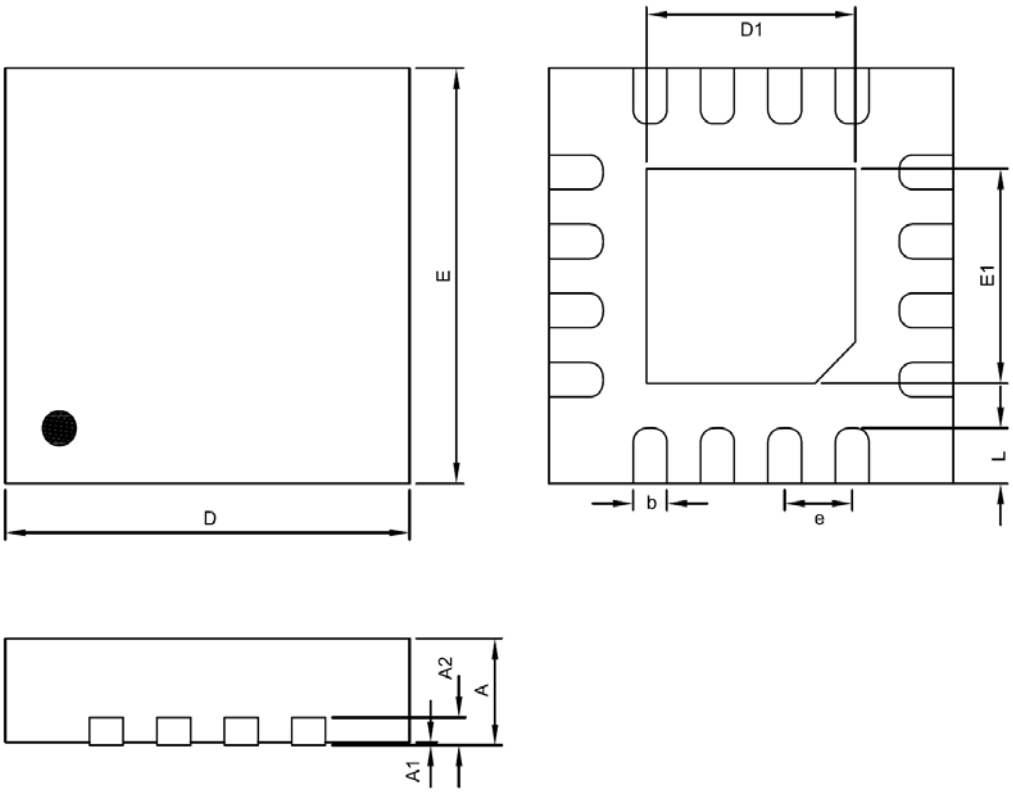
Top Layer



Bottom Layer



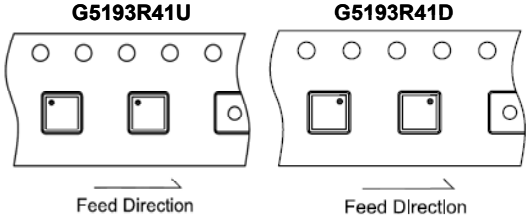
Package Information



TQFN3X3-16 (R4) Package

Symble	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.0276	0.0295	0.0315
A1	0.00	---	0.05	0.0000	---	0.0020
A2	0.19	0.20	0.21	0.0075	0.0079	0.0083
D	2.95	3.00	3.05	0.1161	0.1181	0.1201
E	2.95	3.00	3.05	0.1161	0.1181	0.1201
D1	1.50	1.60	1.75	0.0591	0.0630	0.0689
E1	1.50	1.60	1.75	0.0591	0.0630	0.0689
b	0.18	0.25	0.30	0.0071	0.0098	0.0118
e	0.50 BSC			0.0197 BSC		
L	0.35	0.40	0.45	0.0138	0.0157	0.0177

Taping Specification



PACKAGE	Q'TY/REEL
TQFN3X3-16	3,000 ea