High Efficiency 8A Synchronous Buck Converter

Features

- **Ultra-High Efficiency**
- **Integrated 20mΩ at Vcc=5V N-Channel MOSFET for Low Side**
- **Integrated 20mΩ at Vcc=5V N-Channel MOSFET for High Side**
- **No Current-Sense Resistor (Lossless I_{LIMIT})**
- **Quasi-PWM with 100ns Load-Step Response**
- **1% VOUT Accuracy Over Line and Load**
- **Programmable Switching Frequency**
- **Adjustable Output Range from 0.75V**
- **4.5V to 28V Adapter or Battery Input Range**
- **Integrated Boost Switch**
- **OVP & UVP**
- **Over Temperature Protection (non-latch)**
- **3.3ms Soft-Start**
- **Power-Good Indicator**
- **Fixed 5V, 20mA Linear Regulator**

Applications

- **LCD Monitor/LCD TV**
- **Notebook Computers**
- **I/O Supply**
- **Chipset/RAM Supply as Low as 0.75V**
- **Networking Power Supply**

General Description

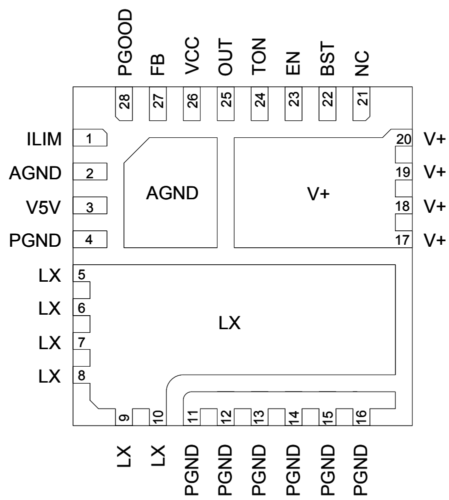
G5312 is a 8A, synchronous DC/DC buck converter with integrated 20mΩ N-channel high-side MOSFET and 20mΩ N-channel low-side MOSFET. It uses constant on-time control scheme to handle wide input/output voltage ratios with ease and provides 100ns “instant-on” response to load transients while maintaining a relatively constant switching frequency. The G5312 achieves high efficiency at a reduced cost by eliminating the current-sense resistor found in traditional current-mode PWMs. Single-stage buck conversion allows these devices to directly step down high-voltage batteries for the highest possible efficiency. The built-in 5V LDO supports 20mA for internal circuits. The G5312 is intended for the main power supply of LCD TV, Notebook Computer, or other low-voltage supplies as low as 0.75V. The G5312 is available in QFN4X4-28 package.

Ordering Information

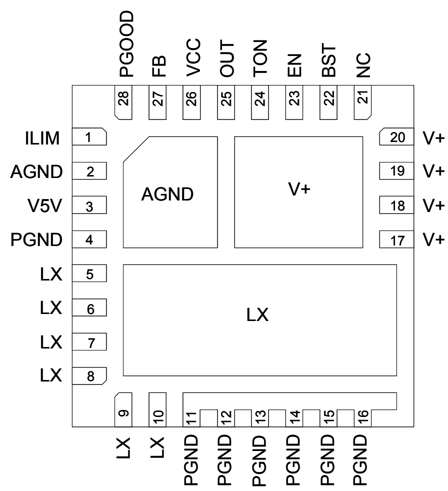
ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE (Green)
G5312QN1U	5312	-40°C to +85°C	QFN4X4-28
G5312QN2U	5312	-40°C to +85°C	QFN4X4-28

Note: QN: QFN4X4-28
1 & 2: Leadframe Code
U : Tape & Reel
Green: Lead Free / Halogen Free

Pin Configuration



G5312QN1U QFN4X4-28



G5312QN2U QFN4X4-28

Note: Recommend connecting the Thermal Pad to the Ground for excellent power dissipation.

Absolute Maximum Ratings

V+ . . . . -0.3V to 30V
VCC, V5V to AGND . . . . -0.3V to 6V
EN, PGOOD, OUT to AGND . . . .-0.3V to 6V
FB, TON, ILIM to AGND . . . .-0.3V to (VCC+0.3V)
BST to PGND . . . . -0.3V to 35V
LX to BST . . . . -6V to 0.3V
LX to PGND . . . .-0.3V to 30V
<20ns. . . . .-3V to 36V

Thermal Resistance of Junction to Ambient (θ_{JA})
QFN4X4-28 . . . . 25°C/W
Thermal Resistance of Junction to Case, (θ_{JC})
QFN4X4-28. . . . . .10°C/W
Junction Temperature . . . . .150°C
Storage Temperature . . . . -65°C to 150°C
Reflow Temperature (soldering, 10sec) . . . . . . 260°C

Electrical Characteristics

(VIN=15V, V_{CC}=V5V, EN=5V, T_A=25°C)

The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V+ Input Voltage Range	V+	4.5	---	28	V
LDO Output Voltage	V5V	4.75	4.95	5.25	V
Line Regulation of V5V	Load = 1mA, V+ = 8V to 28V	---	5	30	mV
Load Regulation of V5V	Load = 20mA	---	50	100	mV
Dropout Voltage of V5V	Load = 10mA	---	0.45	0.7	V
VCC Input Voltage Range	V_{CC}	4.5	---	5.5	V
Error Comparator Threshold (DC Output Voltage Accuracy)	V+ = 15V, FB = OUT	0.7425	0.75	0.7575	V
Soft-Start Ramp Time	Rising edge of EN to 95% output voltage	---	3.3	---	ms
TON Operating Current	R_{TON} = 1000kΩ, V+ = 15V	---	15	---	µA
On Time	VLX=12V, VOUT=1.05V, R_{TON} = 300kΩ, nominal	---	310	---	ns
Minimum On Time	VOUT=0.1V, R_{TON} = 300kΩ	---	80	---	ns
Minimum Off Time	FB=0.7V, LX=-0.1V, ILIM = open	---	400	---	ns
Quiescent Supply Current (V_{CC})	FB forced above the regulation point	---	536	750	µA
Quiescent Supply Current (V+)		---	94	120	µA
V+ Shutdown Current		---	16	25	µA
Shutdown Current (V_{CC})	EN=AGND	---	---	10	µA
Output Shutdown Discharge Resistance	EN=AGND	---	12	32	Ω
Overvoltage Trip Threshold	With respect to error comparator threshold	15	20	25	%
Overvoltage Fault Propagation Delay	FB forced 2% above the trip threshold	10	25	35	µs
Output Undervoltage Protection Threshold	With respect to error comparator threshold	60	70	80	%
Output Undervoltage Protection Blanking Time	From EN signal going high	---	5.5	---	ms
ILIM Source Current	DL, high state	9	10	11	µA
Current-Limit Threshold Range Setting Rrange (Positive Direction)	ILIM	30	---	200	mV
Current Comparator Offset	PGND- ILIM	-10	---	10	mV
Current-Limit Threshold (Zero Crossing)	PGND - LX, EN= 5V	-5	1.5	9	mV

Electrical Characteristics (continued)

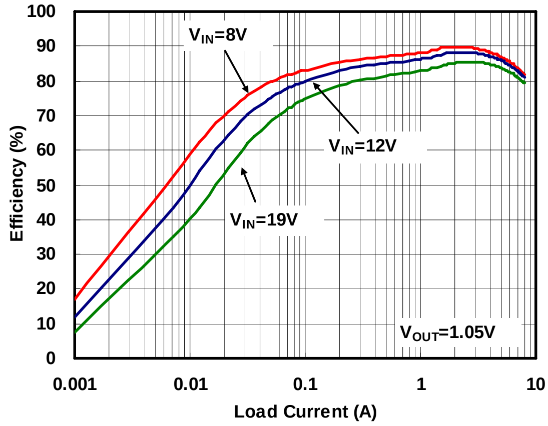
(VIN=15V, V_{CC}= V5V, EN= 5V, T_A=25°C)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
PGOOD Trip Threshold	Measure at FB with respect to error comparator threshold, falling edge	-14	-10	-7.5	%
PGOOD Output Low Voltage	ISINK=1mA	---	---	0.2	V
PGOOD Propagation Delay		---	5	16	µs
Thermal Shutdown Threshold	Hysteresis=17°C	---	147	---	°C
V_{CC} Undervoltage Lockout Threshold	Rising edge, hysteresis = 200mV,PWM disabled below this level	3.7	---	4.3	V
High Side Switch Resistance	BST - LX forced to 5V, V_{CC}=5V	---	20	24	mΩ
Low Side Switch Resistance	V_{CC}=5V	---	20	24	mΩ
BST Switch Forward Voltage	Forwarding Current=10mA	0.2	0.35	0.4	V
Logic Input High Voltage	EN	2.4	---	V5V	V
Logic Input Low Voltage	EN	---	---	0.8	V

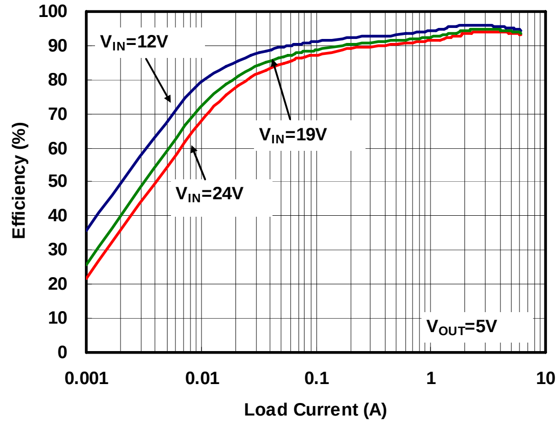
Typical Performance Characteristics

(Circuit of Fig. 1, component of table 1, VIN=19V, VOUT=1.05V, T_A=25˚C, unless otherwise noted.)

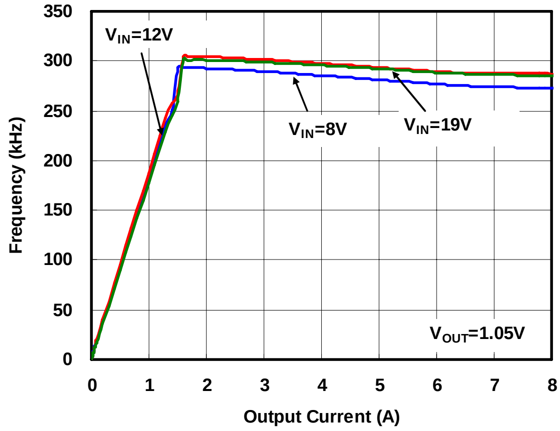
Efficiency vs. Load Current (V_{OUT}=1.05V)



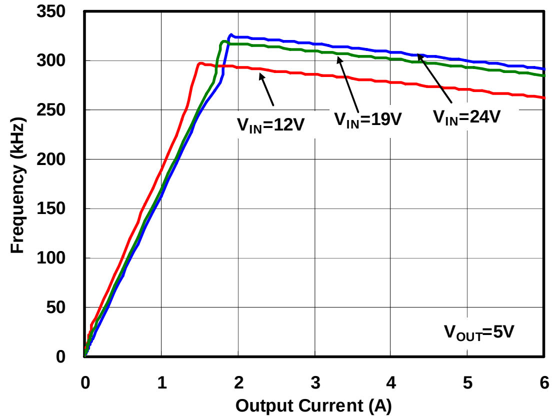
Efficiency vs. Load Current (V_{OUT}=5V)



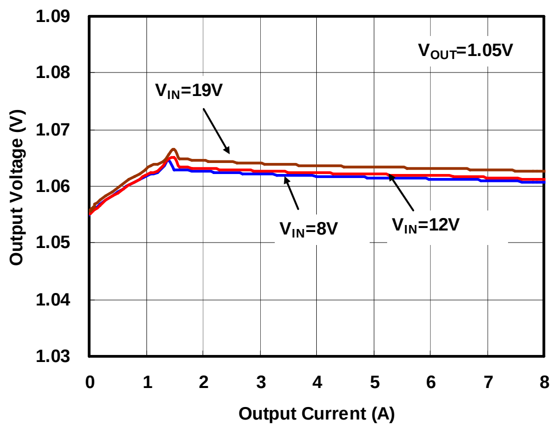
Switching Frequency vs. Load Current (V_{OUT}=1.05V)



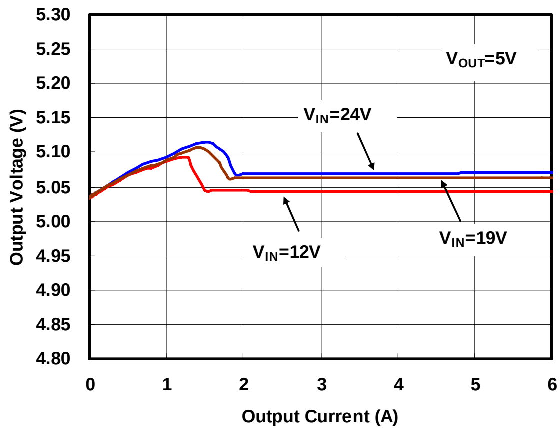
Switching Frequency vs. Load Current (V_{OUT}=5V)



Output Voltage vs. Load Current (V_{OUT}=1.05V)

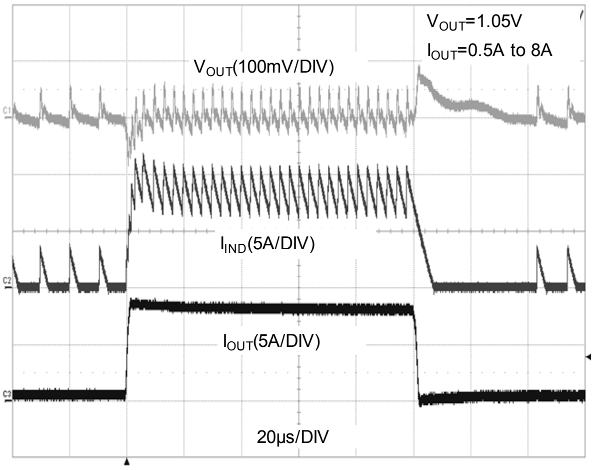


Output Voltage vs. Load Current (V_{OUT}=5V)

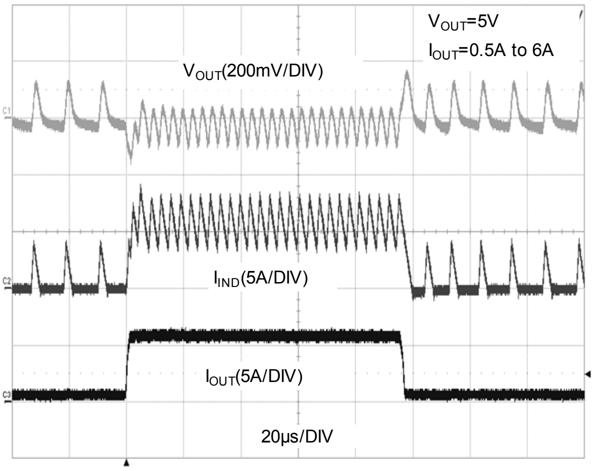


Typical Performance Characteristics (continued)

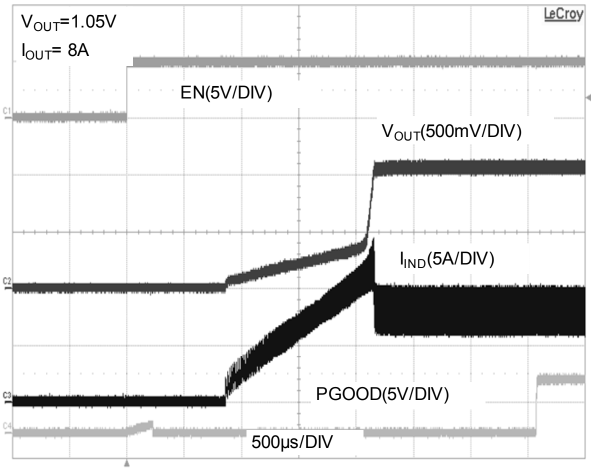
Load Transient Response



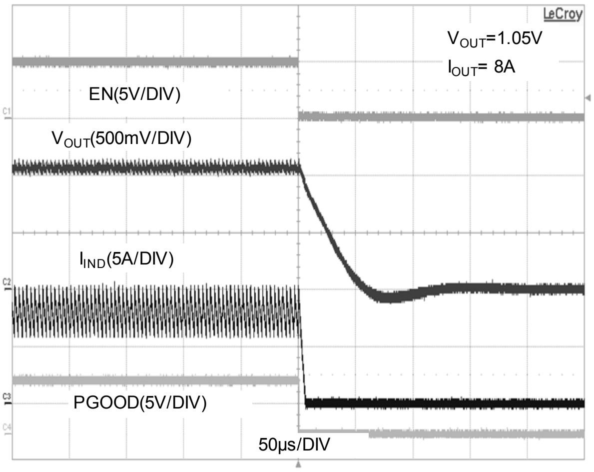
Load Transient Response (V_{OUT}=5V)



Soft-start Waveforms



Soft-stop Waveforms



Pin Description

PIN	NAME	FUNCTION
1	ILIM	Current-Limit Threshold Adjustment. Connect a resistor from ILIM to AGND to set current limit threshold
2	AGND	Analog Ground
3	V5V	5V Linear Regulator Output and Supply for DL Gate Driver. Bypass to PGND with a 10µF (min) ceramic capacitor.
4,11,12,13, 14,15,16	PGND	Power Ground.
5, 6,7,8,9,10,	LX	External Inductor Connection. Connect LX to the switched side of the inductor. LX serves as the lower supply rail for the DH high-side gate driver. LX is also the positive input to the current-limit comparator.
17,18,19,20	V+	Power Supply Input. V+ powers the LDO and is used to set the PWM one-shot Timing. Bypass to PGND with a 4.7µF (min) Capacitor.
21	NC	No Connection
22	BST	Boost Flying-Capacitor Connection. Connect to an external capacitor according to the Standard Application Circuit. See *MOSFET Gate Drivers (DH, DL)* section.
23	EN	Shutdown Input. Drive EN to GND to force the G5312 into shutdown. A rising edge on EN clears the fault latch.
24	TON	On-Time Selection-Control Input. Connect to LX with a resistor, R_{TON}.
25	OUT	Output Voltage Connection. Connect directly to the junction of the external and output filter capaci-tors. OUT senses the output voltage to determine the on-time.
26	VCC	Analog-Supply Input. Connect to the LDO supply voltage V5V, with a series 20Ω resistor. Bypass to AGND with a 1µF (min) ceramic capacitor.
27	FB	Feedback Input. Connect FB to a resistor divider from OUT for an adjustable output.
28	PGOOD	Power-Good Open-Drain Output. PGOOD is low when the output voltage is more than 10% below the normal regulation point or during soft-start. PGOOD is high impedance when the output is in regulation and the soft-start circuit has terminated.

Application Information

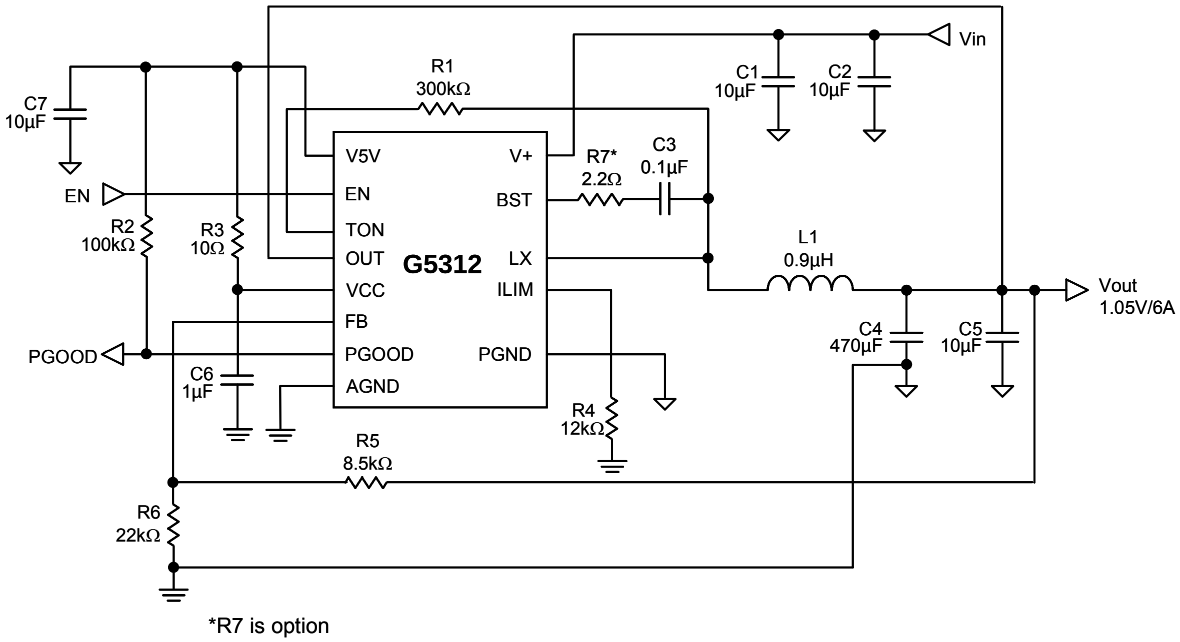


Fig. 1-A 1.05V Standard Application Circuit

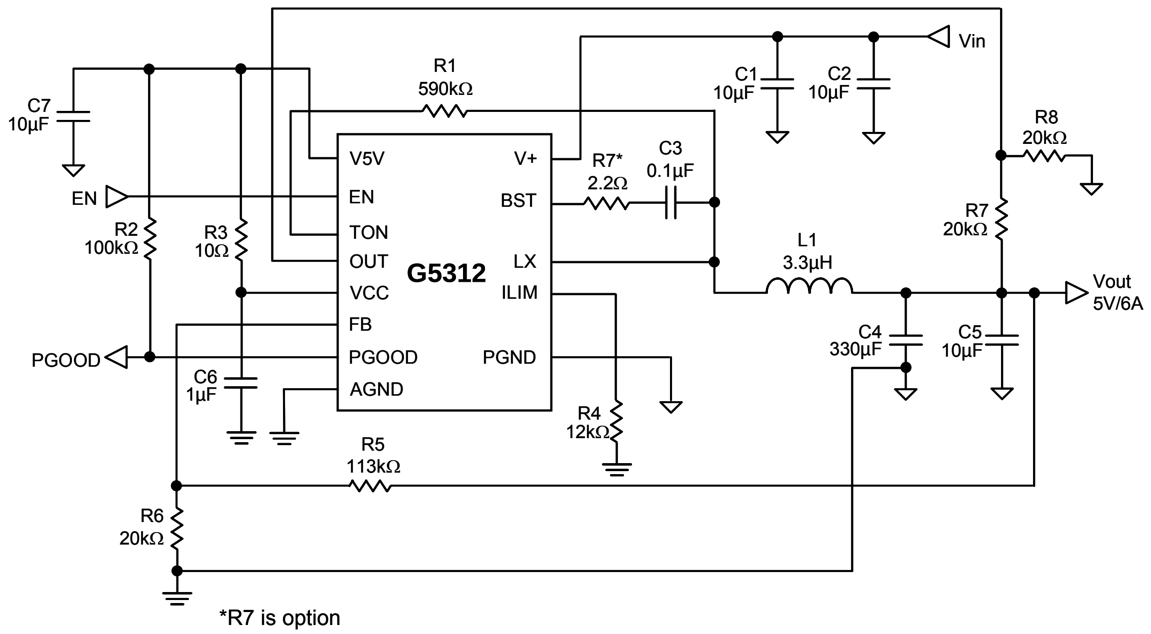


Fig. 1-B 5V Output Application Circuit

Application Information (continued)

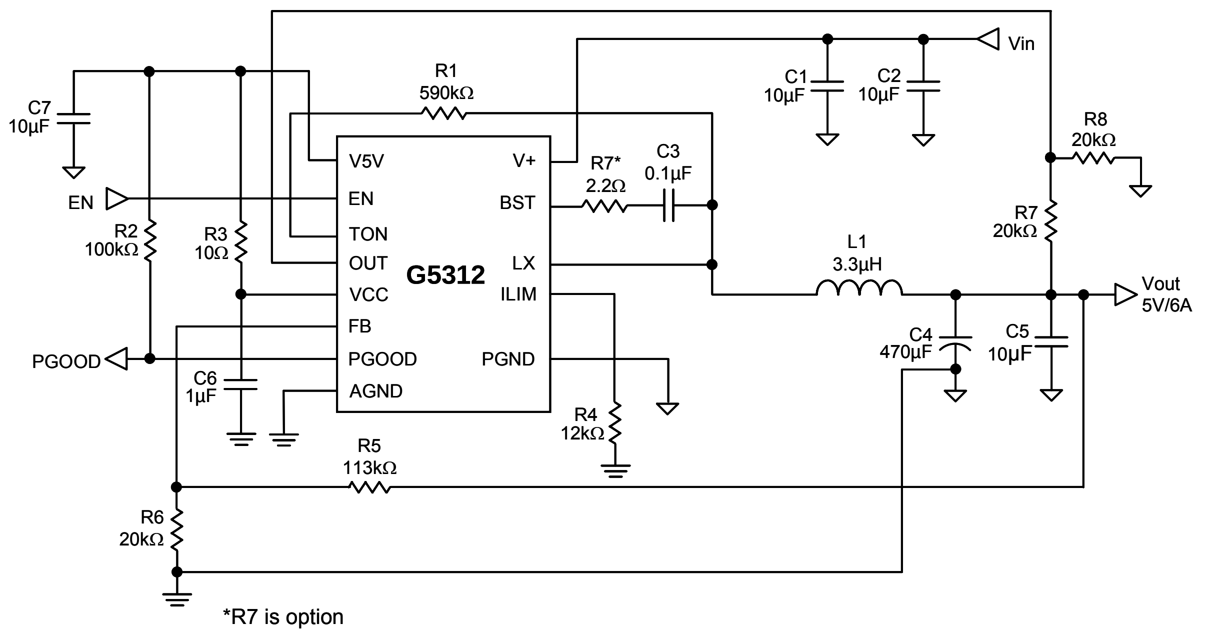


Fig. 1-C 5V Output Application Circuit with Aluminum Type Output Capacitor

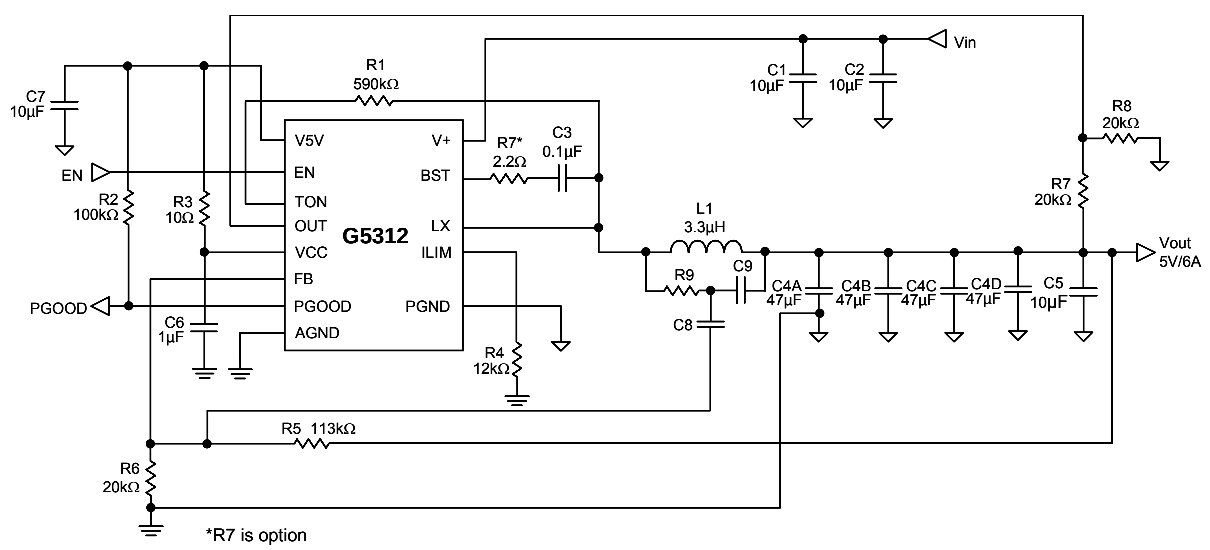


Fig. 1-D 5V Output Application Circuit with MLCC Type Output Capacitor

Block Diagram

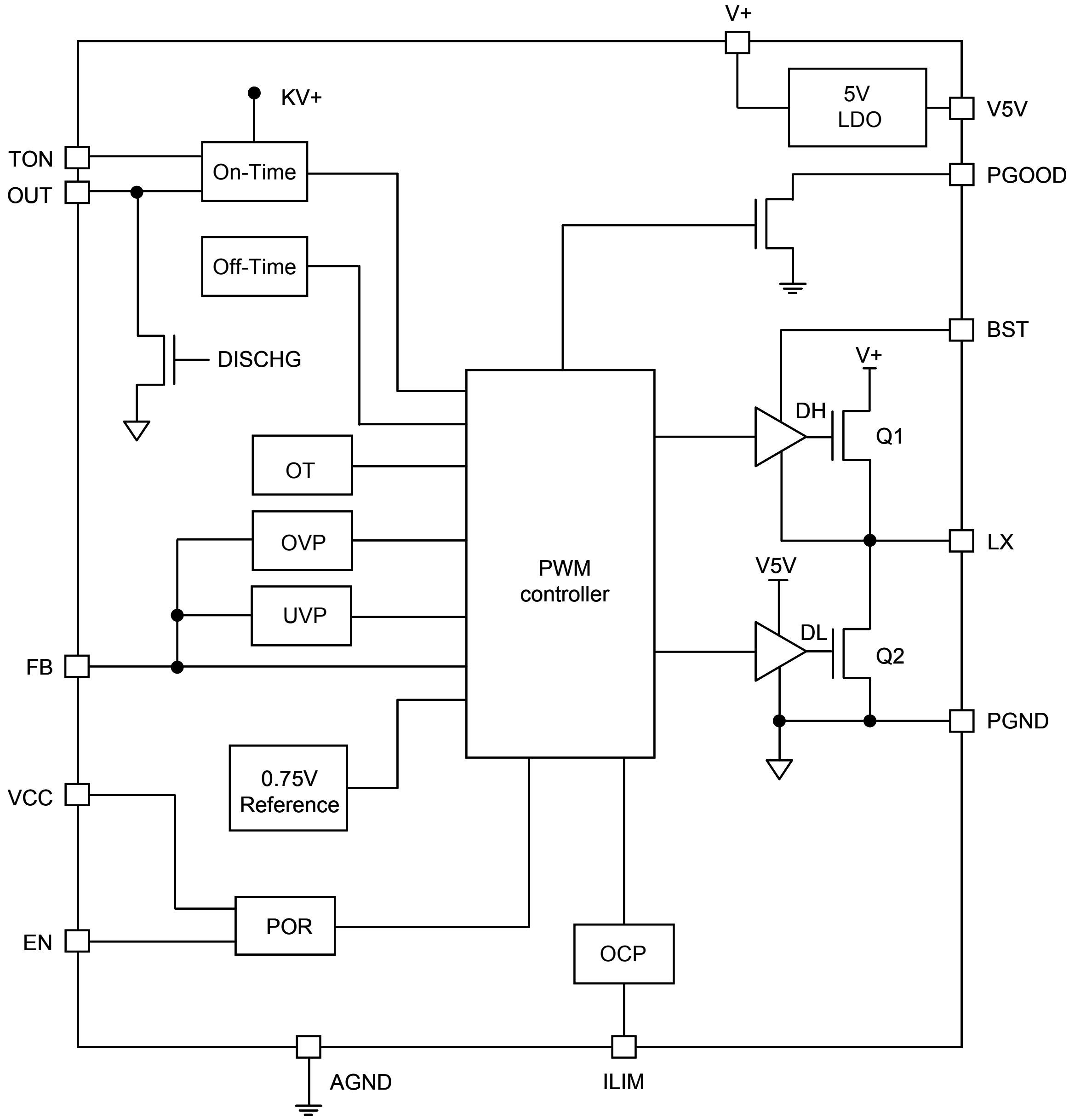


Fig. 2 Block Diagram of G5312

Table 1. Component Selection for Standard Application (Fig. 1-A) :

SYMBOL	SPECIFICATION	MANUFACTURER	PART NUMBER
C1, C2	10µF, 25V	Taiyo Yuden	TMK316BJ106KL
L1	0.9µH	SUMIDA	OR9MC-95
C4	470µF, 2.5V, 15mΩ	KEMET	T520V477M2R5A(1)E015

Detailed Description

G5312 is a 8A, synchronous buck converter with a fixed 5V LDO. A Quasi-PWM control is adapted in G5312. It is a constant-on-time PWM control with input feed-forward while maintaining a relatively constant switching frequency. It advantages in the fast load-transient response compared with conventional constant-on-time PWM control. The Figure 2 shows the Block Diagram of G5312.

5V Linear Regulator

G5312 contains a linear regulator with fixed 5V output (V5V). LDO supports up to 20mA for external load and supports a 5V bias supply for the internal PWM circuit and gate-drivers. Bypass LDO output to GND with 10µF(min) Capacitor and close to the device.

Constant-on-time PMW Control with Input Feed-Forward

The Quasi-PWM control algorithm can be described briefly: the high-side switch on-time is determined by a one-shot whose period is inversely proportional to input voltage and directly proportional to output voltage. Another on-shot determines the minimum off-time. The on-time one-shot can be triggered if the error comparator is low, the low side switch current is below the current-limit threshold, and the minimum off-time one-shot has timed out.

On-Time Selection

G5312 allows to program the on-time. The on time is determined as below

$$T_{ON} = \frac{R_{TON} \times V_{OUT}}{(V_{IN} - 1)} \times 1.08 \times 10^{-11}$$

It results in a nearly constant switching frequency R_{TON} is a resistor connected from LX to the TON pin.

Pulse-Skipping Mode

In Pulse-Skipping Mode, an automatic switchover to PFM takes place at light load. It turns off the low side switch when the inductor current crosses to zero. This scheme will improve the light-load efficiency.

Current Limit

G5312 uses the on-state resistance of low side MOSFET as a current-sensing resistor. If the current–sense voltage (PGND-LX) is above the current-limit threshold, the PWM is not allowed to initiate a new cycle. The actual peak current is the current-limit threshold adding one inductor current ripple. So it depends on the on-resistance of MOSFET, Inductor value, and battery voltage. No external current-sensing resistor is necessary in the output current path. An ILIM pin could be used to adjust the current-limit threshold. The R_{ILIM} resistor between ILIM pin and PGND pin sets the threshold. It is connected to a 10µA current source within G5312 which is turned on when the low-side MOSFET turns on. The equation for the current limit threshold is as follows:

$$I_{LIMIT} = \frac{R_{ILIM}}{R_{DS(ON)}} \times 10^{-5}(A)$$

Gate Drivers

In the low duty factor application, it exists large difference of input voltage and output voltage. Therefore, large low-side MOSFET and moderate-size high-side MOSFET are needed for high efficiency. The DH and DL drivers are optimized for driving high-side and low-side MOSFETs. A non-overlap control circuit is needed to avoid the DH and DL turning on simultaneously. The DL driver with a 0.5Ω pull low transistor helps prevent the DL from being coupled to high during the fast rising-time of the LX node, due to the drain to gate capacitive coupling of low-side synchronous-rectifier MOSFET. A resistor in series with the BST is recommended that will reduce the EMI-producing efficiency loss by increasing the turn-on time of the high-side MOSFET

POR, UVLO, and Soft-Start

Power-on reset (POR) occurs when VCC rises above approximately 2V. It reset the fault latch and soft-start counter. When VCC is below 4.2V, undervolatge lockout (UVLO) inhibits switching and forces DL to high. An internal soft-start timer to ramp up the current limit threshold to 100% of current limit setting within 3.3ms.

Power-Good Indicator

The Output voltage is always monitored for undervoltage by the PGOOD comparator. The PGOOD is open-drain type signal. In shutdown and soft-start period, PGOOD is kept low. After the soft-start timer has timed out, the PGOOD is released if the output voltage is within 10% of normal value.

Fault Protection

G5312 provides undervoltage protection, overvoltage protection, and overtemperature protection.

The undervoltage protection (UVP) function is like foldback current limit function. If the output voltage is under 70% of normal value 3.5ms after shutdown released, the undervoltage protection function is activated. The PWM is latched off and would not restart until VCC power is cycled or EN is toggled.

The overvoltage protection (OVP) function activates when the output voltage is 15% above the set voltage. The low-side MOSFET turn on 100% and the high-side MOSFET turn off. This rapidly discharges the output capacitor and decreases the output voltage. The SMPS is latched off and would not restart until VCC power is cycled or EN is toggled.

The G5312 has an overtemperature protection (OTP) that occurs when the die temperature is above 150C. It will shutdown the LDO, PWM and force high-side and low-side gate drivers output low. It could be released when die cool down or VCC power is cycled or EN is toggled.

Adjustable-Output Feedback

Connecting the FB pin to a resistor divider between OUT to GND to adjust the output voltage from 0.75V. Chose R6=10kΩ and solve the R5 with the equation:

$$R5 = R6 \times \left(\frac{V_{OUT}}{V_{FB}} - 1\right)$$

where V_{FB} = 0.75V norminal.

If Vout output voltage sets above 3.6V, connect OUT pin with an extra resistor divider (R7, R8) between Vout voltage to GND. The Fig-1B shows the 5V output application circuit.

Test Mode

A test mode is provided for system developing stage. It can disable all the OVP, UVP, and thermal shutdown features, and clear the fault latch if it has been set. Force the EN pin above VCC by external sourcing current, G5312 enters a no-fault test mode. (No more than 0.6V above VCC is allowable)

Application Information

Inductor Selection

The inductor value is determined as follows:

$$L = \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN} \times f \times \Delta I_{LPP}}$$

Where ΔI_{LPP} is defined as inductor ripple current.

The inductor ripple current also impacts transient-response performance, especially at low V_{IN}- V_{OUT} differentials. Low inductor values allow the inductor current to slew faster, replenishing charge removed from the output filter capacitors by a sudden load step.

Maintaining the ratio of the inductor ripple current to the designed maximum load current within a 20% to 50% range is prudent.

Current Limit setting

The minimum current-limit threshold must be high enough to support the maximum load current. The valley of the inductor current occurs at $I_{LOAD(MAX)}$ minus half of the inductor current ripple.

I_{LIMIT} equals minimum current-limit threshold voltage divided by the $R_{DS(ON)}$of low side MOSFET, Q2. Use the worst-case maximum value for $R_{DS(ON)}$ from the MOSFET Q2, and add some margin for the rise in $R_{DS(ON)}$ with temperature. A good general rule is to allow 0.5% additional resistance for each °C of temperature rise.

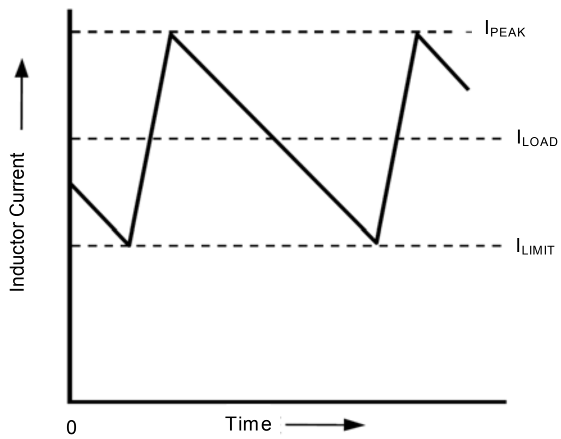


Fig. 3 Current Limit Setting

Output Capacitor Selection

The output filter capacitor must have low enough effective series resistance (ESR) to meet output ripple and load-transient requirements, yet have high enough ESR to satisfy stability requirements. Also, the capacitance must be high enough to absorb the inductor energy going from a full-load to no-load condition without tripping the overvoltage protection circuit.

In CPU V_{CORE} converters and other applications where the output is subject to violent load transients, the output capacitor's size depends on how much ESR is needed to prevent the output from dipping too low under a load transient.

In non-CPU applications, the output capacitor's size depends on how much ESR is needed to maintain an acceptable level of output voltage ripple:

$$R_{ESR} \leq \frac{V_{OUTPP}}{\Delta I_{LPP}}$$

Output Capacitor Stability considerations

Stability is determined by the value of the ESR zero relative to the switching frequency. The point of instability is given by the following equation:

$$f_{ESR} = \frac{f}{\pi}$$

Where f = switching frequency

$$f_{ESR} = \frac{1}{2 \times \pi \times ESR \times C_{OUT}}$$

For a typical 300kHz application, the ESR zero frequency must be well below 95kHz, preferably below 50kHz. An OS-CON or POS CAP type capacitor, (ESR=10~20mΩ) is preferred. If use aluminum type capacitor, parallel a small ceramic capacitor is recommended.

Don't put high-value ceramic capacitors directly across the feedback sense point without taking precautions to ensure stability. Large ceramic capacitors can have a high ESR zero frequency and cause erratic, unstable operation. However, it's easy to add enough series resistance by placing the capacitors a couple of inches downstream from the feedback sense point, which should be as close as possible to the inductor.

Unstable operation manifests itself in two related but distinctly different ways: double-pulsing and fast-feedback loop instability.

Double-pulsing occurs due to noise on the output or due to the ESR is too low to without enough voltage ramp in the output voltage signal. This "fools" the error comparator into triggering a new cycle immediately after the 400ns minimum off-time period has expired. Double-pulsing is more annoying than harmful, resulting in nothing worse than increased output ripple. However, it can indicate the possible presence of loop instability, which is caused by insufficient ESR. Loop instability can result in oscillations at the output after line or load perturbations that can trip the overvoltage protection latch or cause the output voltage to fall below the tolerance limit. The easiest method for checking stability is to apply a very fast zero-to-max load transient and carefully observe the output voltage ripple envelope for over-shoot and ringing. It can help to simultaneously monitor the inductor current with a current probe. Don't allow more than one cycle of ringing after the initial step-response under- or overshoot.

Input Capacitor Selection

The input capacitor must meet the ripple current requirement (I_{RMS}) imposed by the switching currents. Nontantalum chemistries (ceramic, aluminum, or OS-CON) are preferred due to their resistance to power-upsurge currents.

For optimal circuit reliability, choose a capacitor that has less than 10°C temperature rise at the peak ripple current.

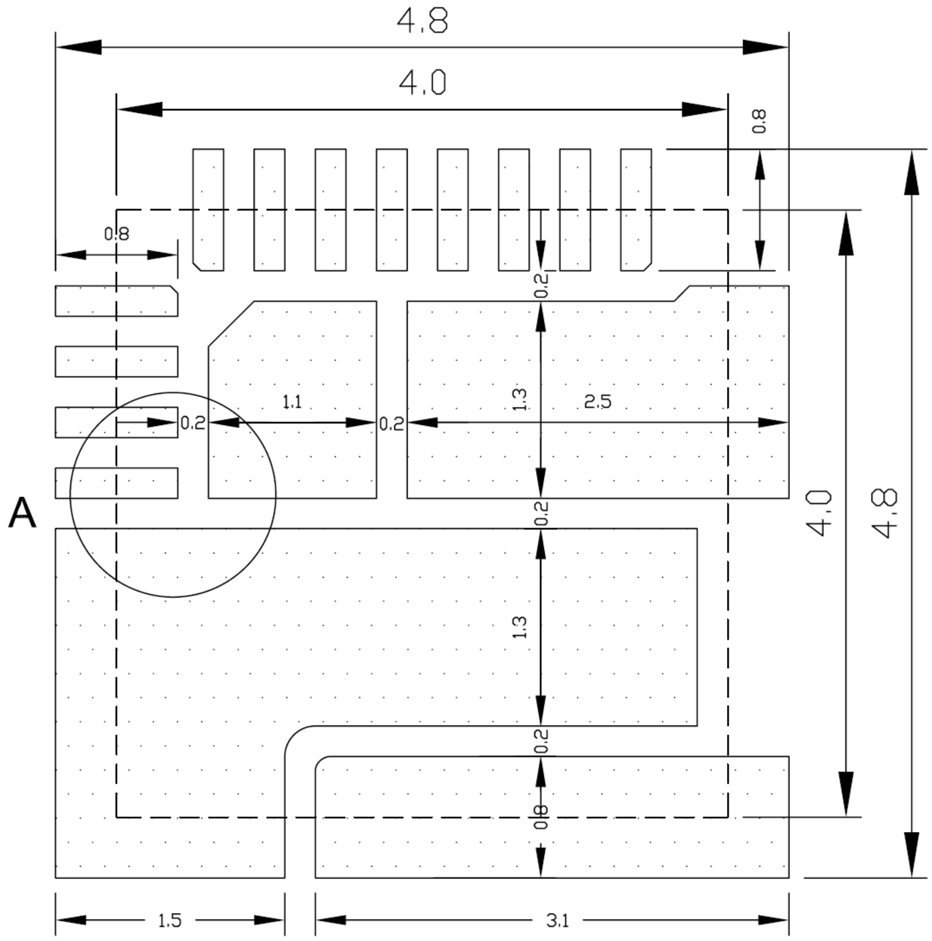
$$I_{RMS} = I_{LOAD}\left(\frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}\right)$$

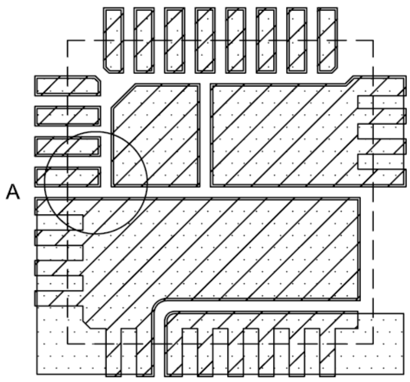
Layout Considerations

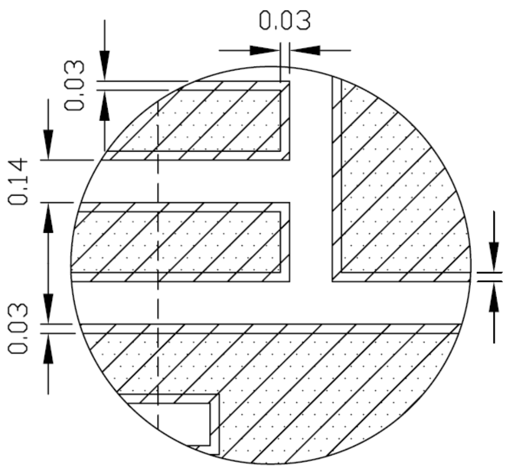
- Connect AGND (Pin2) to ground of bypass VCC, and FB path.
- Connect PGND (Pin4) to ground of bypass V5V.
- Connect AGND and PGND together close to the IC and the negative terminal of Cout.
- Star connection PGND ground plane to system ground (normally, it's defined as ground of power supply or battery pack.).
- Connect PGND of power component Low-side MOSFET source, C_{IN}, and C_{OUT} to system ground by a plane.
- All sensitive analog traces such as OUT, and FB should be placed away from high-voltage switching node such as LX, BST nodes to avoid coupling.

Minimum Footprint PCB Layout Section

G5312QN1U





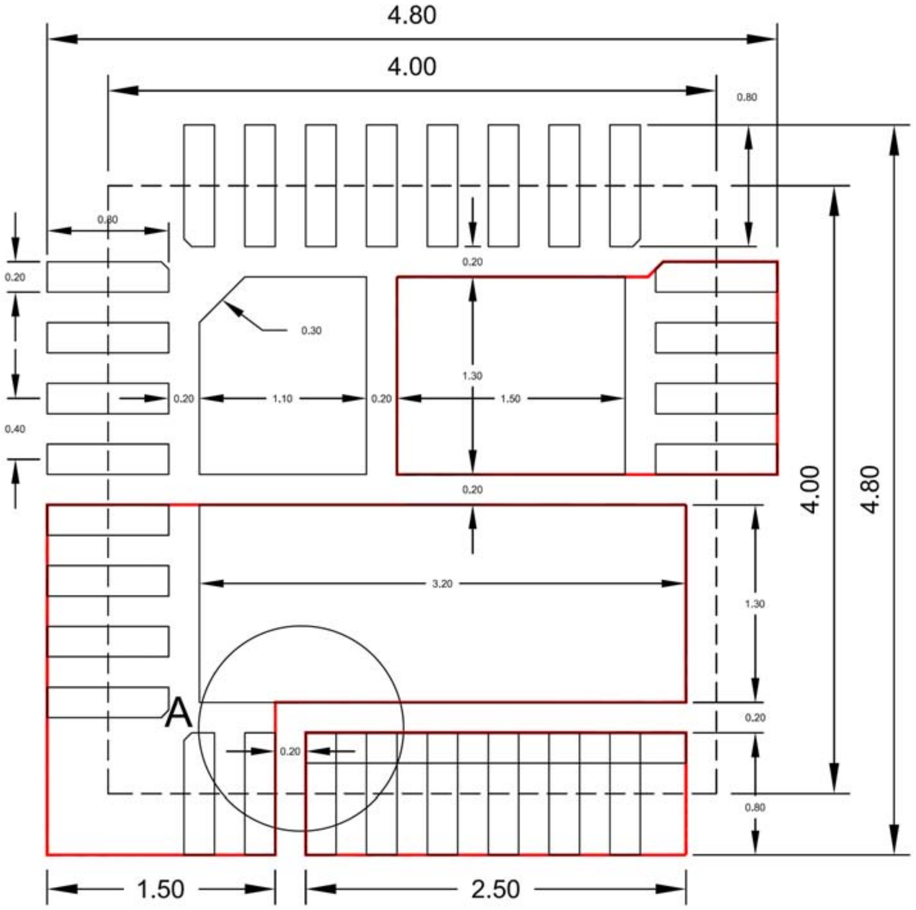


Section A

Minimum Footprint PCB Layout Section (continued)

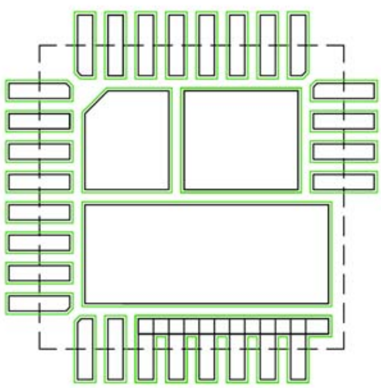
G5312QN2U

QFN4X4-28

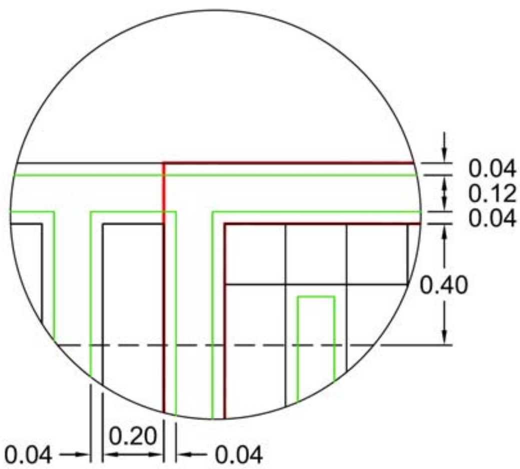


Top Layer

* Recommend Top Layer Thermal Pad Design Following Red Line for Better Characteristic.



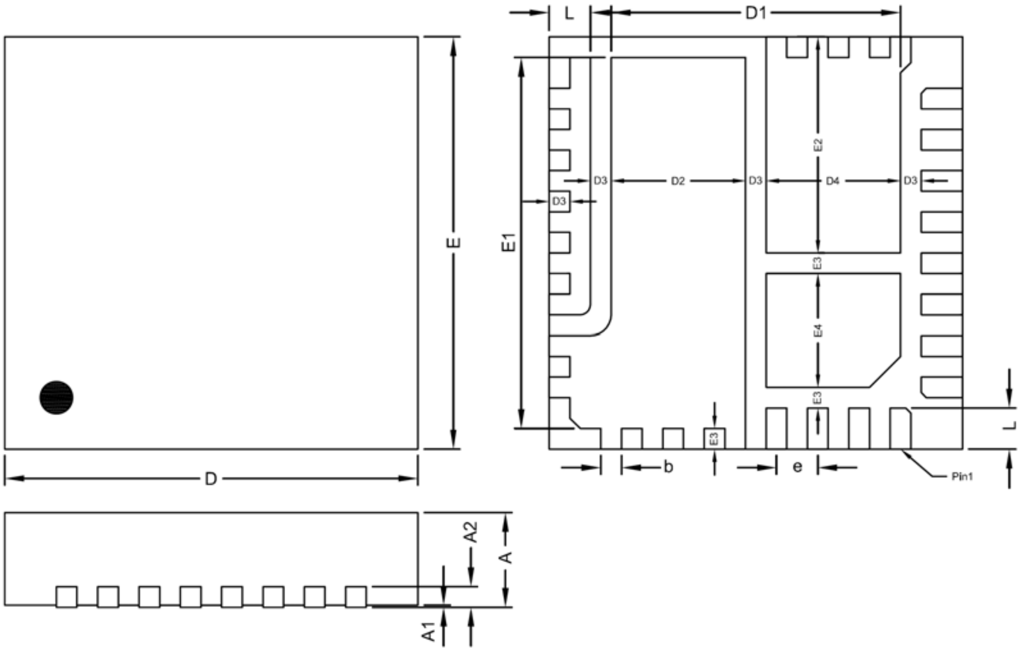
Top Layer with Solder Mask



Section A

Package Information

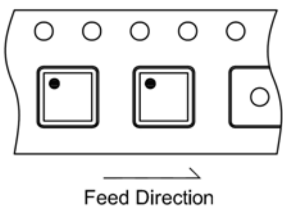
G5312QN1U



QFN4X4-28 Package

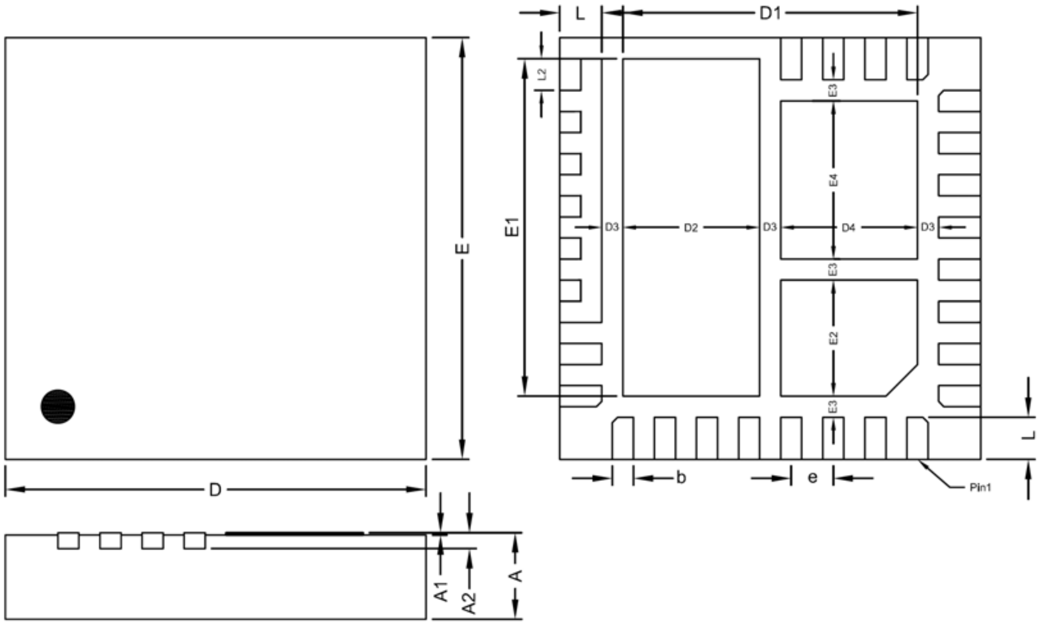
Symble	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.80	0.90	0.0276	0.0315	0.0354
A1	0.00	---	0.05	0.0000	---	0.0020
A2	0.15 BSC			0.0059 BSC		
D	3.95	4.00	4.05	0.1555	0.1575	0.1594
E	3.95	4.00	4.05	0.1555	0.1575	0.1594
D1	2.70	2.80	2.90	0.1063	0.1102	0.1142
E1	3.55	3.60	3.65	0.1398	0.1417	0.1437
D2	1.25	1.30	1.35	0.0492	0.0512	0.0531
E2	2.05	2.10	2.15	0.0807	0.0827	0.0846
D3	0.20 BSC			0.0079 BSC		
E3	0.20 BSC			0.0079 BSC		
D4	1.25	1.30	1.35	0.0492	0.0512	0.0531
E4	1.05	1.10	1.15	0.0413	0.0433	0.0453
b	0.15	0.20	0.25	0.0059	0.0079	0.0098
e	0.40 BSC			0.0157 BSC		
L	0.35	0.40	0.45	0.0138	0.0157	0.0177

Taping Specification



PACKAGE	Q'TY/BY REEL
QFN4X4-28	3,000 ea

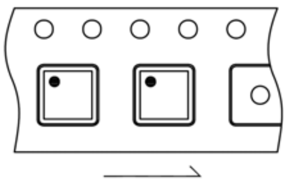
G5312QN2U



QFN4X4-28 Package

Symble	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.80	0.90	0.0276	0.0315	0.0354
A1	0.00	- - -	0.05	0.0000	- - -	0.0020
A2	0.15 BSC			0.0059 BSC		
D	3.95	4.00	4.05	0.1555	0.1575	0.1594
E	3.95	4.00	4.05	0.1555	0.1575	0.1594
D1	2.70	2.80	2.90	0.1063	0.1102	0.1142
E1	3.15	3.20	3.25	0.1240	0.1260	0.1280
D2	1.25	1.30	1.35	0.0492	0.0512	0.0531
E2	1.05	1.10	1.15	0.0413	0.0433	0.0453
D3	0.20 BSC			0.0079 BSC		
E3	0.20 BSC			0.0079 BSC		
D4	1.25	1.30	1.35	0.0492	0.0512	0.0531
E4	1.45	1.50	1.55	0.0571	0.0590	0.0453
b	0.15	0.20	0.25	0.0059	0.0079	0.0098
e	0.40 BSC			0.0157 BSC		
L	0.35	0.40	0.45	0.0138	0.0157	0.0177
L2	0.25	0.30	0.35	0.0098	0.0118	0.0138

Taping Specification



Feed Direction

PACKAGE	Q'TY/BY REEL
QFN4X4-28	3,000 ea