High Efficiency 10A Synchronous Buck Converter for 5V System Power

Features

- **Ultra-High Efficiency**
- **Low Quiescent Current of 40μA**
- **Integrated 8.5mΩ at VCC=5V N-Channel MOSFET for Low Side**
- **Integrated 20mΩ at VCC=5V N-Channel MOSFET for High Side**
- **No Current-Sense Resistor (Lossless I_{LIMIT})**
- **Quasi-PWM with 100ns Load-Step Response**
- **1% VOUT Accuracy Over Line and Load**
- **Programmable Switching Frequency**
- **4.5V to 5.5V Adjustable Output Range**
- **5.5V to 28V Adapter or Battery Input Range**
- **Integrated Boost Switch**
- **OVP & UVP**
- **Over Temperature Protection (non-latch)**
- **3.3ms Soft-Start**
- **Power-Good Indicator**
- **Fixed 5V, 80mA Bootstrapped Linear Regulator**

General Description

G5330A is a 10A, synchronous DC/DC buck converter with integrated 20mΩ N-channel high-side MOSFET and 8.5mΩ N-channel low-side MOSFET. It uses constant on-time control scheme to handle wide input/output voltage ratios with ease and provides 100ns "instant-on" response to load transients while maintaining a relatively constant switching frequency. The G5330A achieves high efficiency at a reduced cost by eliminating the current-sense resistor found in traditional current-mode PWMs. Single-stage buck conversion allows these devices to directly step down high-voltage batteries for the highest possible efficiency. The built-in 5V LDO supports 80mA for internal circuit with automatic bootstrapping to DC/DC converter output. The G5330A is intended for the 5V system power supply of Notebook Computer. The G5330A is available in QFN4X4-28 package.

Applications

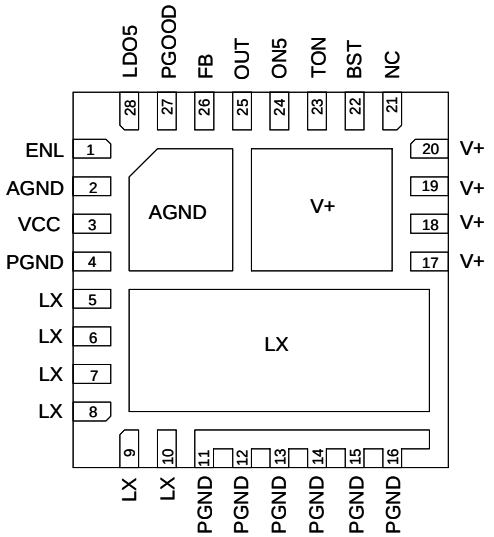
- **Notebook Computers**
- **I/O Supply**
- **Networking Power Supply**

Ordering Information

ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE (Green)
G5330AQN1U	5330A	-40°C to +85°C	QFN4X4-28

Note: QN: QFN4X4-28
1: Bonding Code
U : Tape & Reel

Pin Configuration



G5330A QFN4X4-28

Note: Recommend connecting the Thermal Pad to the Ground for excellent power dissipation.

Absolute Maximum Ratings

V+ to AGND. . . . . -0.3V to 30V
VCC, LDO5 to AGND . . . . . -0.3V to 6V
ON5, PGOOD, OUT to AGND . . . . . .-0.3V to 6V
FB, TON, ENL to AGND . . . . . .-0.3V to (VCC+0.3V)
BST to PGND . . . . . .-0.3V to 35V
LX to BST. . . . . -6V to 0.3V

Thermal Resistance of Junction to Ambient (θ_{JA})
QFN4X4-28. . . . . 25°C/W
Junction Temperature . . . . . .150°C
Storage Temperature . . . . . -65°C to 150°C
Reflow Temperature (soldering, 10sec) . . . . . 260°C

Electrical Characteristics

(VIN=15V, VCC=5V, ON5=5V, T_A=25°C)

The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V+ Input Voltage Range	V+	5.5	---	28	V
LDO Output Voltage	LDO5	4.75	5.0	5.25	V
Line Regulation of LDO5	Load=1mA; V+=8V to 28V	---	5	30	mV
Load Regulation of LDO5	Load=20mA	---	---	60	mV
Dropout Voltage of LDO5	Load=10mA	---	0.4	0.7	V
LDO5 Bootstrap Switch Resistance	LDO5 to OUT; OUT=5V	---	3.5	6	Ω
VCC Input Voltage Range	VCC	4.5	5	5.5	V
Error Comparator Threshold (DC Output Voltage Accuracy)	V+ = 15V, FB = OUT	1.2375	1.25	1.2625	V
Soft-Start Ramp Time	Rising edge of ON5 to 95% output voltage	---	3.3	---	ms
TON Operating Current	R_{TON} = 1000kΩ, V+ = 15V	---	15	---	µA
On Time	VLX=12V, VOUT=1.25V, R_{TON} = 430kΩ, nominal	---	310	---	ns
Minimum On Time	VOUT=0.1V, R_{TON} = 430kΩ	---	80	---	ns
Minimum Off Time	FB=1.1V, LX=-0.1V,	---	400	---	ns
Quiescent Supply Current (V+)	FB forced above the regulation point	---	40	---	µA
Shutdown Current (V+)		---	1	---	µA
Output Shutdown Discharge Resistance	ON5=AGND	---	12	32	Ω
Overvoltage Trip Threshold	With respect to error comparator threshold	7.5	11	15	%
Overvoltage Fault Propagation Delay	FB forced 2% above the trip threshold	10	25	35	µs
Output Undervoltage Protection Threshold	With respect to error comparator threshold	60	70	80	%
Output Undervoltage Protection Blanking Time	From ON5 signal going high	---	5.5	---	ms
Current-Limit Threshold		10	13	16	A
Zero Current Threshold (Zero Crossing)	PGND - LX	-5	3	9	mV
PGOOD Trip Threshold	Measure at FB with respect to error comparator threshold, falling edge	-14	-10	-7.5	%
PGOOD Output Low Voltage	ISINK=1mA	---	---	0.2	V
PGOOD Propagation Delay		---	17	22.5	µs
Thermal Shutdown Threshold	Hysteresis=15°C	---	150	---	°C
VCC Undervoltage Lockout Threshold	Rising edge, hysteresis = 200mV,PWM disabled below this level	3.7	---	4.3	V
High Side Switch Resistance	BST - LX forced to 5V, VCC=5V	---	20	24	mΩ
Low Side Switch Resistance	VCC=5V	---	8.5	10	mΩ
BST Switch Forward Voltage	Forwarding Current=10mA	0.2	0.35	0.4	V
Logic Input High Voltage	ENL	1.4	---	---	V
Logic Input Low Voltage	ENL	---	---	0.4	V
Logic Input High Voltage	ON5	2.4	---	---	V
Logic Input Low Voltage	ON5	---	---	0.8	V

Pin Description

PIN	NAME	FUNCTION
1	ENL	Enable the IC and LDO5.
2	AGND	Analog Ground
3	VCC	Analog Supply Input and Supply for Internal circuits. Bypass to PGND with a 10µF (min) ceramic capacitor.
4,11,12,13,14,15,16	PGND	Power Ground. Source node of low side power MOSFET.
5,6,7,8,9,10	LX	External Inductor Connection. Connect LX to the switched side of the inductor. LX serves as the lower supply rail for the DH high-side gate driver. LX is also the positive input to the current-limit comparator.
17,18,19,20	V+	Power Supply Input. V+ is used to set the PWM one-shot Timing. Bypass to GND with a 4.7µF (min) Capacitor.
21	NC	No connection
22	BST	Boost Flying-Capacitor Connection. Connect to an external capacitor according to the Standard Application Circuit. See *MOSFET Gate Drivers (DH, DL)* section.
23	TON	On-Time Selection-Control Input. Connect to LX with a resistor, R_{TON}.
24	ON5	Drive ON5 to GND to force the buck converter into shutdown. A rising edge on ON5 clears the fault latch.
25	OUT	Output Voltage Connection. Connect directly to the junction of the external and output filter capacitors. OUT senses the output voltage to determine the on-time.
26	FB	Feedback Input. Connect FB to a resistor divider from OUT for an adjustable output.
27	PGOOD	Power-Good Open-Drain Output. PGOOD is low when the output voltage is more than 10% below the normal regulation point or during soft-start. PGOOD is high impedance when the output is in regulation and the soft-start circuit has terminated.
28	LDO5	5V Linear Regulator Output. Supply for DL Gate Driver. Bypass to AGND with 10µF (min) ceramic capacitor.

Application Information

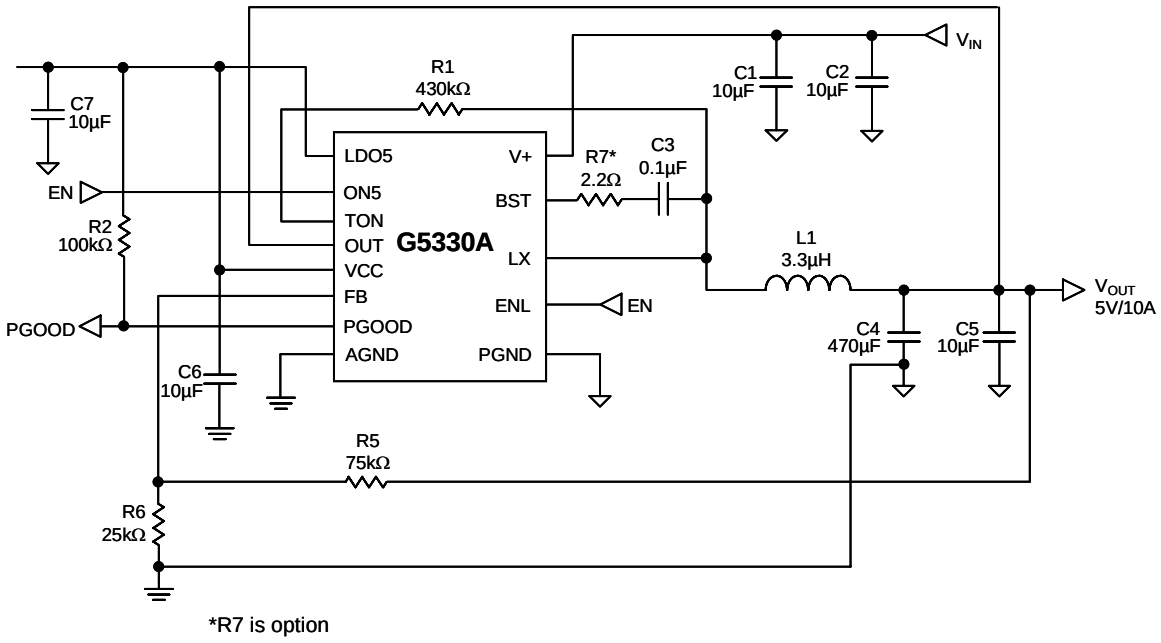


Fig. 1 Standard Application Circuit

Block Diagram

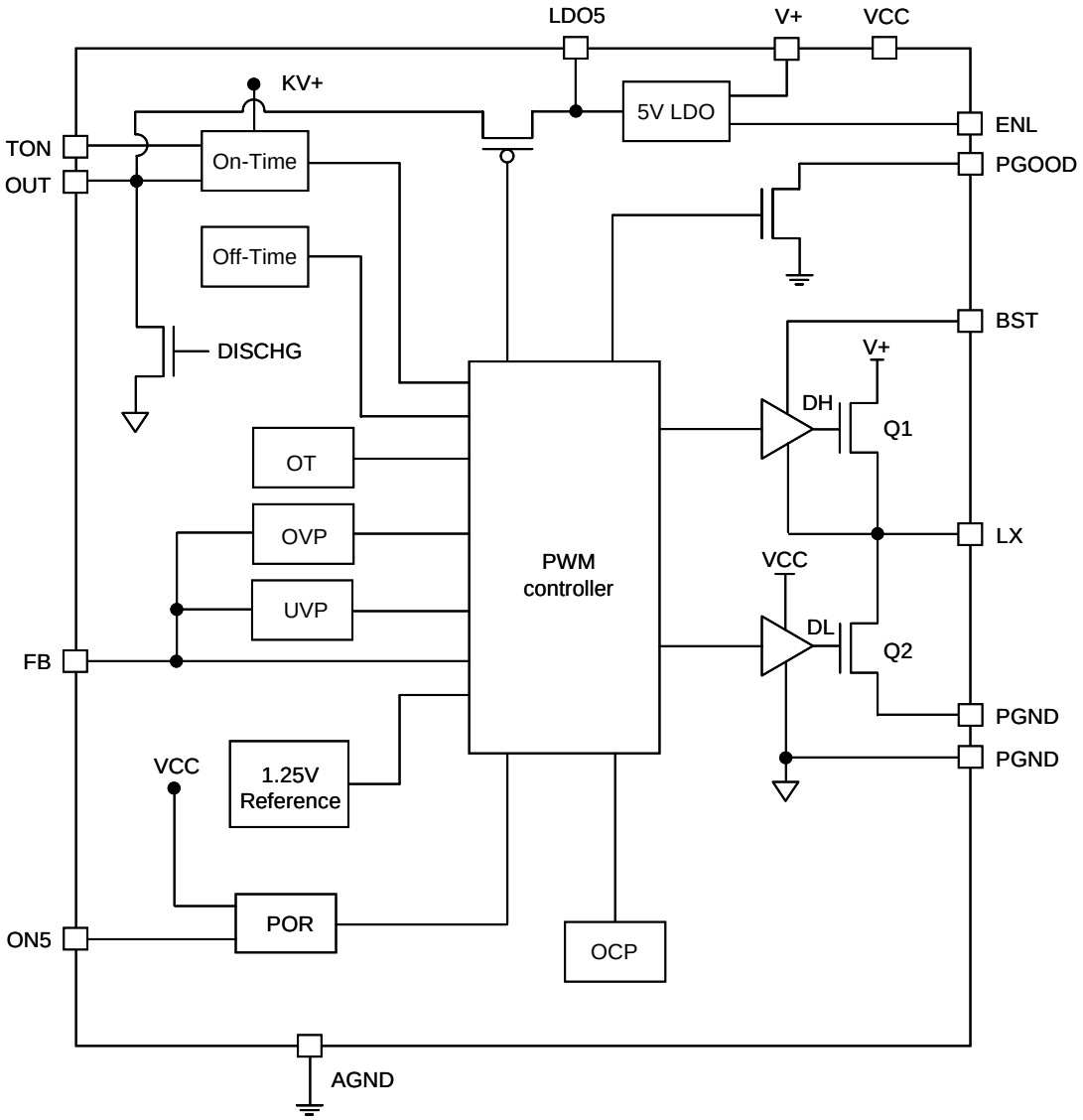


Fig. 2 Block Diagram of G5330A

Table 1. Component Selection for Standard Application (Fig. 1) :

SYMBOL	SPECIFICATION	MANUFACTURER	PART NUMBER
C1, C2	10µF, 25V	Taiyo Yuden	TMK316BJ106KL
L1	3.3µH	TOKO	FDA1055-3R3M
C4	470µF, 2.5V, 15mΩ	KEMET	T520V477M2R5A(1)E015

Detailed Description

G5330A is a 10A, synchronous buck converter with a fixed 5V LDO. A Quasi-PWM control is adapted in G5330A. It is a constant-on-time PWM control with input feed-forward while maintaining a relatively constant switching frequency. It advantages in the fast load-transient response compared with conventional constant-on-time PWM control. The Figure 2 shows the Block Diagram of G5330A.

5V Bootstrapped Linear Regulation

G5330A contains a LDO with fixed 5V output (LDO5) enable by ENL. It supports up to 80mA for the internal PWM circuit and gate-drivers. Bypass VCC to PGND with 10μF (min) capacitor and close to the device. After the soft-start of DC/DC converter, an internal 3.5Ω PMOS switch automatic bootstraps the OUT to LDO5, and simultaneously turns off 5V linear regulator.

Constant-on-time PMW Control with Input Feed-Forward

The Quasi-PWM control algorithm can be described briefly: the high-side switch on-time is determined by a one-shot whose period is inversely proportional to input voltage and directly proportional to output voltage. Another on-shot determines the minimum off-time. The on-time one-shot can be triggered if the error comparator is low, the low side switch current is below the current-limit threshold, and the minimum off-time one-shot has timed out.

On-Time Selection

G5330A allows to program the on-time. The on time is determined as below

$$T_{ON} = \frac{R_{TON} \times V_{OUT}}{(V_{IN} - 1)} \times 7 \times 10^{-12}$$

It results in a nearly constant switching frequency R_{TON} is a resistor connected from LX to the TON pin.

Pulse-Skipping Mode

In Pulse-Skipping Mode, an automatic switchover to PFM takes place at light load. It turns off the low side switch when the inductor current crosses to zero. This scheme will improve the light-load efficiency.

Current Limit

G5330A uses the on-state resistance of low side MOSFET as a current-sensing resistor. If the current–sense voltage (PGND-LX) is above the current-limit threshold, the PWM is not allowed to initiate a new cycle. The actual peak current is the current-limit threshold adding one inductor current ripple. So it depends on the on-resistance of MOSFET, Inductor value, and battery voltage. No external current-sensing resistor is necessary in the output current path. The current-limit threshold is set as 13A internally.

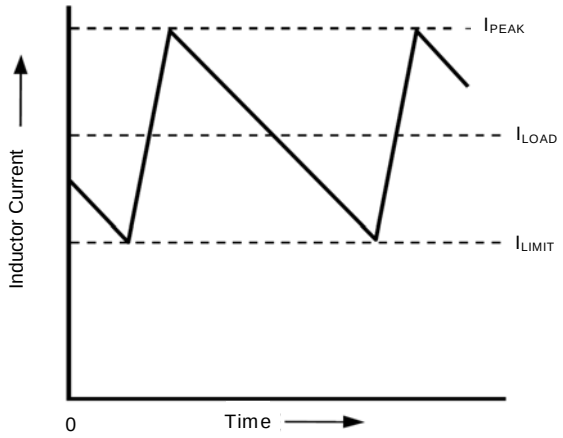


Fig. 3 Current Limit Setting

Gate Drivers

In the low duty factor application, it exists large difference of input voltage and output voltage. Therefore, large low-side MOSFET and moderate-size high-side MOSFET are needed for high efficiency. The DH and DL drivers are optimized for driving high-side and low-side MOSFETs. A non-overlap control circuit is needed to avoid the DH and DL turning on simultaneously. The DL driver with a 0.5Ω pull low transistor helps prevent the DL from being coupled to high during the fast rising-time of the LX node, due to the drain to gate capacitive coupling of low-side synchronous-rectifier MOSFET. A resistor in series with the BST is recommended that will reduce the EMI-producing efficiency loss by increasing the turn-on time of the high-side MOSFET.

POR, UVLO, and Soft-Start

Power-on reset (POR) occurs when VCC rises above approximately 2V. It reset the fault latch and soft-start counter. When VCC is below 4.2V, undervoltage lockout (UVLO) inhibits switching and forces DL to high. An internal soft-start timer ramps up the current limit threshold to 100% of current limit setting within 3.3ms.

Power-Good Indicator

The Output voltage is always monitored for undervoltage by the PGOOD comparator. The PGOOD is open-drain type signal. In shutdown and soft-start period, PGOOD is kept low. After the soft-start timer has timed out, the PGOOD is released if the output voltage is within 10% of normal value.

Fault Protection

G5330A provides undervoltage protection, overvoltage protection, and overtemperature protection.

The undervoltage protection (UVP) function is like foldback current limit function. If the output voltage is under 70% of normal value 3.5ms after shutdown released, the undervoltage protection function is activated. The PWM is latched off and would not restart until VCC power is cycled or ON5 is toggled.

The overvoltage protection (OVP) function activates when the output voltage is 11% above the set voltage. The low-side MOSFET turn on 100% and the high-side MOSFET turn off. This rapidly discharges the output capacitor and decreases the output voltage. The SMPS is latched off and would not restart until VCC power is cycled or ON5 is toggled.

The G5330A has an overtemperature protection (OTP) that occurs when the die temperature is above 150°C. It will shutdown the PWM and force high-side and low-side gate drivers output low. It could be released when die cool down or VCC power is cycled or ON5 is toggled.

Adjustable-Output Feedback

Connecting the FB pin to a resistor divider between OUT to GND to adjust the output voltage between 4.5V to 5.5.V.

Chose R6=25kΩ and solve the R5 with the equation:

$$R5 = R6 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right)$$

where V_{FB} = 1.25V norminal.

Test Mode

A test mode is provided for system developing stage. It can disable all the OVP, UVP, and thermal shutdown features, and clear the fault latch if it has been set. Force the ON5 pin above VCC by external sourcing current, G5330A enters a no-fault test mode. (No more than 0.6V above VCC is allowable)

Application Information

Inductor Selection

The inductor value is determined as follows:

$$L = \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN} \times f \times \Delta I_{LPP}}$$

Where ΔI_{LPP} is defined as inductor ripple current.

The inductor ripple current also impacts transient-response performance, especially at low V_{IN}-V_{OUT} differentials. Low inductor values allow the inductor current to slew faster, replenishing charge removed from the output filter capacitors by a sudden load step.

Maintaining the ratio of the inductor ripple current to the designed maximum load current within a 20% to 50% range is prudent.

Output Capacitor Selection

The output filter capacitor must have low enough effective series resistance (ESR) to meet output ripple and load-transient requirements, yet have high enough ESR to satisfy stability requirements. Also, the capacitance must be high enough to absorb the inductor energy going from a full-load to no-load condition without tripping the overvoltage protection circuit.

In CPU V_{CORE} converters and other applications where the output is subject to violent load transients, the output capacitor's size depends on how much ESR is needed to prevent the output from dipping too low under a load transient.

In non-CPU applications, the output capacitor's size depends on how much ESR is needed to maintain an acceptable level of output voltage ripple:

$$R_{ESR} \leq \frac{V_{OUTPP}}{\Delta I_{LPP}}$$

Output Capacitor Stability considerations

Stability is determined by the value of the ESR zero relative to the switching frequency. The point of instability is given by the following equation:

$$f_{ESR} = \frac{f}{\pi}$$

Where f = switching frequency

$$f_{ESR} = \frac{1}{2 \times \pi \times ESR \times C_{OUT}}$$

For a typical 300kHz application, the ESR zero frequency must be well below 95kHz, preferably below 50kHz. An OS-CON or POS CAP type capacitor, (ESR=10~20mΩ) is preferred. If use aluminum type capacitor, parallel a small ceramic capacitor is recommended.

Don't put high-value ceramic capacitors directly across the feedback sense point without taking precautions to ensure stability. Large ceramic capacitors can have a high ESR zero frequency and cause erratic, unstable operation. However, it's easy to add enough series resistance by placing the capacitors a couple of inches downstream from the feedback sense point, which should be as close as possible to the inductor.

Unstable operation manifests itself in two related but distinctly different ways: double-pulsing and fast-feedback loop instability.

Double-pulsing occurs due to noise on the output or due to the ESR is too low to without enough voltage ramp in the output voltage signal. This "fools" the error comparator into triggering a new cycle immediately after the 400ns minimum off-time period has expired. Double-pulsing is more annoying than harmful, resulting in nothing worse than increased output ripple. However, it can indicate the possible presence of loop instability, which is caused by insufficient ESR. Loop instability can result in oscillations at the output after line or load perturbations that can trip the overvoltage protection latch or cause the output voltage to fall below the tolerance limit. The easiest method for checking stability is to apply a very fast zero-to-max load transient and carefully observe the output voltage ripple envelope for over-shoot and ringing. It can help to simultaneously monitor the inductor current with a current probe. Don't allow more than one cycle of ringing after the initial step-response under- or over-shoot.

Input Capacitor Selection

The input capacitor must meet the ripple current requirement (I_{RMS}) imposed by the switching currents. Nontantalum chemistries (ceramic, aluminum, or OS-CON) are preferred due to their resistance to power-upsurge currents.

For optimal circuit reliability, choose a capacitor that has less than 10°C temperature rise at the peak ripple current.

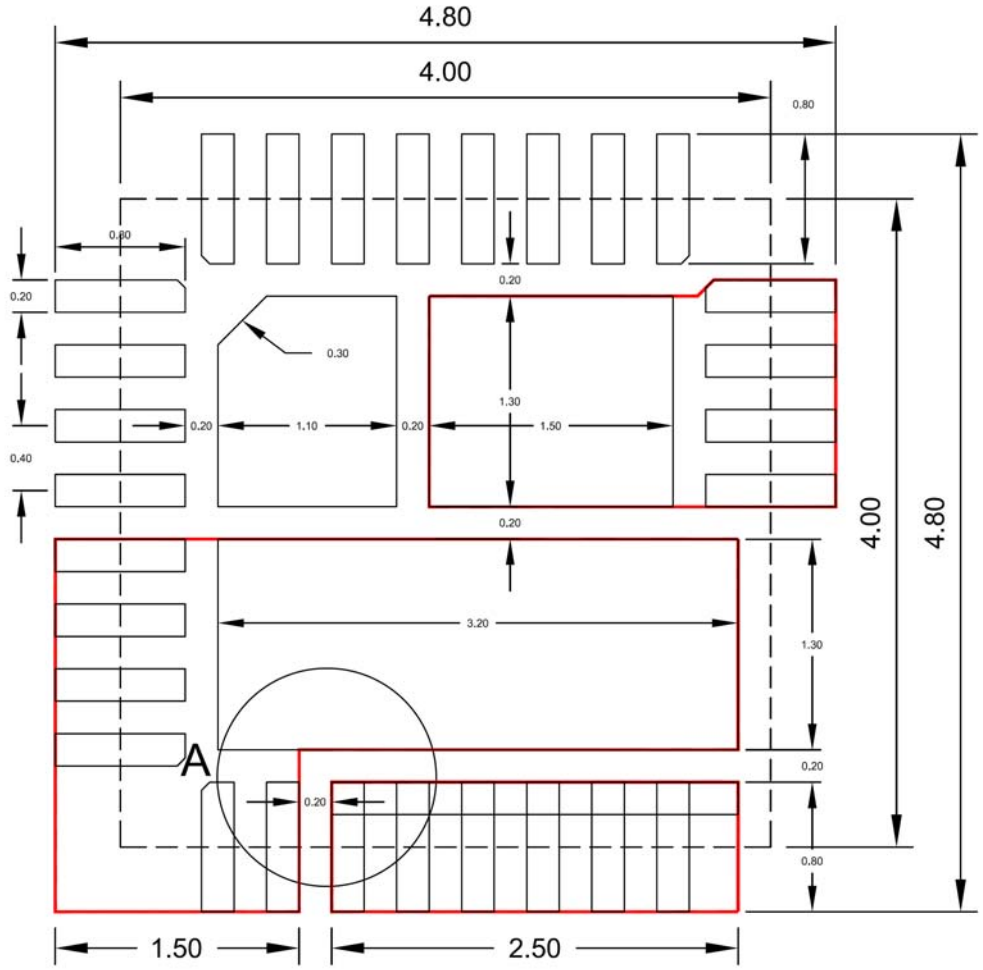
$$I_{RMS} = I_{LOAD}\left(\frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}\right)$$

Layout Considerations

- Connect AGND (Pin2) to ground of bypass LDO5 and FB path.
- Connect PGND (Pin4) to ground of bypass VCC.
- Connect AGND and PGND together close to the IC and the negative terminal of C_{OUT}.
- Star connection PGND ground plane to system ground (normally, it's defined as ground of power supply or battery pack.).
- Connect PGND of power component Low-side MOSFET source, C_{IN}, and C_{OUT} to system ground by a plane.
- All sensitive analog traces such as OUT, and FB should be placed away from high-voltage switching node such as LX, BST nodes to avoid coupling.

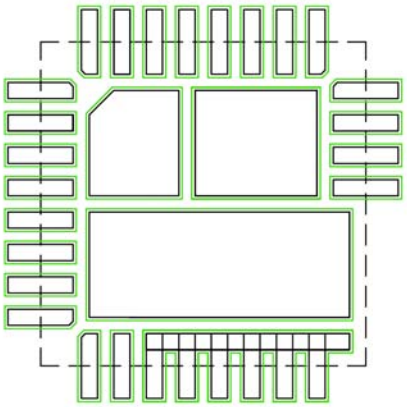
Minimum Footprint PCB Layout Section

QFN4X4-28

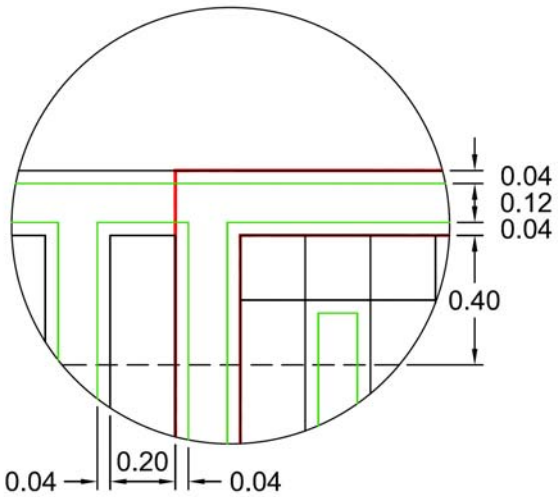


Top Layer

* Recommend Top Layer Thermal Pad Design Following Red Line for Better Characteristic.

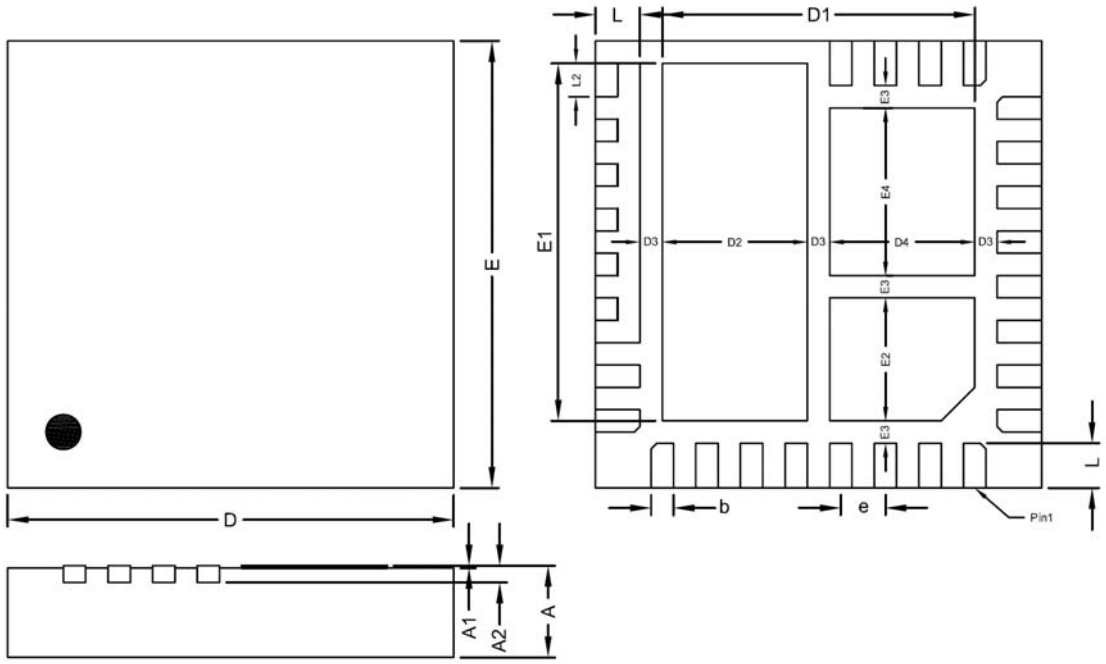


Top Layer with Solder Mask



Section A

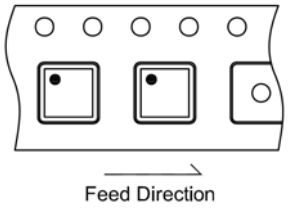
Package Information



QFN4X4-28 Package

Symble	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.80	0.90	0.0276	0.0315	0.0354
A1	0.00	---	0.05	0.0000	---	0.0020
A2		0.15 BSC			0.0059 BSC	
D	3.95	4.00	4.05	0.1555	0.1575	0.1594
E	3.95	4.00	4.05	0.1555	0.1575	0.1594
D1	2.70	2.80	2.90	0.1063	0.1102	0.1142
E1	3.15	3.20	3.25	0.1240	0.1260	0.1280
D2	1.25	1.30	1.35	0.0492	0.0512	0.0531
E2	1.05	1.10	1.15	0.0413	0.0433	0.0453
D3		0.20 BSC			0.0079 BSC	
E3		0.20 BSC			0.0079 BSC	
D4	1.25	1.30	1.35	0.0492	0.0512	0.0531
E4	1.45	1.50	1.55	0.0571	0.0590	0.0453
b	0.15	0.20	0.25	0.0059	0.0079	0.0098
e		0.40 BSC			0.0157 BSC	
L	0.35	0.40	0.45	0.0138	0.0157	0.0177
L2	0.25	0.30	0.35	0.0098	0.0118	0.0138

Taping Specification



PACKAGE	Q'TY/BY REEL
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