

High Efficiency Step Down Controller

Features

- Ultra-High Efficiency
- Low Quiescent Current of 110 μ A
- No Current-Sense Resistor (Lossless I_{LIMIT})
- Quasi-PWM with 100ns Load-Step Response
- 1.5% VOUT Accuracy Over Line and Load
- Programmable Switching Frequency
- 0.8V to 5.5V Adjustable Output Range
- 4.5V to 28V Adapter or Battery Input Range
- Integrated Boost Switch
- UVP (non-latch)
- Over Temperature Protection (non-latch)
- 3.3ms Soft-Start
- Drives Large Synchronous-Rectifier EFTs
- Power-Good Indicator
- Fixed 5V, 10mA Linear Regulator

Applications

- I/O Supply
- Networking Power Supply

General Description

G5415A is a synchronous step down controller. It uses constant on-time control scheme to handle wide input/output voltage ratios with ease and provides 100ns “instant-on” response to load transients while maintaining a relatively constant switching frequency. The G5415A achieves high efficiency at a reduced cost by eliminating the current-sense resistor found in traditional current-mode PWMs. Efficiency is further enhanced by an ability to driver large synchronous rectifier MOSFETs. Single-stage buck conversion allows these devices to directly step down high-voltage batteries for the highest possible efficiency. The built-in 5V LDO supports 10mA for internal circuit. The G5415A is intended for the main power supply for the networking system or other low-voltage supplies as low as 0.8V. The G5415A is available in TQFN3X3-16 package.

Ordering Information

ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE (Green)
G5415AR41U	5415A	-40°C to +85°C	TQFN3X3-16

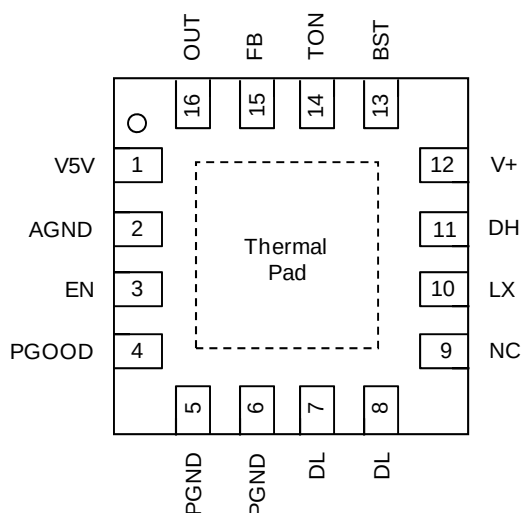
Note: R4: TQFN3X3-16

1: Bonding Code

U: Tape & Reel

Green: Lead Free / Halogen Free

Pin Configuration



G5415A TQFN3X3-16

Note: Recommend connecting the Thermal Pad to the Ground for excellent power dissipation.

Absolute Maximum Ratings

V+ to AGND -0.3V to 30V
 V5V, PGOOD, OUT, EN to AGND -0.3V to 6V
 FB, TON to AGND -0.3V to (V5V+0.3V)
 DL to PGND -0.3V to (V5V+0.3V)
 BST to PGND -0.3V to 35V
 DH to LX -0.3V to 6V
 LX to BST -6V to 0.3V
 LX to PGND -0.3V to 30V
 <30ns -6V to 36V
 Thermal Resistance of Junction to Ambient (θ_{JA})
 TQFN3X3-16 68°C/W

Continuous Power Dissipation ($T_A=25^\circ\text{C}$)
 TQFN3X3-16 1.47W
 Thermal Resistance of Junction to Case (θ_{JC})
 TQFN3X3-16 7.5°C/W
 Junction Temperature 150°C
 Storage Temperature -65°C to 150°C
 Reflow Temperature (soldering, 10sec) 260°C
 ESD (HBM) 2KV
 ESD (MM) 200V

Electrical Characteristics

(VIN=12V, V5V=5V, EN=5V, $T_A=25^\circ\text{C}$)

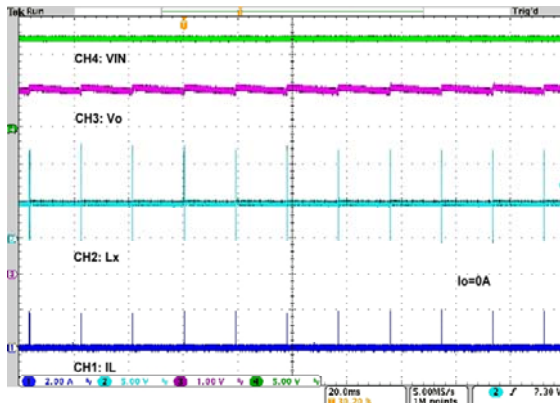
The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V+ Input Voltage Range	V+	4.5	---	26	V
LDO Output Voltage	V5V	4.75	5.0	5.25	V
Line Regulation of V5V	Load=1mA; V+=8V to 26V	---	5	30	mV
Load Regulation of V5V	Load=10mA	---	---	70	mV
Dropout Voltage of V5V	Load=10mA	---	1.0	1.2	V
Error Comparator Threshold (DC Output Voltage Accuracy)	V+=12V, FB=OUT	788	800	812	mV
Soft-Start Ramp Time	Rising edge of V5V>UVLO to 95% output voltage	2.2	3.3	6.8	ms
TON Operating Current	$R_{TON} = 240k\Omega$, V+=12V	---	50	---	μA
On Time	V+=12V, VOUT=3.3V, $R_{TON}=240k\Omega$, nominal	---	660	---	ns
Minimum On Time	VOUT=0.1V, $R_{TON}=240k\Omega$	---	80	---	ns
Minimum Off Time	FB=0.7V, LX=-0.1V,	---	300	---	ns
Quiescent Supply Current (V+)	FB forced above the regulation point	---	110	---	μA
Shutdown Current (V+)		---	1	---	μA
Output Shutdown Discharge Resistance	EN=AGND	---	12	32	Ω
Output Undervoltage Protection Threshold	With respect to error comparator threshold	60	70	80	%
Output Undervoltage Protection Blanking Time	From V5V>UVLO	2.2	5.5	6.8	ms
Current-Limit Threshold Voltage		105	120	135	mV
Zero Current Threshold (Zero Crossing)	PGND - LX	---	3	---	mV
PGOOD Trip Threshold	Measure at FB with respect to error comparator threshold, falling edge. Hysteresis=32mV	-14	-10	-7.5	%
PGOOD Output Low Voltage	ISINK=1mA	---	---	0.2	V
PGOOD Propagation Delay		---	5	16	μs
Thermal Shutdown Threshold	Hysteresis=20°C	---	165	---	°C
V5V Undervoltage Lockout Threshold (UVLO)	Rising edge, hysteresis = 200mV, PWM disabled below this level	3.7	3.9	4.3	V
DH Gate-Driver On-Resistance	BST-LX forced to 5V	---	5	---	Ω
DL Gate-Driver On-Resistance (Pull-up)	DL, high state,	---	1	---	Ω
DL Gate-Driver On-Resistance (Pull-down)	DL, low state	---	0.5	---	Ω
DH Gate-Driver Source/Sink Current	DG forced to 2.5V, BST-LX forced to 5V	---	1	---	A
DL Gate-Driver Source Current	DL forced to 2.5V, V5V forced to 5V	---	1	---	A
DL Gate-Driver Sink Current	DL forced to 2.5V, V5V forced to 5V	---	2	---	A
Dead Time	DL rising	---	15	---	ns
	DH rising	---	15	---	
BST Switch Forward Voltage	Forwarding Current=10mA	0.2	0.35	0.4	V
Logic Input High Voltage	EN	1.4	---	V5V	V
Logic Input Low Voltage	EN	---	---	0.7	V

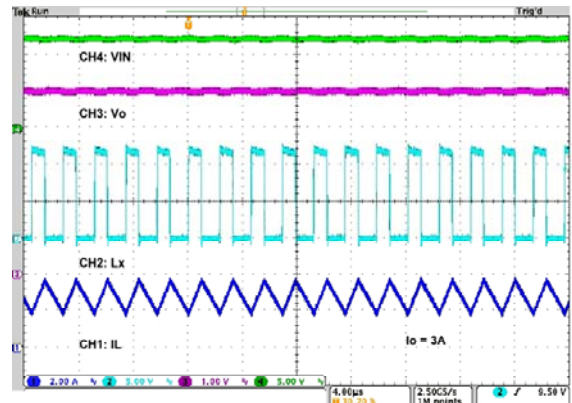
Typical Performance Characteristics

$V_{IN}=12V$, $V_5V=5V$, $EN=5V$, $V_O=5V$, $T_A=25^{\circ}C$.

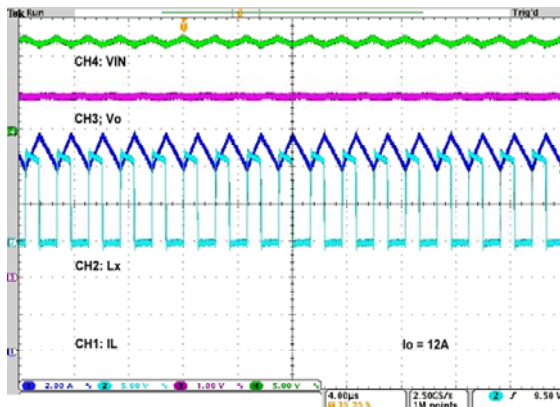
Stability



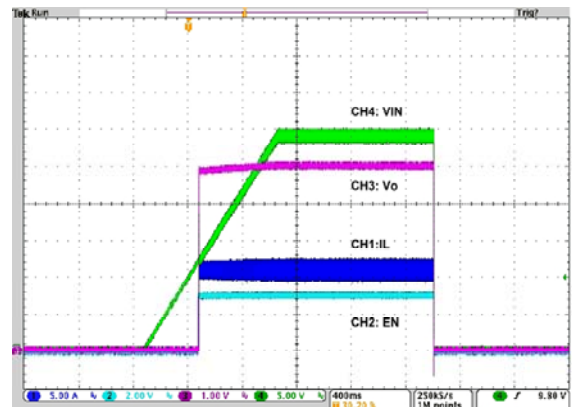
Stability



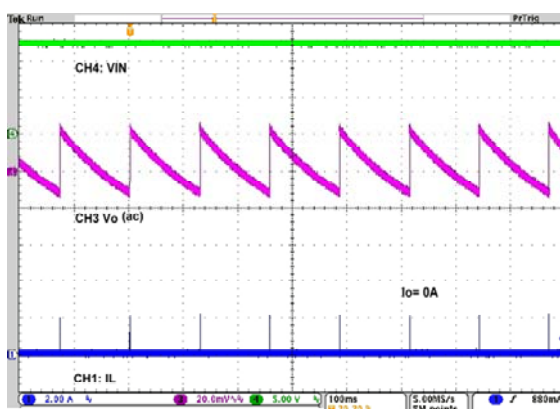
Stability



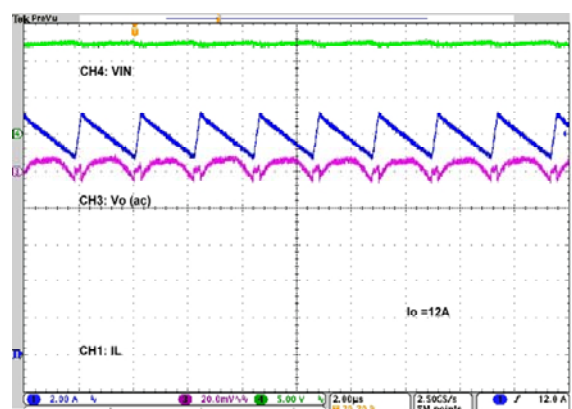
Operation with Vin Chattering



Ripple

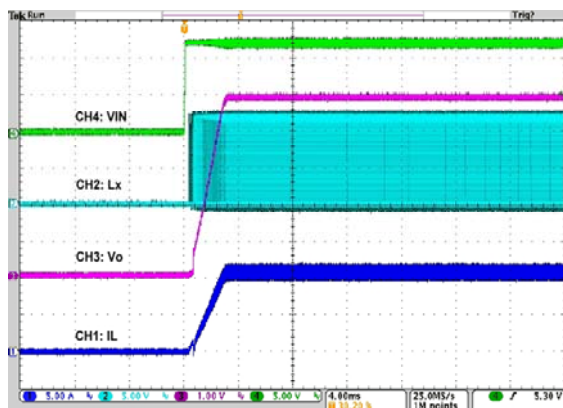


Ripple

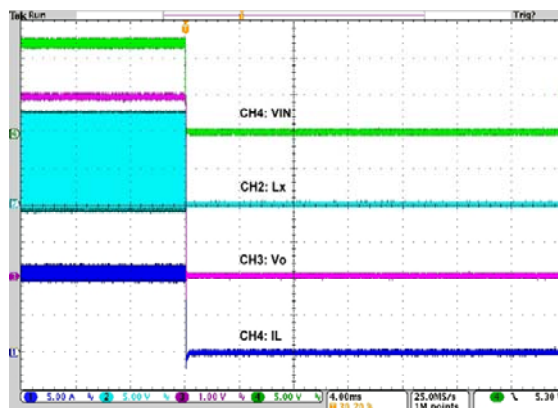


Typical Performance Characteristics (continued)

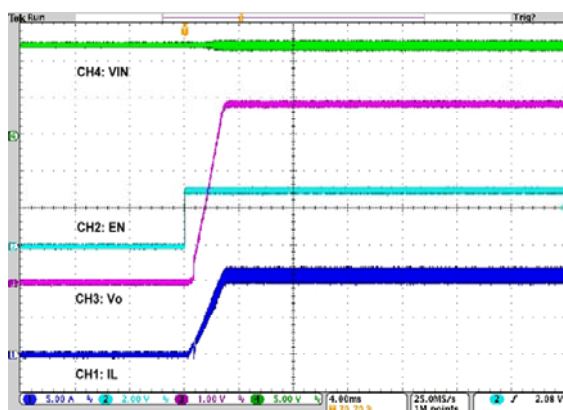
Power ON



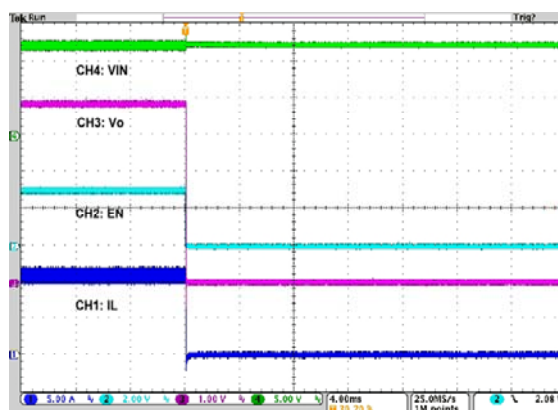
Power OFF



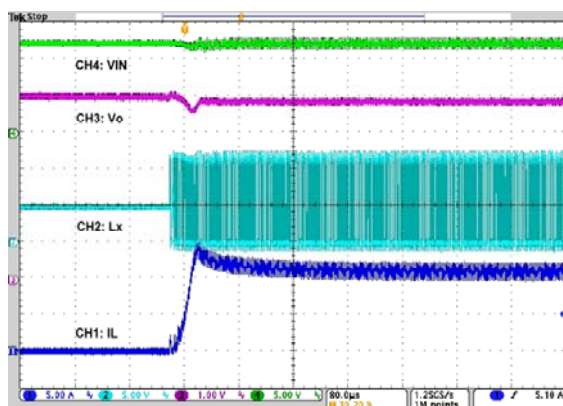
EN ON



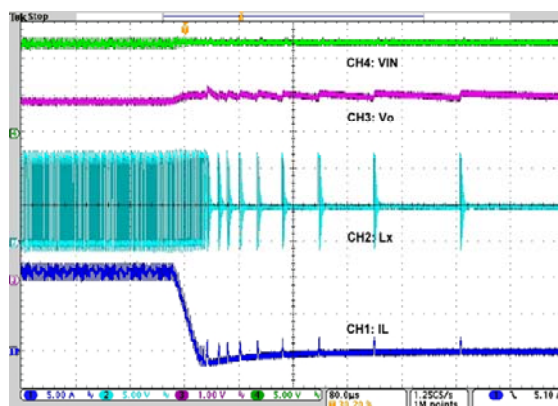
EN OFF



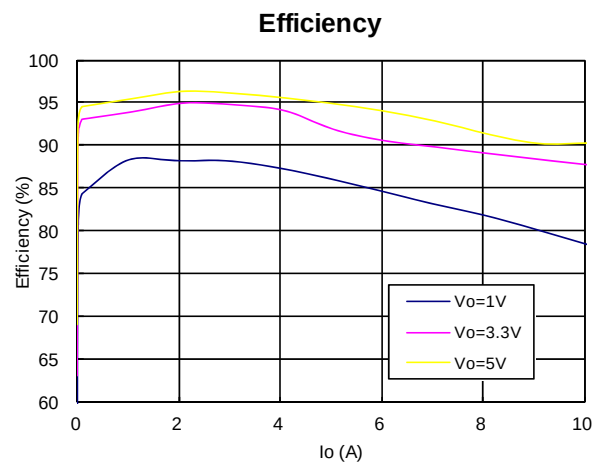
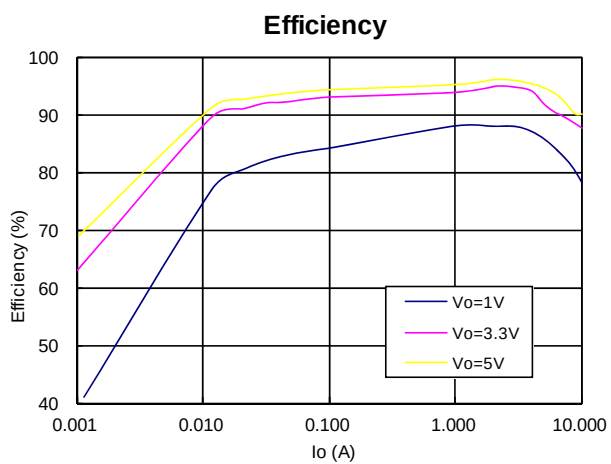
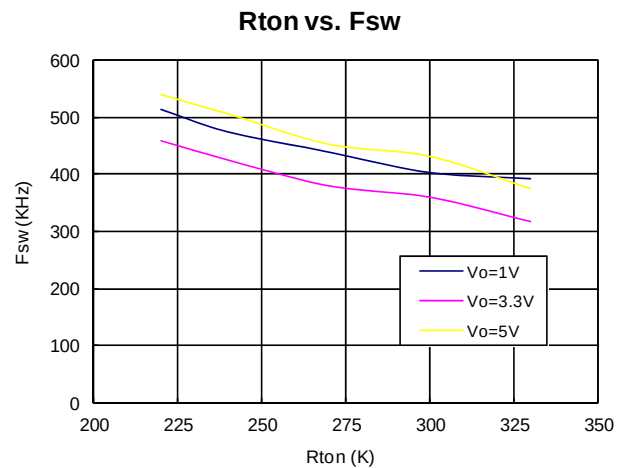
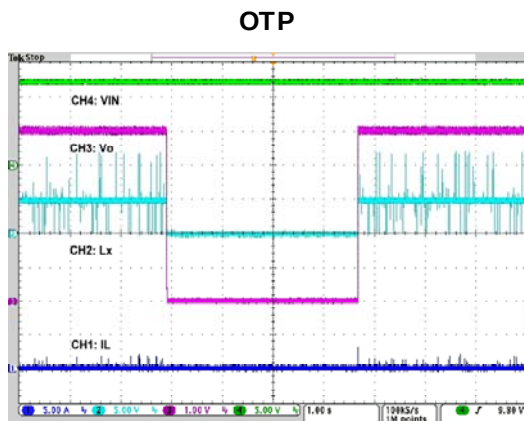
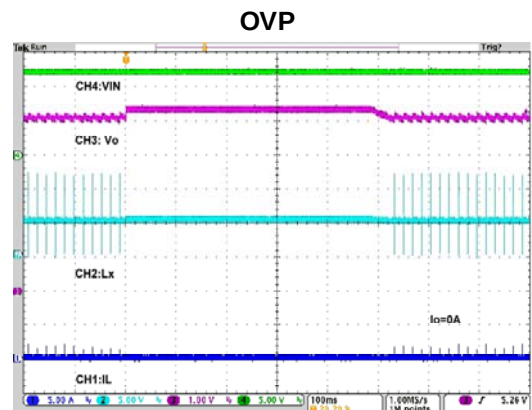
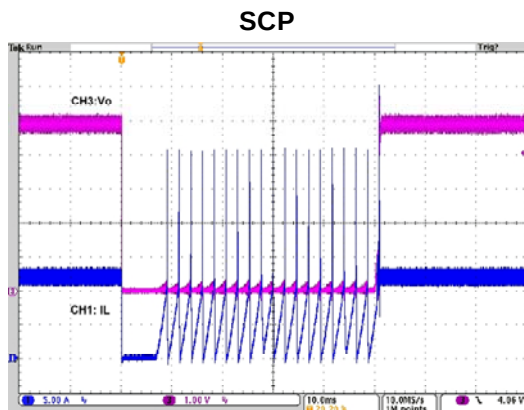
Load transient



Load transient



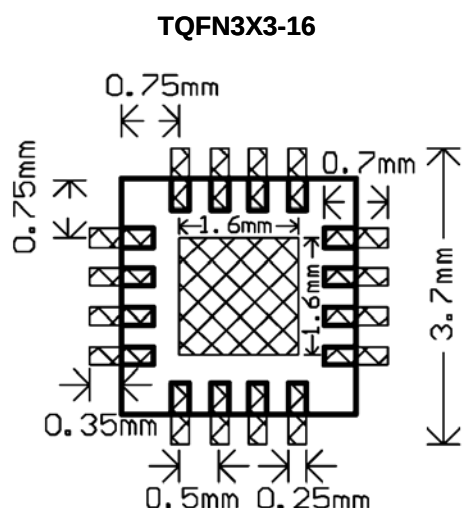
Typical Performance Characteristics (continued)



Pin Description

PIN	NAME	FUNCTION
1	V5V	5V Linear Regulator Output. Supply for Internal circuits. Bypass to AGND with a 4.7 μ F (min) ceramic capacitor.
2	AGND	Analog Ground
3	EN	Enable Input. Enable the 5V LDO and Buck Converter.
4	PGOOD	Power-Good Open-Drain Output. PGOOD is low when the output voltage is more than 10% below the normal regulation point or during soft-start. PGOOD is high impedance when the output is in regulation and the soft-start circuit has terminated.
5, 6	PGND	Power Ground.
7, 8	DL	Low Side Gate Driver Output.
9	NC	No connection
10	LX	External Inductor Connection. Connect LX to the switched side of the inductor. LX serves as the lower supply rail for the DH high-side gate driver. LX is also the positive input to the current-limit comparator.
11	DH	High Side Gate Driver Output.
12	V+	Power Supply Input. V+ is used to set the PWM one-shot Timing. Bypass to GND with a 4.7 μ F (min) Capacitor.
13	BST	Boost Flying-Capacitor Connection. Connect to an external capacitor according to the Standard Application Circuit. See <i>MOSFET Gate Drivers (DH, DL)</i> section.
14	TON	On-Time Selection-Control Input. Connect to LX with a resistor, R _{TON} .
15	FB	Feedback Input. Connect FB to a resistor divider from OUT for an adjustable output.
16	OUT	Output Voltage Connection. Connect directly to the junction of the external and output filter capacitors. OUT senses the output voltage to determine the on-time.

Minimum Footprint PCB Layout Section



Block Diagram

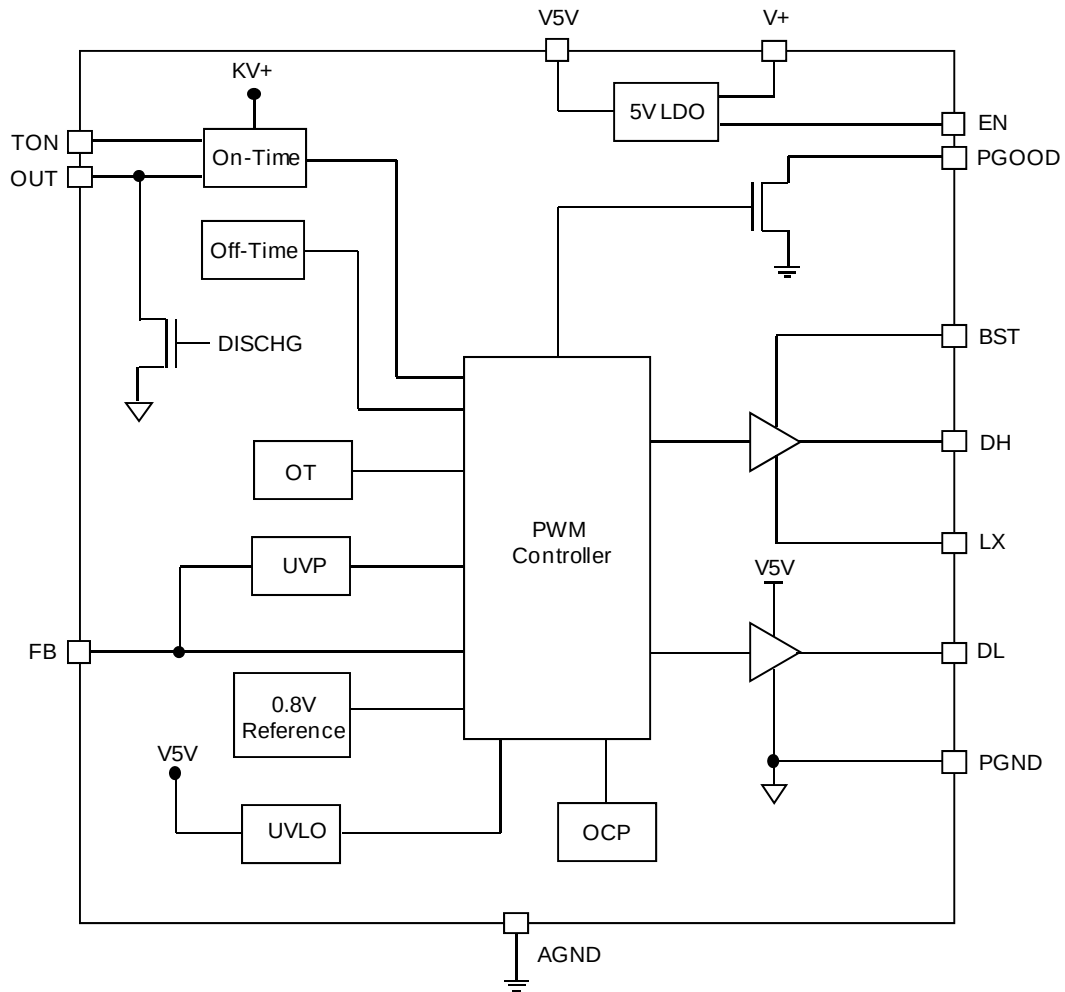


Fig. 1 Block Diagram of G5415A

Application Information

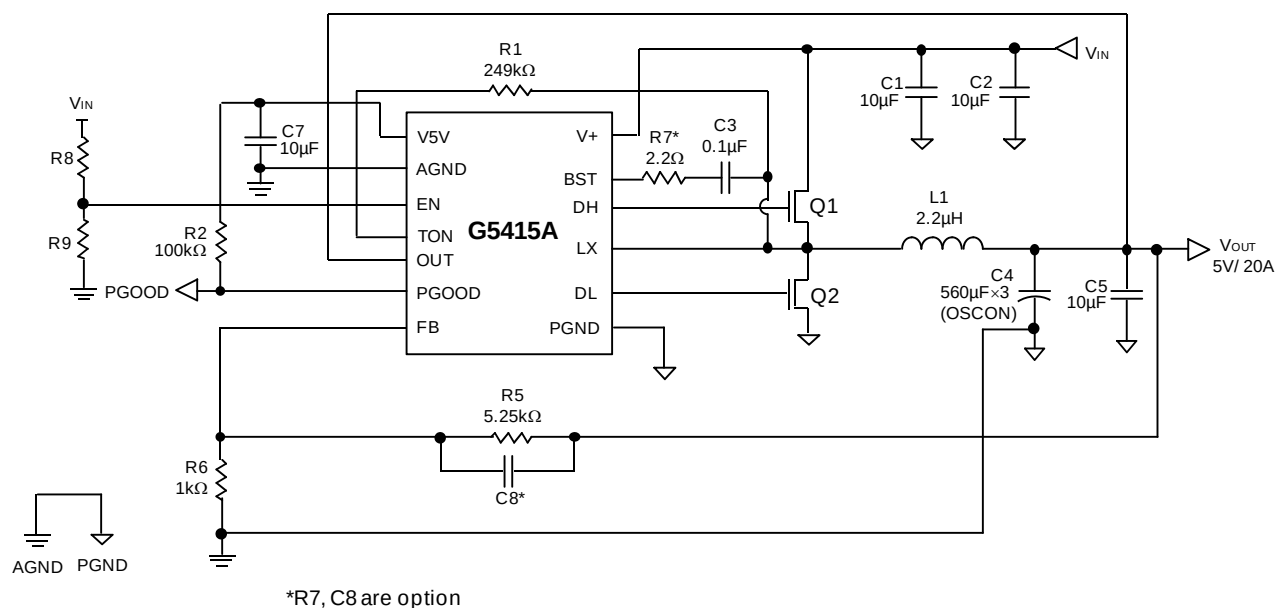


Fig. 2-A Standard Application Circuit

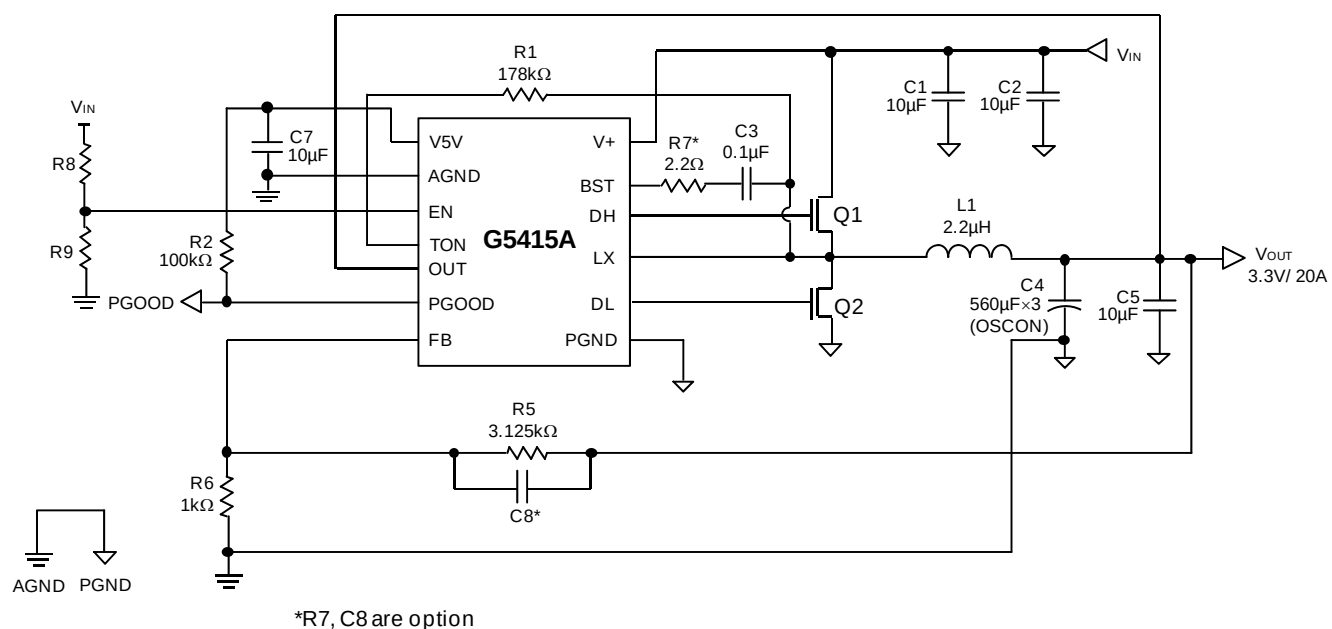


Fig. 2-B Standard Application Circuit

Detailed Description

G5415A is a synchronous step down controller with a fixed 5V LDO. A Quasi-PWM control is adapted in G5415A. It is a constant-on-time PWM control with input feed-forward while maintaining a relatively constant switching frequency. It advantages in the fast load-transient response compared with conventional constant-on-time PWM control. The Figure 2 shows the Block Diagram of G5415A. An EN pin is provided to turn on/off G5415A. It is recommended to connect a resistor divider from V+, or controlled by enable signal no more than V5V.

5V Linear Regulation

G5415A contains a LDO with fixed 5V output (V5V) enable by EN. It supports up to 10mA for the internal PWM circuit and gate-drivers. It can not support external circuit. Bypass V5V to AGND with 10μF (min) capacitor and close to the device.

Constant-on-time PMW Control with Input Feed-Forward

The Quasi-PWM control algorithm can be described briefly: the high-side switch on-time is determined by a one-shot whose period is inversely proportional to input voltage and directly proportional to output voltage. Another on-shot determines the minimum off-time. The on-time one-shot can be triggered if the error comparator is low, the low side switch current is below the current-limit threshold, and the minimum off-time one-shot has timed out.

On-Time Selection

G5415A allows to program the on-time. The on time is determined as below

$$T_{ON} = \frac{R_{TON} \times V_{OUT}}{(V_{IN} - 0.8)} \times 9.58 \times 10^{-12} + 4.63 \times 10^{-8}$$

($V_{OUT} < 4V$)

$$T_{ON} = \frac{R_{TON}}{(V_{IN} - 0.8)} \times 4.1 \times 10^{-11} + 2.46 \times 10^{-8}$$

($V_{OUT} \geq 4V$)

It results in a nearly constant switching frequency R_{TON} is a resistor connected from LX to the TON pin.

Pulse-Skipping Mode

In Pulse-Skipping Mode, an automatic switchover to PFM takes place at light load. It turns off the low side switch when the inductor current crosses to zero. This scheme will improve the light-load efficiency.

Current Limit

G5415A uses the on-state resistance of low side MOSFET as a current-sensing resistor. If the current-sense voltage (PGND-LX) is above the current-limit threshold, the PWM is not allowed to initiate a new cycle. The actual peak current is the current-limit threshold adding one inductor current ripple. So it depends on the on-resistance of MOSFET, Inductor value, and battery voltage. No external current-sensing resistor is necessary in the output current path. The current limit threshold voltage is set as 120mV internally. The equation of current limit is as following:

$$I_{LIM} = \frac{120 \text{ mV}}{R_{DS(on)}}$$

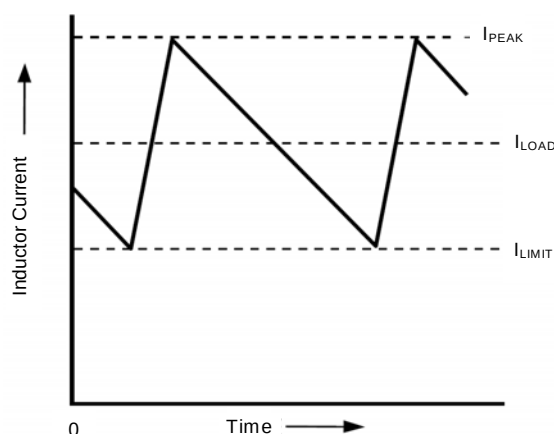


Fig. 3 Current Limit Setting

Gate Drivers

In the low duty factor application, it exists large difference of input voltage and output voltage. Therefore, large low-side MOSFET and moderate-size high-side MOSFET are needed for high efficiency. The DH and DL drivers are optimized for driving high-side and low-side MOSFETs. A non-overlap control circuit is needed to avoid the DH and DL turning on simultaneously. The DL driver with a 0.5Ω pull low transistor helps prevent the DL from being coupled to high during the fast rising-time of the LX node, due to the drain to gate capacitive coupling of low-side synchronous-rectifier MOSFET. A resistor in series with the BST is recommended that will reduce the EMI-producing efficiency loss by increasing the turn-on time of the high-side MOSFET.

UVLO and Soft-Start

When V5V is below 4V, undervoltage lockout (UVLO) inhibits switching and forces DL to high. It reset the fault latch and soft-start counter. An internal soft-start timer ramps up the current limit threshold to 100% of current limit setting within 3.3ms.

Power-Good Indicator

The Output voltage is always monitored for undervoltage by the PGOOD comparator. The PGOOD is open-drain type signal. In shutdown and soft-start period, PGOOD is kept low. After the soft-start timer has timed out, the PGOOD could be activated. A CD pin could be adjusted the PGOOD propagation delay time if the output voltage is within 10% of normal value.

Fault Protection

G5415A provides undervoltage protection, overvoltage protection, and overtemperature protection.

The undervoltage protection (UVP) function is like foldback current limit function. If the output voltage is under 70% of normal value 5.5ms after shutdown released, the undervoltage protection function is activated. The SMPS would turn off high-side and low-side MOSFETS, and restart after 9ms.

The G5415A has an overtemperature protection (OTP) that occurs when the die temperature is above 165°C. It will shutdown the SMPS and force high-side and low-side gate drivers output low. It could be released when die cool down or EN is toggled.

Adjustable-Output Feedback

Connecting the FB pin to a resistor divider between OUT to GND to adjust the output voltage between 0.8V to 5.5V.

Chose R6=10kΩ and solve the R5 with the equation:

$$R5 = R6 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right)$$

where $V_{FB} = 0.8V$ nominal.

Application Information

Inductor Selection

The inductor value is determined as follows:

$$L = \frac{V_{OUT} (V_{IN} - V_{OUT})}{V_{IN} \times f \times \Delta I_{LPP}}$$

Where ΔI_{LPP} is defined as inductor ripple current.

The inductor ripple current also impacts transient-response performance, especially at low V_{IN} - V_{OUT} differentials. Low inductor values allow the inductor current to slew faster, replenishing charge removed from the output filter capacitors by a sudden load step.

Maintaining the ratio of the inductor ripple current to the designed maximum load current within a 20% to 50% range is prudent.

Output Capacitor Selection

The output filter capacitor could be used with MLCC type capacitor. It is recommended to use 22μF×5 (minimum) as output capacitor for 500kHz switching frequency application.

Input Capacitor Selection

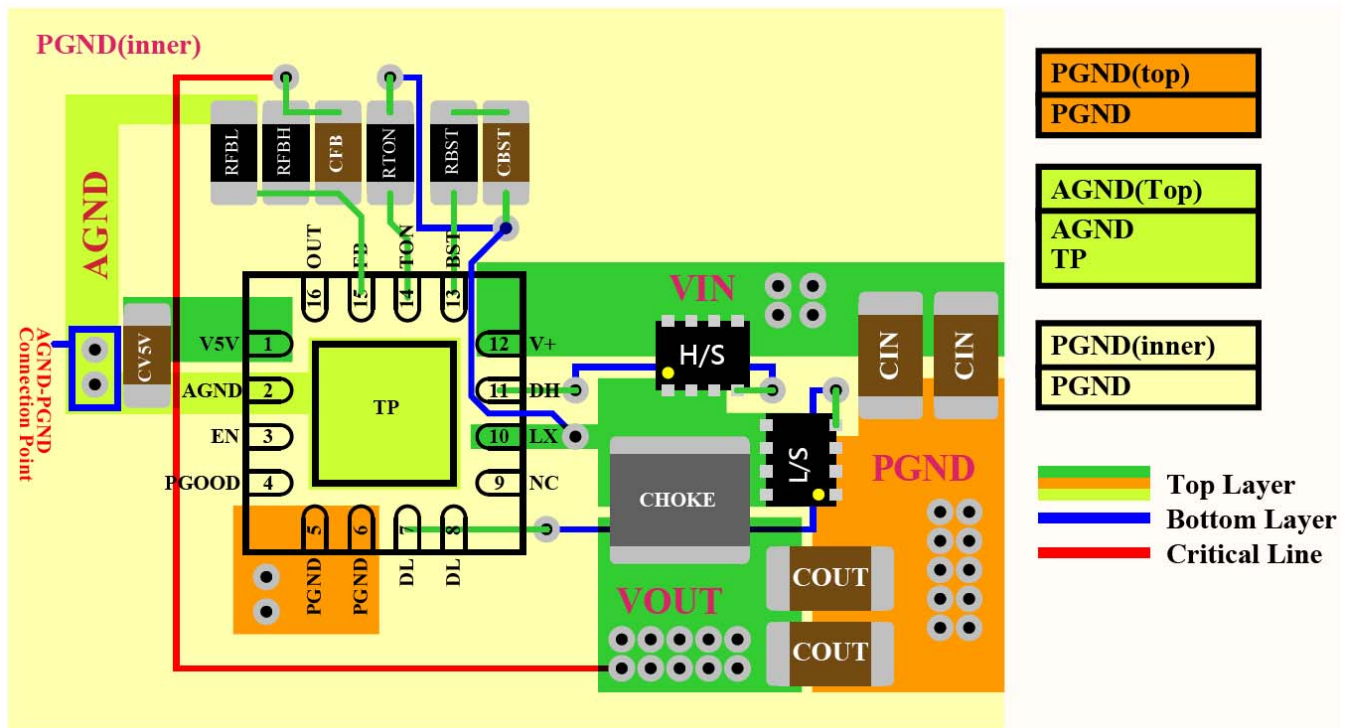
The input capacitor must meet the ripple current requirement (I_{RMS}) imposed by the switching currents. Nontantalum chemistries (ceramic, aluminum, or OS-CON) are preferred due to their resistance to power-upsurge currents.

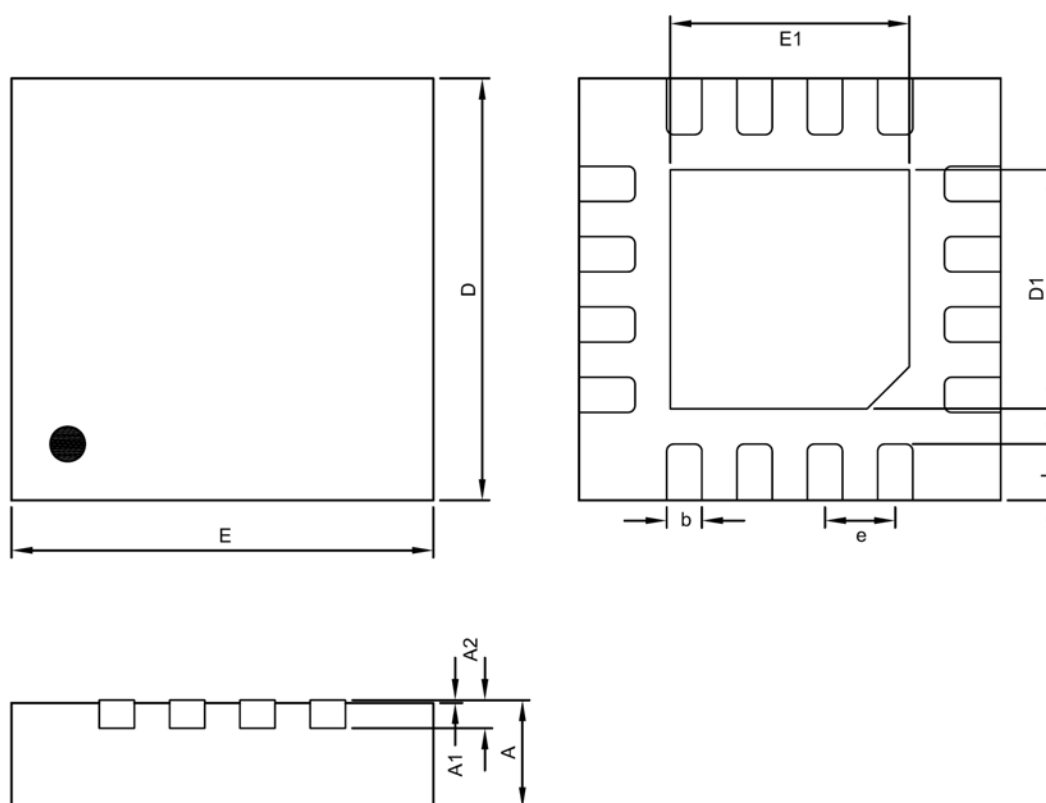
For optimal circuit reliability, choose a capacitor that has less than 10°C temperature rise at the peak ripple current.

$$I_{RMS} = I_{LOAD} \left(\frac{\sqrt{V_{OUT} (V_{IN} - V_{OUT})}}{V_{IN}} \right)$$

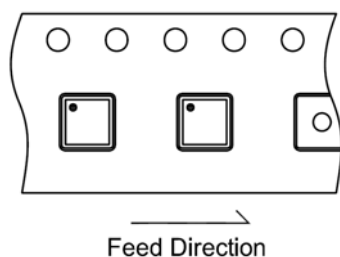
PCB Layout Guide

- Connect AGND (Pin2) to ground of bypass VCC and FB path.
- Connect AGND and PGND together close to the IC and the negative terminal of COUT.
- Star connection PGND ground plane to system ground (normally, it's defined as ground of power supply or battery pack.).
- Connect PGND of power component Low-side MOSFET source, CIN, and COUT to system ground by a plane.
- All sensitive analog traces such as OUT, and FB should be placed away from high-voltage switching node such as LX, BST nodes to avoid coupling.



Package Information

TQFN3X3-16 Package

Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.0276	0.0295	0.0315
A1	0.00	---	0.05	0.0000	---	0.0020
A2	0.20 REF			0.0079 REF		
D	2.95	3.00	3.05	0.1161	0.1181	0.1201
E	2.95	3.00	3.05	0.1161	0.1181	0.1201
D1	1.60	1.70	1.80	0.0630	0.0669	0.0689
E1	1.60	1.70	1.80	0.0630	0.0669	0.0689
b	0.18	0.25	0.30	0.0071	0.0098	0.0118
e	0.50 BSC			0.0197 BSC		
L	0.35	0.40	0.45	0.0138	0.0157	0.0177

Taping Specification


PACKAGE	Q'TY/REEL
TQNF3X3-16	3,000 ea

GMT Inc. does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and GMT Inc. reserves the right at any time without notice to change said circuitry and specifications.