Complete DDR Memory Power Solution

Features

- ***Synchronous Buck Converter (VDDQ)***
- **Ultra-High Efficiency**
- **Integrated 8.5mΩ at VCC=5V N-Channel MOSFET for Low Side**
- **Integrated 20mΩ at VCC=5V N-Channel MOSFET for High Side**
- **No Current-Sense Resistor (Lossless I_{LIMIT})**
- **Quasi-PWM with 100ns Load-Step Response**
- **Adjustable Output Range from 0.75V to 3.6V for 1.8V(DDR2) /1.5V(DDR3) /1.35V(DDR3L) /1.2V(LPDDR3) /1.2V(DDR4)**
- **2V to 26V Battery Input Range**
- **Programmable Switching Frequency**
- **OVP & UVP of VDDQ Output**
- **Power-Good Indicator**

- ***1.5A LDO (VTT), Buffered Reference (VTTREF)***
- **Support DDR2 (0.9 VTT) and DDR3 (0.75 VTT) and DDR4 (0.6 VTT) Requirements**
- **VLDOIN Voltage Range: 1.2V to 3.6V**
- **Requires Only 20µF Ceramic VTT Output Capacitance**
- **Supports High-Z in S3 and Soft-Off in S5**
- **Integrated Divider Tracks 1/2 VDDQSNS for Both VTT and VTTREF**
- **Remote Sensing (VTTSNS)**
- **±20mV Accuracy for VTT and VTTREF**
- **10mA Buffered Reference (VTTREF)**
- **Built-In Soft-Start to Reduce the VLDOIN Surging Current**
- **Over Current Protection of VTT Output**
- **Thermal Shutdown Protection**
-

- ***2.5V/1A LDO (V2P5)***
- **Support DDR4 VPP Requirement**

General Description

The G5416 is intended for DDR2/DDR3/DDR3L/ LPDDR3/DDR4 memory systems. It integrates a synchronous buck PWM converter with a 1.5A sink-source linear regulator and buffered reference.

The PWM converter uses constant on-time control scheme to handle wide input/output voltage ratios with ease and provides 100ns “instant-on” response to load transients while maintaining a relatively constant switching frequency. The G5416 achieves high efficiency at a reduced cost by eliminating the current-sense resistor found in traditional current-mode PWMs. Single-stage buck conversion allows these devices to directly step down high-voltage batteries for the highest possible efficiency.

The 1.5A sink/source tracking termination regulator is specifically designed for low-cost/ low-external component count systems. The regulator contains a high speed operational amplifier that provides fast load transient response with only 20µF (2x10µF) of ceramic output capacitance. The G5416 supports remote sensing functions and all features required to power the DDR2/DDR3/DDR3L/LPDDR3/DDR4 VTT bus termination according to the JEDEC specification. In addition, the G5416 includes integrated sleep-state controls placing VTT in High-Z in S3 (suspend to RAM) and soft-off for VTT and VTTREF in S5 (Shutdown).

The 2.5V/ 1.0A LDO supports the 2.5V requirement of DDR4 application. It converts 3.3V input power to 2.5V supply for V2P5.

The G5416 provides OVP, UVP, over current and thermal shutdown protection functions and is available in a 30-pin 4X4 QFN package.

Applications

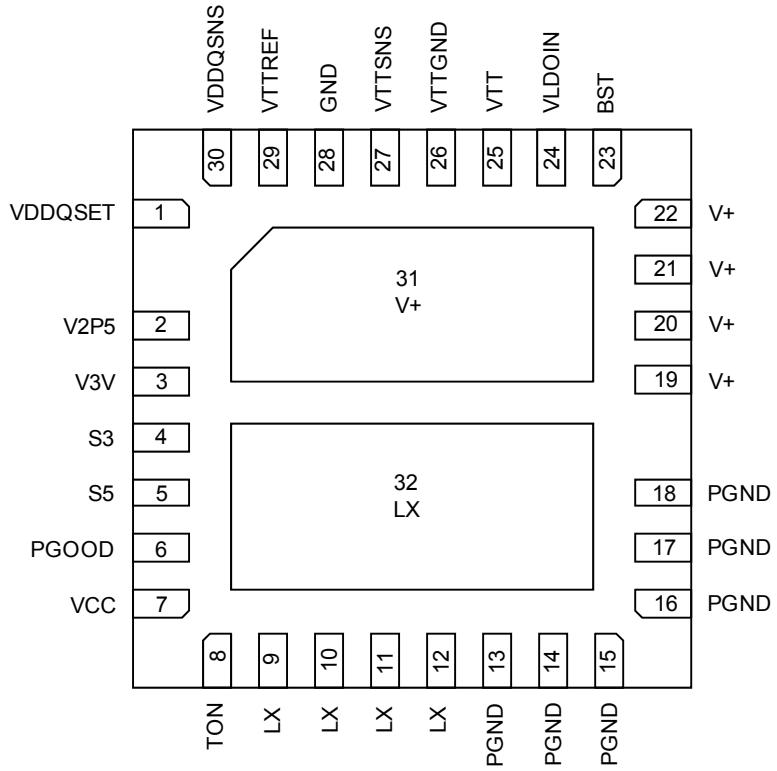
- **Notebook Computers**
- **DRAM Supply as Low as 0.75V**

Ordering Information

ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE (Green)
G5416QS1U	5416	-40°C to +85°C	QFN4X4-30

Note: QS: QFN4X4-30
1: Bonding Code
U : Tape & Reel
Green : Lead Free / Halogen Free

Pin Configuration



G5416 QFN4X4-30

Absolute Maximum Ratings

V+ to GND . . . . . -0.3V to 30V
VCC, VLDOIN, V3V to GND . . . . . .-0.3V to 6V
V2P5 to GND . . . . . .-0.3V to V3V+0.3V
PGOOD to GND. . . . . -0.3V to 6V
VTT, VDDQSET, VDDQSNS, VTTSNS, VTTREF, S3,
S5, MODE, TON to GND . . . . . -0.3V to 6V
BST to GND . . . . . .-0.3V to 36V
LX to BST . . . . . .-6V to 0.3V
LX to PGND . . . . . .-0.3V to 30V
<20ns . . . . . -6V to 36V
Thermal Resistance Junction to Ambient, (θ_{JA})
QFN4X4-30 . . . . . 25°C/W
Junction Temperature . . . . . 150°C
Storage Temperature . . . . . -65°C to 150°C
Reflow Temperature (soldering, 10sec) . . . . . 260°C

Electrical Characteristics

(V+=15V, VCC=5V, V3V=3.3V, VLDOIN=VDDQSNS=1.2V, T_A=25°C)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Synchronous Buck PWM Converter					
Input Voltage Range	Battery Voltage, V+	2	---	26	V
	VCC	4.5	---	5.5	
Error Comparator Threshold (DC Output Voltage Accuracy)	V+ = 4.5V to 24V, VDDQSET = VDDQ	0.7425	0.75	0.7575	V
Load Regulation Error	ILOAD = 0 to 3A	---	10	---	mV
Line Regulation Error	VCC = 4.5V to 5.5V, V+ = 4.5V to 24V	---	5	---	mV
Quiescent Supply Current 1 (V_{CC1})	V_{S3}=5V, V_{S5}=5V, VDDQSET forced above the regulation point in adjust mode	---	500	---	µA
Quiescent Supply Current 2 (V_{CC2})	V_{S3}=0V, V_{S5}=5V, VDDQSET forced above the regulation point in adjust mode, V3V floating	---	270	---	µA
Quiescent Supply Current 3 (V_{CC3})	V_{S3}=0V, V_{S5}=5V, VDDQSET forced above the regulation point in adjust mode, V3V=3.3V	---	300	---	µA
Shutdown Current (V_{CC3})	V_{S3}=0V, V_{S5}=0V	---	0.1	5	µA
Minimum ON Time		---	100	---	ns
Minimum OFF Time		---	350	---	ns
Operation ON Time	V+=19V, V_{DDQSNS}=1.2V, R_{TON} = 560kΩ, nominal	---	159	---	ns
Overvoltage Trip Threshold	With respect to error comparator threshold; 5% hysteresis	12	17	22	%
Overvoltage Fault Propagation Delay	VDDQSET forced 2% above the trip threshold in adjust mode	---	30	---	µs
Output Undervoltage Protection Threshold		---	440	---	mV
Output Undervoltage Protection Blanking Time	From VDDQ enable	---	2.3	---	ms
Current-Limit Threshold		10.5	12	15.5	A
Current-Limit Threshold (Zero Crossing)	PGND – LX	---	3	---	mV
PGOOD Trip Threshold	Measure at VDDQSET with respect to error comparator threshold, falling edge	-13	-10	-7	%
PGOOD Propagation Delay		---	5.2	---	µs
PGOOD Soft Start Time	From S5 enable to PGOOD ready		4.2		ms
PGOOD Output Low Voltage	ISINK=1mA	---	---	0.4	V
V_{CC} Undervoltage Lockout Threshold	Rising edge, hysteresis =200mV,PWM disabled below this level	3.9	4.2	4.5	V
High Side Switch Resistance	BST - LX forced to 5V; VCC=5V	---	20	24	mΩ
Low Side Switch Resistance	VCC=5V	---	8.5	10	mΩ
BST Diode Forward Voltage	Force 10mA current	0.2	0.4	0.5	V

Electrical Characteristics (continued)

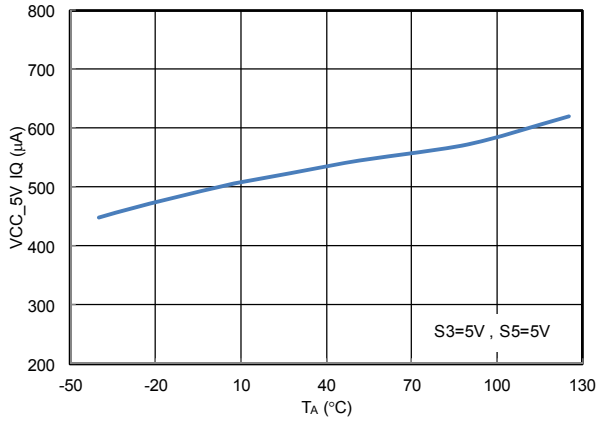
(V+=15V, VCC =5V, V3V=3.3V, VLDOIN=VDDQSNS=1.2V, T_A=25°C)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1.5A LDO, Buffered Reference					
Supply Current, VLDOIN	no load, V_{S5}=5V, V_{S3} =5V	---	0.03	2	mA
Standby Current, VLDOIN	no load, V_{S5}=5V, V_{S3} =0V	---	0.1	10	µA
Shutdown Current, VLDOIN	no load, V_{S5}=0V, V_{S3} =0V	---	0.1	1	µA
VDDQSNS Input Impedance	V_{S5}=5V, V_{S3} =5V	---	30	---	kΩ
VDDQ Shutdown Discharge Resistance	V_{S5}=0V	---	17	---	Ω
VTTSNS Input current	V_{S5}=5V, V_{S3} =5V	---	0.3	1	µA
VTT Output Voltage		0.9/0.75/0.675/0.6			V
VTT Output Voltage Load Regulation (VTTREF-VTT)	I_{VTT}=0	-20	---	20	mV
	$\|I_{VTT}\|$<1A	-30	---	30	
	$\|I_{VTT}\|$<1.5A	-40	---	40	
VTT Source Current Limit	VTT=VDDQSNS/2 *0.95, VTTOK=high	1.6	2.8	---	A
	VTT=0	1	1.5	---	
VTT Sink Current Limit	VTT=VDDQSNS/2 *1.05, VTTOK=high	1.6	2.8	---	A
	VTT=VDDQSNS	1	1.5	---	
VTT Leakage Current in S3 Mode	V_{S3}=0V,V_{S5}=5V	-10	---	10	µA
VTT Discharge Current	V_{S5}=0V, V_{S3} =0V, VDDQSNS=0, VTT=0.5V	10	20	---	mA
VTTREF Output Voltage	$\|I_{VTTREF}\|$<10mA, $V_{VDDQSNS}$ =1.8V	0.882	---	0.918	V
	$\|I_{VTTREF}\|$<10mA, $V_{VDDQSNS}$ =1.5V	0.735	---	0.765	
	$\|I_{VTTREF}\|$<10mA, $V_{VDDQSNS}$ =1.35V	0.661	---	0.688	
	$\|I_{VTTREF}\|$<10mA, $V_{VDDQSNS}$ =1.2V	0.588	---	0.612	
VTTREF Source Current	$V_{VDDQSNS}$=1.5V, V_{VTTREF}=0	---	-30	---	mA
VTTREF Sink Current	$V_{VDDQSNS}$= V_{VTTREF} =1.5V	---	70	---	mA
High Level Input Voltage	S3 , S5	1.6	---	---	V
Low Level Input Voltage	S3 , S5	---	---	1	V
Logic Input Leakage Current	S3 , S5	-1	---	1	µA
VTTSNS Leakage Current	V_{S5}=5V, V_{S3} =0V	-1	---	1	µA
Thermal Shutdown		---	150	---	°C
Thermal Shutdown Hystersis		---	18	---	°C
2.5V/1.0A LDO					
Input Voltage Range	V3V	3.0	3.3	3.6	V
V2P5 Output Voltage	V2P5	2.45	2.5	2.55	V
Dropout Voltage	Io=800mA	---	500	---	mV
Load Regulation	Io=10mA ~800mA	---	---	25	mV
Line Regulation	V3V=3.0V ~3.6V, Io=1mA	---	---	10	mV
Current Limit		1.1	1.6	1.95	A
Short Circuit Current		---	0.6	---	A
V2P5 Soft Start Time	From S5 enable to V2P5 ready	---	0.8	---	ms
V2P5 Shutdown Delay Time	From S5 disable to V2P5 off	30	---	---	ms
VPP Shutdown Discharge Resistance	V_{S5}=0V	---	140	---	Ω

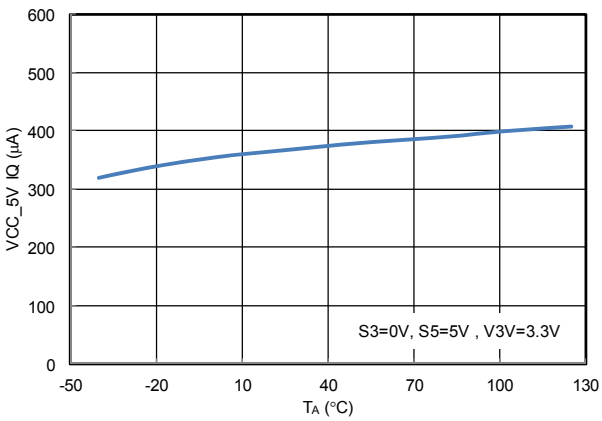
Typical Performance Characteristics

T_A=25°C.

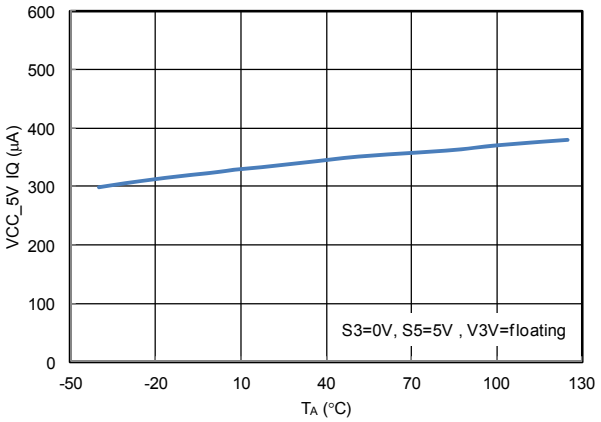
VCC_5V IQ vs. T_A



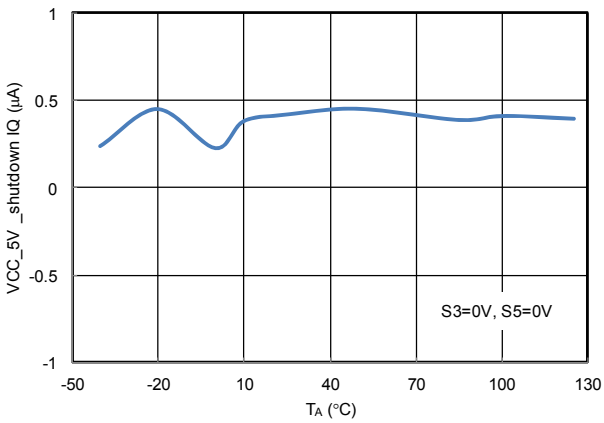
VCC_5V IQ vs. T_A



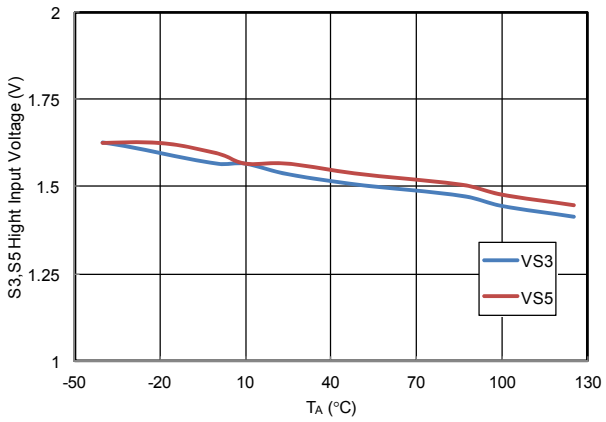
VCC_5V IQ vs. T_A



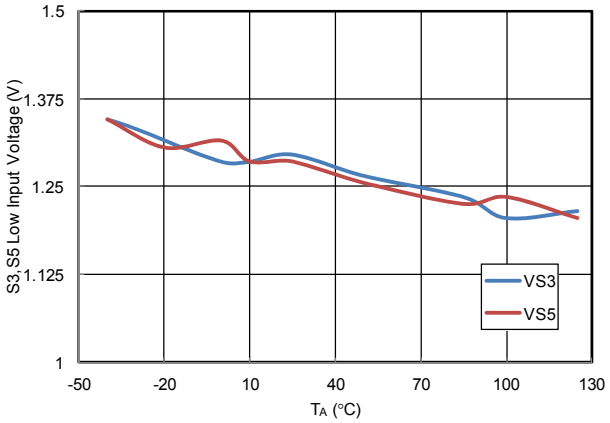
VCC_5V Shutdown IQ vs. T_A



S3,S5 High Input Voltage vs. T_A

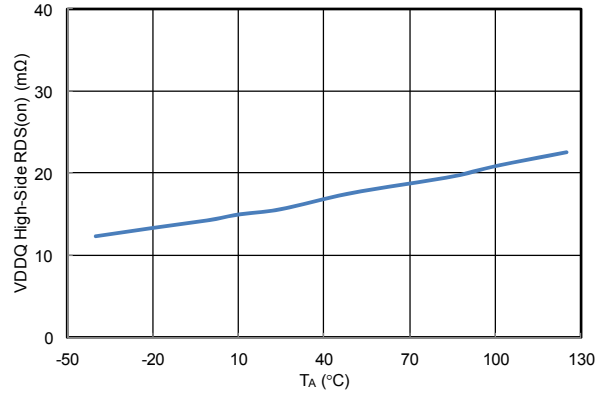


S3,S5 Low Input Voltage vs. T_A

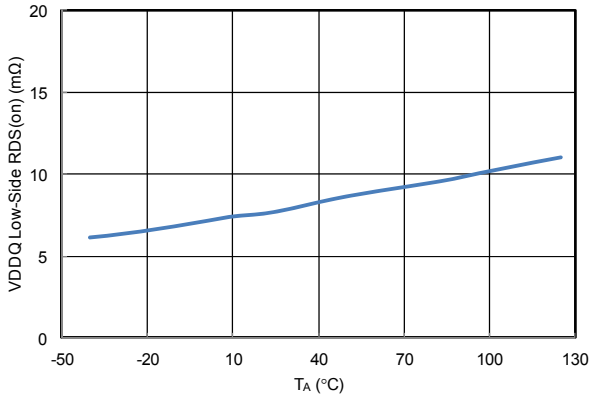


Typical Performance Characteristics (continued)

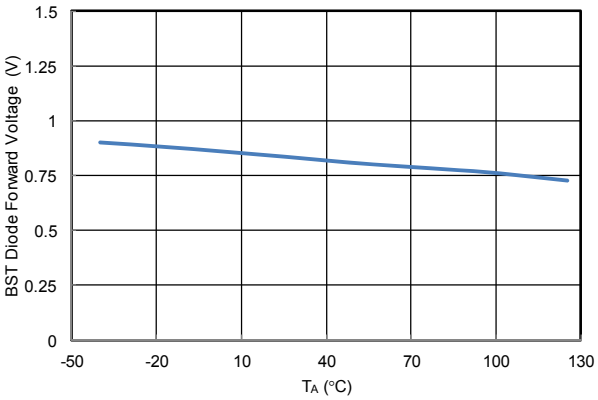
VDDQ High-Side RDS(on) vs. T_A



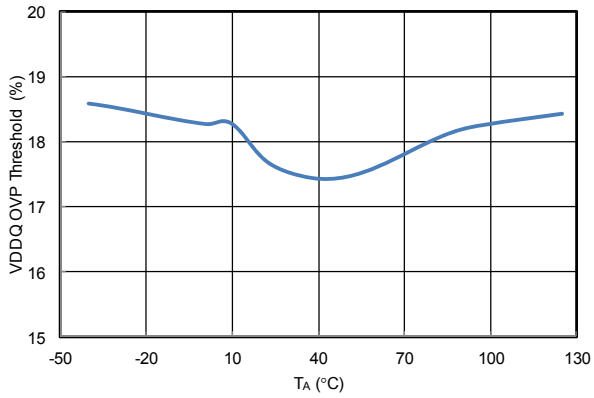
VDDQ Low-Side RDS(on) vs. T_A



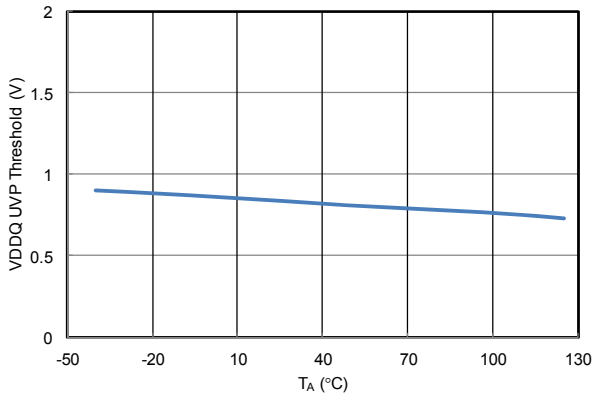
BST Diode Forward Votage



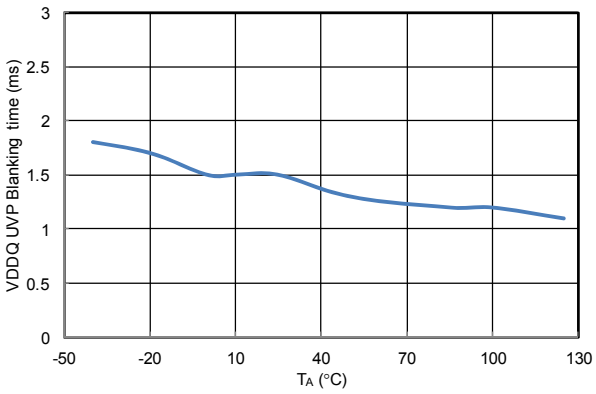
VDDQ OVP Threshold vs. T_A



VDDQ UVP Threshold vs. T_A

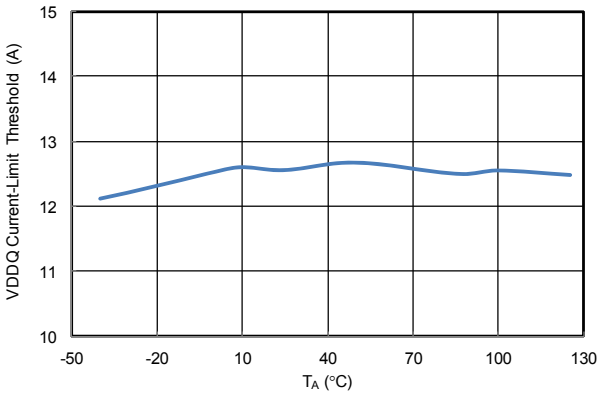


VDDQ UVP Blanking Time vs. T_A

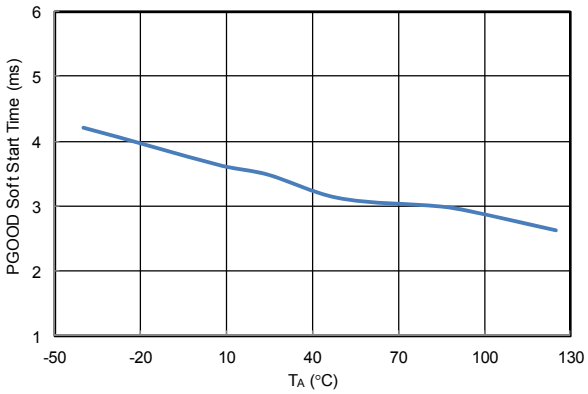


Typical Performance Characteristics (continued)

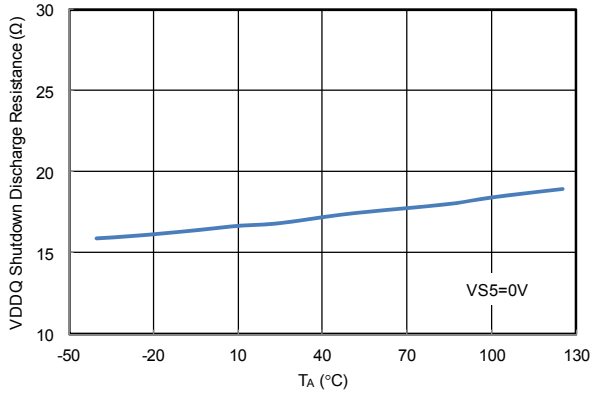
VDDQ Current-Limit Threshold vs. T_A



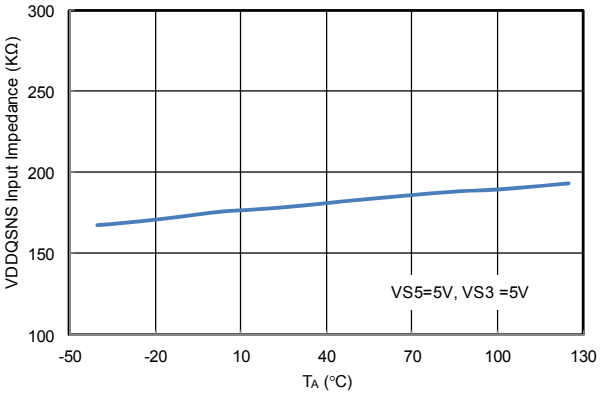
PGOOD Soft Start Time vs. T_A



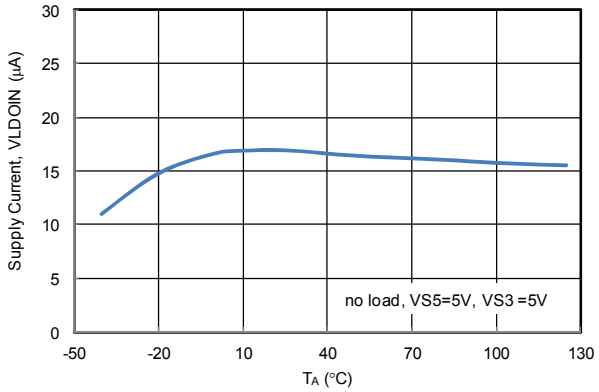
VDDQ Shutdown Discharge Resistance



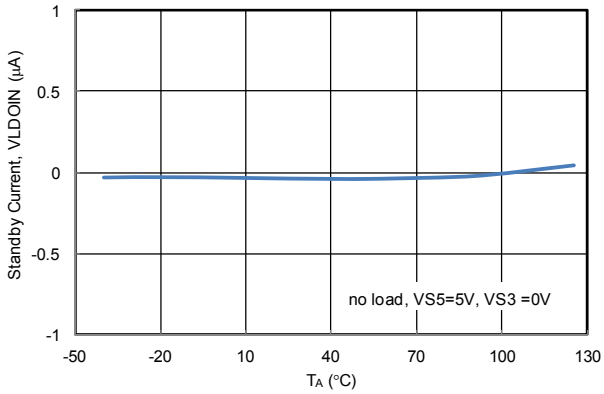
VDDQSNS Input Impedance



Supply Current, VLDOIN

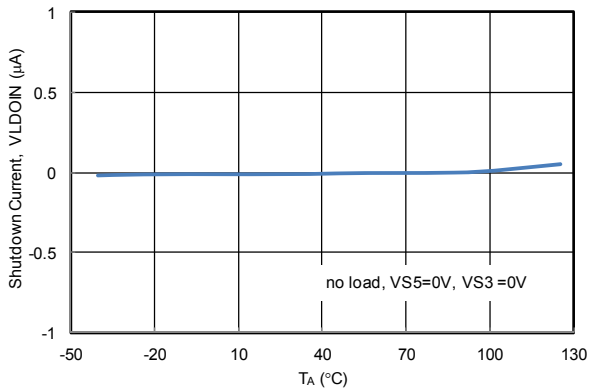


Standby Current, VLDOIN

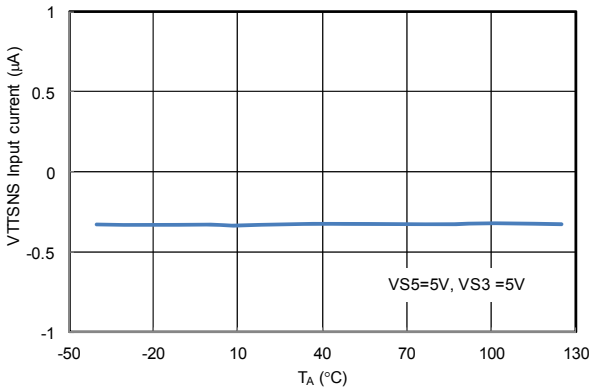


Typical Performance Characteristics (continued)

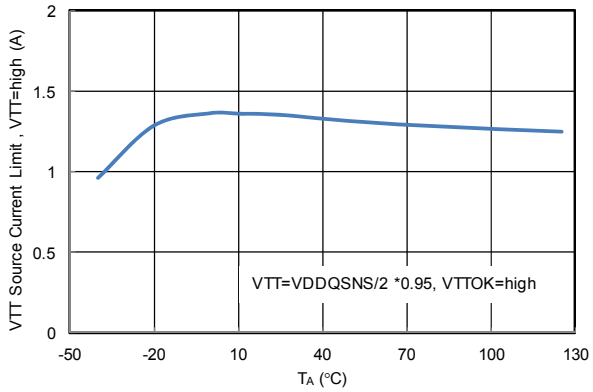
Shutdown Current VLDOIN



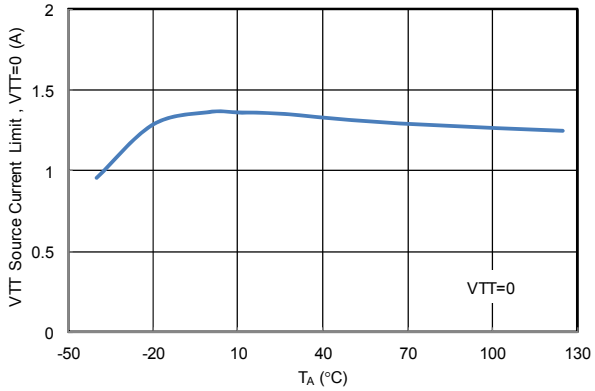
VTTSNS Input Current



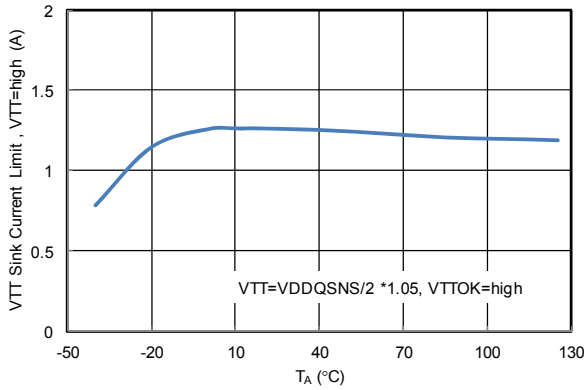
VTT Source Current Limit, VTT=high



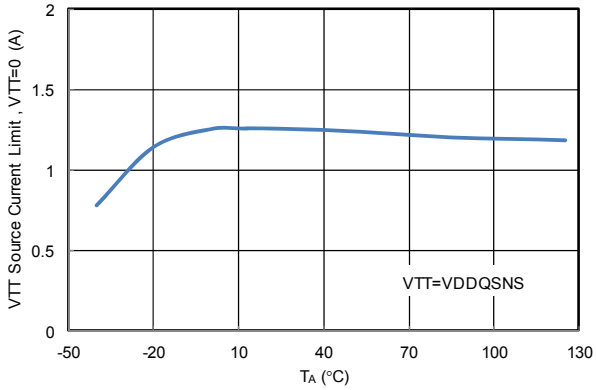
VTT Source Current Limit, VTT=0



VTT Sink Current Limit, VTT=high

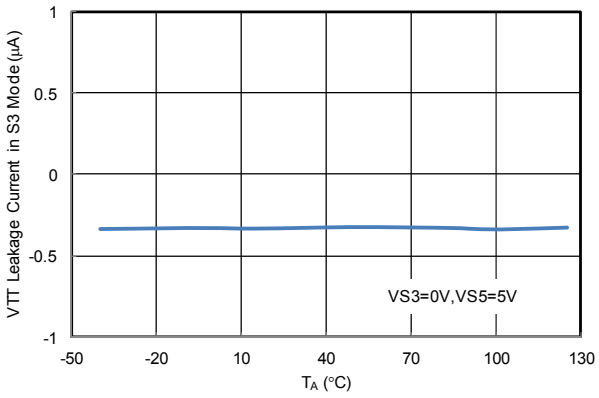


VTT Sink Current Limit, VTT=VDDQSNS

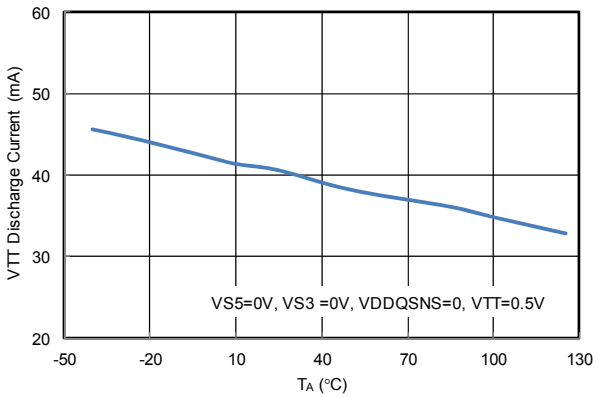


Typical Performance Characteristics (continued)

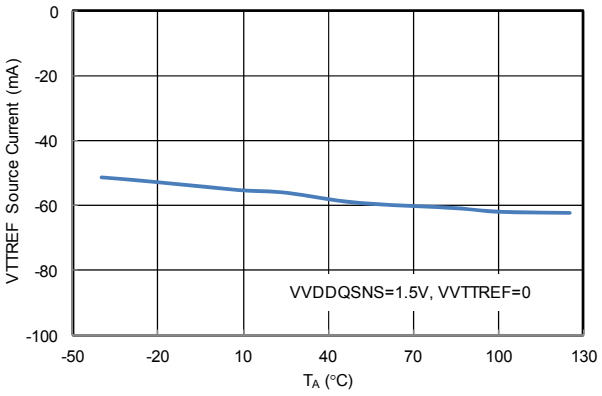
VTT Leakage Current in S3 Mode



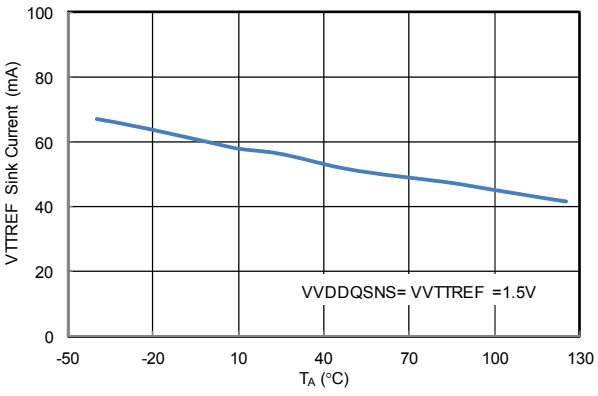
VTT Discharge Current



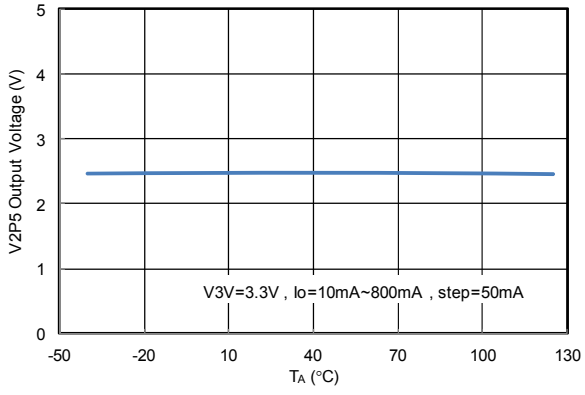
VTTREF Source Current



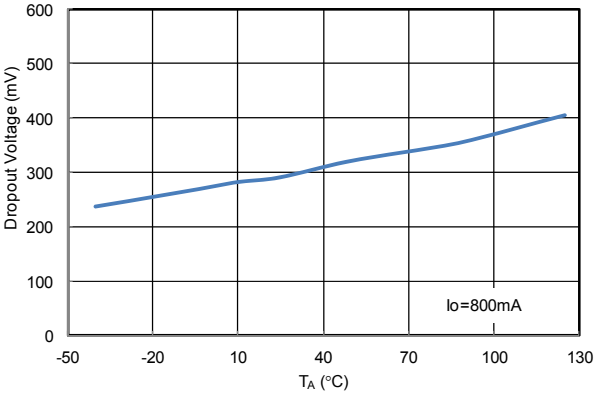
VTTREF Sink Current



V2P5 Output Voltage

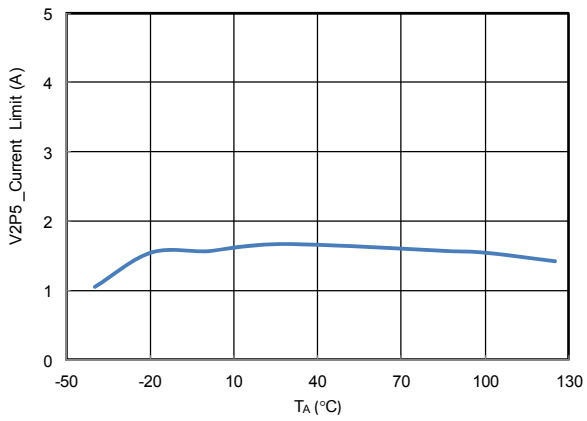


Dropout Voltage

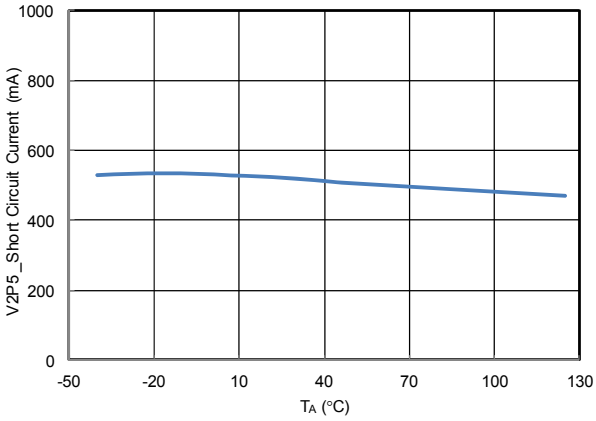


Typical Performance Characteristics (continued)

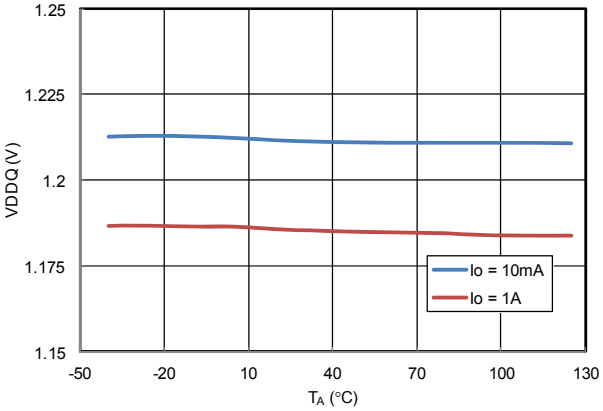
V2P5_Current Limit



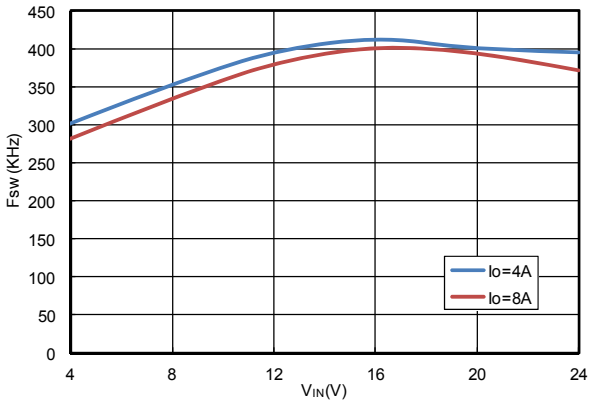
Short Circuit Current



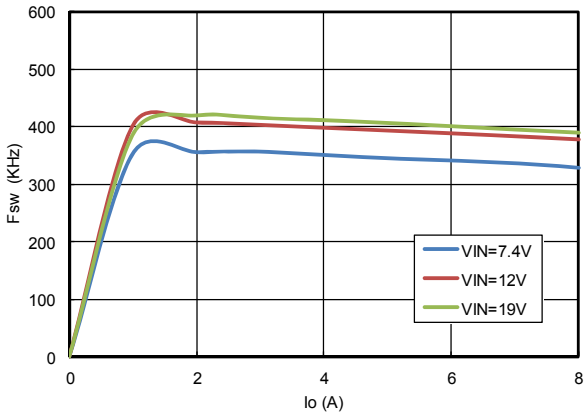
VDDQ Output Voltage vs. T_A



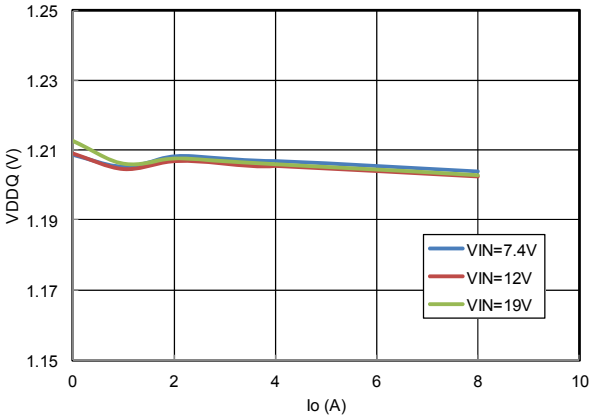
VDDQ Switching Frequency vs. Input Voltage



VDDQ Switching Frequency vs. Load Current

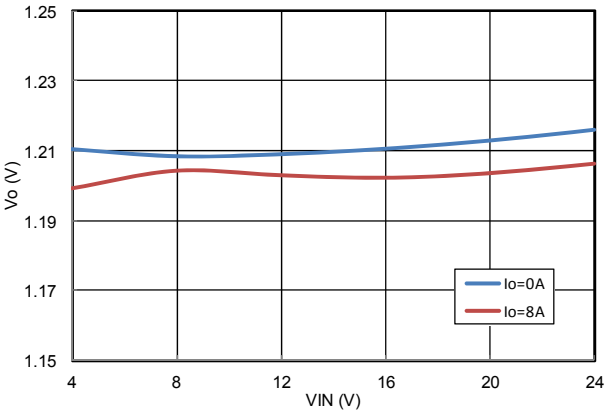


VDDQ Load Regulation,V_{OUT}=1.2V

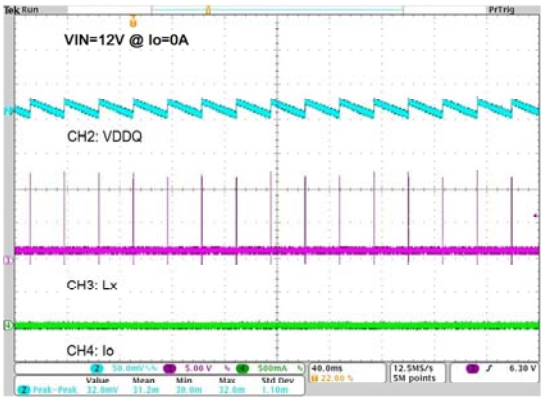


Typical Performance Characteristics (continued)

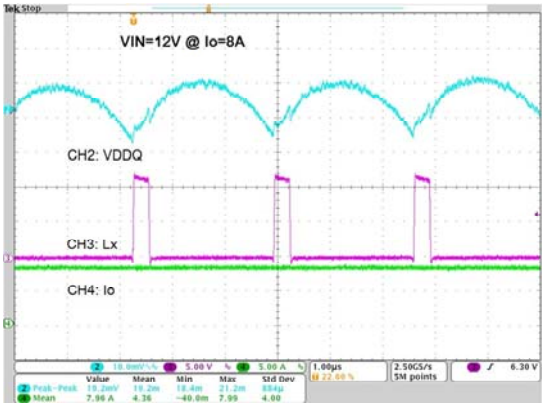
VDDQ Line Regulation,V_{OUT}=1.2V



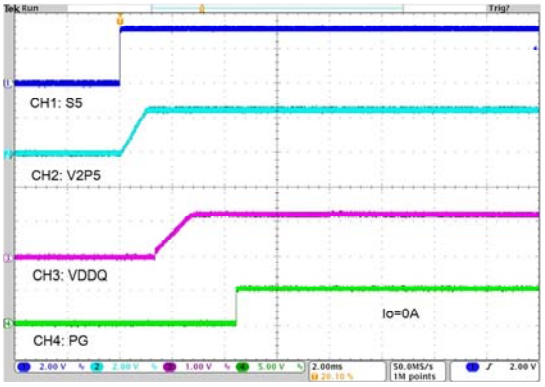
VDDQ Output Voltage Ripple,I_{OUT}=0A



VDDQ Output Voltage Ripple,I_{OUT}=8A



Start-Up, $I_{VDDQOUT}$=0A



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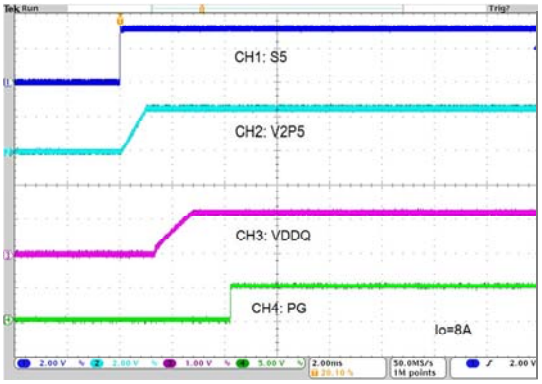
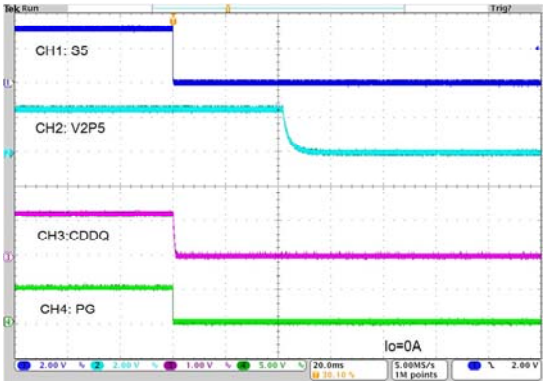
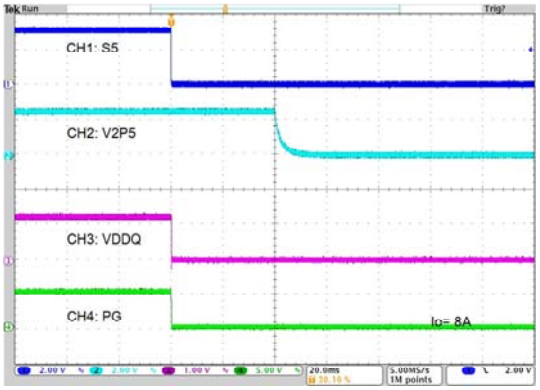


Shutdown, $I_{VDDQOUT}$=0A

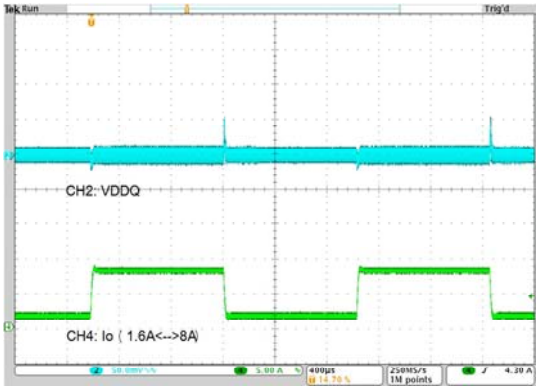


Typical Performance Characteristics (continued)

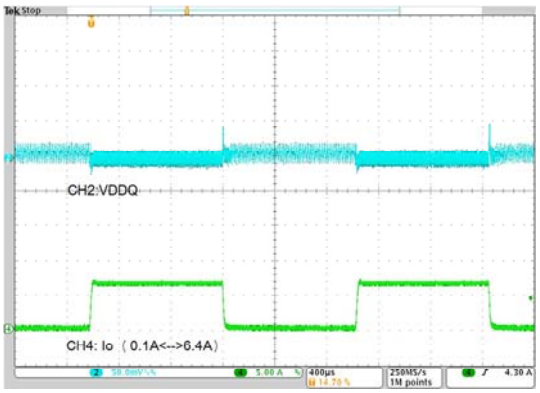
Shutdown, $I_{VDDQOUT}$=8A



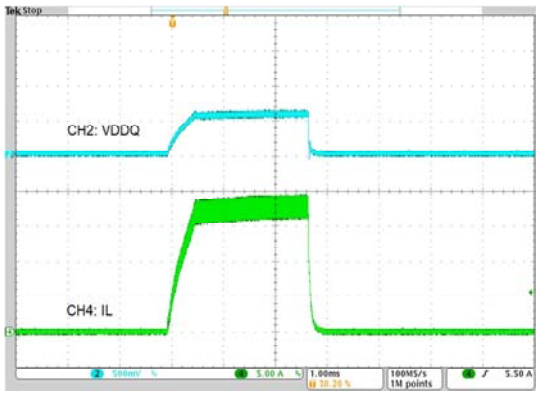
VDDQ Transient Response, 1.6A to 8A



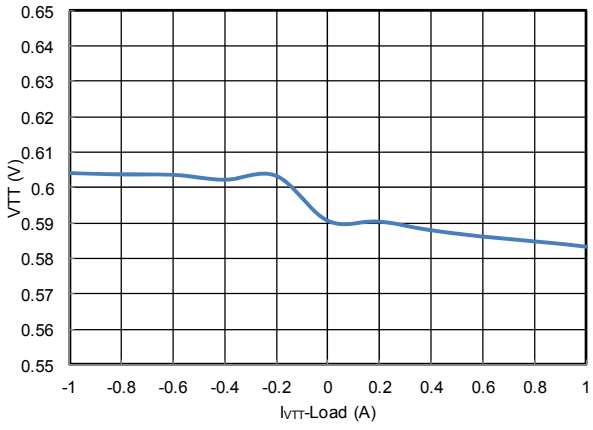
VDDQ Transient Response, 0.1A to 6.4A



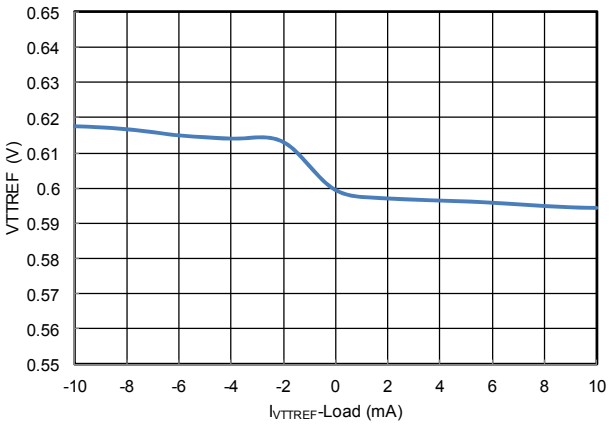
VDDQ Short Circuit Current



VTT Load Regulation, VTT=0.6V

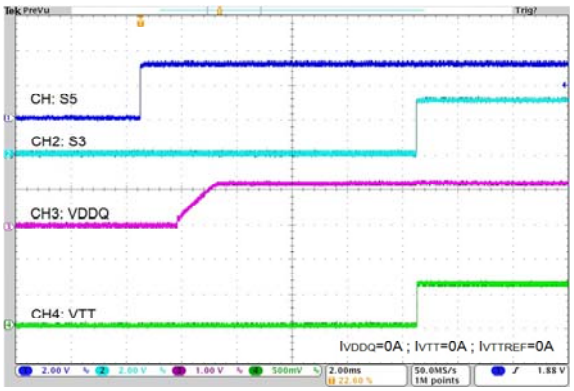


VTTREF Load Regulation, VTT=0.6V

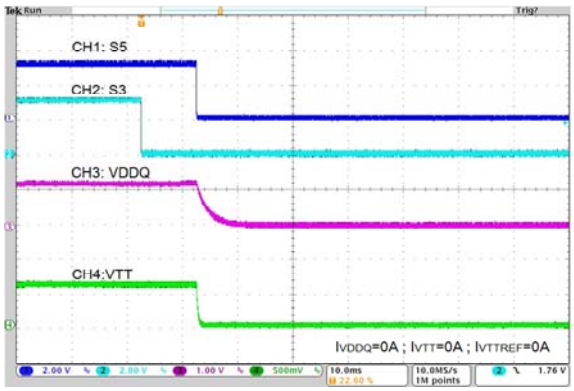


Typical Performance Characteristics (continued)

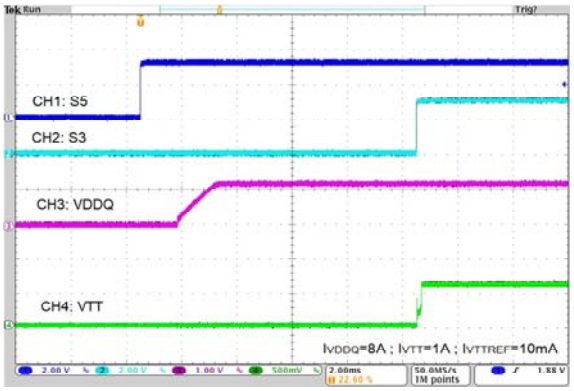
VTT Start-Up@S3, I_{VDDQ}=0A, I_{VTT}=0A, I_{VTTREF}=0A



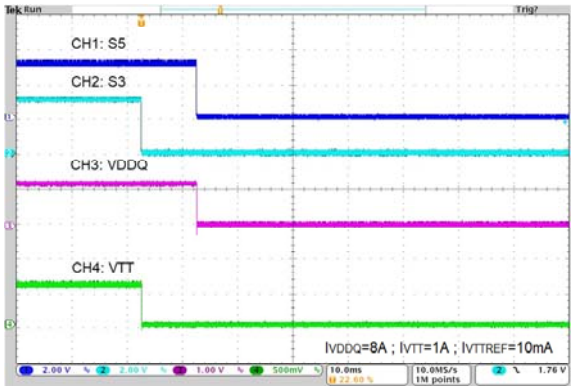
VTT Shutdown@S3, I_{VDDQ}=0A, I_{VTT}=0A, I_{VTTREF}=0A



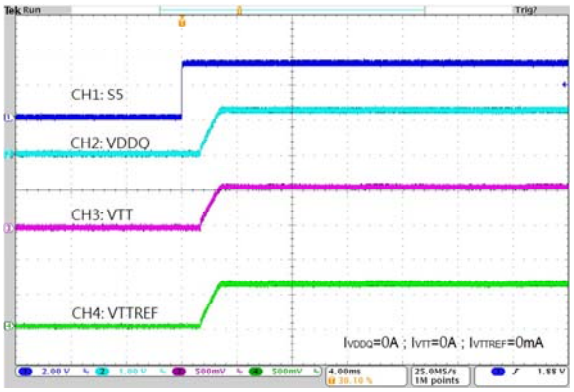
VTT Start-Up@S3, I_{VDDQ}=8A, I_{VTT}=1A, I_{VTTREF}=10mA



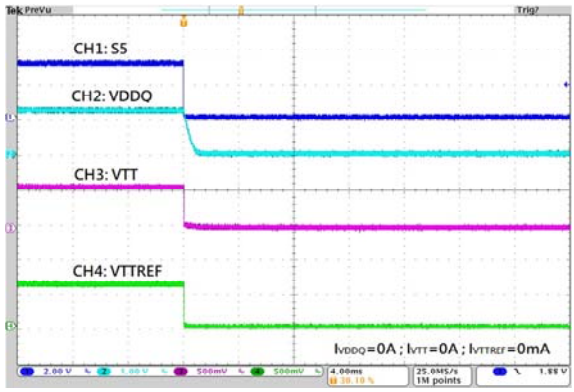
VTT Shutdown@S3, I_{VDDQ}=8A, I_{VTT}=1A, I_{VTTREF}=10mA



VTT Start-Up@S5, I_{VDDQ}=0A, I_{VTT}=0A, I_{VTTREF}=0A

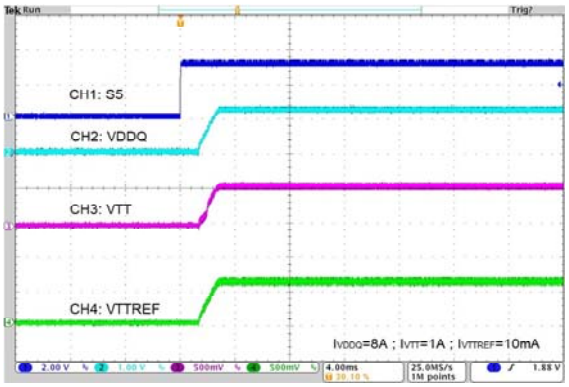


VTT Shutdown@S5, I_{VDDQ}=0A, I_{VTT}=0A, I_{VTTREF}=0A

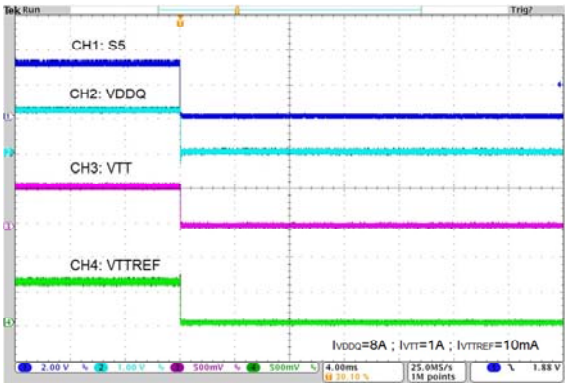


Typical Performance Characteristics (continued)

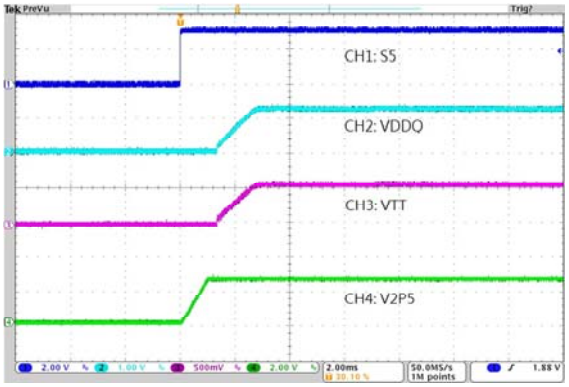
VTT Start-Up@S5, I_{VDDQ}=8A, I_{VTT}=1A, I_{VTTREF}=10mA



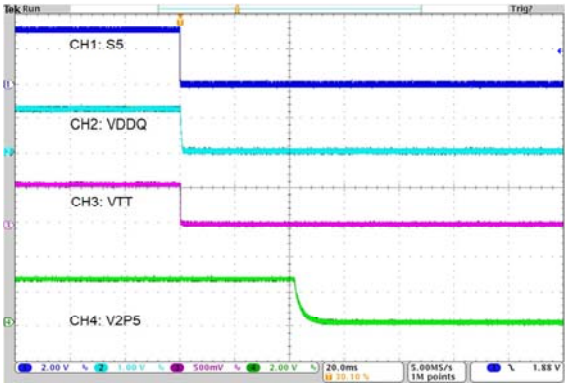
VTT Shutdown@S5, I_{VDDQ}=8A, I_{VTT}=1A, I_{VTTREF}=10mA



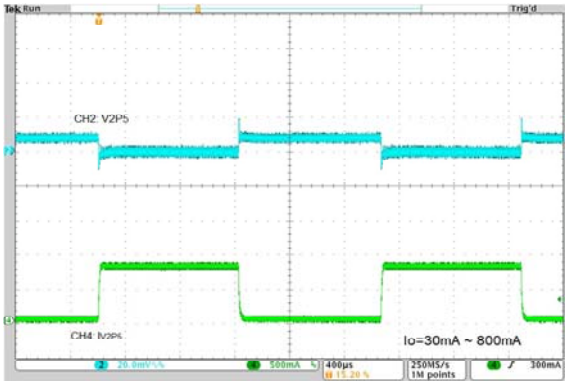
V2P5 Soft Start Time



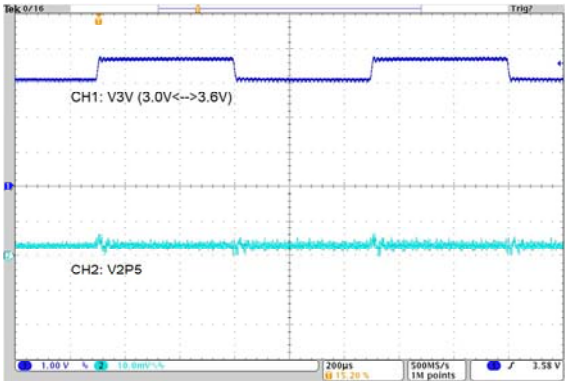
V2P5 Shutdown Delay Time



V2P5 Load Transient



V2P5 LineTransient



Pin Description

PIN	NAME	FUNCTION
1	VDDQSET	Feedback Input. Connect VDDQSET to a resistor divider from VDDQ for an adjustable output. VDDQ=0.75 × (1+ $\frac{R7}{R10}$).
2	V2P5	2.5V/1A LDO Output
3	V3V	3.3V Input Power of LDO
4	S3	Active Low Suspend to RAM Mode Control Pin, VTT is turned off and left Hi-Z
5	S5	Active Low Shutdown Pin. VTT and VTTREF are turned off and discharged to Ground.
6	PGOOD	Power-Good Open-Drain Output. PGOOD is low when the output voltage is more than 10% below the normal regulation point or during soft-start. PGOOD is high impedance when the output is in regulation and the soft-start circuit has terminated.
7	VCC	Supply Input. Connect to the system supply voltage, +4.5V to +5.5V. Bypass to GND with a 1μF (min) ceramic capacitor.
8	TON	Set ON-time through a pull-up resistor connecting to LX
9,10, 11,12,32	LX	External Inductor Connection. Connect LX to the switched side of the inductor. LX serves as the lower supply rail for the DH high-side gate driver. LX is also the positive input to the current-limit comparator.
13,14,15, 16,17,18	PGND	Power Ground for DL driver and low-side power MOSFET
19, 20, 21,22,31,	V+	Power Supply Input. Bypass to GND with a 10μF (min) capacitor
23	BST	Boost Flying-Capacitor Connection.
24	VLDOIN	Power Supply for the VTT and VTTREF output stage
25	VTT	Output Voltage for connection to termination resistors, equal to VDDQSNS/2
26	VTTGND	Power Ground output for the VTT output
27	VTTSNS	Voltage Sense Input for the VTT LDO
28	GND	Ground
29	VTTREF	Buffered Reference Output, equal to VDDQSNS/2
30	VDDQSNS	VDDQ sense input

Application Information

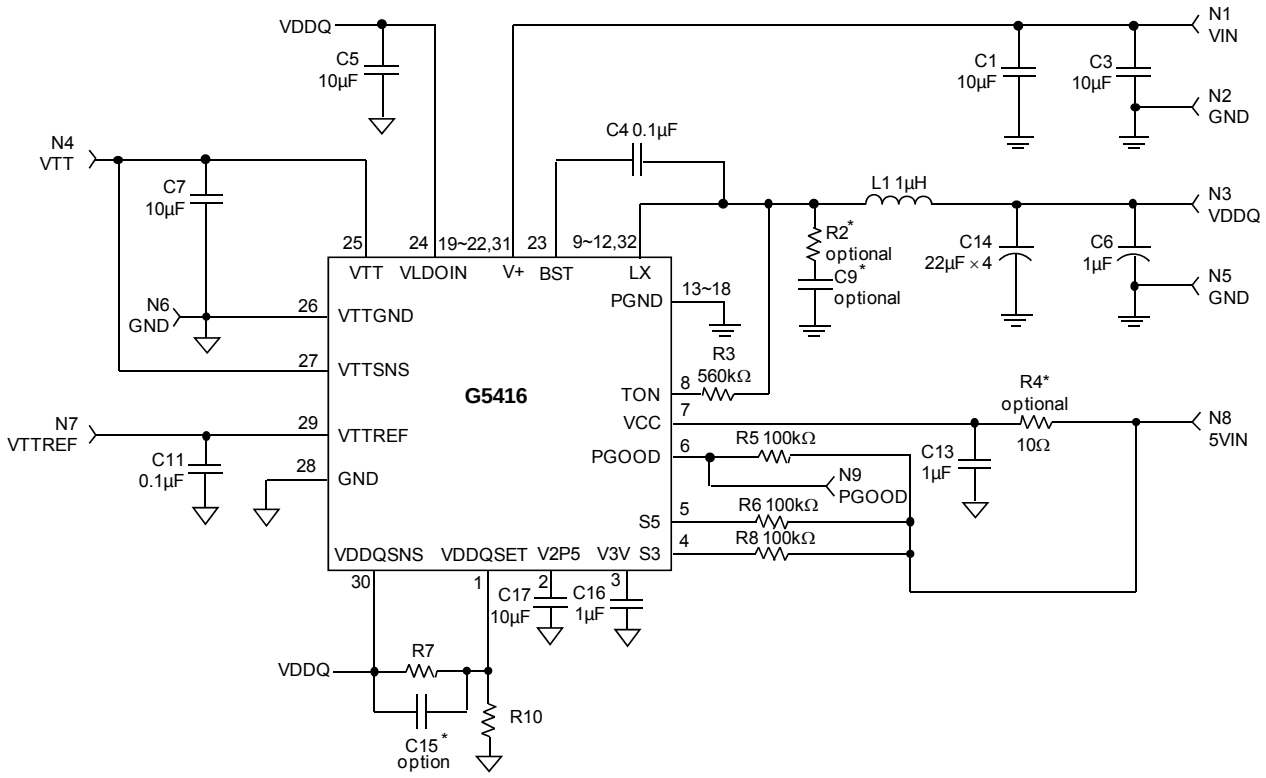


Table 1. Component Selection for Standard Application:

SYMBOL	SPECIFICATION	MANUFACTURER	PART NUMBER
U1	DC-DC regulator with DDR memory power supplies	GMT	G5416QS1U
C1,C3	10µF, 25V	TAIYO YUDEN	TMK316BJ106ML
C14,	22µF, 6.3V,		
L1	1µH, 2.5mΩ	SUMIDA	CDEP125
C5,C7	10µF, 6.3V	TAIYO YUDEN	JMK316BJ106KD

Block Diagram

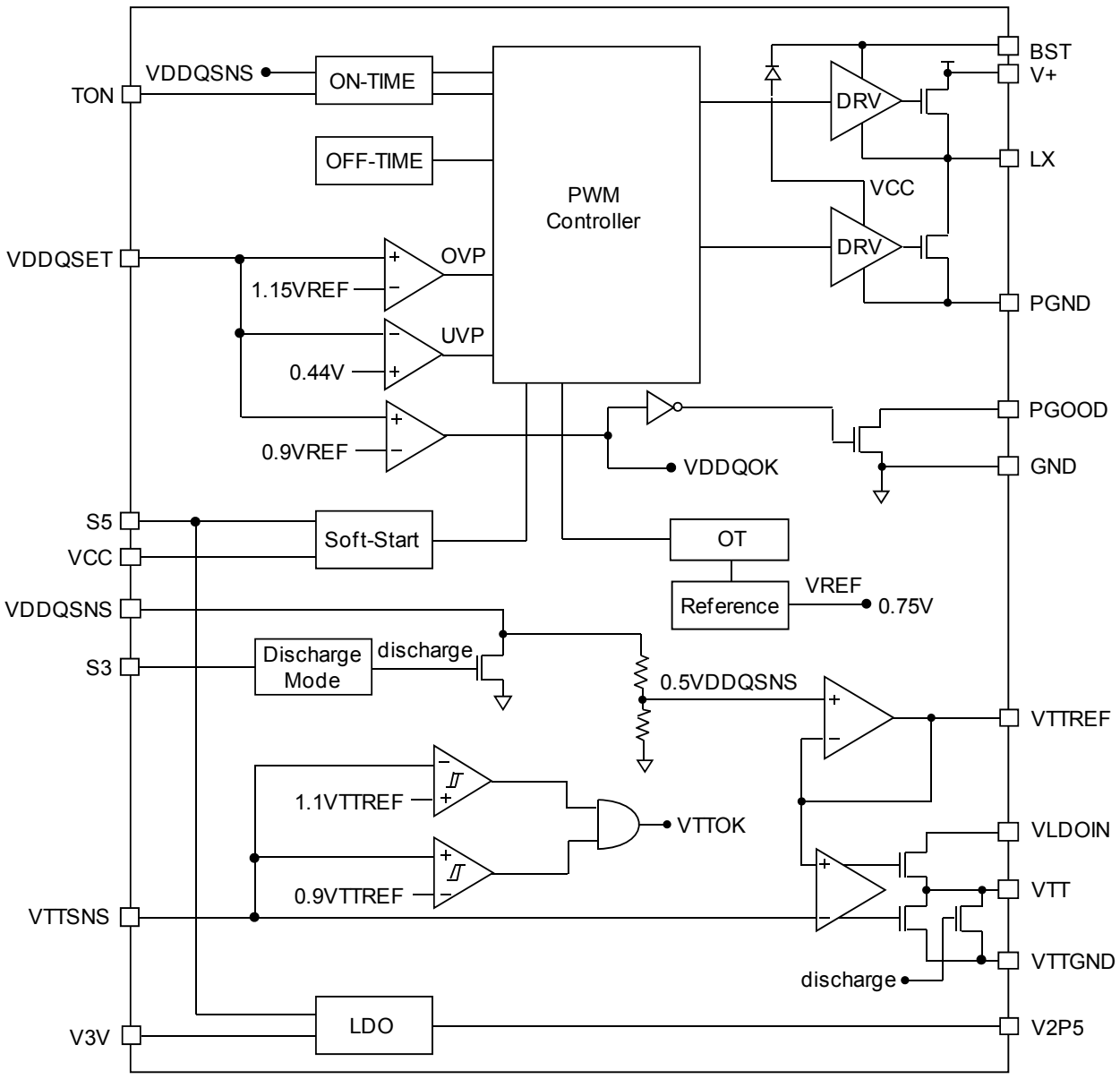


Figure 1 Block Diagram

Detailed Description

G5416 provides a step down converter and targeted to the low-voltage supply of notebook computers. A Quasi-PWM control is adapted in G5416. It is a constant-on-time PWM control with input feed-forward while maintaining a relatively constant switching frequency. It advantages in the fast load-transient response compared with conventional constant-on-time PWM control. Figure 1 shows the Block Diagram.

5V bias Supply (VCC)

G5416 required an external 5V bias supply for the PWM circuit, LDO, buffered reference and gate-drivers. In the notebook computer, there is a high efficiency 5V system supply and eliminate the cost of external LDO. If no 5V supply existed in the system, it can be generated 5V by LDO such like G920.

Constant-on-time PMW Control with Input Feed-Forward

The Quasi-PWM control algorithm can be described briefly: the high-side switch on-time is determined by a one-shot whose period is inversely proportional to input voltage and directly proportional to output voltage. Another on-shot determines the minimum off-time. The on-time one-shot can be triggered if the error comparator is low, the low side switch current is below the current-limit threshold, and the minimum off-time one-shot has timed out.

On-Time Selection

G5416 allows to program the on-time. The on time is determined as below

$$T_{ON} = \frac{R_{TON} \times V_{OUT}}{(V_{IN} - 0.9)} \times 2.05 \times 10^{-12} + 8.39 \times 10^{-8}$$

It results in a nearly constant switching frequency R_{TON} is a resistor connected from LX to the TON pin.

Current Limit

G5416 uses the on-state resistance of low side MOSFET as a current-sensing resistor. If the current -sense voltage (PGND-LX) is above the current-limit threshold, the PWM is not allowed to initiate a new cycle. The actual peak current is the current-limit threshold adding one inductor current ripple. So it depends on the on-resistance of low-side MOSFET, Inductor value, and battery voltage. No external current-sensing resistor is necessary in the output current path. The current limit threshold is set above 10.5A internally.

Gate Drivers

In the low duty factor application, like notebook computer, it exists large difference of input voltage and output voltage. Therefore, large low-side MOSFET and moderate-size high-side MOSFET are needed for high efficiency. The DH and DL drivers are optimized for driving high-side and low-side MOSFETs. A non-overlap control circuit is needed to avoid the DH and DL turning on simultaneously. The DL driver with a 0.5Ω pull low transistor helps prevent the DL from being coupled to high during the fast rising-time of the LX node, due to the drain to gate capacitive coupling of low-side synchronous-rectifier MOSFET. A resistor in series with the BST is recommended that will reduce the EMI-producing efficiency loss by increasing the turn-on time of the high-side MOSFET.

POR, UVLO, and Soft-Start of VDDQ

Power-on reset (POR) occurs when VCC rises above approximately 2V. It reset the fault latch and soft-start counter. When VCC is below 4.0V, undervoltage lockout (UVLO) inhibits switching and turns off the high-side, low-side MOSFETs.

Power-Good Indicator

The Output voltage is always monitored for undervoltage by the PGOOD comparator. The PGOOD is open-drain type signal. In shutdown and soft-start period, PGOOD is kept low. After the soft-start timer has timed out, the PGOOD is released if the output voltage is within 10% of normal value.

Fault Protection

G5416 provides undervoltage protection, overvoltage protection, and thermal protection.

The undervoltage protection (UVP) function is like foldback current limit function. If the output voltage is under 70% of normal value 2.3ms after shutdown released, the undervoltage protection function is activated. The PWM is latched off and would not restart until VCC power is cycled or enable signal is toggled.

The overvoltage protection (OVP) function activates when the output voltage is 17% above the set voltage. The high-side MOSFET turns off and the low-side MOSFET turns on. This rapidly discharges the output capacitor and decrease the output voltage. The PWM is latched off and would not restart until VCC power is cycled or enable signal is toggled.

The thermal protection (OT) function activates when die temperature exceeds the threshold value (typically: 147°C) the SMPS is shut down. This is non-latch protection.

VDDQ-Output Voltage Setting

Connect the VDDQSET pin to a resistor divider between VDDQSNS and GND to adjust the output voltage between 0.75V to 3.6V.

Chose R10=10kΩ and solve the R7 with the equation:

$$R7 = R10 \times \left(\frac{V_{VDDQ}}{V_{REF}} - 1 \right)$$

where V_{REF} = 0.75V

VTT SINK/SOURCE Regulator

The G5416 provides a 1.5A sink/source tracking termination regulator designed specially for low-cost, low external components system where space is at premium such as notebook PC applications. The G5416 integrates high performance low−dropout linear regulator (LDO) that is capable of sourcing and sinking current up to 1.5A. This VTT linear regulator is implemented with ultimately fast response feedback loop so that small ceramic capacitors are enough to keep tracking to the VTTREF within ±20mV at all conditions including fast load transient. To achieve tight regulation with minimum effect of trace resistance, a remote sensing terminal, VTTSNS, should be connected to the positive node of VTT output capacitor as a separate trace from the high current line from VTT.

VTTREF Regulator

The VTTREF block consists of an on-chip 1/2 divider, LPF and buffer. This regulator can source/sink current up to 10mA. Bypass VTTREF to GND using a 0.1µF ceramic capacitor to ensure stable operation.

Power on Sequence

To operate safely, the G5416 must keep VCC voltage higher than V3V, VLDOIN, VDDQSNS, S3 and S5 pins' voltage .This condition is due to the internal parasitic diodes between VCC to other pins by ESD issue. If the VCC voltage is lower than the other pins voltage, the G5416 will consume extra current through the parasitic diodes during the power-on period.

VTT Soft-Start

The soft-start function of the VTT is achieved via a current clamp, allowing the output capacitors to be charged with low and constant current that gives linear ramp up of the output voltage. The current limit threshold is changed in two stages using an internal VTTOK signal. When VTT is outside the VTTOK threshold, the current limit level is 1.5A. When VTT rises above (VTTREF - 10%) or falls below (VTTREF + 10%) the current limit level switches to 2.8A. The thresholds are typically VTTREF 10% (from outside regulation to inside) and 15% (when it falls outside). The soft-start function is completely symmetrical and it works not only from GND to VTTREF voltage, but also from VDDQSNS to VTTREF voltage. Note that the VTT output is in a high impedance state during the S3 state (S3 = low, S5 = high) and its voltage can be up to VDDQSNS voltage depending on the external condition. Note that VTT does not start under a full load condition.

S3, S5 Control and Soft-Off

The S3 and S5 terminals should be connected to SLP_S3 and SLP_S5 signals respectively. VDDQ, VTTREF and VTT are turned on at normal state (S3 = high, S5 = high). VDDQ, VTTREF are kept alive while VTT is turned off and left high impedance in standby state (S3 = low, S5 = high). VDDQ, VTT and VTTREF outputs are turned off and discharged to the ground through internal MOSFETs during shutdown state (S5 = low), the detail discharge function is described in Discharge Mode Selection section. The control function is showed on the Table 2.

Table 2. S3 and S5 Control Table

STATE	S3	S5	VTT	VTTREF
Normal	Hi	Hi	VTTREF	VDDQSNS/2
Standby	Lo	Hi	OFF (High-Z)	VDDQSNS/2
Shutdown	Lo	Lo	0V (Discharge)	0V (Discharge)

Discharge Mode

G5416 discharges VDDQ, VTTREF and VTT outputs during S3 and S5 are both low. G5416 is with non-tracking-discharge mode, and discharges outputs using internal MOSFETs which are connected to VDDQSNS and VTT. The current capability of these MOSFETs is limited to discharge slowly.

VTT Current Protection

The LDO has a constant overcurrent limit (OCL) at 2.8A. This trip point is reduced to 1.5A before the outputvoltage comes within 10% of the target voltage or goes outside of 15% of the target voltage.

V2P5 LDO

The LDO (V2P5) converts 3.3V input power to 2.5V output for DDR4 application. It has a current limit at 1.1A, and with 500mV dropout voltage in 800mA load condition. V2P5 is enabled by S5. It is keeping higher than VDDQ during turn-on and turn-off. The turn-on and turn-off sequence is shown as Figure 2. Keep the V3V pin floating if the LDO is not used.

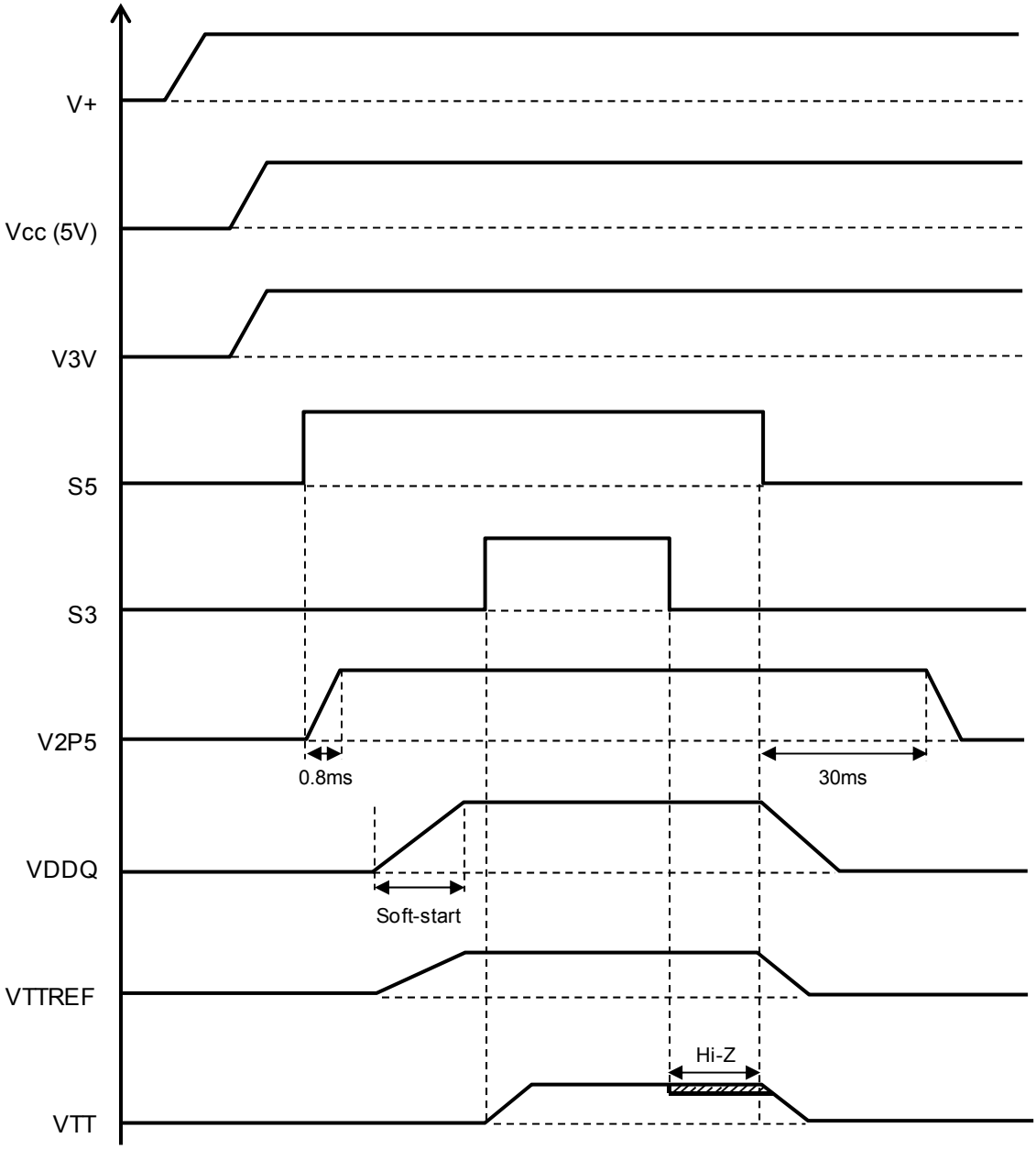
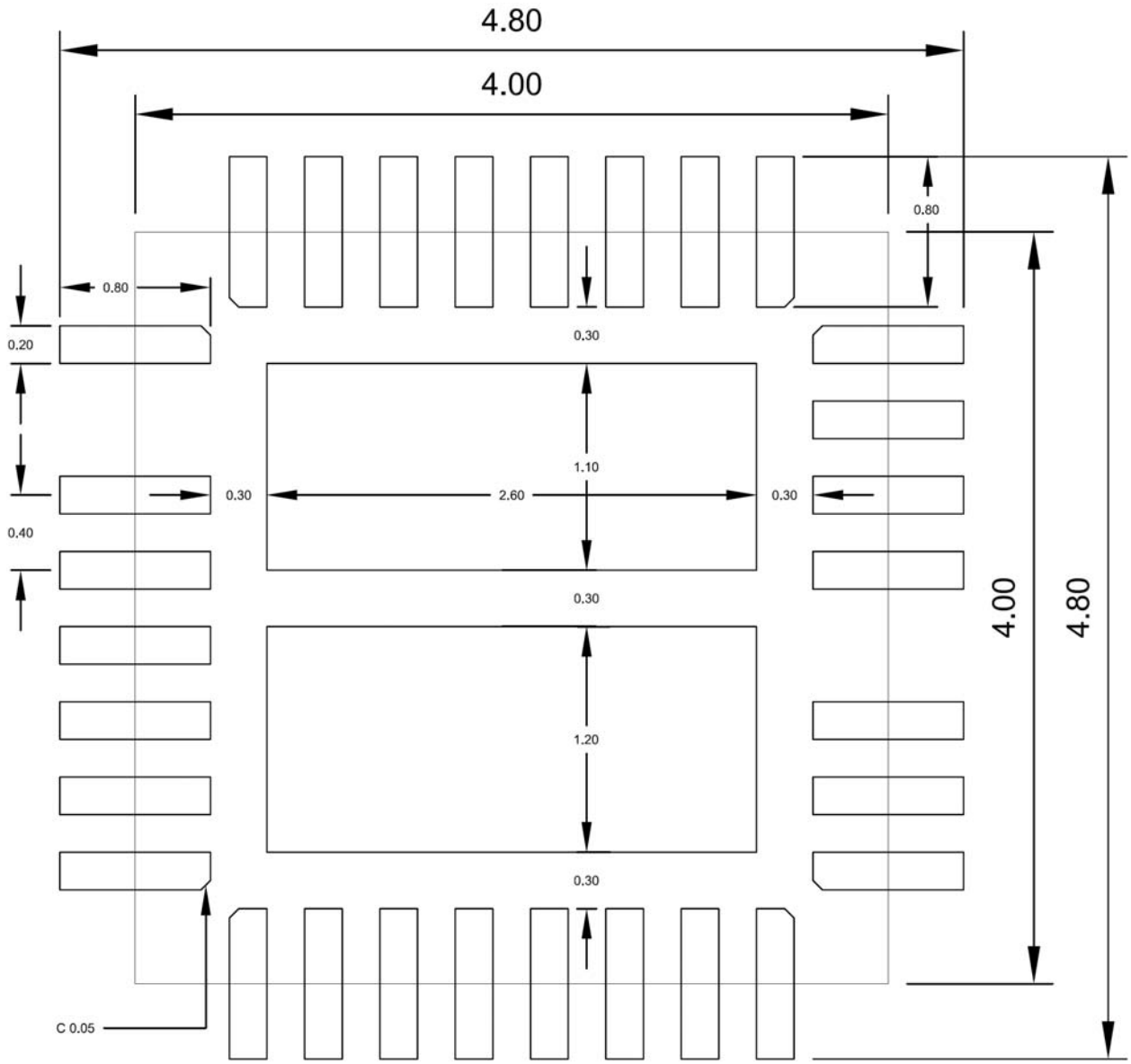


Figure 2. Power Sequence

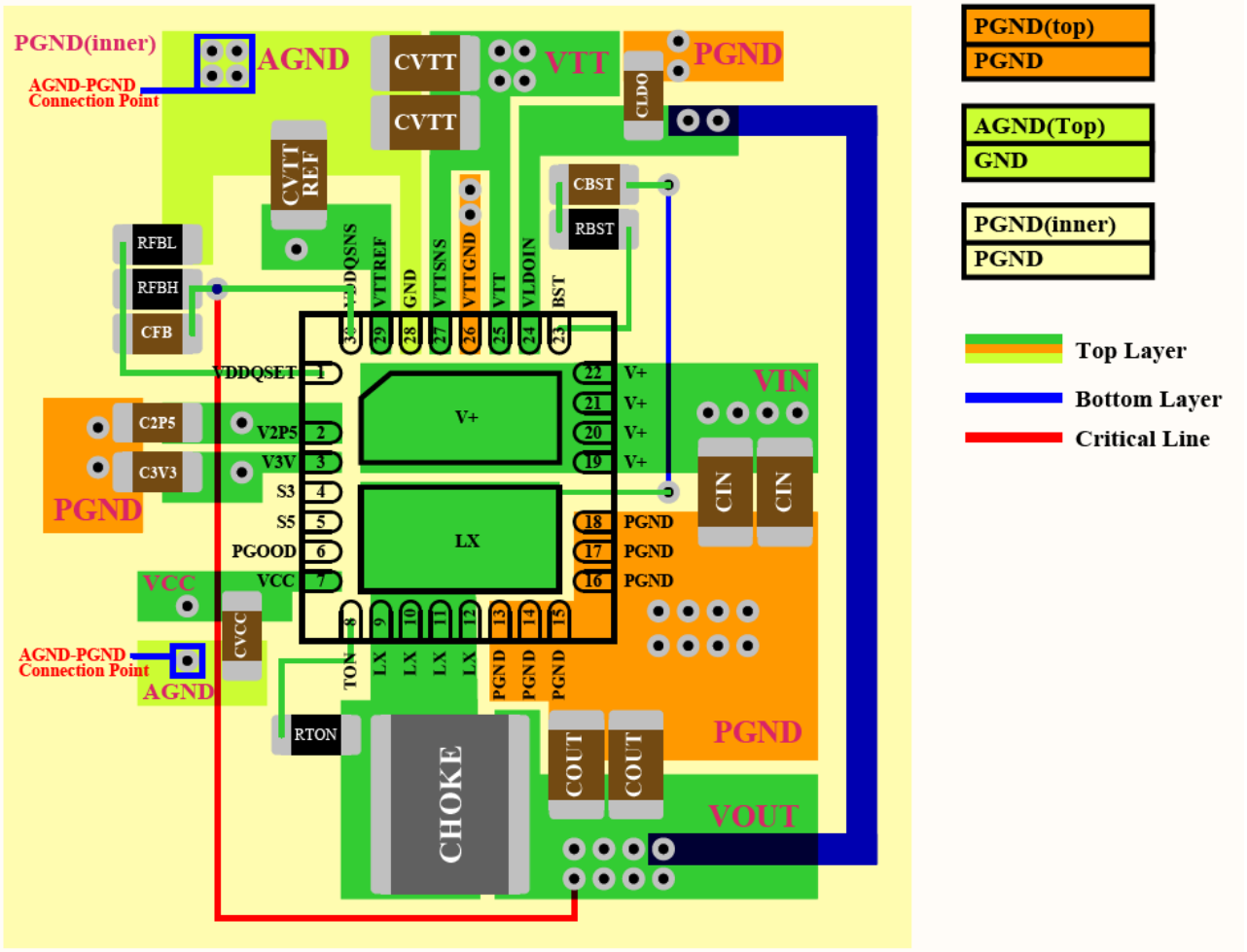
Minimum Footprint PCB Layout Section

QFN4X4-30

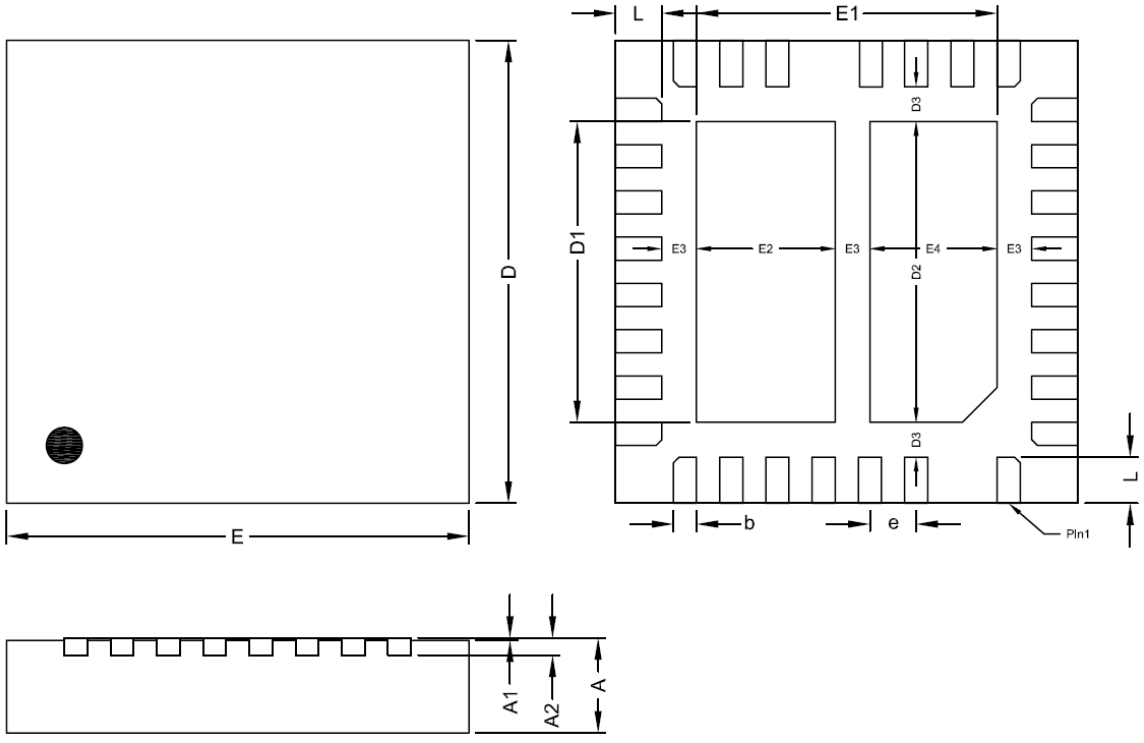


PCB Layout Guide

- Place the CIN as close to the V+ pin as possible.
- Keep the traces for the CIN, inductor and the COUT, short, direct and wide.
- Connect the GND and AGND at COUT capacitor.
- Keep the trace for the FB away from the switching high current paths.
- The VLDOIN input thermal need input Capacitor close the pin. The VOUT Connect to VLDOIN traces must wide and avoid switching paths interference.



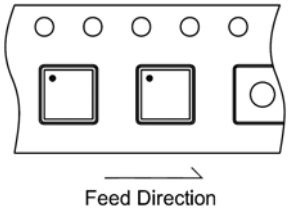
Package Information



QFN4X4-30 Package

Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.80	0.90	0.0276	0.0315	0.0354
A1	0.00	---	0.05	0.0000	---	0.0020
A2		0.20 REF			0.0079 REF	
D	3.95	4.00	4.05	0.1555	0.1575	0.1594
E	3.95	4.00	4.05	0.1555	0.1575	0.1594
D1	2.50	2.60	2.70	0.0984	0.1023	0.1063
E1	2.50	2.60	2.70	0.0984	0.1023	0.1063
D2	2.55	2.60	2.65	0.1004	0.1024	0.1043
E2	1.15	1.20	1.25	0.0453	0.0472	0.0492
D3		0.30 REF			0.0118 REF	
E3		0.30 REF			0.0118 REF	
E4	1.05	1.10	1.15	0.0413	0.0433	0.0453
b	0.15	0.20	0.25	0.0059	0.0079	0.0098
e		0.40 BSC			0.0157 BSC	
L	0.35	0.40	0.45	0.0138	0.0157	0.0177

Taping Specification



PACKAGE	Q'TY/BY REEL
QFN4X4-30	3,000 ea