High Efficiency, Quick Response, 8A Synchronous Step-down DC/DC

Features

- **5.5V ~ 23V Input Voltage Operation.**
- **Low Ron for internal switches (Top/Bottom MOS Ron):20/10mΩ**
- **5V LDO output supply 100mA**
- **Integrated bypass switch: 1.5Ω**
- **Internal 0.6ms soft-start**
- **8.0A output current capability**
- **Quick Response constant-on-time architecture to achieve fast response**
- **750kHz switching Frequency**
- **+/-1% feedback reference voltage**
- **Power good indicator**
- **Output Over-/Under-voltage Protection.**
- **Over-Current Protection**
- **Ultrasonic Mode**
- **AQFN3X3-12 FC Package**

General Description

The G5425 provides a high Efficiency synchronous buck converter with fixed 5V output voltage and capable of delivering 8A. The device supports a wide range input voltage from 5.5V to 23V. G5425 adopts quick response COT architecture to achieve fast transient response.

G5425 integrates a 100mA LDO and switch over for efficiency improving.

G5425 features enable control, under/over voltage protect, short circuit protect, valley current limit, thermal shutdown.

G5425 provides compact solution for TCON power system. It is available in a AQFN3X3-12 FC package.

Applications

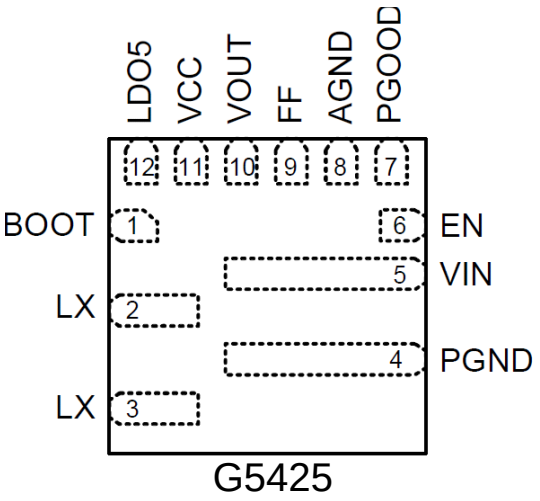
- **Notebook Computers**
- **Notebook, Tablet Computers**

Ordering Information

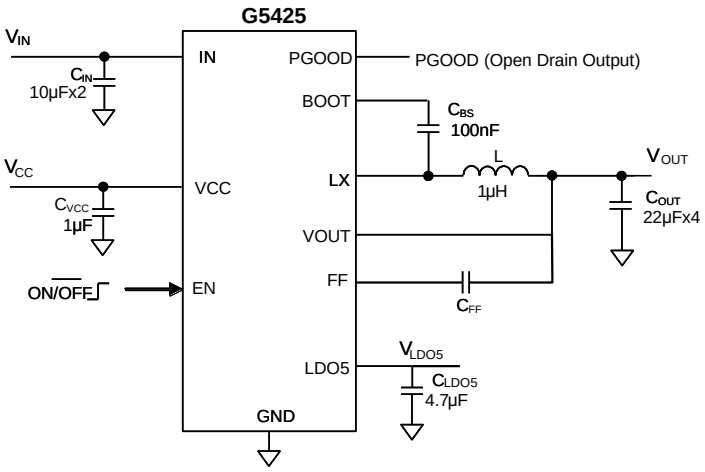
ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE (Green)
G5425M11U	5425	-40°C~+85°C	AQFN3X3-12 FC

Note: M1: AQFN3X3-12 FC
1: Bonding code
U: Tape & Reel
Green: Lead free/ Halogen Free

Pin Configuration



Typical Application Circuit



Absolute Maximum Ratings

VIN, EN to AGND . . . . . .-0.3V to +27V
LX to PGND. . . . . -0.3V to +27V
<20ns. . . . . -6V to +32V
BOOT to LX. . . . . -0.3V to +5V
LDO5, VOUT to AGND . . . . . .-0.3V to +6.3V
All other pins to AGND . . . . . -0.3V to +6.3V
Operating Ambient Temperature. . . . . -40°C to +85°C
Storage Temperature range . . . . . .-55°C to +150°C
Reflow Temperature (Soldering, 10sec) . . . . . .260°C
ESD Susceptibility (HBM). 2kV
ESD Susceptibility (MM). 200V

Recommended Operation Conditions

IN . . . . . 4.5V to +23V
Operating Ambient Temperature. . . . . .-40°C to 85°C
Operating Junction Temperature. . . . . +150°C

1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Device is ESD sensitive. Handling precaution recommended. The Human Body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.

Thermal Information

THERMAL METRIC		AQFN3X3-12	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance	72.6	°C/W
$R_{\theta JC\_top}$	Junction to case top thermal resistance	17.5	°C/W
$R_{\theta JB}$	Junction to board thermal resistance	15.1	°C/W
Ψ_{JT}	Junction to top characterization parameter	0.5	°C/W
Ψ_{JB}	Junction to board characterization parameter	15.3	°C/W
$R_{\theta JC\_bot}$	Junction to case bottom thermal resistance	N/A	°C/W

1. Package thermal metric is obtained using the method described in JEDEC specification JESD51-7, using a four-layer board.
2. The maximum power dissipation is $P_{D(MAX)} = \frac{(T_{JMAX} - T_A)}{R_{\theta JA}}$, Exceeding the maximum allowable power dissipation results in excessive die temperature, and the device will enter thermal shutdown.

Electrical characteristics

(VIN=12V, T_A=25°C.)

The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified.

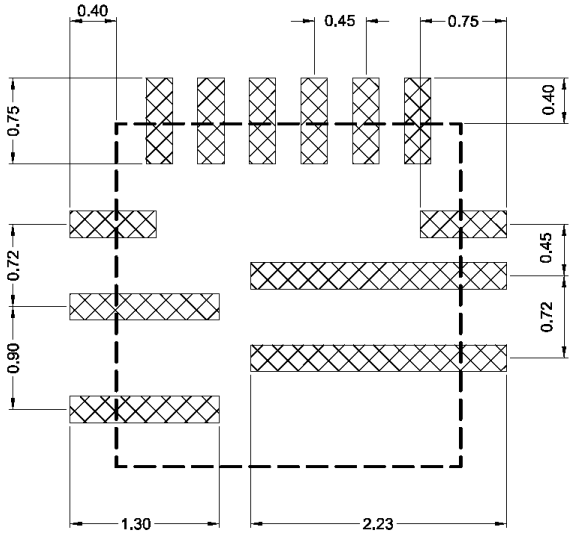
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
VIN Operation Range	V_{IN}		5.5	---	23	V
VIN Under Voltage Lockout Threshold	V_{UVLO}	VIN rising	---	---	5.4	V
VIN Under Voltage Lockout Hysteresis	ΔV_{UVLO}		---	300	---	mV
VIN Quiescent current	I_Q	I_{OUT}=0,V_{OUT}=105%,V_{EN}=2V	---	100	130	μA
VIN Shutdown current	I_{SD}	EN=0	---	50	60	μA
Output Set Voltage	V_{REF}		5.049	5.1	5.151	V
Top MOS R_{ON}	R_{DSUP}		---	20	---	mΩ
Bottom MOS R_{ON}	R_{DSDN}		---	10	---	mΩ
Current Limit	I_{LIM}		9	---	---	A
Discharge MOS R_{ON}	R_{DIS}		---	50	---	Ω
Operating Frequency	f_{SW}		---	0.75	---	MHz
Minimum On Time	T_{ON_MIN}		---	60	---	ns
Minimum Off Time	T_{OFF_MIN}		---	200	---	ns
Soft-start Time	T_{SS}	From EN high to PGOOD high	1.3	1.65	2	ms
Output Rising time	T_r	From 10% to 90% V_{out}	---	0.6	---	ms
Power Good Threshold	V_{PG}	V_{FB} falling, PG from high to low	---	85	---	%V_{REF}
		V_{FB} rising, PG from low to high	---	90	---	%V_{REF}
Power Good Delay Time	T_{PG_F}	Low to high	---	250	---	μs
	T_{PG_R}	High to low	---	10	---	μs
Output OVP Threshold	V_{OVP}		115	120	125	%V_{REF}
Output OVP Hysteresis			---	3	---	%V_{REF}
Output OVP Response Time	T_{OVP}		---	20	---	μs
Output UVP Threshold	V_{UVP}		---	60	---	%V_{REF}
Output UVP Response Time	T_{UVP}		---	20	---	μs
UV Blank time	T_{UVBLK}		---	1.65	---	ms
VCC Regulator Voltage	V_{CC}		3.235	3.3	3.366	V
LDO Output Voltage	V_{LDO}	VIN=12V, No Load	4.925	5	5.075	V
LDO Dropout Voltage	$V_{DROPOUT}$	I_{LDO}=100mA	---	200	---	mV
LDO Output Current Limit	I_{LMTLDO}		150	---	300	mA
Bypass Switch RON	R_{BYP}		---	1.5	---	Ω

Electrical Characteristics (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Bypass Switch Turn-on Voltage	V_{BYP}		4.5	4.7	---	V
Bypass Switch Switchover Hysteresis	$V_{BYP,HYS}$		---	0.2	---	V
Bypass Switch OVP			---	120	---	$\%V_{LDO}$
Enable Logic High Threshold	V_{EN_HIGH}		---	---	0.8	V
Enable Logic Low Threshold	V_{EN_LOW}		0.4	---	---	V
Ultrasonic mode Threshold voltage	V_{EN_USM}		---	---	1.7	V
Normal Mode	V_{EN_NOR}		2.3	---	---	V
Thermal Shutdown Temperature	T_{SD}		---	150	---	°C
Thermal Shutdown Hysteresis	T_{HYS}		---	20	---	°C

Minimum Footprint PCB Layout Section

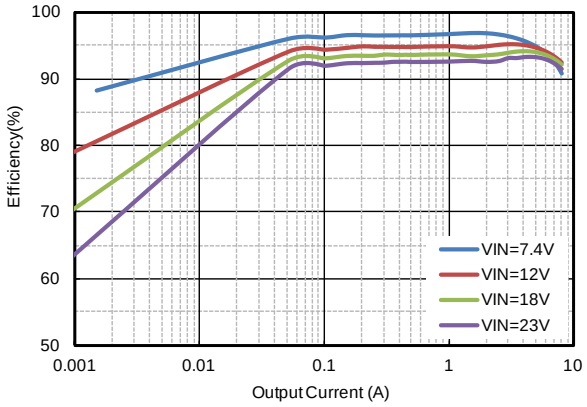
AQFN3X3-12



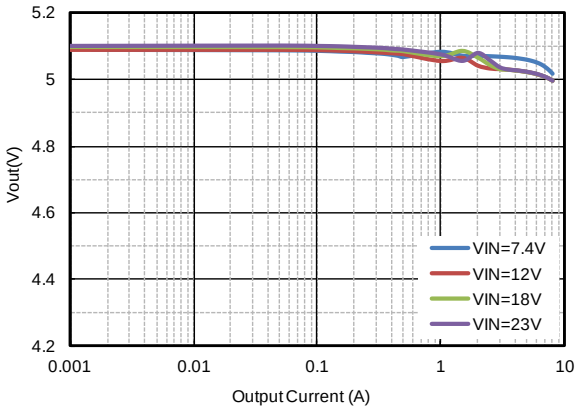
Typical Performance Characteristics

V_{IN}=12V, T_A =25°C.

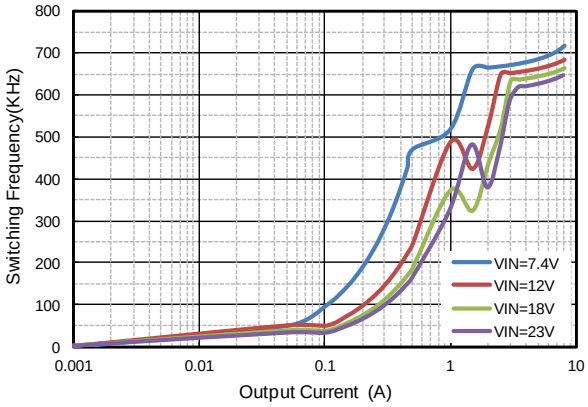
Output Current vs. Efficiency



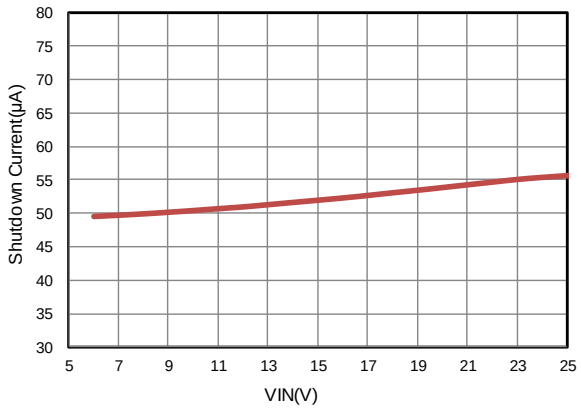
Output Current vs. VOUT



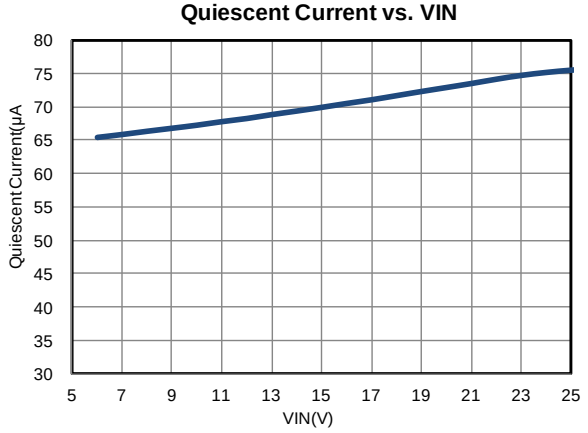
Outout Curren vs. Frequency



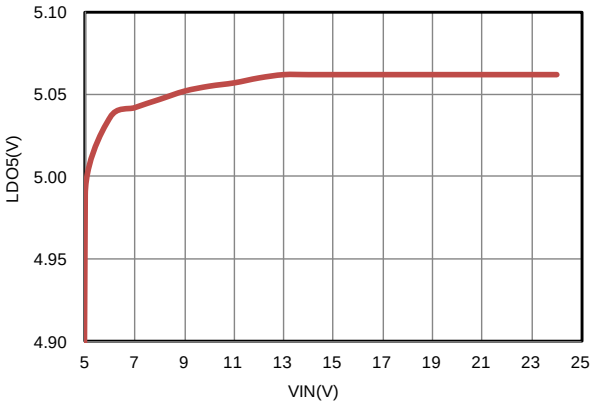
Shutdown Current vs. VIN



Quiescent Current vs. VIN

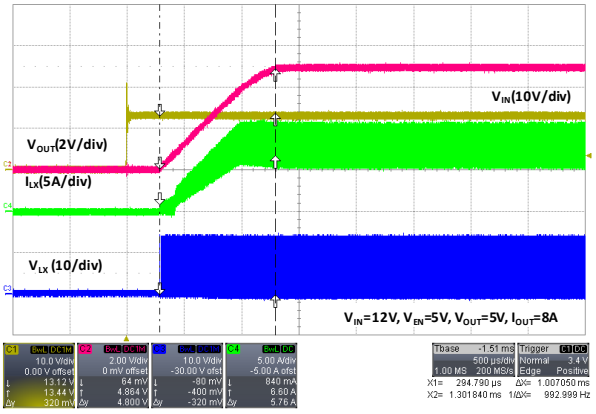


VLOD5 vs. VIN

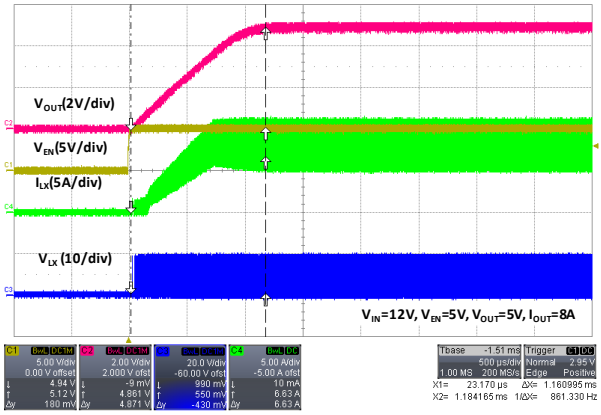


Typical Performance Characteristics (Continued)

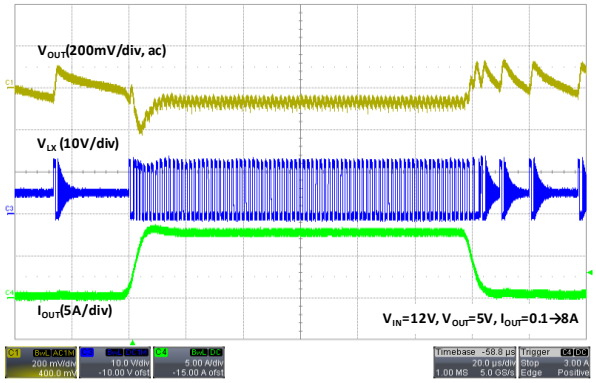
Power On form VIN



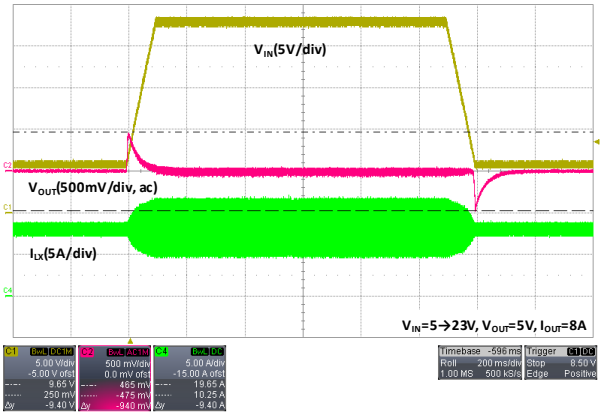
Power On form EN



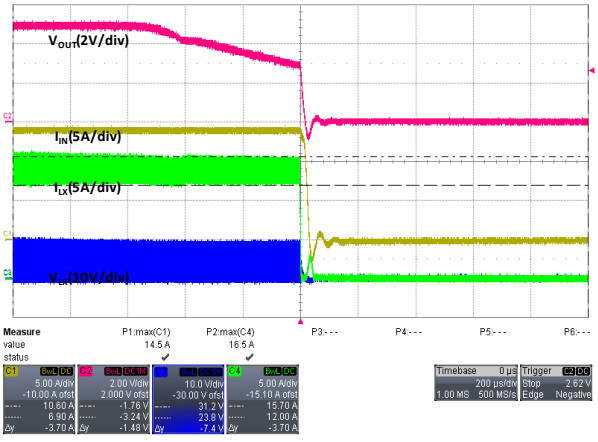
Load Transient Response



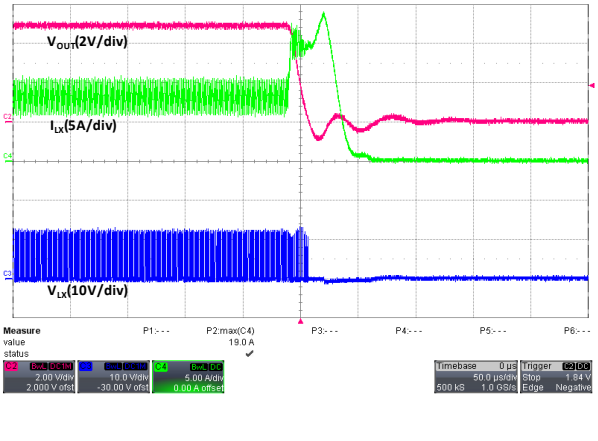
Line Transient Response



Over Current Limit



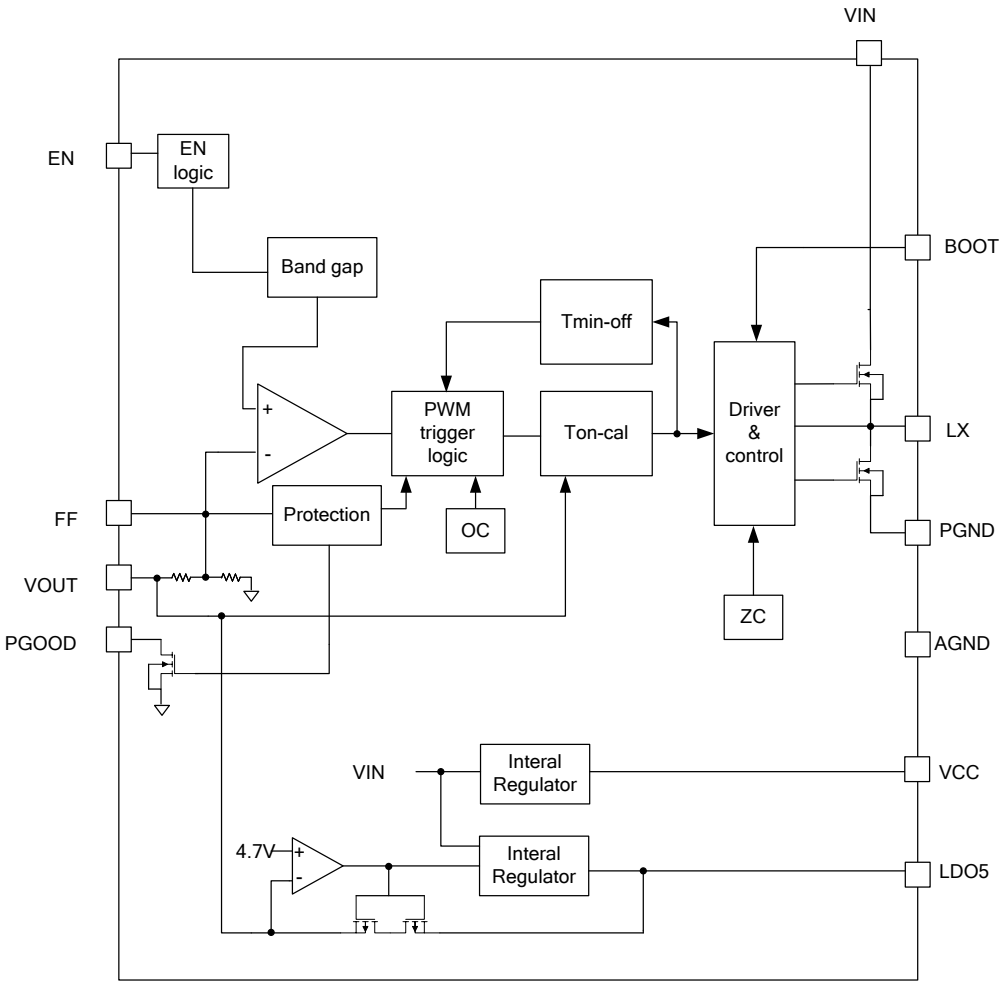
Output Short Circuit



Pin Description

Pin	Name	Function
1	BOOT	Boot-strap pin. Decouple this pin to LX with a 100nF capacitor
2,3	LX	Inductor pin. Connect this pin to the switching node of inductor.
4	PGND	Power ground.
5	VIN	Power supply input. Decouple this pin to GND with at least 10µF
6	EN	Enable control. Pull this pin high to turn on the buck converter. Set voltage between 0.8V and 1.7V will enter USM mode. If voltage above 2.3V, then it is normal mode. Do not leave this pin floating.
7	PGOOD	Open drain power good indicator. Externally pull high when the output voltage is in regulation range. Otherwise pull low
8	AGND	Analog ground.
9	FF	Output feed forward pin. Connect RC network from the output to this pin.
10	VOUT	Output pin. Connect to the output of DC-DC regulator. The pin also provide the bypass input for internal LDO
11	VCC	3.3V linear regulator output for internal control circuit. A capacitor (typical 1µF) should be connected to AGND. Do not connect this pin to external load.
12	LDO5	5V LDO output. Decouple this pin to ground with at least 4.7µF capacitor

Block Diagram



Function Description

The G5425 is high-performance 8A synchronous step-down regulators. The device integrates main switch and synchronous switch with low $R_{DS(on)}$ to enhance efficiency. The input range is from 5.5V to 23V and the output voltage is fixed at 5.1V.

The G5425 includes a 5V linear regulator (LDO) with bypass switch, when VOUT rises above 4.7V, the power path of LDO will change from VIN to VOUT, and therefore the power dissipation of LDO will be much reduced.

Enable and Disable operation

The G5425's EN pin is used to control converter, When V_{EN} is below the logic low level which is 0.4V, the IC enters shutdown mode. When V_{EN} is between 0.8V to 1.7V, the IC enters ultrasonic mode. When V_{EN} is above 2.3V, the IC enters normal mode.

Soft-start

The G5425 has a built-in soft-start to control the rise time of the output voltage and limit the inrush current during start-up period. Typical soft-start time is 0.6mS.

Ultrasonic mode

When a lightly load is applied, the controller skips the pulses automatically, the switching period may be very long. In ultrasonic mode, controller will limit the switching period smaller then 30uS to eliminate audio frequency modulation.

Current limit

The G5425 current limit is fixed 9A and it is a cycle-by-cycle valley type. It measures the inductor current through low-side MOSFET during off-time period. Once current is larger than the current limit, the next on-time is blocked until the inductor current falls below the threshold. When current limit occurs, the output voltage will drop, if output voltage triggers under -voltage protection, the IC will stop switching to avoid damage.

Output Over-voltage and under-voltage protection

The G5425 includes OVP and UVP function. If the output voltage rises above the regulation level, the high-side switch will keep off and the low-side switch will turn on until the inductor current reaches to zero or next on-time is triggered. If the output voltage exceeds the OVP threshold for longer than 20uS, the OVP will triggered. If the output voltage drops below the UVP threshold for longer than 20uS, the UVP will triggered. Both protections are latch-off type; the IC will shut down until re-toggle EN pin or power the IC off and on again.

Output Temperature Protection

If the device temperature exceeds the OTP threshold, typically 150°C, the IC will shutdown. The OTP is also latch-off type.

Linear Regulators (LDO5&VCC)

The G5425 includes a 5V linear regulator which can supply up to 100mA for external load, it's recommended to connect LDO5 pin to GND with a 4.7uF ceramic capacitor. When VOUT rises above 4.7V, the power path of LDO will change from VIN to VOUT, and therefore the power dissipation of LDO will be much reduced.
The G5425 also includes a 3.3V linear regulator to supply internal circuitry, do not connect VCC pin to external loads.

Power Good Output (PGOOD)

PGOOD is an open-drain output pin. This pin will pull to ground if the output voltage is lower than 90% of regulation voltage and during soft-start state. Otherwise this pin will go to a high impedance state.

Input Capacitor Selection

To minimize the potential noise problem, place a typical X5R or better grade ceramic capacitor really close to the VIN and GND pins with values greater then 20uF are recommended.

Output Capacitor Selection

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration. For most applications, the capacitance greater then 66uF can work well.

Inductor Selection

The inductor value is determined as follows:

$$L = \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN} \times f \times \Delta I_{LPP}}$$

Where ΔI_{LPP} is defined as inductor ripple current.

The inductor ripple current also impacts transient-response performance, especially at low conversion ratio condition. Low inductor values allow the inductor current to slew faster, replenishing charge removed from the output filter capacitors by a sudden load step.
Maintaining the ratio of the inductor ripple current to the designed maximum load current within a 20% to 50% range is prudent.

External Bootstrap Capacitor

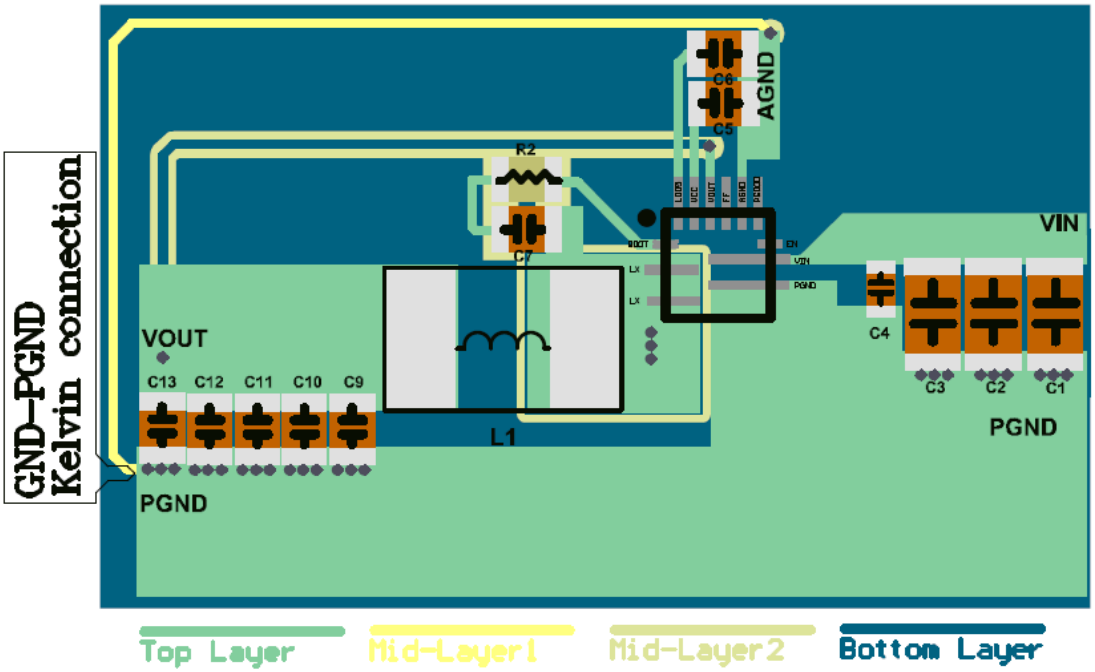
This capacitor provides the gate driver voltage of high side MOSFET. Place a 100nF low ESR ceramic capacitor between BS and LX pin.

PCB Layout Considerations

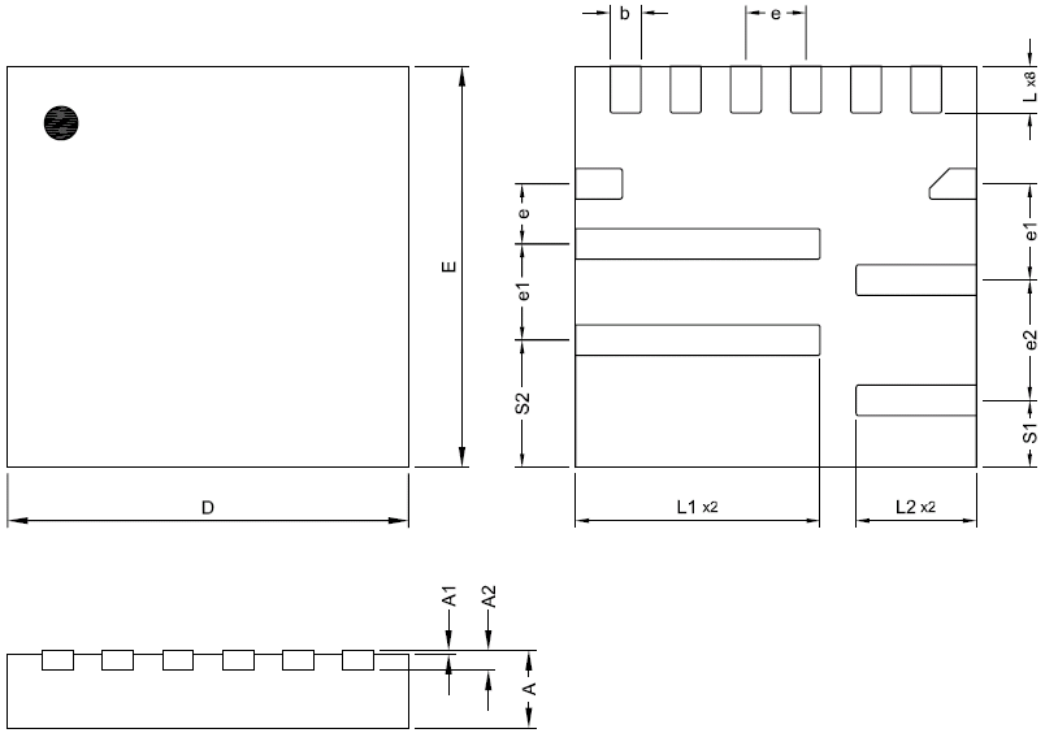
Layout is a critical portion of good power supply design. There are several signal paths that conduct fast change currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance.

1. The input capacitor must be placed as close to the IC as possible.
2. Connect AGND (Pin8) to ground of bypass LDO5 and VCC paths.
3. Connect AGND and PGND together close to the IC and the negative terminal of COUT.
4. Compensation components must be connected as close to the IC as possible.
5. Connect PGND of CIN, and COUT to system ground by a plane.
6. LX should be connected to inductor by wide and short trace. Keep sensitive components away from this trace.
7. All sensitive analog traces such as OUT should be placed away from high-voltage switching node such as LX, BST nodes to avoid coupling.

Recommended PCB Layout



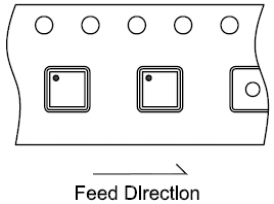
Package Information



AQFN3X3-12 Package

Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.50	0.55	0.60	0.0197	0.0217	0.0236
A1	0.00	---	0.05	0.0000	---	0.0020
A2		0.150 REF			0.0059 REF	
D	2.95	3.00	3.05	0.1161	0.1181	0.1201
E	2.95	3.00	3.05	0.1161	0.1181	0.1201
b	0.18	0.23	0.28	0.0071	0.0091	0.0110
e		0.45 BSC			0.0177 BSC	
e1		0.72 BSC			0.0283 BSC	
e2		0.90 BSC			0.0354 BSC	
L	0.25	0.35	0.45	0.0098	0.0138	0.0177
L1	1.73	1.83	1.93	0.0681	0.0720	0.0760
L2	0.80	0.90	1.00	0.0315	0.0354	0.0394
S1	0.40	0.50	0.60	0.0159	0.0197	0.0236
S2	0.85	0.95	1.05	0.0335	0.0374	0.0413

Taping Specification



PACKAGE	Q'TY/REEL
AQFN3X3-12	3,000 ea