G5851

Mobile Phone Power Management System

Features

- **2.8V ~ 5.5V Input Voltage Operation.**
- **95% Efficient DC/DC Converter**
- **Built-in 4-ch synchronous buck converter, 7-ch LDOs, and 1-ch low quiescent current LDO for RTC.**
- **Bucks and LDOs can be set to lower Iq at low load.**
- **Low Power consumption (Sleep Mode) < 20μA.**
- **Buck1 and Buck2 Supports DVS Function, 25mV/step.**
- **Built-In Power ON/OFF Sequence for PMU.**
- **Built-In Short Circuit Protection (SCP), Under Voltage Protection (UVP), and cycle-by cycle current limit for DC/DC Converters.**
- **7-channel LDOs are Programmable to Voltage Options by I^2C.**
- **Real Time Clock**
- **SIM Card I/F Level Shifter**
- **Built-In Thermal Shutdown Function.**
- **Built-In VCC OVP Function.**
- **Built-In Power Key Function.**
- **WLCSP7X7-49 Package (0.4mm pitch).**

General Description

The G5851 provide a complete power supply solution for handsets or data card. It contains 4 dc/dc converters and 7 LDOs to power each critical blocks of mobile phone, and is optimized for maximum battery life, featuring a low ground current when in standby mode operation. All channels DC/DC converters operate at one fixed frequency of 3.0MHz to optimize size, cost, and efficiency. All Synchronous converters operate at pulse skipping mode at light load. The G5851 features a I^2C compatible interface.

The G5851 is available in WLCSP package.

Applications

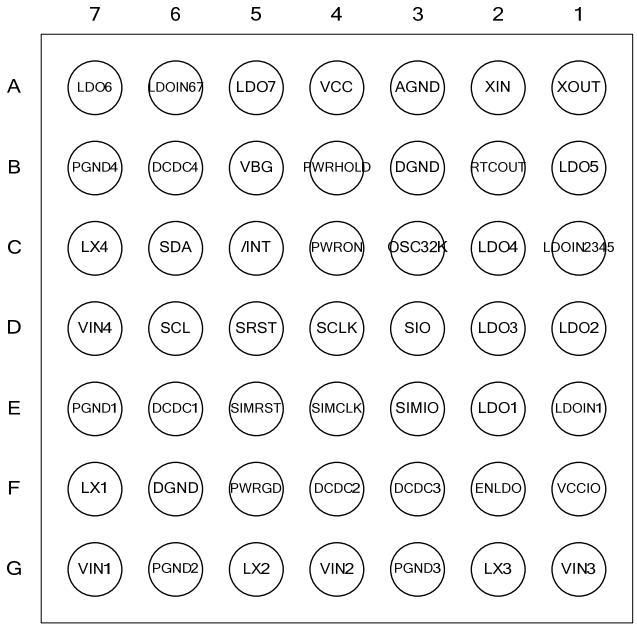
- **Mobile Handsets**
- **Smart Phone**

Ordering Information

ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE (Green)
G5851B81U	5851	-40°C~+85°C	WLCSP7X7-49

Note: B8:WLCSP7x7-49
1: Bonding code
U: Tape & Reel
Green : Lead Free / Halogen Free.

Pin Configuration



Bottom View
WLCSP 7X7-49

Absolute Maximum Ratings

VCC, VIN1, VIN2, VIN3, VIN4, LDOIN1, LDOIN2345, LDOIN67, VCC_IO . . . . . -0.3V to +6.3V
DCDC1, DCDC2, DCDC3, DCDC4, LDO1, LDO2, LDO3, LDO4, LDO5, LDO6, LDO7, RTCOUT . . . . . -0.3V to +6.3V
LX1, LX2, LX3, LX4 . . . . . -0.3V to +6.3V
SCL, SDA, ENLDO, PWRON, PWRHOLD, VBG, /INT, PWRGD . . . . . .-0.3V to +6.3V
SCLK, SRST, SIO . . . . . .-0.3V to (LDO1+0.3)V
SIMCLK, SIMRST, SIMIO . . .-0.3V to (VCC_IO+0.3)V
OSC_32K . . . . . .-0.3V to (DCDC4+0.3)V

Thermal Resistance Junction to Ambient, (θ_{JA})
WLCSP7X7-49 . . . . . .27.7°C/W
Continuous Power Dissipation (T_A=25°C)
WLCSP7X7-49. . . . . 5.38W
Operating Ambient Temperature .-35°C to 85°C
Storage Temperature Range. . . . . -55°C to +150°C
Reflow Temperature (soldering, 10 sec) . . . . . 260°C
ESD-HBM. 2kV
ESD-MM. 200V

1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Device are ESD sensitive. Handling precaution recommended. The Human Body model is a 100pF capacitor discharged through a 1.5KΩ resistor into each pin.

Electrical characteristics

(VCC=VIN1=VIN2=VIN3=VIN4=3.7V, LDOINx=3.7V, T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
GENERAL						
VCC minimum Startup Voltage	V_{VCC_ST}		---	---	2.6	V
VCC Operating Voltage for PMU	V_{VCC_PMU}		2.8	---	5.5	V
VCC Over Voltage threshold	V_{VCC_OVLO}		5.8	6.0	---	V
PMU Stand-by Supply Current	I_{VCC}	ALL converters enter ECO mode, and without loading current.	---	160	250	uA
PMU Shutdown Current	I_{PMU_SD}	PMU shutdown	---	20	---	µA
OSCILLATOR						
Frequency	F_{OSC}	DCDC1~DCDC4	2.6	3.0	3.4	MHz
DCDC1 Buck Converter						
Soft-Start Internal	SS_CH1		---	2	---	mS
VO1 regulation voltage accuracy	%VO1		-1.5	---	1.5	%
Maximum Duty Cycle	D_{max1}		---	100	---	%
VIN1 Leakage Current	I_{VIN1_LK}	V_{LX1}=0V, VIN1=5.0V	---	1	5	µA
LX1 Leakage Current	I_{LX1_LK}	V_{LX1}=5.0V	---	1	5	µA
Switch ON Resistance	Ron1-N		---	120	---	mΩ
	Ron1-P		---	150	---	
Peak Current Limit	I_{LIM_CH1}		---	2.5	---	A
Under Voltage Protection Threshold	ΔV_{UVP_CH1}	ΔV_{UVP_CH1}=$VOUT_{SET}$-$VOUT_{UVP}$	---	100	---	mV
DCDC2 Buck Converter						
Soft-Start Internal	SS_CH2		---	2	---	mS
VO2 regulation voltage accuracy	%VO2		-1.5	---	1.5	%
Maximum Duty Cycle	D_{max2}		---	100	---	%
VIN2 Leakage Current	I_{VIN2_LK}	V_{LX2}=0V, VIN2=5.0V	---	1	5	µA
LX2 Leakage Current	I_{LX1_LK}	V_{LX2}=5.0V	---	1	5	µA
Switch ON Resistance	Ron2-N		---	120	---	mΩ
	Ron2-P		---	150	---	
Peak Current Limit	I_{LIM_CH2}		---	2.5	---	A
Under Voltage Protection Threshold	ΔV_{UVP_CH2}	ΔV_{UVP_CH2}=$VOUT_{SET}$-$VOUT_{UVP}$	---	100	---	mV

Electrical characteristics (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
DCDC3 Buck Converter						
Soft-Start Internal	SS_CH3		---	2	---	mS
VO3 regulation voltage accuracy	%VO3		-1.5	---	1.5	%
Maximum Duty Cycle	D_{max3}		---	100	---	%
VIN3 Leakage Current	I_{VIN3_LK}	V_{LX3}=0V, VIN3=5.0V	---	1	5	μA
LX3 Leakage Current	I_{LX3_LK}	V_{LX3}=5.0V	---	1	5	μA
Switch ON Resistance	Ron3-N		---	120	---	mΩ
	Ron3-P		---	150	---	
Peak Current Limit	I_{LIM_CH3}		---	2.5	---	A
Under Voltage Protection Threshold	$\%V_{UVP\_CH3}$	Ratio=V_{UVP}/V_{OUT}	---	75	---	%
DCDC4 Buck Converter						
Soft-Start Internal	SS_CH4		---	2	---	mS
VO4 regulation voltage accuracy	%VO4		-1.5	---	1.5	%
Maximum Duty Cycle	D_{max4}		---	100	---	%
VIN4 Leakage Current	I_{VIN4_LK}	V_{LX4}=0V, VIN4=5.0V	---	1	5	μA
LX4 Leakage Current	I_{LX4_LK}	V_{LX4}=5.0V	---	1	5	μA
Switch ON Resistance	Ron4-N		---	120	---	mΩ
	Ron4-P		---	150	---	
Peak Current Limit	I_{LIM_CH4}		---	2.5	---	A
Under Voltage Protection Threshold	$\%V_{UVP\_CH4}$	Ratio=V_{UVP}/V_{OUT}	---	90	---	%
RTCLDO						
Input voltage range	V_{VINRTC}	VCC	2.5	---	5.5	V
Standby current	I_{Q1_RTC}	V_{VCC}=3.7v	---	5	8	μA
Output voltage	V_{RTCO}	Io=0.1mA, VRTC=2'b11	---	3.0	---	V
Dropout Voltage	V_{DO1_RTC}	Io=50mA, VRTC=2'b11	---	---	800	mV
	V_{DO2_RTC}	Io=10mA, VRTC=2'b11	---	---	150	mV
Maximum Output Current		V_{VCC}=4.2v, LDO1=95%*V_{SET}	60	---	200	mA
LDO1,LDO2, LDO3, LDO4, LDO5						
Input voltage range	V_{LDOIN}		2.8	---	5.5	V
Soft-Start Internal	SS_{LDO}		---	2	---	mS
Output Voltage accuracy	$\%V_{LDO}$	Io=100mA,	-1.5	---	1.5	%
Continuous output current at ECO mode	I_{O_ECO}	ECOLDOx=1'b1	---	---	5	mA
LDO Input Current	I_{LDOIN}	Io=0mA, ECOLDOx=1'b0	---	---	32	μA
	I_{LDOIN_ECO}	Io=0mA, ECOLDOx=1'b1	---	---	8	μA
Dropout Voltage	V_{DOLDO}	Io=300mA	---	200	400	mV
	V_{DOLLDO}	Io=50mA	---	35	70	mV
Output current limit	I_{LIMLDO}	LDOIN>LDO+1.0V,	350	400	---	mA
LDO Load Regulation		LDOIN>LDO+1.0V, Io=1mA~200mA	---	---	1	%
Short Circuit Protection threshold	$\%V_{SCPLDO}$	Ratio=V_{SCP}/V_{OUT}	---	12.5	---	%
Ripple Rejection	PSRR	f=10Hz~3kHz, Io=100mA	---	65	---	dB
Output Noise Voltage		f=10Hz~100kHz	---	45	---	uVrms

Electrical characteristics (continued)

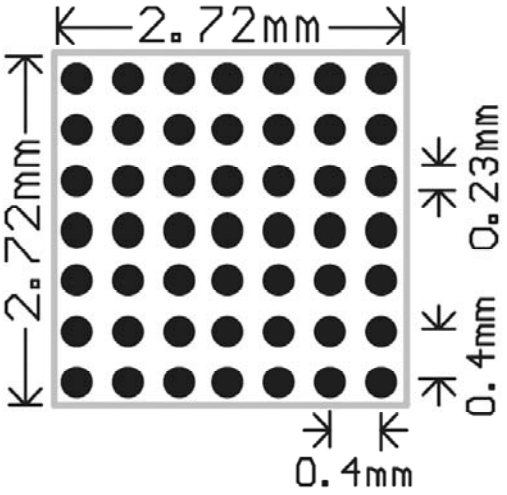
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
LDO6, LDO7						
Input voltage range	V_{LDOIN}		1.5	---	5.5	V
Soft-Start Internal	SS_{LDO}		---	2	---	mS
Output Voltage accuracy	$\%V_{LDO}$	Io=100mA,	-1.5	---	1.5	%
Continuous output current at ECO mode	I_{O_ECO}	ECOLDOx=1'b1	---	---	5	mA
LDO Input Current	I_{LDOIN}	Io=0mA, ECOLDOx=1'b0	---	---	32	µA
	I_{LDOIN_ECO}	Io=0mA, ECOLDOx=1'b1	---	---	8	µA
Dropout Voltage	$V_{DOLDO67}$	Io=200mA, VCC=3V	---	200	400	mV
	$V_{DOLLDO67}$	Io=50mA, VCC=3V	---	35	70	mV
Output current limit	I_{LIMLDO}	LDOIN>LDO+1.0V,	350	400	---	mA
LDO Load Regulation		LDOIN>LDO+1.0V, Io=1mA~200mA	---	---	1	%
Short Circuit Protection threshold	$\%V_{SCPLDO}$	Ratio=V_{SCP}/V_{OUT}	---	12.5	---	%
Ripple Rejection	PSRR	f=10Hz~3kHz, Io=100mA	---	65	---	dB
Output Noise Voltage		f=10Hz~100kHz	---	45	---	µVrms
32.768kHz Real Time Clock						
RTC Supply Current	I_{Q_RTC}	RTCOUT=3.0V	---	1	---	µA
OSC_32K Duty Cycle	D_{OSC_32K}		40	---	60	%
OSC_32K Output high voltage	V_{OH_OSC}	Follow DCDC4 output voltage	---	DCDC4	---	V
OSC_32K Output Sink Current	I_{SINK_OSC}	OSC_32K=0.4V, RTCOUT=3.0V	---	1	---	mA
OSC_32K Output Source Current	I_{SOURCE_OSC}	OSC_32K=RTCOUT-0.4V, RTCOUT=3.0V	---	1	---	mA
Protection						
UVP Protection Fault Delay	T_{D_Fault}	DCDC1~DCDC4	128	---	---	mS
Thermal Shutdown Detect	T_{SD}		---	150	---	°C
Thermal Shutdown Hysteresis	ΔT_{SD}		---	20	---	°C
Control Signal						
Logic-Input Threshold (PWRON, PWRHOLD, ENLDO)	V_{TH}	High threshold	1.4	---	---	V
	V_{TL}	Low threshold	---	---	0.5	V
PWRON internal pull high resistance	R_{PWRON}		---	200	---	kΩ
PWRHOLD internal pull low current	$I_{PWRHOLD}$	PWRHOLD=5V	---	---	5	µA
ENLDO sink current	I_{ONPMU_SINK}	ENLDO=5V	---	---	5	µA
Open-Drain Output Low Voltage (/INT, PWRGD)	V_{ODLOW}	I_{SINK}=5mA, V_{VCC}=3.7V	---	---	100	mV
Open-Drain Output Leakage Current (/INT, PWRGD)	I_{LK_OD}	V_{OD}=5V	---	---	1	µA
PWRGD Delay Time	T_{DLY_PWRGD}		45	64	83	mS

Electrical characteristics (continued)

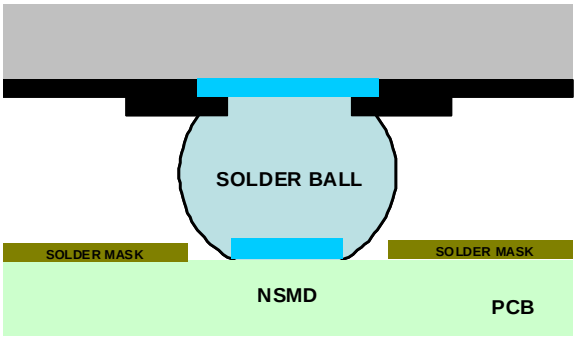
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
SIM Card Interface						
Logic-Input Threshold	V_{TH_SIM}	High threshold	V_{CC_IO}-0.6	---	---	V
(SIMCLK, SIMRST)	V_{TL_SIM}	Low threshold	---	---	0.6	V
SIMIO Output Sink Current	I_{SINK_SIMIO}	SIMIO=0.4V, SIO=0	200	---	---	µA
SIMIO Output Source Current	I_{SOURCE_SIMIO}	SIMIO=0.7xV_{VCC_IO}, SIO=V_{LDO1}	20	---	---	µA
SIMIO internal pull high resistance	R_{SIMIO}	To VCC_IO	16	20	24	kΩ
SCLK, SRST Output Sink Current	I_{SINK_S}	SCLK=SRST=0.2x V_{LDO1}, SIMCLK=SIMRST=0	20	---	---	µA
SCLK, SRST Output Source Current	I_{SOURCE_S}	SCLK=SRST=0.9x V_{LDO1}, SIMCLK=SIMRST=V_{VCC_IO}	200	---	---	µA
SIO Output Sink Current	I_{SINK_SIMIO}	SIO=0.4V, SIMIO=0	200	---	---	µA
SIO Output Source Current	I_{SOURCE_SIMIO}	SIO=0.8xV_{LDO1}, SIMIO=V_{VCC_IO}	20	---	---	µA
SIO internal pull high resistance	R_{SIO}	To LDO1	8	10	12	kΩ
SRST, SIO rise/fall time	T_{R_S},T_{F_S}	V_{LDO1}=1.8V, load with 30pF	---	---	1	µS
SCLK rise/fall time	T_{R_SCLK}, T_{F_SCLK}	V_{LDO1}=1.8V, load with 30pF	---	---	50	nS
SCLK Frequency	f_{SCLK}	SCLK load with 30pF	5	---	---	MHz
SCLK Duty Cycle	D_{SCLK}	SIMCLK Duty=50%, f_{SIMCLK}=5MHz	47	---	53	%
SCLK Propagation Delay	T_{PD_SCLK}		---	30	50	nS
SMBus Interface						
Logic Input High Voltage	V_{IH}	SCL, SDA	1.4	---	---	V
Logic Input Low Voltage	V_{IL}	SCL, SDA	---	---	0.5	V
Logic Input Current		Logic inputs forced to VCC or GND	-2	---	2	µA
SMBus Input Capacitance		SCL, SDA	---	5	---	pF
SMBus Clock Frequency	f_{SCL}	Fast mode	---	---	400	kHz
		High-speed mode, load 400pF max	---	---	1.7	MHz
		High-speed mode, load 100pF max	---	---	3.4	MHz
SCL Clock Low Time	t_{LOW}	Fast mode	1.3	---	---	µS
SCL Clock High Time	t_{HIGH}	Fast mode	0.6	---	---	µS
SDA Setup Time	$t_{SU:DAT}$	Fast mode	100	---	---	nS
SDA Hold Time	$t_{HD:DAT}$	Fast mode	0	---	0.9	µS
Bus-Free Time from START and STOP	t_{BUF}	Fast mode	1.3	---	---	µS
Hold Time Repeated START Condition	$t_{HD:STA}$	Fast mode	0.6	---	---	µS
Setup Time Repeated START Condition	$t_{SU:STA}$	Fast mode	0.6	---	---	µS
Setup Time for STOP Condition	$t_{SU;STO}$	Fast mode	0.6	---	---	µS
Rise Time of SCL/SDA signals	t_r	10% to 90% points	20	---	300	nS
Fall Time of SCL/SDA signals	t_f	90% to 10% points	20	---	300	nS

Minimum Footprint PCB Layout Section

WLCSP7X7-49



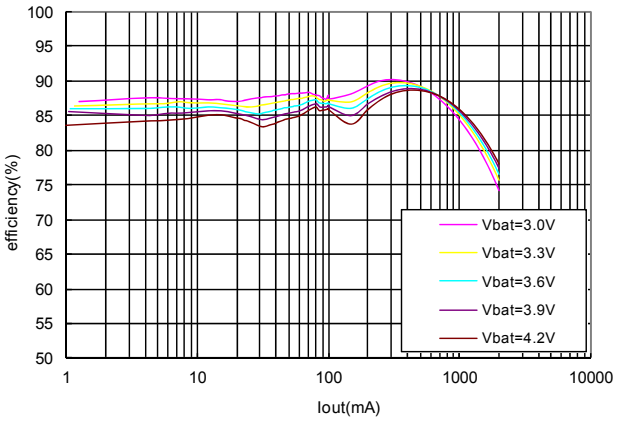
1. NSMD Structure
2. Pad size = 228.6um (9mils)
3. Solder mask open =330.2um (2mils + 9mils + 2mils)



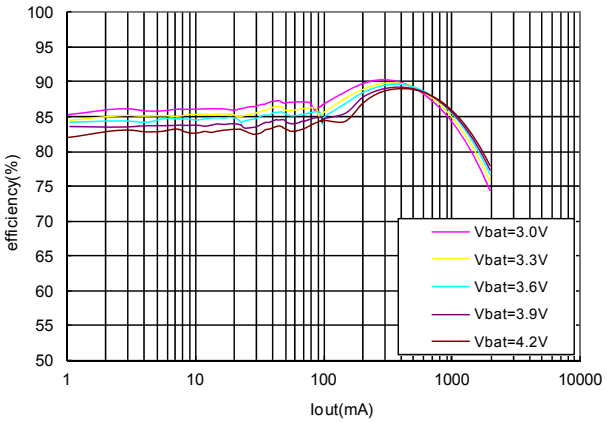
Typical Performance Characteristics

(T_A=25°C)

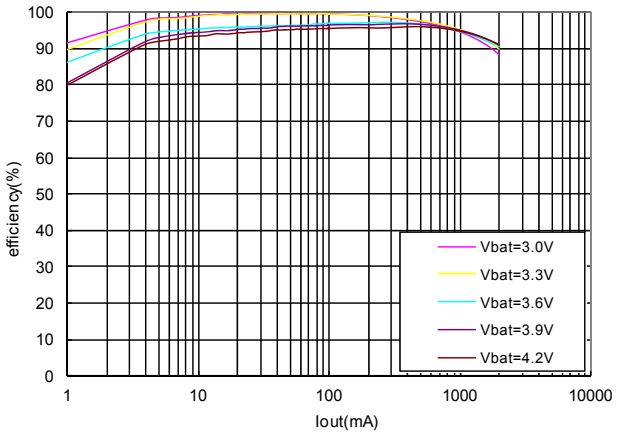
CH1 Step-Down Efficiency vs. Output Current



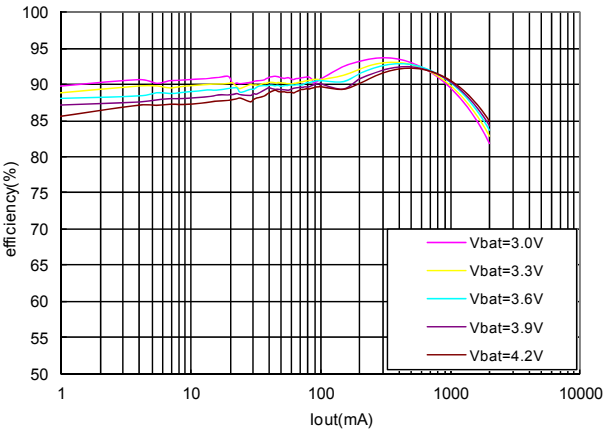
CH2 Step-Down Efficiency vs. Output Current



CH3 Step-Down Efficiency vs. Output Current

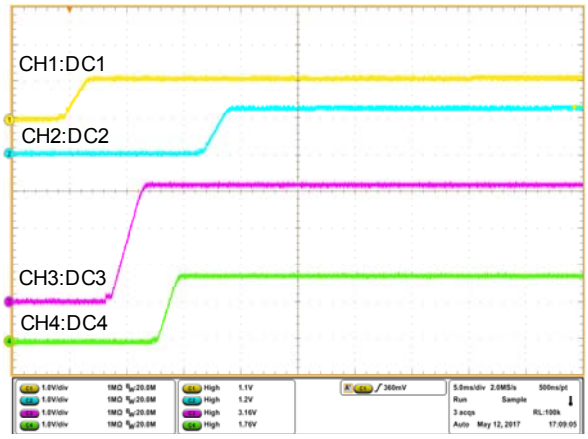


CH4 Step-Down Efficiency vs. Output Current

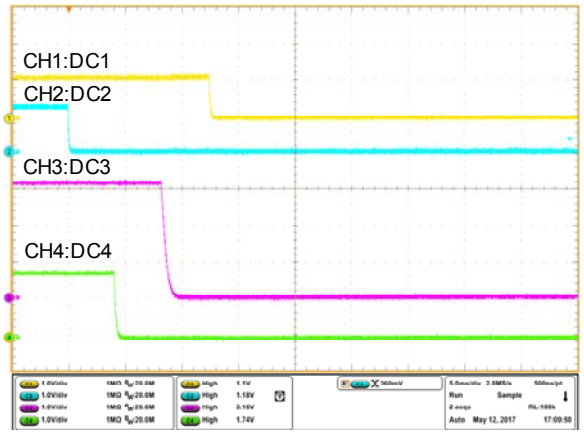


Typical Performance Characteristics (continued)

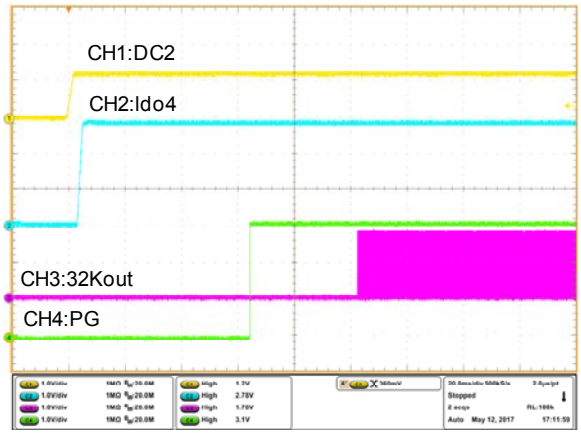
Power on sequence ;Vbat=3.7V



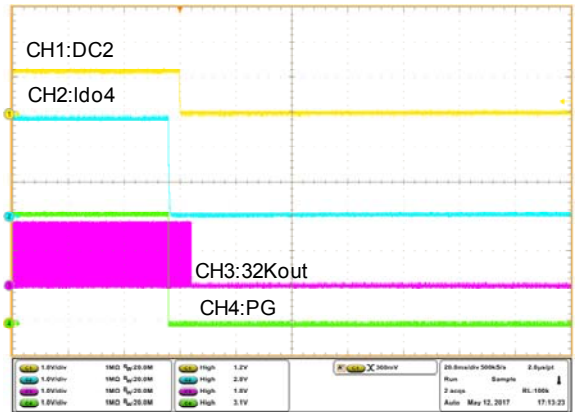
Power off sequence ;Vbat=3.7V



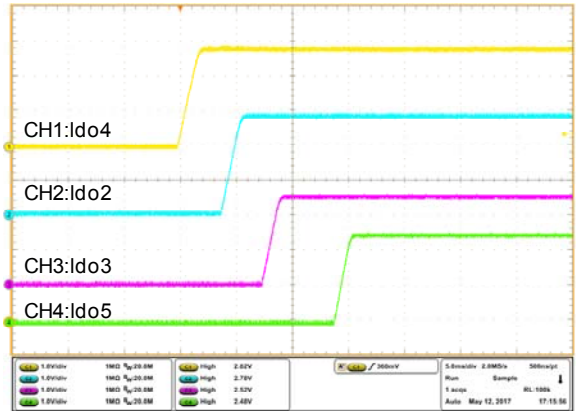
Power on sequence ;Vbat=3.7V



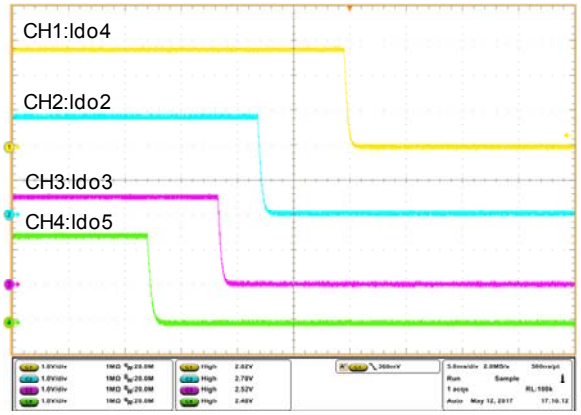
Power off sequence ;Vbat=3.7V



Power on sequence ;Vbat=3.7V

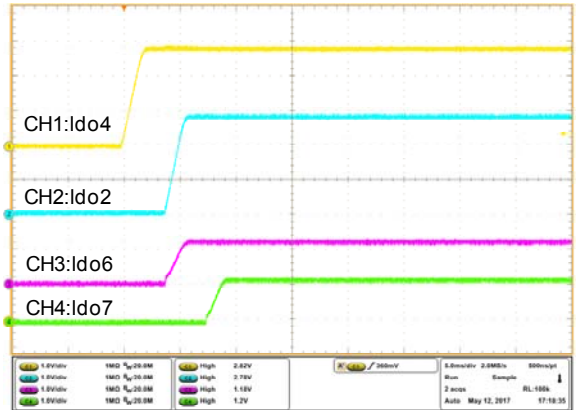


Power off sequence ;Vbat=3.7V

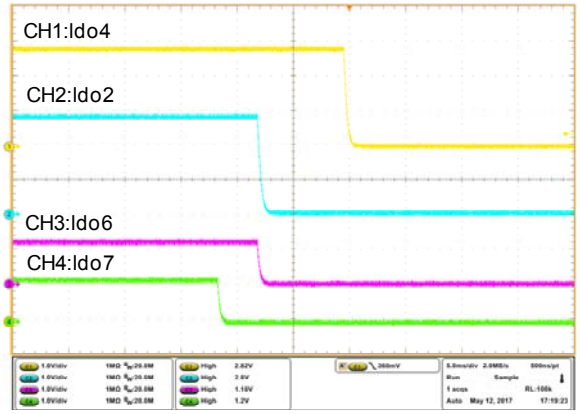


Typical Performance Characteristics (continued)

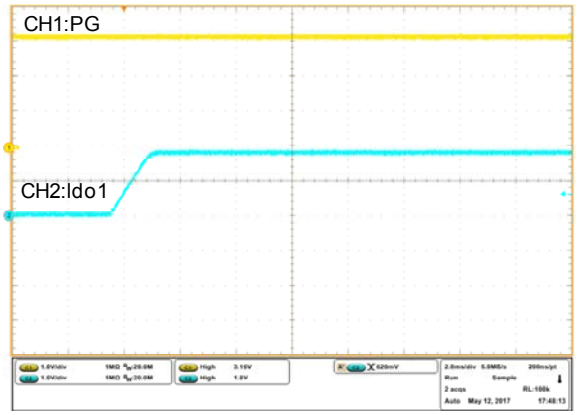
Power on sequence ;Vbat=3.7V



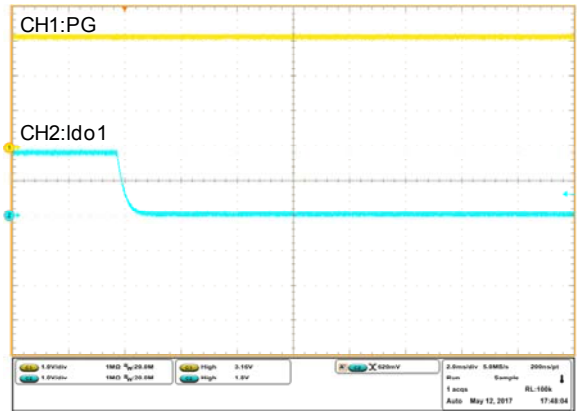
Power off sequence ;Vbat=3.7V



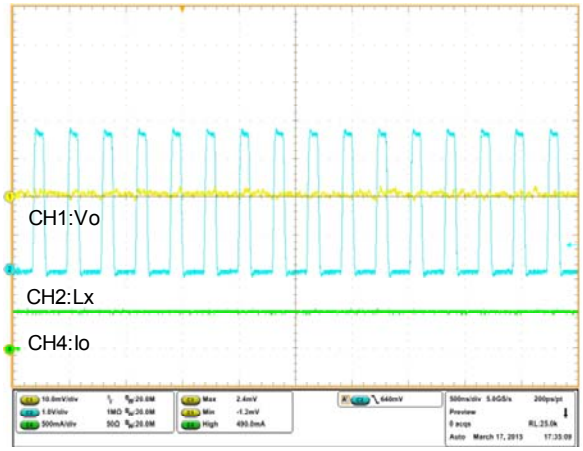
Power on sequence ;Vbat=3.7V



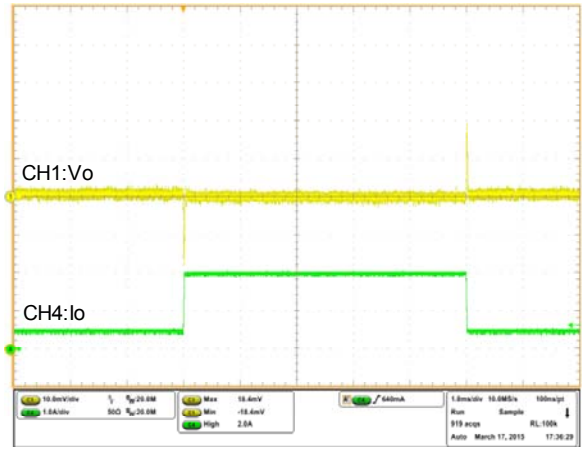
Power off sequence ;Vbat=3.7V



DC1 Ripple ;Vbat=3.7V Io=500mA

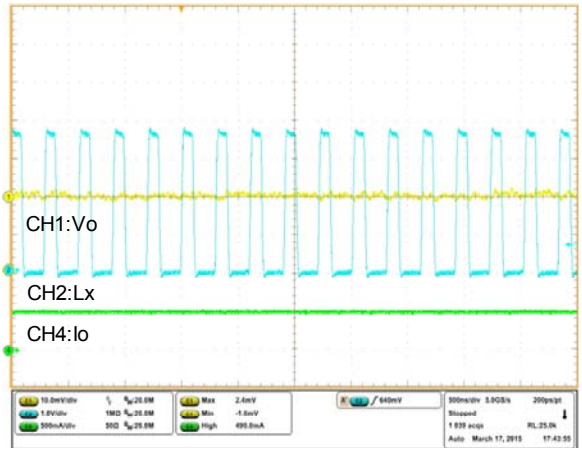


DC1 Load Transient ;Vbat=3.7V Io=500-2000mA

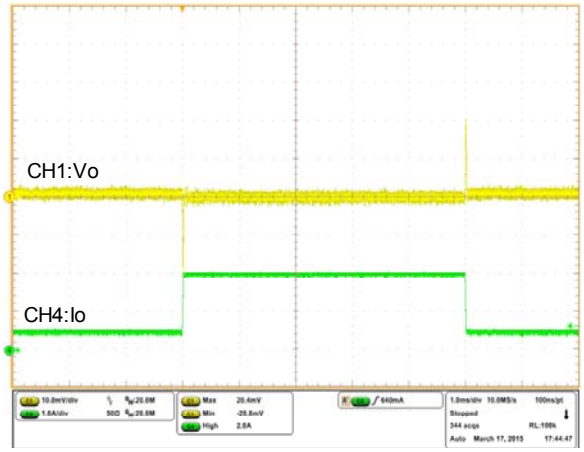


Typical Performance Characteristics (continued)

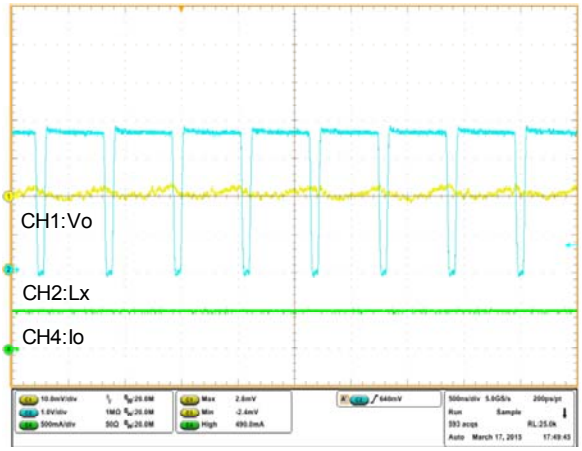
DC2 Ripple ;Vbat=3.7V Io=500mA



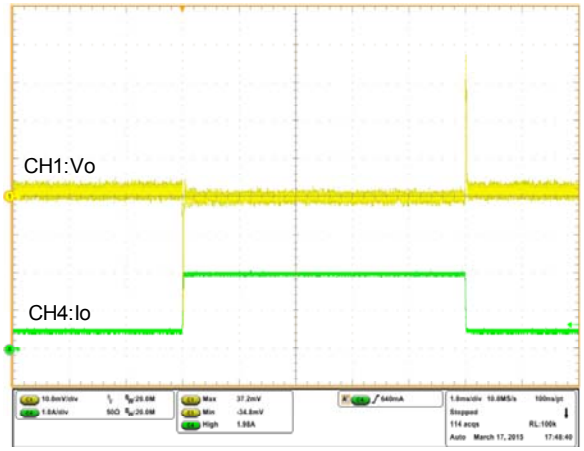
DC2 Load Transient ;Vbat=3.7V Io=500-2000mA



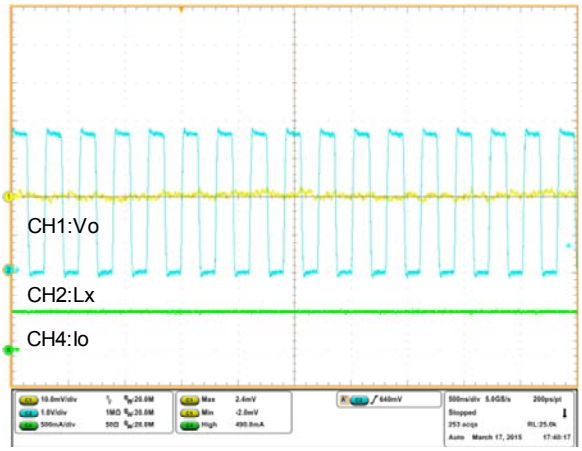
DC3 Ripple ;Vbat=3.7V Io=500mA



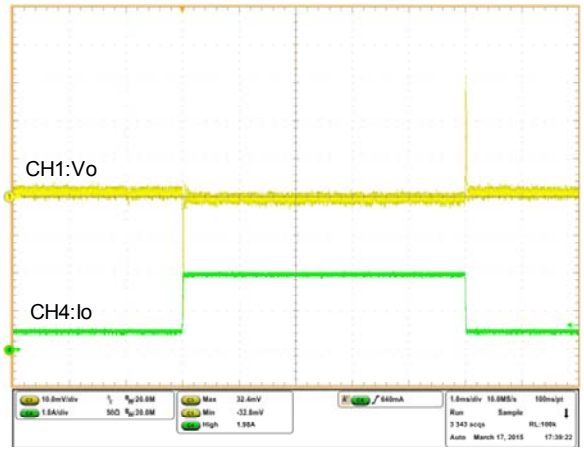
DC3 Load Transient ;Vbat=3.7V Io=500-2000mA



DC4 Ripple ;Vbat=3.7V Io=500mA

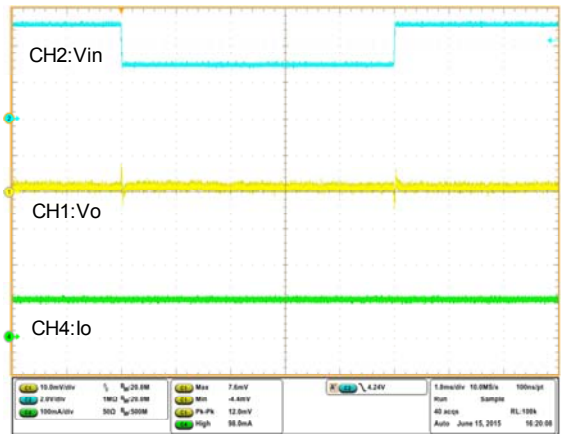


DC4 Load Transient ;Vbat=3.7V Io=500-2000mA

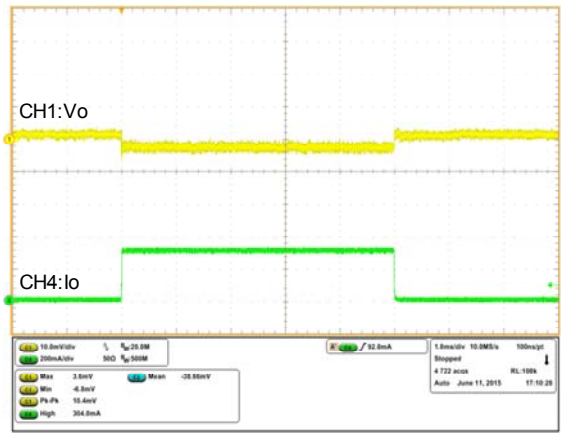


Typical Performance Characteristics (continued)

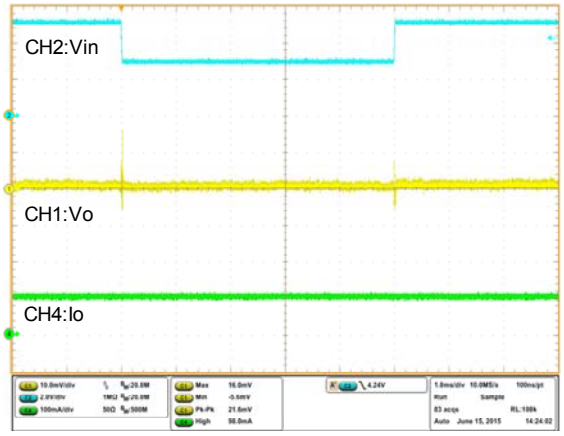
LDO1 Line transient



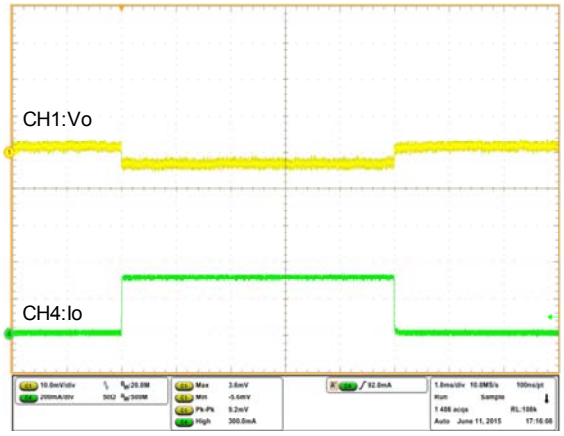
LDO1 load transient;Vbat=3.7V Vldoin=3.2V Io=0-300mA



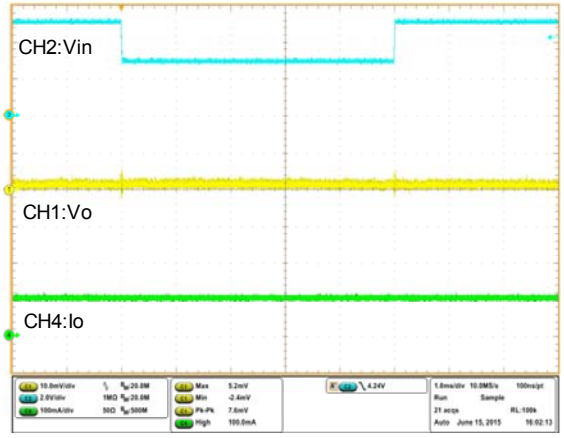
LDO2 Line transient



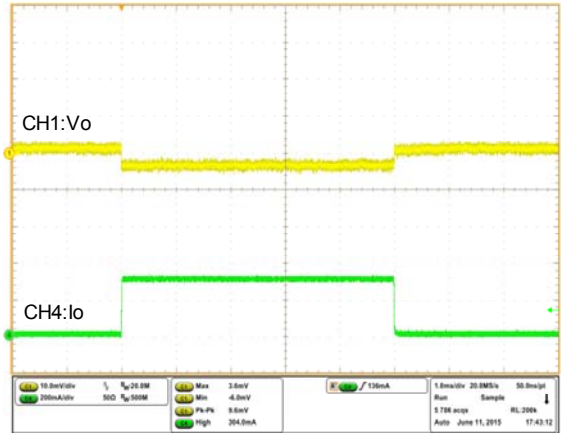
LDO2 load transient;Vbat=3.7V Vldoin=3.2V Io=0-300mA



LDO3 Line transient

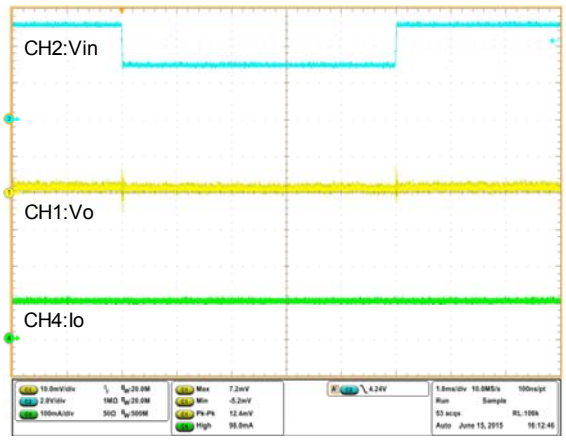


LDO3 load transient;Vbat=3.7V Vldoin=3.2V Io=0-300mA

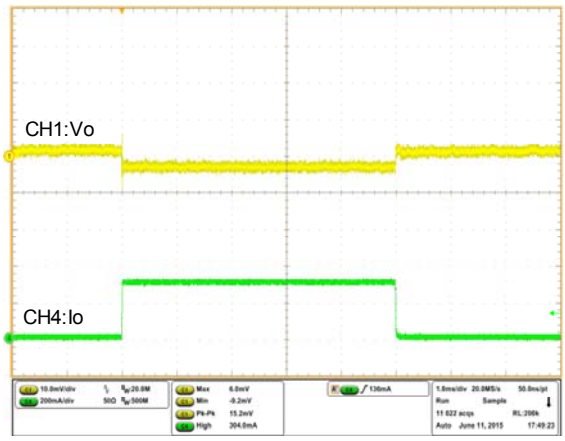


Typical Performance Characteristics (continued)

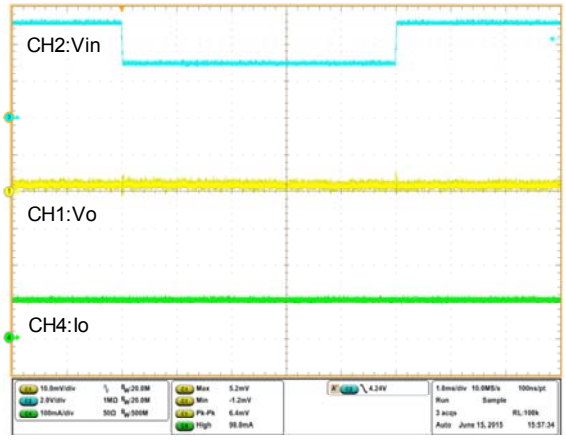
LDO4 Line transient



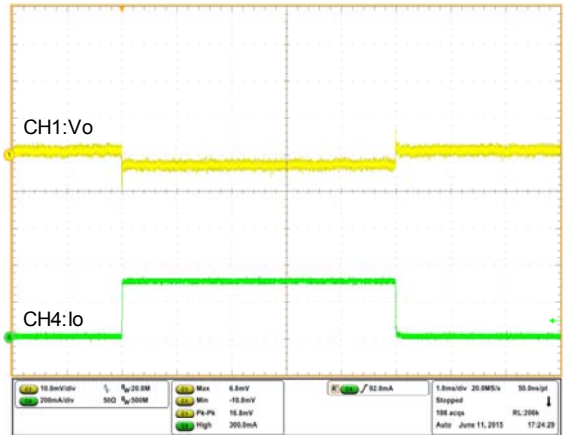
LDO4 load transient;Vbat=3.7V Vldoin=3.2V Io=0-300mA



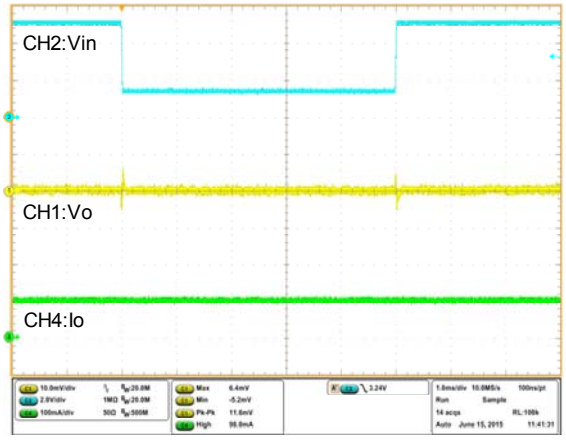
LDO5 Line transient



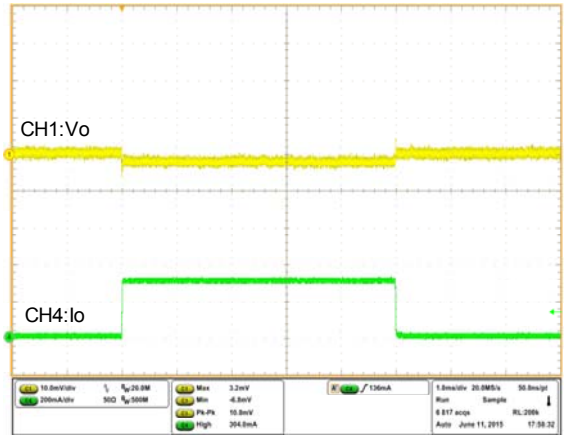
LDO5 load transient;Vbat=3.7V Vldoin=3.2V Io=0-300mA



LDO6 Line transient

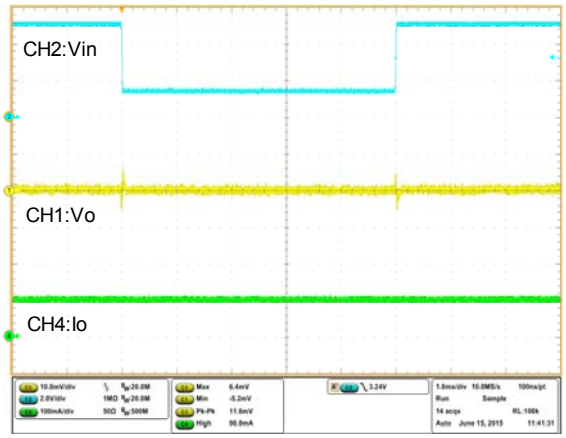


LDO6 load transient;Vbat=3.7V Vldoin=1.8V Io=0-300mA

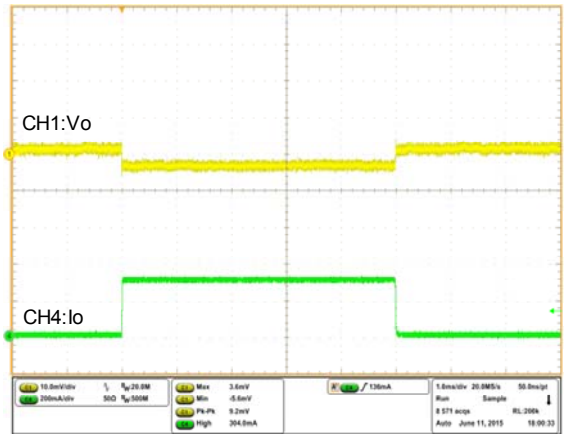


Typical Performance Characteristics (continued)

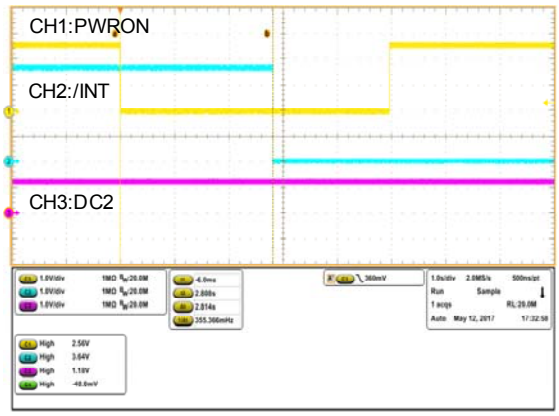
LDO7Line transient



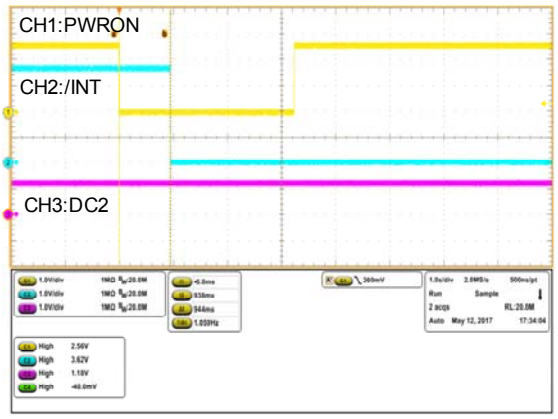
LDO7 load transient;Vbat=3.7V Vldoin=1.8V Io=0-300mA



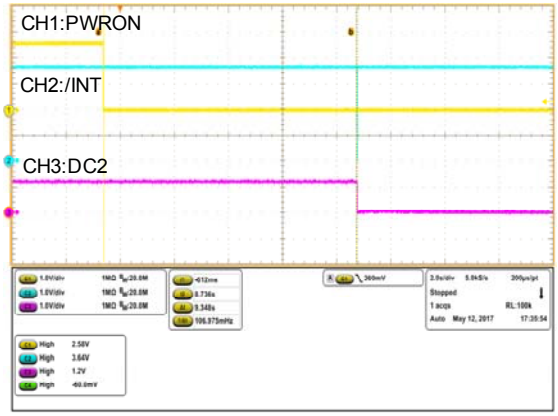
PWRON IT



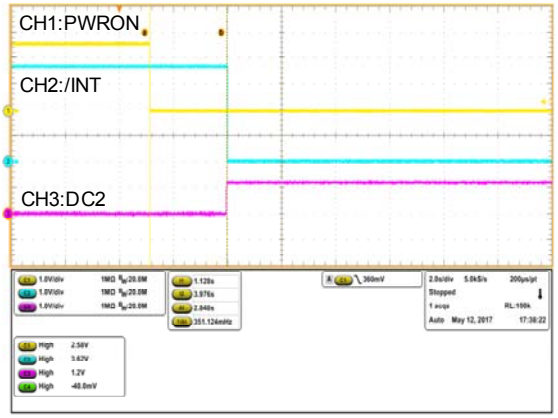
PWRON LP



PWRON LPOFF

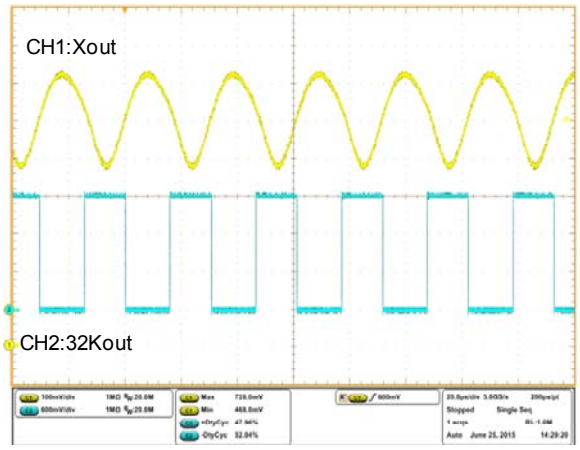


PWRON LPOFF to ON

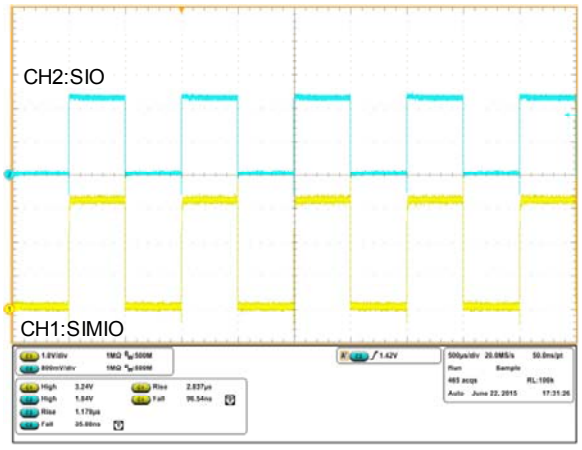


Typical Performance Characteristics (continued)

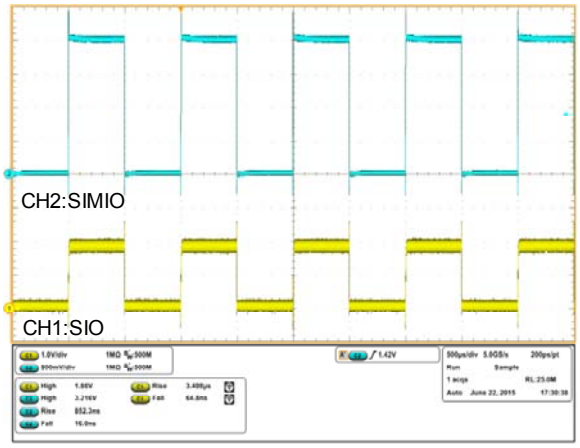
32Kout



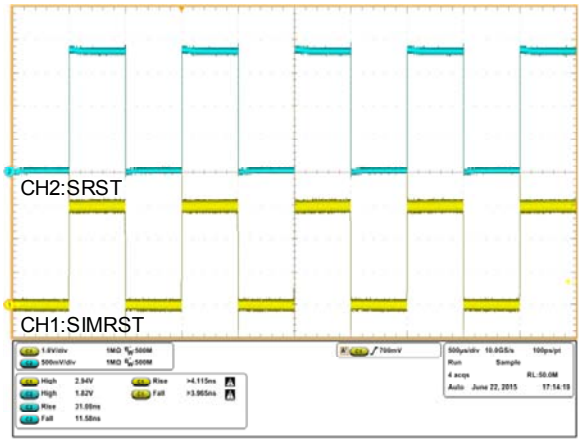
SIMIO input ; SIO output



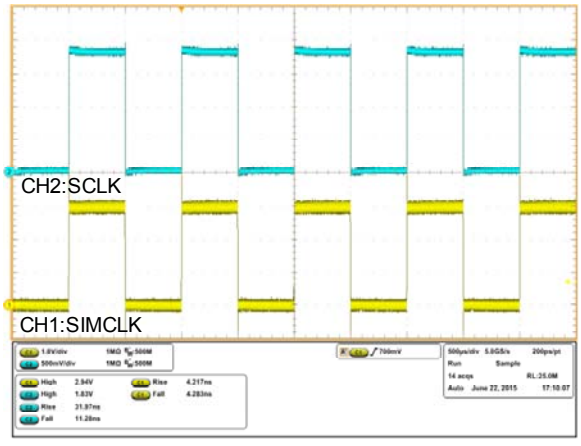
SIO input ; SIMIO output



SIMRST input ; SRST output

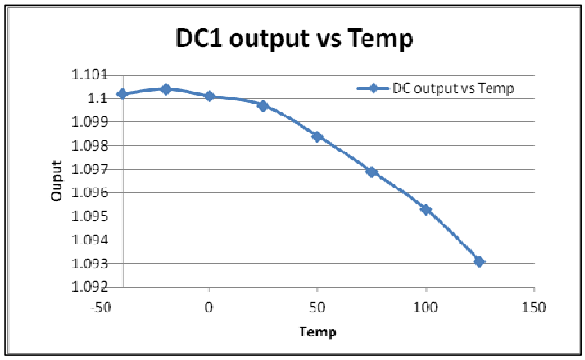


SIMCLK input ; SCLK output

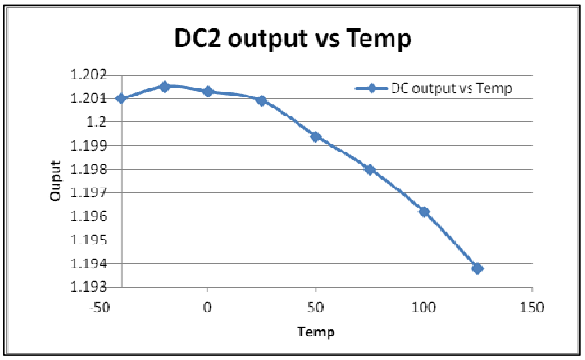


Typical Performance Characteristics (continued)

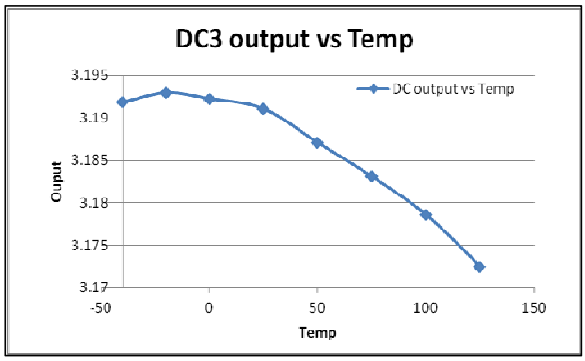
DC1 Vo vs. Temp



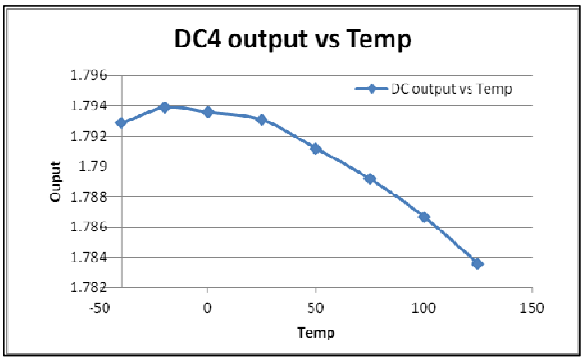
DC2 Vo vs. Temp



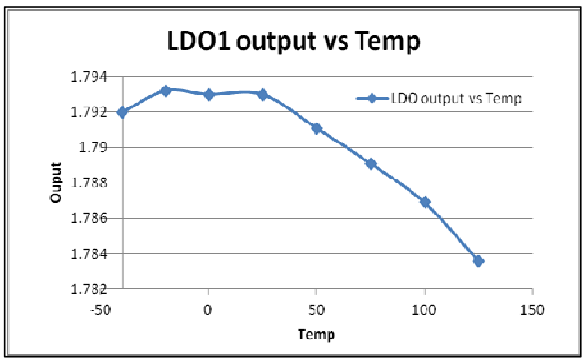
DC3 Vo vs. Temp



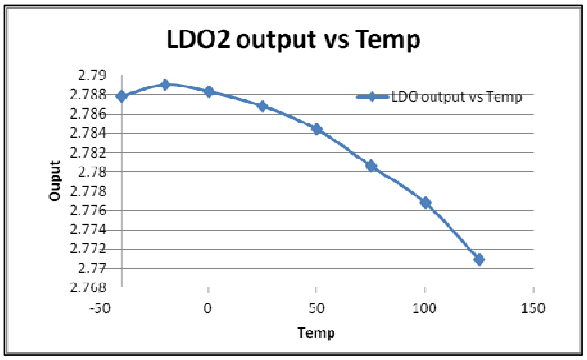
DC4 Vo vs. Temp



LDO1 Vo vs. Temp

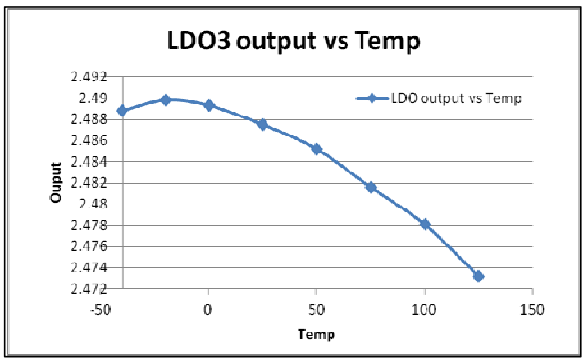


LDO2 Vo vs. Temp

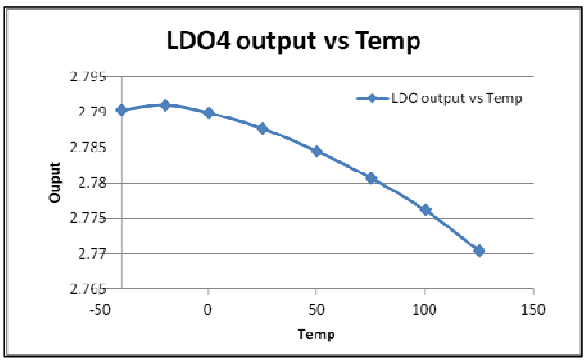


Typical Performance Characteristics (continued)

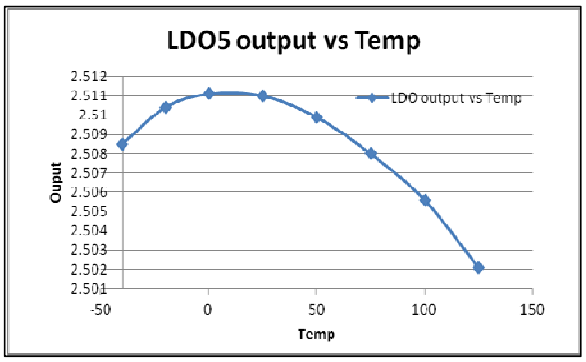
LDO3 Vo vs. Temp



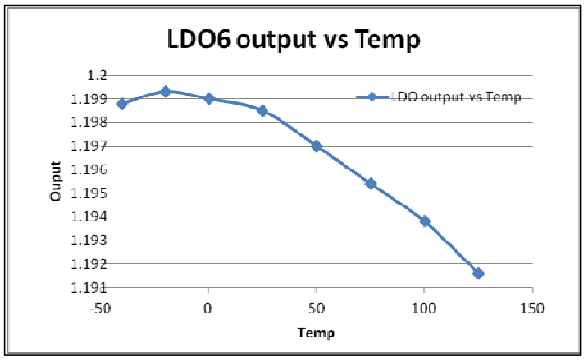
LDO4 Vo vs. Temp



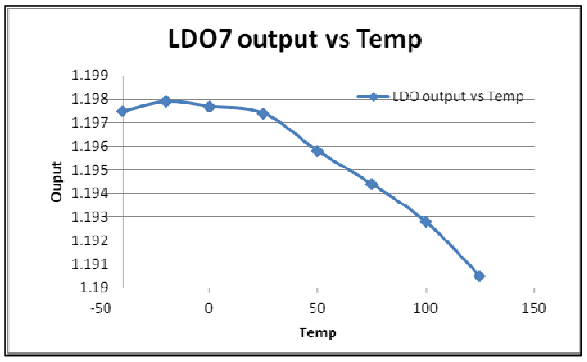
LDO5 Vo vs. Temp



LDO6 Vo vs. Temp



LDO7 Vo vs. Temp

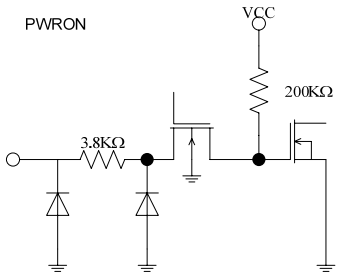


Pin Description

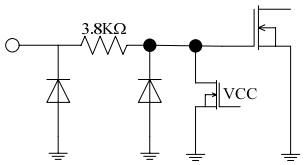
Pin No	Pin Name	Function
G7	VIN1	Power Input of DCDC1 Buck Converter.
F7	LX1	Inductor switch node of DCDC1 Buck Converter.
E7	PGND1	Power Ground of DCDC1 Buck Converter.
E6	DCDC1	Sensing Input of DCDC1 Buck Converter's output voltage.
G4	VIN2	Power Input of DCDC2 Buck Converter.
G5	LX2	Inductor switch node of DCDC2 Buck Converter.
G6	PGND2	Power Ground of DCDC2 Buck Converter.
F4	DCDC2	Sensing Input of DCDC2 Buck Converter's output voltage.
G1	VIN3	Power Input of DCDC3 Buck Converter.
G2	LX3	Inductor switch node of DCDC3 Buck Converter.
G3	PGND3	Power Ground of DCDC3 Buck Converter.
F3	DCDC3	Sensing Input of DCDC3 Buck Converter's output voltage.
D7	VIN4	Power Input of DCDC4 Buck Converter.
C7	LX4	Inductor switch node of DCDC4 Buck Converter.
B7	PGND4	Power Ground of DCDC4 Buck Converter.
B6	DCDC4	Sensing Input of DCDC4 Buck Converter's output voltage.
E1	LDOIN1	Power Input of LDO1.
E2	LDO1	LDO Output of LDO1.
C1	LDOIN2345	Power Input of LDO2 ,LDO3, LDO4, and LDO5.
D1	LDO2	LDO Output of LDO2.
D2	LDO3	LDO Output of LDO3.
C2	LDO4	LDO Output of LDO4.
B1	LDO5	LDO Output of LDO5.
A6	LDOIN67	Power Input of LDO6 and LDO7.
A7	LDO6	LDO Output of LDO6.
A5	LDO7	LDO Output of LDO7.
D4	SCLK	Level-shifted SIM clock output.
D5	SRST	Level-shifted SIM reset output.
D3	SIO	Level-shifted SIM bi-directional data input/output.
E4	SIMCLK	Non-level-shifted SIM clock input
E5	SIMRST	Non-level-shifted SIM reset input
E3	SIMIO	Non-level-shifted SIM bi-directional data input/output
B2	RTCOUT	LDO Output of RTC LDO. Bypass this pin to ground with a 2.2uF ceramic capacitor.
A1	XOUT	Crystal Oscillator Output
A2	XIN	Crystal Oscillator Input
C3	OSC_32K	32.768kHz clock output
C5	/INT	Interrupt Indicator with open drain output.
F5	PWRGD	Indicator of PMU power on/off with open drain output.
C6	SDA	Data Input PIN of I^2C interface.
D6	SCL	Clock Input PIN of I^2C interface.
C4	PWRON	Power on/off key, internal pull high to VCC
B4	PWRHOLD	Power on/off signal from Microprocessor, internal pull low to GND.
F2	ENLDO	Power on/off signal of LDO2~LDO7 from Microprocessor, internal pull low to GND.
B5	VBG	1.21V Reference Voltage Output. Bypass this pin to ground with a 0.22uF ceramic capacitor.
F1	VCC_IO	Power input of SIM card signal from Microprocessor
A4	VCC	IC Power Supply Input pin. Bypass with a 10uF or greater ceramic capacitor.
A3	AGND	Chip analog ground
B3,F6	DGND	Chip digital ground

Equivalent Circuits of Inputs and Outputs

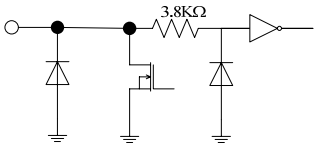
PWRON



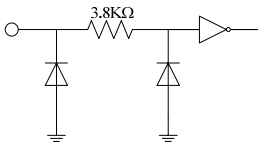
PWRHOLD, ENLDO,



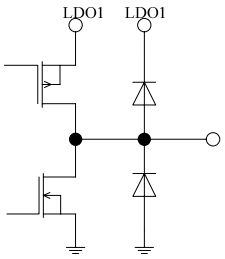
SDA



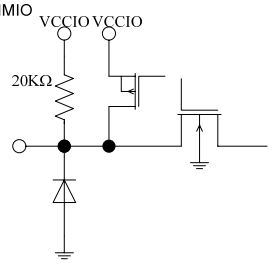
SIMCLK,SIMRST
SCL



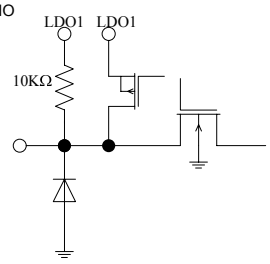
SCLK,SRST



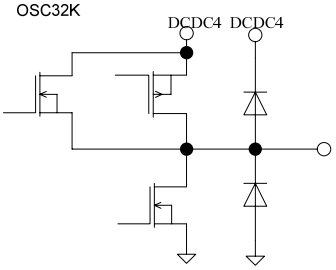
SIMIO



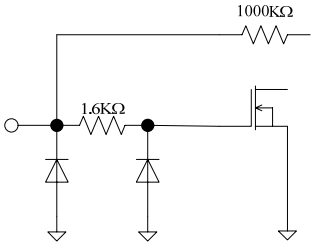
SIO



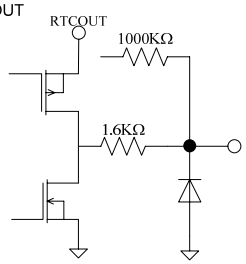
OSC32K



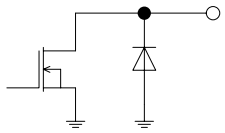
XIN



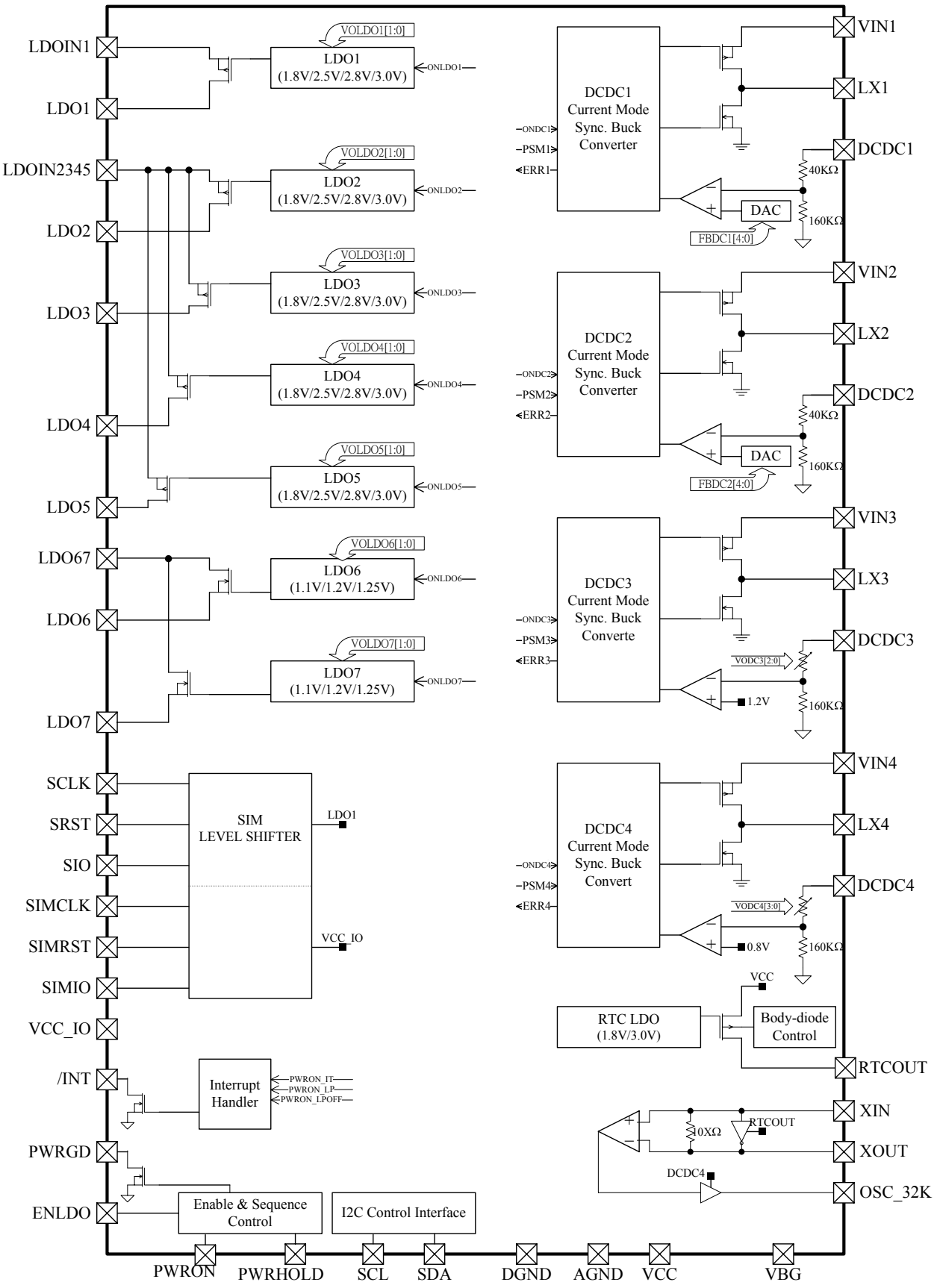
XOUT



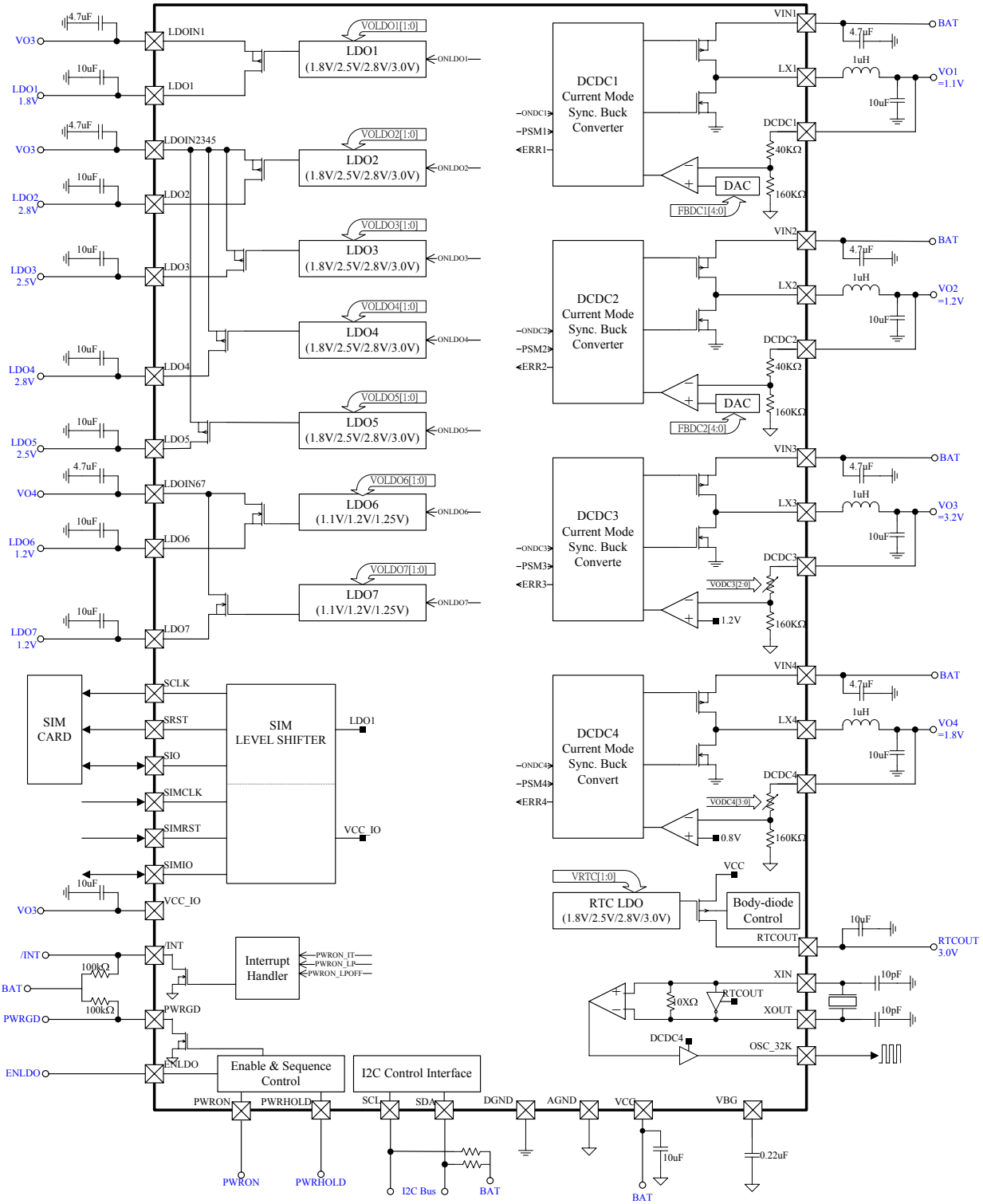
/INT, PWRGD



Block Diagram



Application circuit



I2C Interface

G5851 I2C slave address=7'b0010010. The write or read bit stream (N≥1) is shown below:

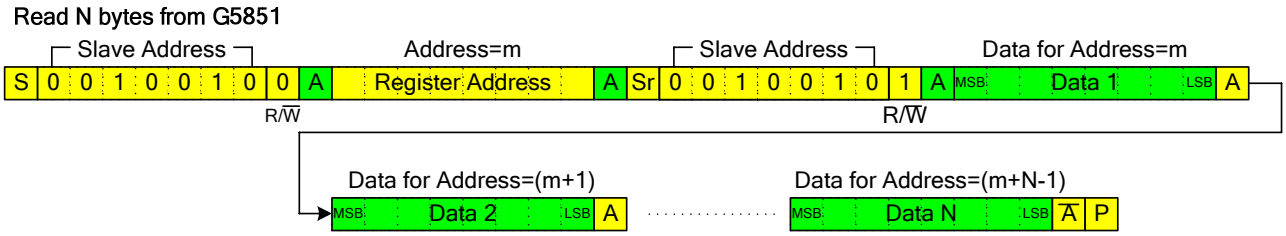
Driven by Master

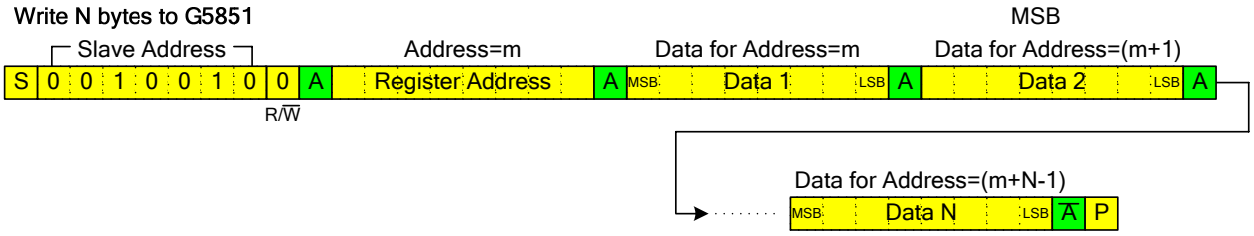
Driven by G5851

S Start

P Stop

Sr Repeat Start





I2C Register Map

Address	Byte Name		Data							
			b7	b6	b5	b4	b3	b2	b1	b0
00h	A0	Meaning	DEVON	SLEEP		LPOFF	ERRDC1	ERRDC2	ERRDC3	ERRDC4
		Default	0	0		1	0	0	0	0
		Read/Write	R/W	R/W		R/W	R	R	R	R
01h	A1	Meaning	SLPDC1	SLPDC2	SLPDC3	SLPDC4			VRTC[1:0]	
		Default	0	0	0	0			1	1
		Read/Write	R/W	R/W	R/W	R/W			R/W	R/W
02h	A2	Meaning	SLPLDO1	SLPLDO2	SLPLDO3	SLPLDO4	SLPLDO5	SLPLDO6	SLPLDO7	
		Default	0	0	0	0	0	0	0	
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
03h	A3	Meaning	ONDC1	ONDC2	ONDC3	ONDC4				
		Default	1	1	1	1				
		Read/Write	R/W	R/W	R/W	R/W				
04h	A4	Meaning	ONLDO1	ONLDO2	ONLDO3	ONLDO4	ONLDO5	ONLDO6	ONLDO7	
		Default	0	1	1	1	1	1	1	
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
05h	A5	Meaning	FPWM1	FPWM2	FPWM3	FPWM4	ECODC1	ECODC2	ECODC3	ECODC4
		Default	0	0	0	0	1	1	1	1
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
06h	A6	Meaning	ECOLDO1	ECOLDO2	ECOLDO3	ECOLDO4	ECOLDO5	ECOLDO6	ECOLDO7	
		Default	0	0	0	0	0	0	0	
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
07h	A7	Meaning				FBDC1[4:0]				
		Default				0	1	1	1	1
		Read/Write				R/W	R/W	R/W	R/W	R/W
08h	A8	Meaning				FBDC2[4:0]				
		Default				1	0	0	1	1
		Read/Write				R/W	R/W	R/W	R/W	R/W
09h	A9	Meaning		VODC3[2:0]			VODC4[3:0]			
		Default		1	0	1	1	1	0	1
		Read/Write		R/W	R/W	R/W	R/W	R/W	R/W	R/W
0Ah	A10	Meaning		VOLDO1[2:0]				VOLDO2[2:0]		
		Default		0	1	1		1	0	1
		Read/Write		R/W	R/W	R/W		R/W	R/W	R/W
0Bh	A11	Meaning		VOLDO3[2:0]				VOLDO4[2:0]		
		Default		1	0	0		1	0	1
		Read/Write		R/W	R/W	R/W		R/W	R/W	R/W
0Ch	A12	Meaning		VOLDO5[2:0]			VOLDO6[1:0]		VOLDO7[1:0]	
		Default		1	0	0	0	1	0	1
		Read/Write		R/W	R/W	R/W	R/W	R/W	R/W	R/W
0Dh	A13	Meaning	TIME_IT[1:0]		TIME_LP[1:0]		TIME_LPOFF[1:0]			
		Default	0	1	0	0	1	1		
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W		
0Eh	A14	Meaning	MASK_ IT		MASK_ LP		MASK_ LPOFF			INT
		Default	0		0		0			0
		Read/Write	R/W		R/W		R/W			R/W
0Fh	A15	Meaning	PWRON_ IT		PWRON_ LP		PWRON_ LPOFF			
		Default	0		0		0			
		Read/Write	R		R		R			
10h	A16	Meaning	VER[2:0]							
		Default	0	0	0					
		Read/Write	R	R	R					
11h	A17	Meaning	TIMER[7:0]							
		Default	0	0	0	0	1	1	1	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
F1h	GMT Testing	Meaning	TM[4:1]				ENCNT			
		Default	0	0	0	0	0			
		Read/Write	R/W	R/W	R/W	R/W	R/W			

I2C Register Reset Conditions

VCC<2.3V	PMU shutdown	Condition of registers 00h,01h,02h,0Dh~F1h	Condition of registers 03h~0Ch
TRUE	X	Reset	Reset
FALSE	TRUE	NO Reset	Reset
	FALSE	NO Reset	NO Reset

I2C Register Function Table

<table>
<tr><th>Byte Name</th><th>Data Bit</th><th>Data Name</th><th>Function Description</th></tr>
<tr><td>A0</td><td>b7</td><td>DEVON</td><td>Write 0 to DEVON to start PMU power-off sequence when PMU is in operation mode.
When PWRON_LPOFF=1’b0, write 1 to DEVON to enable PMU power-on sequence when PMU is in shutdown mode.
Write 1 to DEVON to keep PMU in operation mode after PMU start-up by PWRON press.</td></tr>
<tr><td>A0</td><td>b6</td><td>SLEEP</td><td>SLEEP, combined with the status of PWRHOLD, A0.DEVON, A1.SLPDCx, and A2.SLPLDOx, is used to control the operation status of PMU
<table>
<tr><th>SLEEP</th><th>PWRHOLD =Low ,and DEVON=0</th><th>SLPDCx, SLPLDOx</th><th>DCDC and LDO</th></tr>
<tr><td>0</td><td>TRUE</td><td>X</td><td>Shutdown</td></tr>
<tr><td>0</td><td>FALSE</td><td>X</td><td>Operation</td></tr>
<tr><td rowspan="2">1</td><td rowspan="2">TRUE</td><td>0</td><td>Shutdown</td></tr>
<tr><td>1</td><td>Operation</td></tr>
<tr><td>1</td><td>FALSE</td><td>X</td><td>Operation</td></tr>
</table></td></tr>
<tr><td>A0</td><td>b4</td><td>LPOFF</td><td>Enable PMU shutdown when PWRON long pressed with duration longer than TdPWRONLPOFF defined by register A13.TIME_LPOFF
<table>
<tr><th>T>$T_{dPWRONLPOFF}$</th><th>PMU shutdown</th></tr>
<tr><td>0</td><td>NO</td></tr>
<tr><td>1</td><td>YES</td></tr>
</table></td></tr>
<tr><td>A0</td><td>b3~b0</td><td>ERRDC1 ~ERRDC4</td><td>Record whether the UVP protection of DCDC1~DCDC4 ever occurs respectively.
<table>
<tr><th>ERRDCx</th><th>Protection Occurs</th></tr>
<tr><td>0</td><td>NO</td></tr>
<tr><td>1</td><td>YES</td></tr>
</table></td></tr>
<tr><td>A1</td><td>b7~b4</td><td>SLPDC1 ~SLPDC4</td><td>SLPDCx is used to control the operating status of DC/DC converters when PMU is in sleep mode.
<table>
<tr><th>SLPDCx</th><th>DCDCx Status in SLEEP mode</th></tr>
<tr><td>0</td><td>Shutdown</td></tr>
<tr><td>1</td><td>Operation</td></tr>
</table></td></tr>
<tr><td>A1</td><td>b1~ b0</td><td>VRTC [1:0]</td><td>Setting the output voltage of RTC LDO
<table>
<tr><th>VRTC[1:0]</th><th>RTCOUT</th></tr>
<tr><td>11</td><td>3.0V</td></tr>
<tr><td>10</td><td>2.8V</td></tr>
<tr><td>01</td><td>2.5V</td></tr>
<tr><td>00</td><td>1.8V</td></tr>
</table></td></tr>
<tr><td>A2</td><td>b7~b1</td><td>SLPLDO1 ~SLPLDO7</td><td>SLPLDOx is used to control the operating status of LDOs when PMU is in sleep mode.
<table>
<tr><th>SLPLDOx</th><th>LDOx Status in SLEEP mode</th></tr>
<tr><td>0</td><td>Shutdown</td></tr>
<tr><td>1</td><td>Operation</td></tr>
</table></td></tr>
<tr><td>A3</td><td>b7~b4</td><td>ONDC1 ~ONDC4</td><td>DCDC1, DCDC2, DCDC3 and DCDC4 Enable Signal.
<table>
<tr><th>ONDCx</th><th>DCDCx Status</th></tr>
<tr><td>0</td><td>Shutdown</td></tr>
<tr><td>1</td><td>Operation</td></tr>
</table></td></tr>
<tr><td>A4</td><td>b7~b1</td><td>ONLDO1 ~ONLDO7</td><td>LDO1 ~ LDO7 Enable Signal.
<table>
<tr><th>ONLDOx</th><th>LDOx Status</th></tr>
<tr><td>0</td><td>Shutdown</td></tr>
<tr><td>1</td><td>Operation</td></tr>
</table></td></tr>
<tr><td>A5</td><td>b7~b4</td><td>FPWM1 ~FPWM4</td><td>Setting the operating mode of DCDC1, DCDC2, DCDC3 and DCDC4
<table>
<tr><th>FPWMx</th><th>DCDCx Mode</th></tr>
<tr><td>0</td><td>PWM/PSM</td></tr>
<tr><td>1</td><td>PWM</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Byte Name</th><th>Data Bit</th><th>Data Name</th><th>Function Description</th></tr>
<tr><td>A5</td><td>b3~b0</td><td>ECO_DC1
~ECO_DC4</td><td>Enable low quiescent current operation of DCDC1, DCDC2, DCDC3 and DCDC4 in PSM.
<table>
<tr><td>ECO_DCx</td><td>Low I_Q</td></tr>
<tr><td>0</td><td>Disable</td></tr>
<tr><td>1</td><td>Enable</td></tr>
</table></td></tr>
<tr><td>A6</td><td>b7~b1</td><td>ECOLDO1
~ECOLDO7</td><td>Enable low quiescent current operation of LDO1~LDO7..
<table>
<tr><td>ECO_LDOx</td><td>Low I_Q</td></tr>
<tr><td>0</td><td>Disable</td></tr>
<tr><td>1</td><td>Enable</td></tr>
</table></td></tr>
<tr><td>A7
A8</td><td>b4~b0</td><td>FBDC1
[4:0]/
FBDC2
[4:0]</td><td>Setting the feedback reference voltage of DCDC1,and DCDC2. VO1/2=VFBx/0.8
<table>
<tr><td>FBDC1[4:0]</td><td>VFBx</td><td>VO1/VO2</td><td>FBDC1[4:0]</td><td>VFBx</td><td>VO1/VO2</td></tr>
<tr><td>11111</td><td>1.20V</td><td>1.500V</td><td>01111</td><td>0.88V</td><td>1.100V</td></tr>
<tr><td>11110</td><td>1.18V</td><td>1.475V</td><td>01110</td><td>0.86V</td><td>1.075V</td></tr>
<tr><td>11101</td><td>1.16V</td><td>1.450V</td><td>01101</td><td>0.84V</td><td>1.050V</td></tr>
<tr><td>11100</td><td>1.14V</td><td>1.425V</td><td>01100</td><td>0.82V</td><td>1.025V</td></tr>
<tr><td>11011</td><td>1.12V</td><td>1.400V</td><td>01011</td><td>0.80V</td><td>1.000V</td></tr>
<tr><td>11010</td><td>1.10V</td><td>1.375V</td><td>01010</td><td>0.78V</td><td>0.975V</td></tr>
<tr><td>11001</td><td>1.08V</td><td>1.350V</td><td>01001</td><td>0.76V</td><td>0.950V</td></tr>
<tr><td>11000</td><td>1.06V</td><td>1.325V</td><td>01000</td><td>0.74V</td><td>0.925V</td></tr>
<tr><td>10111</td><td>1.04V</td><td>1.300V</td><td>00111</td><td>0.72V</td><td>0.900V</td></tr>
<tr><td>10110</td><td>1.02V</td><td>1.275V</td><td>00110</td><td>0.70V</td><td>0.875V</td></tr>
<tr><td>10101</td><td>1.00V</td><td>1.250V</td><td>00101</td><td>0.68V</td><td>0.850V</td></tr>
<tr><td>10100</td><td>0.98V</td><td>1.225V</td><td>00100</td><td>0.66V</td><td>0.825V</td></tr>
<tr><td>10011</td><td>0.96V</td><td>1.200V</td><td>00011</td><td>0.64V</td><td>0.800V</td></tr>
<tr><td>10010</td><td>0.94V</td><td>1.175V</td><td>00010</td><td>0.62V</td><td>0.775V</td></tr>
<tr><td>10001</td><td>0.92V</td><td>1.150V</td><td>00001</td><td>0.60V</td><td>0.750V</td></tr>
<tr><td>10000</td><td>0.90V</td><td>1.125V</td><td>00000</td><td>0.60V</td><td>0.750V</td></tr>
</table></td></tr>
<tr><td>A9</td><td>b6~ b4</td><td>VODC3
[2:0]</td><td>Setting the output voltage of DCDC3
<table>
<tr><td>VODC3[2:0]</td><td>VO3</td><td>VODC3[2:0]</td><td>VO3</td></tr>
<tr><td>111</td><td>3.4V</td><td>011</td><td>3.1V</td></tr>
<tr><td>110</td><td>3.3V</td><td>010</td><td>3.0V</td></tr>
<tr><td>101</td><td>3.2V</td><td>001</td><td>2.9V</td></tr>
<tr><td>100</td><td>3.15V</td><td>000</td><td>2.8V</td></tr>
</table></td></tr>
<tr><td>A9</td><td>b3~ b0</td><td>VODC4
[3:0]</td><td>Setting the output voltage of DCDC4.
<table>
<tr><td>VODC4[3:0]]</td><td>VO4</td><td>VODC4[3:0]]</td><td>VO4</td><td>VODC4[3:0]]</td><td>VO4</td><td>VODC4[3:0]]</td><td>VO4</td></tr>
<tr><td>1111</td><td>1.90V</td><td>1011</td><td>1.70V</td><td>0111</td><td>1.35V</td><td>0011</td><td>1.15V</td></tr>
<tr><td>1110</td><td>1.85V</td><td>1010</td><td>1.50V</td><td>0110</td><td>1.30V</td><td>0010</td><td>1.10V</td></tr>
<tr><td>1101</td><td>1.80V</td><td>1001</td><td>1.45V</td><td>0101</td><td>1.25V</td><td>0001</td><td>1.05V</td></tr>
<tr><td>1100</td><td>1.75V</td><td>1000</td><td>1.40V</td><td>0100</td><td>1.20V</td><td>0000</td><td>1.00V</td></tr>
</table></td></tr>
<tr><td>A10
A11
A12</td><td>b6~b4</td><td>VOLDO1
[2:0]
/VOLDO3
[2:0]
/VOLDO5
[2:0]</td><td>Setting the output voltage of LDO1, LDO3, and LDO5
<table>
<tr><td>VOLDOx[2:0]</td><td>LDOx</td><td>VOLDOx[2:0]</td><td>LDOx</td></tr>
<tr><td>111</td><td>3.3V</td><td>011</td><td>1.8V</td></tr>
<tr><td>110</td><td>3.0V</td><td>010</td><td>1.5V</td></tr>
<tr><td>101</td><td>2.8V</td><td>001</td><td>1.2V</td></tr>
<tr><td>100</td><td>2.5V</td><td>000</td><td>1.0V</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Byte Name</th><th>Data Bit</th><th>Data Name</th><th>Function Description</th></tr>
<tr><td>A10
A11</td><td>b2~b0</td><td>VOLDO2
[2:0]
/VOLDO4
[2:0]</td><td>Setting the output voltage of LDO2, and LDO4
<table>
<tr><td>VOLDOx[2:0]</td><td>LDOx</td><td>VOLDOx[2:0]</td><td>LDOx</td></tr>
<tr><td>111</td><td>3.3V</td><td>011</td><td>1.8V</td></tr>
<tr><td>110</td><td>3.0V</td><td>010</td><td>1.5V</td></tr>
<tr><td>101</td><td>2.8V</td><td>001</td><td>1.2V</td></tr>
<tr><td>100</td><td>2.5V</td><td>000</td><td>1.0V</td></tr>
</table></td></tr>
<tr><td>A12</td><td>b4~ b0</td><td>VOLDO6
[1:0]
/VOLDO7
[1:0]</td><td>Setting the output voltage of LDO6, and LDO7
<table>
<tr><td>VOLDOx[1:0]</td><td>LDOx</td></tr>
<tr><td>11</td><td>1.3V</td></tr>
<tr><td>10</td><td>1.25V</td></tr>
<tr><td>01</td><td>1.2V</td></tr>
<tr><td>00</td><td>1.1V</td></tr>
</table></td></tr>
<tr><td>A13</td><td>b7,b6</td><td>TIME_IT
[1:0]</td><td>TIME_IT[1:0] is used to defined the PWRON falling-edge de-bouncing delay time $T_{dbPWRONF}$.
When PWRON is toggled low with duration longer than $T_{dbPWRONF}$, PMU enters power-on process and the register A15.PWRON_IT is 1’b1.
<table>
<tr><td>TIME_IT[1:0]</td><td>$T_{dbPWRONF}$</td></tr>
<tr><td>00</td><td>128mS</td></tr>
<tr><td>01</td><td>3.0S</td></tr>
<tr><td>10</td><td>3.5S</td></tr>
<tr><td>11</td><td>4.0S</td></tr>
</table></td></tr>
<tr><td>A13</td><td>b5,b4</td><td>TIME_LP
[1:0]</td><td>TIME_LP[1:0] is used to defined the PWRON long-press delay time $T_{dPWRONLP}$.
When PWRON is toggled low with duration longer than $T_{dPWRONLP}$, the register A15.PWRON_LP is 1’b1.
<table>
<tr><td>TIME_LP[1:0]</td><td>$T_{dPWRONLP}$</td></tr>
<tr><td>00</td><td>1.0S</td></tr>
<tr><td>01</td><td>1.5S</td></tr>
<tr><td>10</td><td>2.0S</td></tr>
<tr><td>11</td><td>2.5S</td></tr>
</table></td></tr>
<tr><td>A13</td><td>b3,b2</td><td>TIME_LPOFF
[1:0]</td><td>TIME_LPOFF[1:0] is used to defined the PWRON long-press delay time $T_{dPWRONLPOFF}$.
When PWRON is toggled low with duration longer than $T_{dPWRONLPOFF}$, PMU enters power-off process, and the register A15.PWRON_LPOFF is 1’b1. The function of PWRON long-press delay to turn off PMU can be inactive by writing 0 to the register A1.LPOFF.
<table>
<tr><td>TIME_LPOFF[1:0]</td><td>$T_{dPWRONLPOFF}$</td></tr>
<tr><td>00</td><td>6.0S</td></tr>
<tr><td>01</td><td>7.0S</td></tr>
<tr><td>10</td><td>8.0S</td></tr>
<tr><td>11</td><td>10.0S</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Byte Name</th><th>Data Bit</th><th>Data Name</th><th>Function Description</th></tr>
<tr><td>A14</td><td>b7</td><td>MASK_ IT</td><td>By writing 1’b1 to MASK_IT to disable asserting /INT low when the event of PWRON falling with duration longer than TdbPWRONF occurs.</td></tr>
<tr><td>A14</td><td>b5</td><td>MASK_ LP</td><td>By writing 1’b1 to MASK_LP to disable asserting /INT low when the event of PWRON falling with duration longer than TdPWRONLP occurs.</td></tr>
<tr><td>A14</td><td>b3</td><td>MASK_ LPOFF</td><td>By writing 1’b1 to MASK_LPOFF to disable asserting /INT low when the event of PWRON falling with duration longer than TdPWRONLPOFF occurs.</td></tr>
<tr><td>A14</td><td>b0</td><td>INT</td><td>INT is used to control the output status of /INT pin. When interrupt events happen, /INT pin goes low and the bit A15.INT is set to 1’b1. After Micro-processor write the bit to be 1’b0, /INT pin goes to high-Z state.<table><tr><td>INT</td><td>/INT Pin Status</td></tr><tr><td>0</td><td>Hi-Z</td></tr><tr><td>1</td><td>Low</td></tr></table></td></tr>
<tr><td>A15</td><td>b7</td><td>PWRON_IT</td><td>PWRON_IT is used to record the PWRON falling status. PWRON_IT is reset to 0 at each PWRON falling edge or VCC plug-in/out.<table><tr><td>PWRON_IT</td><td>$T>T_{dbPWRONF}$</td></tr><tr><td>0</td><td>NO</td></tr><tr><td>1</td><td>YES</td></tr></table></td></tr>
<tr><td>A15</td><td>b5</td><td>PWRON_LP</td><td>PWRON_LP is used to record the PWRON long press status. PWRON_LP is reset to 0 at each PWRON falling edge or VCC plug-in/out.<table><tr><td>PWRON_LP</td><td>$T>T_{dPWRONLP}$</td></tr><tr><td>0</td><td>NO</td></tr><tr><td>1</td><td>YES</td></tr></table></td></tr>
<tr><td>A15</td><td>b3</td><td>PWRON_ LPOFF</td><td>PWRON_LPOFF is used to record the PWRON long press status. PWRON_LPOFF is reset to 0 at each PWRON falling edge or VCC plug-in/out.<table><tr><td>PWRON_LPOFF</td><td>$T>T_{dPWRONLPOFF}$</td></tr><tr><td>0</td><td>NO</td></tr><tr><td>1</td><td>YES</td></tr></table></td></tr>
<tr><td>A16</td><td>b7~b5</td><td>VER[2:0]</td><td>VER[2:0] is the version code of G5851.</td></tr>
<tr><td>A17</td><td>b7~b0</td><td>TIMER[7:0]</td><td>Setting OSC_32K clock buffer delay Timer. T_{DLY_X32K}=(TIMER[7:0]-1)*7.6mS.</td></tr>
</table>

FUNCTION DESCRIPTION

PMU

The G5851 includes four DC/DC Converter, and seven LDO regulators to generate a multiple-output power-supply system.

	Topology	Default V_{OUT}	V_{OUT} range	Current rating	ON/OFF Control
DCDC1	3MHz Sync. Buck Converter	1.1V	32-steps DVS from 0.75v to 1.5v configured by I^2C	2.0A	Controlled by PWRON/PWRHOLD and individual register bit A3.ONDCx
DCDC2	3MHz Sync. Buck Converter	1.2V	32-steps DVS from 0.75v to 1.5v configured by I^2C	2.0A	
DCDC3	3MHz Sync. Buck Converter	3.2V	8-steps voltages from 2.8v to 3.4v configured by I^2C	2.0A	
DCDC4	3MHz Sync. Buck Converter	1.8V	16-steps voltages from 1.0v to 1.9v configured by I^2C	2.0A	
LDO1	pMOS LDO	1.8V	8-steps voltages from 1.0v to 3.3v configured by I^2C	300mA	Controlled by register bit A4.ONLDO1
LDO2	pMOS LDO	2.8V	8-steps voltages from 1.0v to 3.3v configured by I^2C	300mA	Controlled by ENLDO and individual register bit A4.ONLDOx
LDO3	pMOS LDO	2.5V	8-steps voltages from 1.0v to 3.3v configured by I^2C	300mA	
LDO4	pMOS LDO	2.8V	8-steps voltages from 1.0v to 3.3v configured by I^2C	300mA	Controlled by register bit A4.ONLDO4
LDO5	pMOS LDO	2.5V	8-steps voltages from 1.0v to 3.3v configured by I^2C	300mA	Controlled by ENLDO and individual register bit A4.ONLDOx
LDO6	nMOS LDO	1.2V	4-steps voltages from 1.1v to 1.3v configured by I^2C	300mA	
LDO7	nMOS LDO	1.2V	4-steps voltages from 1.1v to 1.3v configured by I^2C	300mA	
RTCLDO	pMOS LDO	3.0V	4-steps voltages from 1.8v to 3.0v configured by I^2C	50mA	Always On

PMU Power ON/OFF Initiation

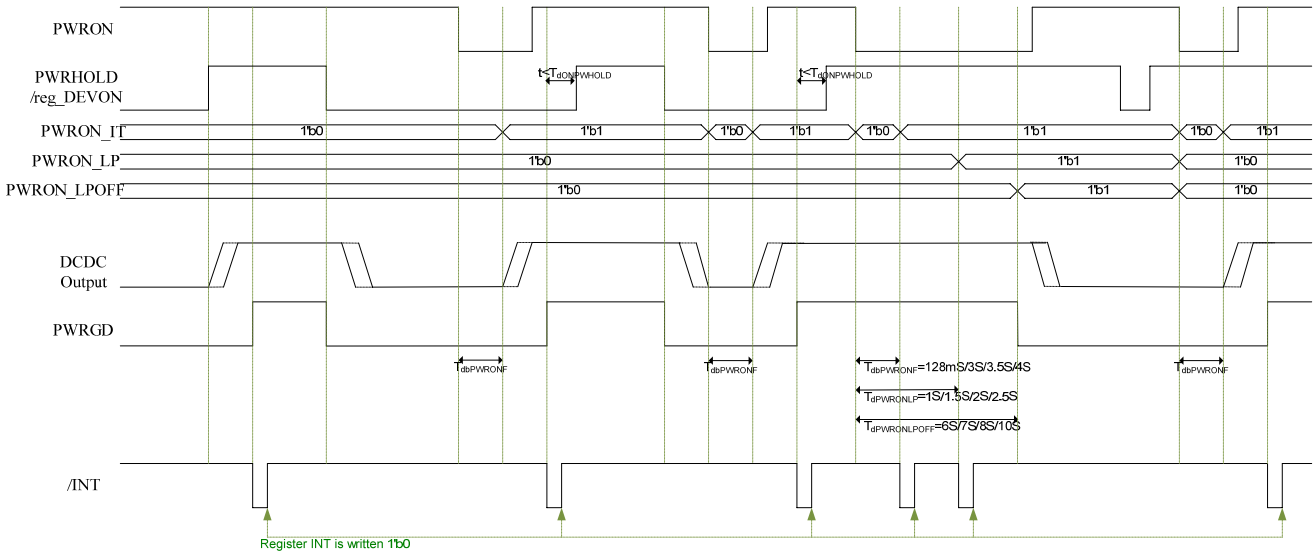
The following conditions are available to turn on the PMU of G5851:

- PWRON low-level pressed with duration longer than $T_{dbPWRONF}$
- Toggle PWRHOLD high-level or write 1 to register DEVON (when PWRON_LPOFF=1'b0)

When the PMU start-up process is initiated by the PWRON low-level pressed, the microprocessor needs pull high PWRHOLD pin or write 1 to register DEVON in 480mS delay from PWRGD rising edge. If no high-level signal is applied to PWRHOLD pin and register DEVON is 0 after 480mS from PWRGD rising edge, the PMU starts the power-off process and enters shutdown mode.

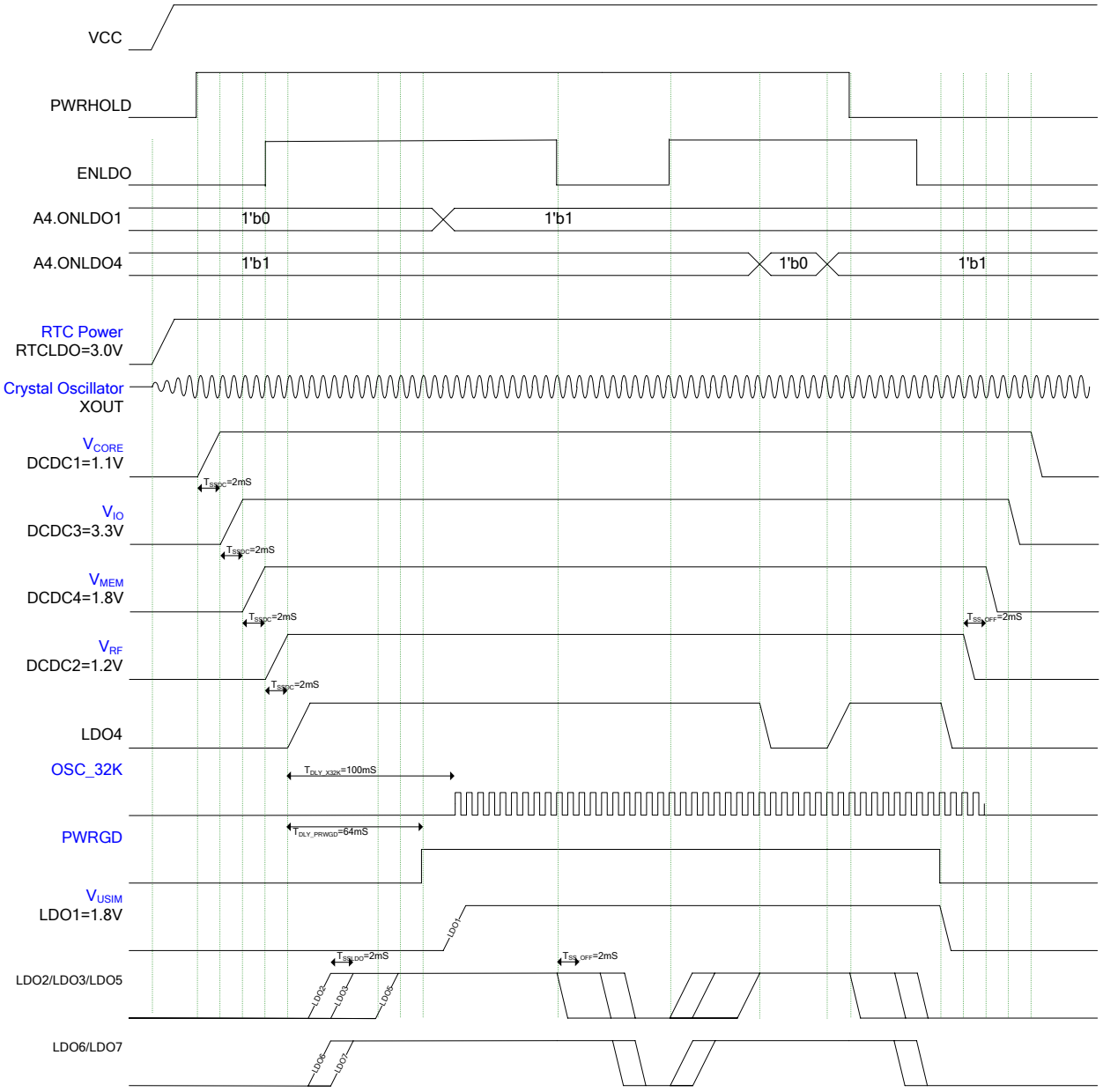
The following conditions are available to turn off the PMU of G5851:

- PWRON low-level pressed with duration longer than $T_{dPWRONLPOFF}$ (if LPOFF=1'b1)
- Toggle PWRHOLD low-level and write 0 to register DEVON after 480mS delay from the rising edge of PWRGD.
- Output voltage UVP of DCDC converters occurs with duration longer than 128mS
- G5851 thermal shutdown occurs.



PMU Power ON/OFF Sequence

When the power on condition is met, these four DC/DC converters, and LDO4 start up in sequence. After these four DC/DC converters finish power on sequence, the open-drain output PWRGD is high with T_{DLY_PWRGD}(100mS typ.) from LDO4 finishes power on. After LDO4 is power-on ready, microprocessor can toggle high to ENLDO pin to start up these LDOs except for LDO1. LDO1 only can start up by writing 1 to register bit ONLDO1 after PWRGD is high.



PMU Fault Protection

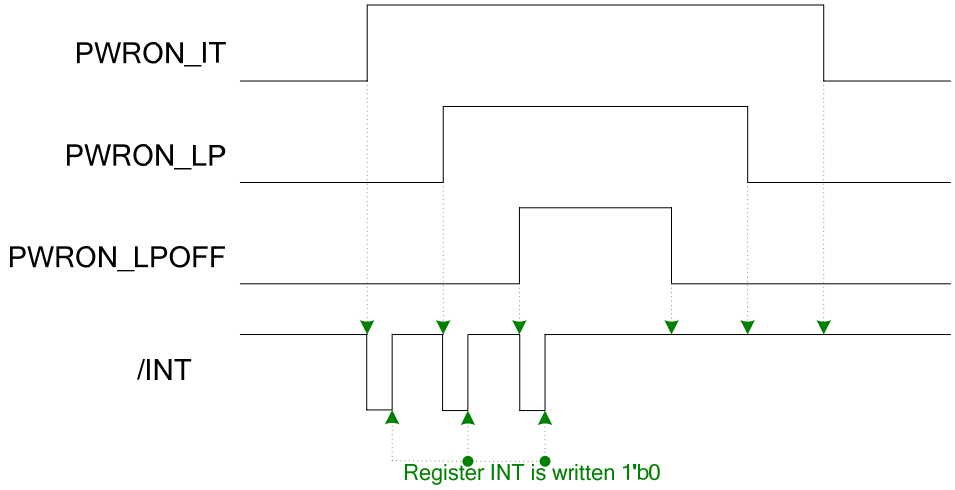
G5851 PMU provides VCC over voltage protection, over-current protection, under-voltage protection, short-circuit protection, and thermal shutdown protection to achieve complete protection.

	Protection type	Threshold	Protection methods	Reset Method
VCC	OVP	VCC>5.8V	IC shutdown	Reset by the power-on/off initiation conditions
DCDC1 Buck	Current Limit	PMOS current>2.5A	PMOS Off, NMOS on	Automatic Reset at next cycle
	UVP	VOUT1< $VOUT_{SET}$-100mV	IC shutdown if period above 128ms	Reset by the power- on/off initiation conditions
DCDC2 Buck	Current Limit	PMOS current>2.5A	PMOS Off, NMOS on	Automatic Reset at next cycle
	UVP	VOUT2< $VOUT_{SET}$-100mV	IC shutdown if period above 128ms	Reset by the power- on/off initiation conditions
DCDC3 Buck	Current Limit	PMOS current>2.5A	PMOS Off, NMOS on	Automatic Reset at next cycle
	UVP	VOUT3<75%*$VOUT_{SET}$	IC shutdown if period above 128ms	Reset by the power- on/off initiation conditions
DCDC4 Buck	Current Limit	PMOS current>2.5A	PMOS Off, NMOS on	Automatic Reset at next cycle
	UVP	VOUT4<90%*$VOUT_{SET}$	IC shutdown if period above 128ms	Reset by the power- on/off initiation conditions
RTCLDO	Current Limit	PMOS current>60mA		PMOS current<60mA
LDO1~LDO5 LDO	Current Limit	PMOS current>350mA		PMOS current<350mA
	UVP	VOUTX<12.5%*$VOUTX_{SET}$	PMOS Off	Reset by the power- on/off initiation conditions, toggle low to ENLDO, or I^2C ONLDO control
LDO6~LDO7 LDO	Current Limit	NMOS current>350mA		NMOS current<350mA
	UVP	VOUTX<12.5%*$VOUTX_{SET}$	NMOS Off	Reset by the power- on/off initiation conditions, toggle low to ENLDO, or I^2C ONLDO control
Thermal	TSD	Junction Temp. >150°C	IC shutdown	Reset by the power- on/off initiation conditions

/INT, Interrupt Signal

The G5851 indicates interrupt signal to external processor by /INT open-drain output. /INT is toggled low and INT bit is set to 1'b1 when these conditions shown below happen. After /INT is toggled low in these conditions, /INT is toggled high by written INT bit 1'b0 through I^2C interface.

/INT Toggle Low	When PMU turns on with event condition		During PMU On	
	No Event	Event Occurred	Event Appear	Event Disappear
PWRON falling-edge de-bouncing (PWRON_IT)	NO	YES	YES	NO
PWRON long press (PWRON_LP)	NO	YES	YES	NO
PWRON long press to turn off PMU (PWRON_LPOFF)	NO	YES	YES	NO



PCB layout guidelines

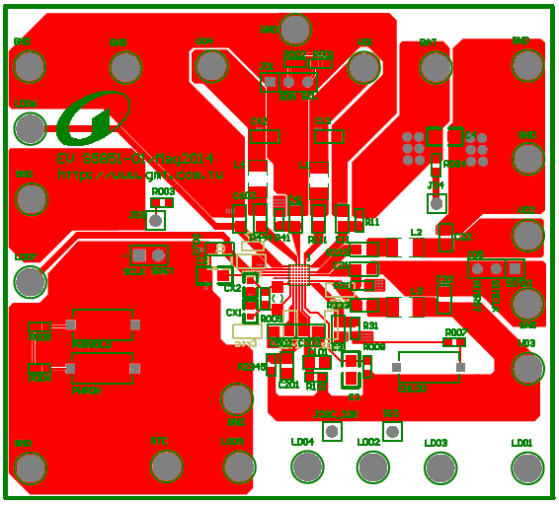
Careful printed circuit layout is extremely important to avoid causing parasitical capacitance and line inductance. The following layout guidelines are recommended to achieve optimum performance.

- Please the buck converter inductor close to the LX pin. Keep traces short, direct, and wide.
- Please ceramic bypass capacitors near the input/output pin.
- All feedback signal must first go through the regulator capacitors.
- Place the crystal and its components close to the oscillator side and the oscillator pins.
- Reduce the parasitic capacitance between XIN and XOUT signals by routing them as far apart as possible.
- Ensure that the ground plane under the oscillator and its components are of good quality.
- Avoid long connections to the crystal and to the load capacitor that create a large loop on the PCB.
- Do not route any digital-signal lines on the opposite side of the PCB under the crystal area.
- Keep other digital signal lines, especially clock lines and frequently switching signal lines, as far away from the crystal connections as possible. Crosstalk from digital signals may disturb the small-amplitude sine-shaped oscillator signal.

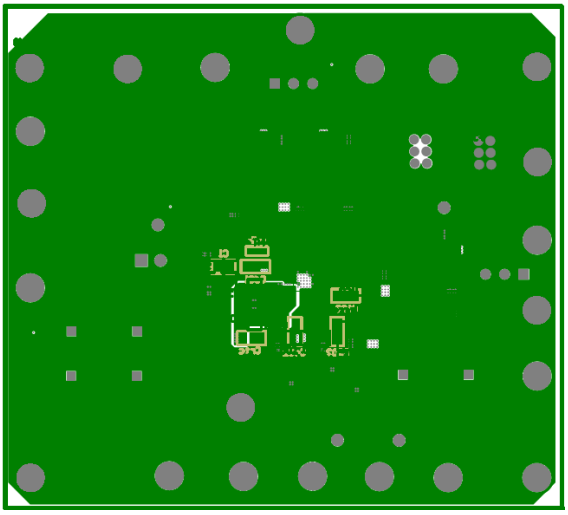
It is recommended to make use of the situation and add a ground guard ring around the crystal signals. And the section between crystal and the load capacitors is laid out symmetrically

EV Board PCB Layout Section

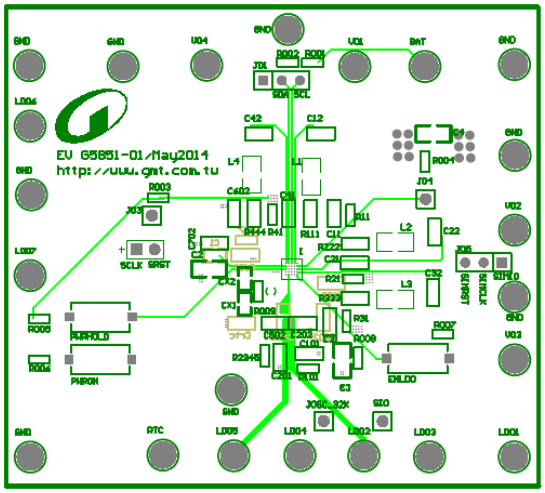
CSP-7X7-49 Top Side



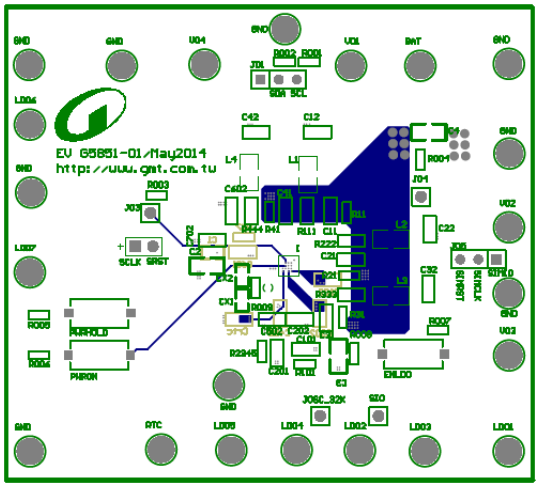
CSP-7X7-49 Mid-Layer 1



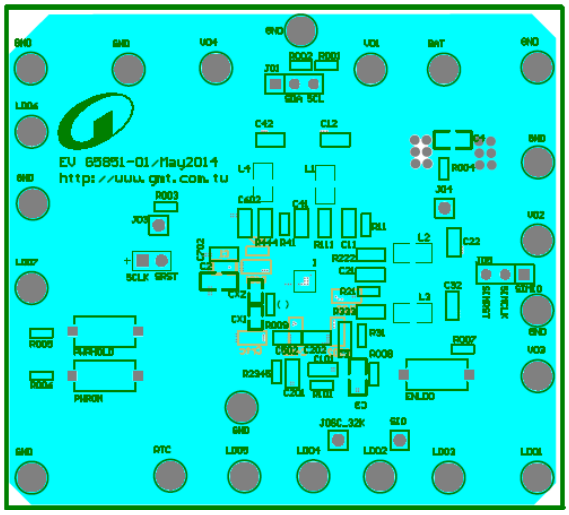
CSP-7X7-49 Mid-Layer 2



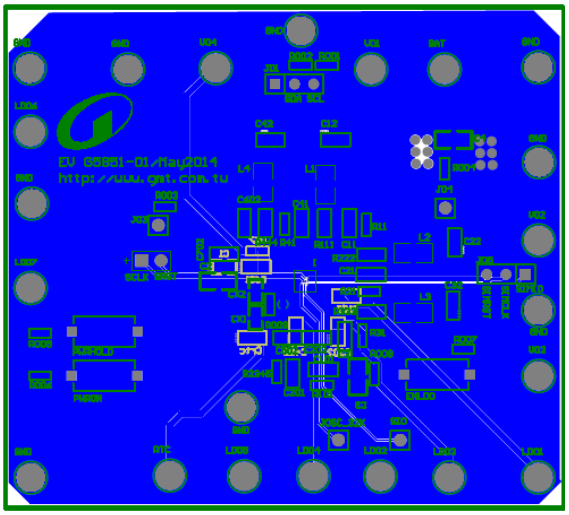
CSP-7X7-49 Mid-Layer 3



CSP-7X7-49 Mid-Layer 4

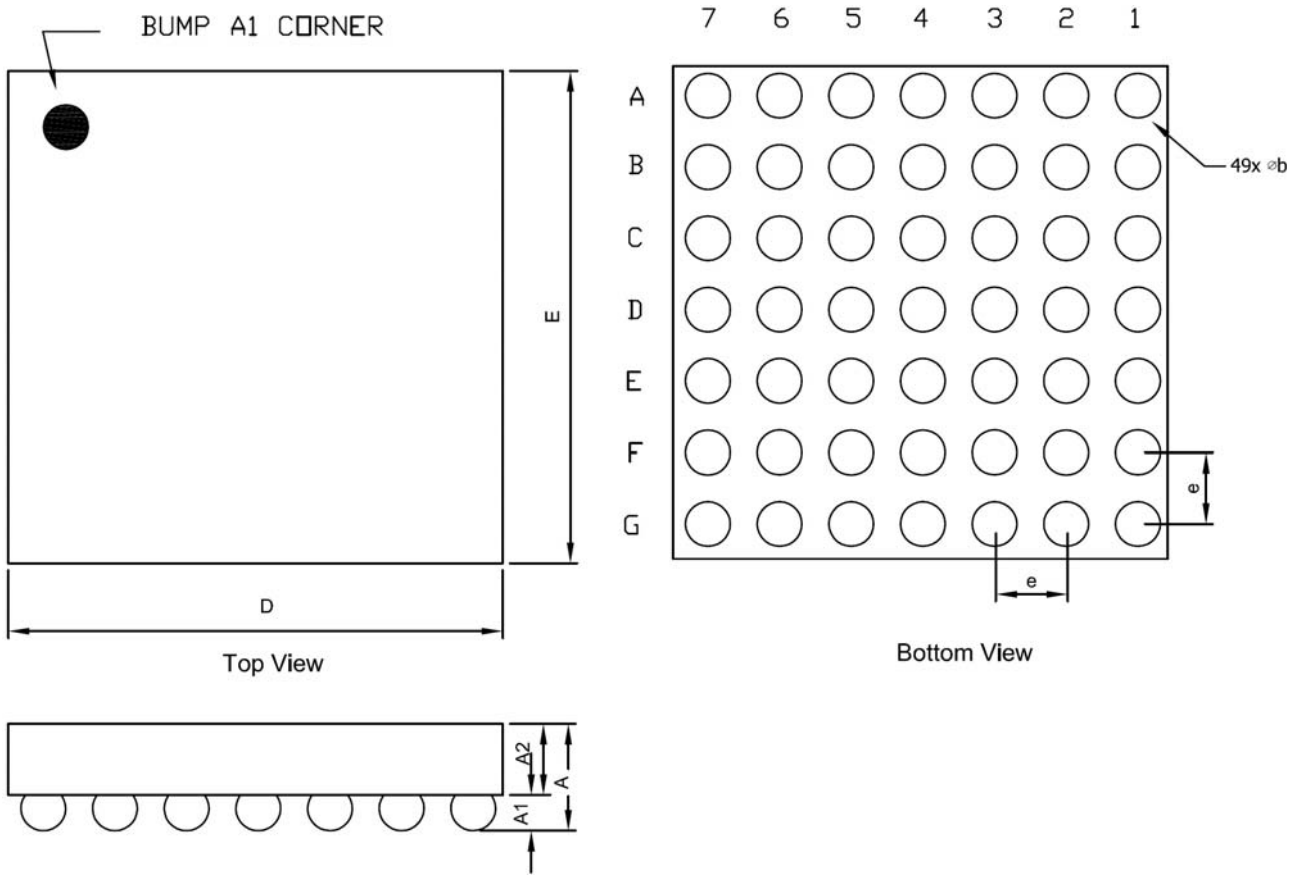


CSP-7X7-49 Bottom Side



EV5851 PCB	Information
Board Material	FR4
Size	75mm×65mm
Board Thickness	1.6mm
Layers	6
Copper Thickness	1 oz.

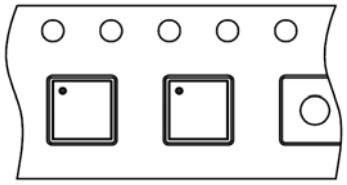
Package Information



WLCSP7X7-49 Package

Symble	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.540	0.600	0.660	0.0213	0.0236	0.0260
A1	0.170	0.200	0.230	0.0067	0.0079	0.0091
A2	0.370	0.400	0.430	0.0146	0.0157	0.0169
D	2.720	2.760	2.800	0.1070	0.1087	0.1102
E	2.720	2.760	2.800	0.1070	0.1087	0.1102
b	0.230	0.260	0.290	0.0091	0.0102	0.0114
e	0.40 BSC			0.0157 BSC		

Taping Specification



PACKAGE	Q'TY/REEL
WLCSP7X7-49	3,000 ea