Manual Reset IC with Adjustable Deglitch Time

Features

- **Manual Reset Input with Adjustable Manual Reset Deglitch Time**
- **Fully Specified Over Temperature**
- **Open-Drain $\overline{\text{RESET}}$ Output**
- **4μA Supply Current**
- **Guaranteed Reset Valid to V_{CC} = 2.2V**
- **Power Supply Transient Immunity**
- **ADFN1.5X1.5-6 Packages**

Applications

- **Computers**
- **Controllers**
- **Intelligent Instruments**
- **Critical μP and μC Power Monitoring**
- **Portable / Battery-Powered Equipment**

General Description

The G601 is a manual reset IC used in μP and digital systems. They provide excellent circuit reliability and low cost.

These circuits perform a single function: they assert a reset signal whenever manual reset is triggered. Manual reset is generated after pull low $\overline{\text{MR}}$ pin lastingly over deglitch time delay set by capacitor connected in MRDLY pin.

The G601 has an open-drain output stage. The open-drain $\overline{\text{RESET}}$ output requires a pull-up resistor that can be connected to a voltage higher than VCC. The reset comparator is designed to ignore fast transients on VCC, and the outputs are guaranteed to be in the correct logic state for VCC down to 2.2V.

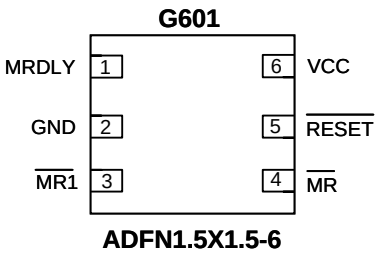
Low supply current makes the G601 ideal for use in portable equipment. The G601 is available in ADFN1.5X1.5-6 packages.

Ordering Information

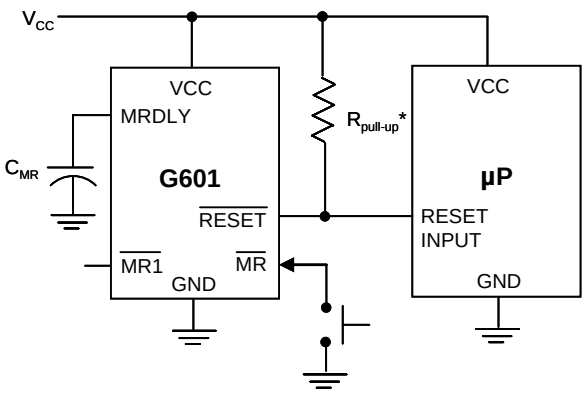
ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE (Green)
G601A31U	60 1x	-40°C ~ +105°C	ADFN1.5X1.5-6

Note: A3:ADFN1.5X1.5-6
1: Bonding Code
U: Tape & Reel

Pin Configuration



Typical Application Circuit



Absolute Maximum Ratings

Terminal Voltage (with respect to GND)
V_{CC}. . . . . ..-0.3V to +6.0V
MRDLY. . . . . .-0.3 to (V_{CC} +0.3V)
$\overline{RESET}$, $\overline{MR}$, $\overline{MR1}$ . . . . . -0.3V to +6.0V

Operating Temperature Range. . . . . .-40°C to +105°C
Storage Temperature Range. . . . . -65°C to +150°C
Reflow Temperature (soldering, 10sec) . . . . . .260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

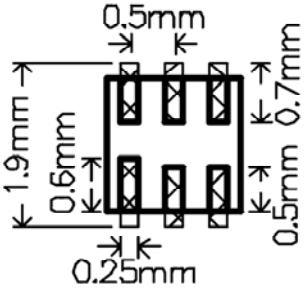
(V_{CC} = full range, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{CC} = 3.3V (Note 1)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
V_{CC} Range			2.2	---	5.5	V
Supply Current	I_{CC}	V_{CC}=3.3V	---	4	6	µA
MRDLY Pin Source Current	I_{MRDH}		0.5	1.1	1.6	µA
MRDLY Pin Sink Current	I_{MRDL}		0.5	1.1	1.6	
MRDLY Pin High Threshold Voltage	V_{MRDH}		---	833	---	mV
MRDLY Pin Low Threshold Voltage	V_{MRDL}		---	108	---	mV
$\overline{MR}$ Deglitch Time/Capacitor Ratio	R_{MRDLY}	$\overline{MR}$ Deglitch Time/MRDLY Capacitor	68	76	84	MΩ
$\overline{MR}$ / $\overline{MR1}$ Input High Threshold	V_{IH}		0.8V_{CC}	---	---	
$\overline{MR}$ / $\overline{MR1}$ Input Low Threshold	V_{IL}		---	---	0.5V_{CC}	
$\overline{MR}$ Pull-up Resistance	R_{MR}		63	70	77	kΩ
$\overline{MR1}$ Off Reverse Input Current	I_{REV}	V_{CC} = 0V, $\overline{MR1}$ =3.3V	---	---	1	µA
$\overline{RESET}$ Output Current Low	I_{OL}	V_{CC} = 3.3V, $V_{\overline{RESET}}$ = 0.5V	2.2	---	---	mA
$\overline{RESET}$ Open-Drain Output Leakage Current		$\overline{RESET}$ deasserted	---	---	1	µA

Note 1: Production testing done at T_A = +25°C; limits over temperature guaranteed by design.

Minimum Footprint PCB Layout Section

ADFN1.5X1.5-6



Pin Description

PIN	NAME	FUNCTION
1	MRDLY	External programmable manual reset deglitch time delay is set by the capacitor connected to MRDLY pin.
2	GND	Ground
3	$\overline{MR1}$	Manual reset input with reversed current protection. A logic low on $\overline{MR1}$ and lasting over deglitch time delay set by MRDLY pin triggers manual reset signal.
4	$\overline{MR}$	Manual reset input. A logic low on $\overline{MR}$ and lasting over deglitch time delay set by MRDLY pin triggers manual reset signal.
5	$\overline{RESET}$	$\overline{RESET}$ Output remains low while VCC is below the reset threshold or manual reset is triggered, and for delay time set by C_D after VCC rises above the reset threshold.
6	VCC	Supply Voltage.

Timing Diagram

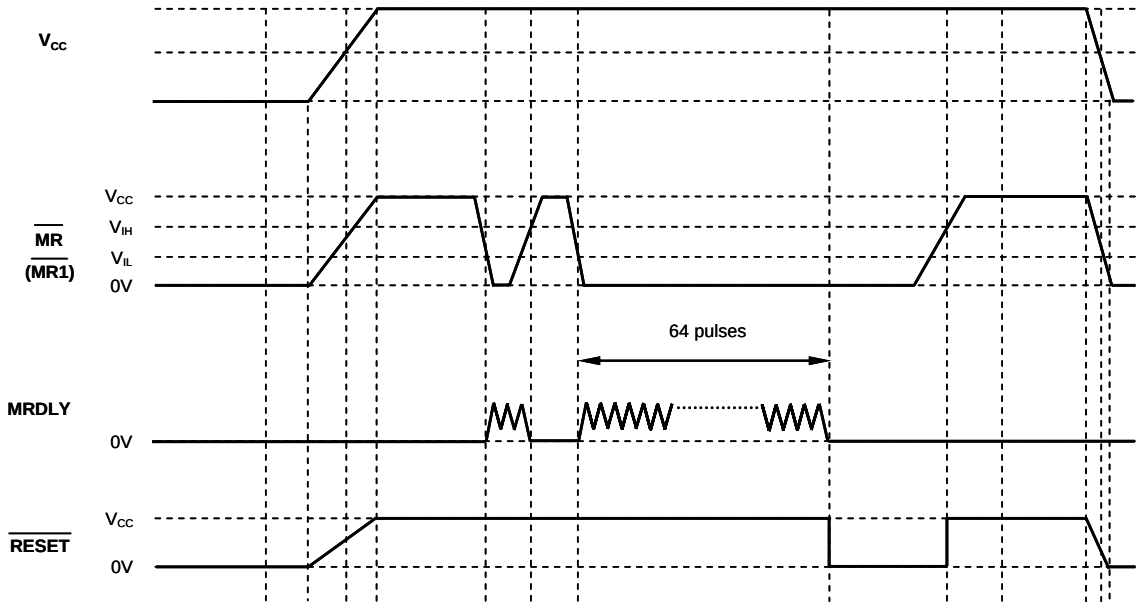


Figure 1

Functional Diagram

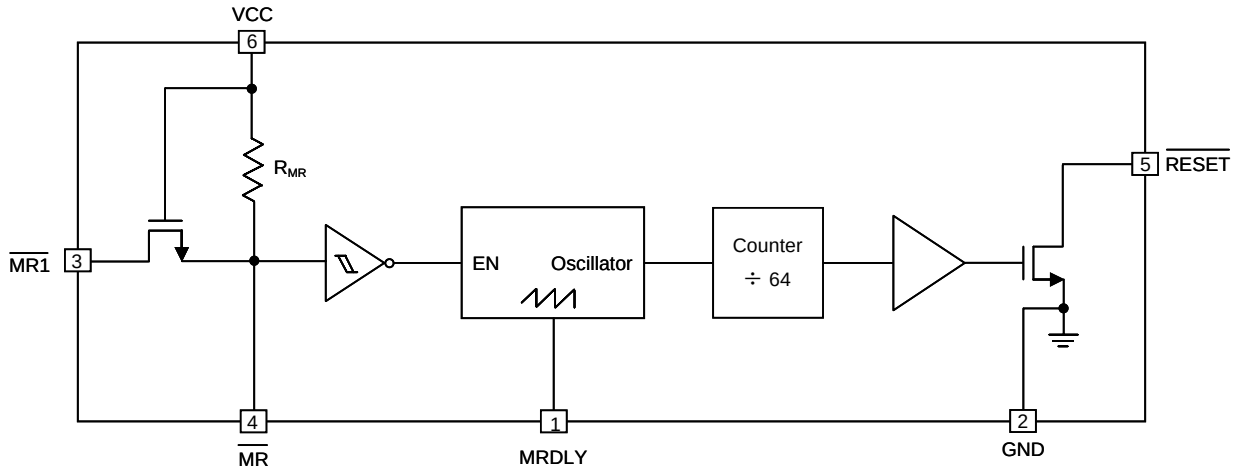


Figure 2

Detailed Description

A microprocessor's (µP's) reset input starts the µP in a known state. The G601 asserts a reset signal whenever the manual reset is triggered, keeping it asserted for a time after manual reset is released. The G601 uses an open-drain output. Connect a pull-up resistor on $\overline{\text{RESET}}$ output to any supply between 0 and 5.5V.

Manual reset is generated after pulling low $\overline{\text{MR}}$ or $\overline{\text{MR1}}$ pins over deglitch time delay set by capacitor connected to MRDLY pin. The formula of deglitch time is

$$T_{MR}(ms) \cong 76000 \times C_{MR}(\mu F)$$

After $\overline{\text{MR}}$ or $\overline{\text{MR1}}$ is release, $\overline{\text{RESET}}$ output goes high.

Fig1 and Fig2 show a timing diagram and a Functional Block.

Interfacing to µPs with Bidirectional Reset Pins

Since the $\overline{\text{RESET}}$ output on the G601 is open drain, this device interfaces easily with µPs that have bidirectional reset pins, such as the Motorola 68HC11. Connecting the $\overline{\text{RESET}}$ output directly to the microcontroller's (µC's) $\overline{\text{RESET}}$ input pin with a single pull-up resistor allows either device to assert reset (Figure 3).

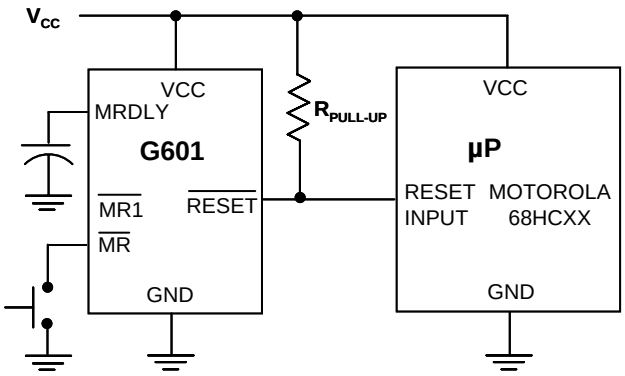


Figure 3. Interfacing to µPs with Bidirectional Reset I/O

Open-Drain $\overline{\text{RESET}}$ Output and $\overline{\text{MR1}}$ Input Allows Use with Multiple Supplies

Generally, the pull-up resistor of $\overline{\text{RESET}}$ is conneced to the V_{CC}. However, some systems may use the open-drain output to level-shift from the V_{CC} supply to reset circuitry powered by some other supply (Figure 4). The pull-up resistor of $\overline{\text{MR}}$ is connected to V_{CC}, basically. If the pull-up resistor is connected to different power supply that would be higher than V_{CC}, it would induce a leakage path from $\overline{\text{MR}}$ pin to V_{CC}. In such condition, $\overline{\text{MR1}}$ pin is recommended to prevent the reversed leakage current. $\overline{\text{MR1}}$ pin is with a level-shift from external supply to V_{CC}. And there will be no leakage path (Figure 5).

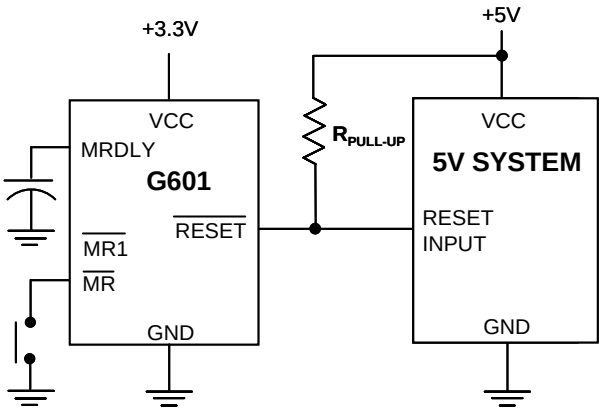


Figure 4. G601 Open-Drain $\overline{\text{RESET}}$ Output Allows use with Multiple Supplies

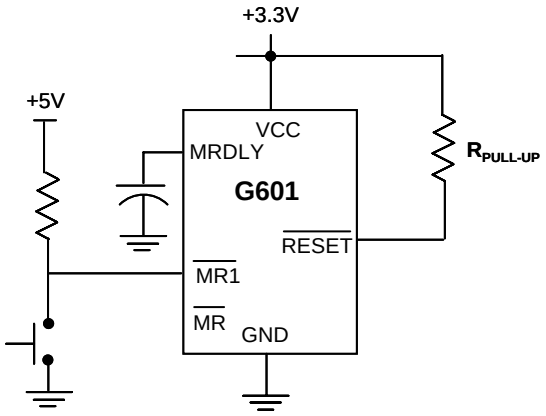
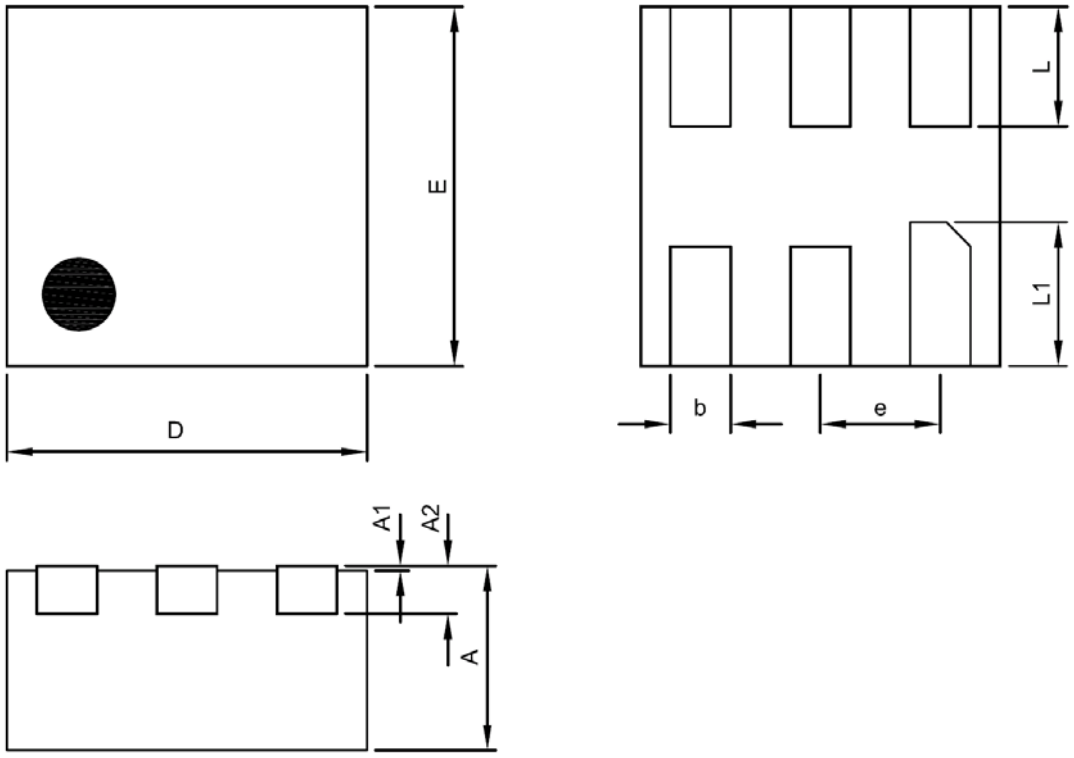


Figure 5. G601 $\overline{\text{MR1}}$ Input Allows use with Multiple Supplies

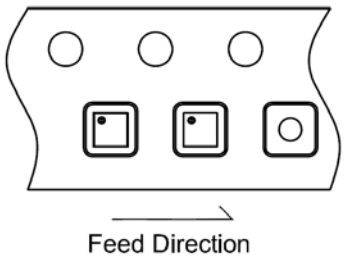
Package Information



ADFN1.5X1.5-6 Package

Symble	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.0276	0.0295	0.0315
A1	0.00	---	0.05	0.0000	---	0.0020
A2	0.10	0.11	0.12	0.0039	0.0043	0.0047
D	1.45	1.50	1.55	0.0570	0.0590	0.0610
E	1.45	1.50	1.55	0.0570	0.0590	0.0610
b	0.20	0.25	0.30	0.0079	0.0098	0.0118
e	0.50 BSC			0.0197 BSC		
L	0.45	0.50	0.55	0.0177	0.0197	0.0217
L1	0.55	0.60	0.65	0.0217	0.0236	0.0256

Taping Specification



PACKAGE	Q'TY/REEL
ADFN1.5X1.5-6	3,000 ea