DDR4 Memory Power Solution

Features

- *Synchronous Buck Converter (VBK1)*
  - Ultra-High Efficiency
  - Integrated 120mΩ at VCC=5V N-Channel MOSFET for Low Side
  - Integrated 150mΩ at VCC=5V P-Channel MOSFET for High Side
  - No Current-Sense Resistor (Lossless ILIMIT)
  - Quasi-PWM with 100ns Load-Step Response
  - Input Voltage Range: 3V to 5.5V
  - Output Voltage: VBK1=2.5V
  - Continual Output Current: 1A
  - Internal Softstart: 1ms
  - 580kHz Switching Frequency
  - Cycle-by-Cycle Overcurrent Protection
  - Latched Output OVP & UVP Protections
- *Synchronous Buck Converter (VBK2)*
  - Ultra-High Efficiency
  - Integrated 8.6mΩ at VCC=5V N-Channel MOSFET for Low Side
  - Integrated 22mΩ at VCC=5V N-Channel MOSFET for High Side
  - No Current-Sense Resistor (Lossless ILIMIT)
  - Quasi-PWM with 100ns Load-Step Response
  - 4.5V to 26V Battery Input Range
  - Output Voltage: VBK2=1.2V
  - Continual Output Current: 8A
  - Internal Softstart: 1.6ms
  - 600kHz Switching Frequency
  - Cycle-by-Cycle Overcurrent Protection
  - Latched Output OVP & UVP Protections
- *0.6V/1.5A LDO (VLDO)*
  - Output Voltage: VLDO=(1/2)*VBK2
  - Continual Output Current: 1.5A
  - Require Only 10μF of Ceramic Output Capacitance
  - ±30mV Accuracy for VLDO
  - Built-In Soft-Start to Reduce the VLDOIN Surging Current
  - Over Current Protection
  - Thermal Shutdown Protection
- *Buffered Reference (VLDOREF)*
  - Buffered, Low Noise, ±10mA Capability
  - 0.8% Output Accuracy
- *Low Quiescent Current:150μA*
- *Power Good Indicator*
- *Output Discharge Function*
- *Power Up and Power Down Sequencing Control*
- *Non-Latch for OT and UVLO protections*
- *18-pin 3mm x 3mm AQFN Package*

Applications

- Notebook Computers, PC Computers, and Servers
- Ultrabook, Tablet Computers
- Single-Board Computer, Industrial PC
- Distributed Power Systems

General Description

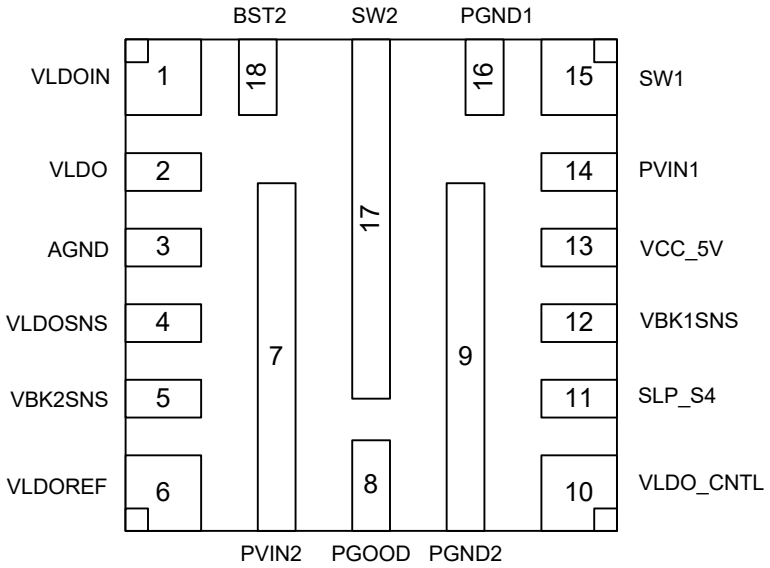
The G6020A is intended for DDR4 memory system.

Ordering Information

ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE (Green)
G6020AMC1D	6020A	-40°C to +85°C	AQFN3X3-18

Note: MC : AQFN3X3-18
1: Bonding Code
D : Tape & Reel
Green : Lead Free / Halogen Free

Pin Configuration



AQFN3x3-18

Absolute Maximum Ratings

PVIN2 to PGND2 . . . . . -0.3V to 26V
SW2 to PGND2. . . . . .-0.3V to 26V
<10ns . . . . . -3V to 28V
BST2 to PGND2. . . . . .-0.3V to 31V
SW2 to BST2. . . . . -6V to 0.3V
SW1 to PGND1 . . . . . -0.3V to 7V
<10ns. . . . . -3V to 8V
Continuous Power Dissipation (T_A = +25°C)*
AQFN3X3-18. . . . . 2.59W

Thermal Resistance Junction to Ambient, (θ_{JA})*
AQFN3X3-18 . . . . . 48.2°C/W
Thermal Resistance Junction to Case, (θ_{JC})
AQFN3X3-18 . . . . . 5.02°C/W
VLDO_CNTL, SLP_S4, VCC_5V, PVIN1, VLDOIN, VBK2SNS, VLDOSNS, VBK1SNS, PGOOD, VLDO, VLDOREF to AGND . . . . . -0.3V to 6V
Junction Temperature . . . . . -45°C to 150°C
Storage Temperature . . . . -55°C to 150°C
ESD (HBM) 2KV
ESD (CDM) 1KV

* Please refer to EV Board PCB Layout Section.

Electrical Characteristics

(PVIN=12V, PVIN_VBK1=5V, VCC_5V=5V, T_A=25°C)

The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply Voltage					
PVIN1 Input Voltage Range		3.0	---	5.5	V
PVIN2 Input Voltage Range		4.5	---	24	
VCC_5V Input Voltage Range		4.5	---	5.5	
VCC_5V Supply Current	V_{SLP_S4}=V_{VLDO_CNTL}=0V	---	5	5.6	µA
	V_{SLP_S4}=5V, V_{VLDO_CNTL}=0V, no load	---	110	165	
	V_{SLP_S4}=V_{VLDO_CNTL}=5V, no load	---	150	225	
UVLO					
VCC_5V Under-Voltage Lockout	Wake up VCC_5V voltage	---	4.1	4.5	V
	Shut down VCC_5V voltage	3.3	3.6	---	
	Hysteresis VCC_5V voltage	---	500	---	mV
VBK1 (Buck Converter)					
VBK1 Sense Voltage		2.45	2.5	2.55	V
VBK1SNS Input Current		---	20	---	µA
VBK1 Discharge Current	V_{SLP_S4}=V_{VLDO_CNTL}=0V, VBK1SNS=0.5V	---	12	---	mA
VBK1 Soft-Start Time		---	1	2	ms
High-Side Switch Resistance	T_J=25°C, PVIN=5V, VCC_5V=5V	---	150	---	mΩ
Low-Side Switch Resistance	T_J=25°C, PVIN=5V, VCC_5V=5V	---	120	---	
Current-Limit Threshold	V_{OUT}=2.5V, L=4.7µH	1.05	1.6	2.1	A
VBK1 Switching Frequency		---	580	---	kHz
Minimum OFF Time		---	195	---	ns
VBK2 (Synchronous Buck PWM Converter)					
VBK2 Sense Voltage		1.188	1.2	1.212	V
VBK2SNS Input Current	VBK2SNS=1.2V	---	40	---	µA
VBK2 Discharge Current	V_{SLP_S4}=V_{VLDO_CNTL}=0V, VBK2SNS=0.5V	---	12	---	mA
VBK2 Soft-Start Time		---	1.6	2.65	ms
VBK2 Ramp Up Delay Time		---	3	---	
High-Side Switch Resistance	T_J=25°C, PVIN=19V, VCC_5V=5V	---	22	---	mΩ
Low-Side Switch Resistance	T_J=25°C, PVIN=19V, VCC_5V=5V	---	8.6	---	
Current-Limit Threshold	V_{OUT}=1.2V, L=0.68µH	9.0	9.8	11.5	A
VBK2 Switching Frequency		---	600	---	kHz
Minimum OFF Time		---	198	---	ns

Electrical Characteristics (continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
PGOOD (VBK1, VBK2)					
PGOOD Threshold	VBK1SNS / VBK2SNS falling (Fault)	---	87	---	%
	VBK1SNS / VBK2SNS rising (Good)	---	93	---	
	VBK1SNS / VBK2SNS rising (Fault)	---	115	---	
	VBK1SNS / VBK2SNS falling (Good)	---	110	---	
PGOOD Sink Current	PGOOD=0.5V, V_{SLP_S4}=V_{VLDO_CNTL}=5V, no load	---	46	---	mA
PGOOD Start-UP Delay	PGOOD from low to high	---	1	---	ms
OVP AND UVP (VBK1, VBK2)					
OVP Threshold Voltage	OVP detect voltage	120	125	130	%
UVO Threshold Voltage	UVP detect voltage	55	60	65	
OVP Delay		---	20	---	µs
UVP Delay		---	250	---	
VLDO (LDO)					
Output Voltage		---	VLDOREF	---	V
Output Voltage Tolerance	T_J=25°C, $\|I_{VLDO}\|$ ≤ 10mA, VBK2SNS=1.2V, $I_{VLDOREF}$=0A	-20	---	20	mV
	T_J=25°C, $\|I_{VLDO}\|$ ≤ 1A, VBK2SNS=1.2V, $I_{VLDOREF}$=0A	-30	---	30	
Source Current Limit	VBK2SNS=1.2V, VLDO=VLDOSNS=0.5V, $I_{VLDOREF}$=0A	1.7	2.2	---	A
Sink Current Limit	VBK2SNS=1.2V, VLDO=VLDOSNS=0.7V, $I_{VLDOREF}$=0A	1.7	2.2	---	
VLDO Leak Current	T_J=25°C, V_{SLP_S4}=V_{VLDO_CNTL}=5V, VLDO=VLDOREF	---	---	5	µA
VLDOSNS Input Bias Current	V_{SLP_S4}=V_{VLDO_CNTL}=5V, VLDO=VLDOREF	-0.5	0	0.5	
VLDOSNS leakage Current	V_{SLP_S4}=5, V_{VLDO_CNTL}=0V, VLDO=VLDOREF	-1	0	1	
VLDO output Delay Relative to VLDO_CNTL		---	---	35	µs
VLDO Discharge Current	T_J=25°C, V_{SLP_S4}=V_{VLDO_CNTL}=0V, VBK2SNS=1.2V, VLDO=0.5V, $I_{VLDOREF}$=0A	---	5.7	---	mA
VLDOREF (Buffered Reference)					
Output Voltage		---	1/2* VBK2SNS	---	V
Output Voltage Tolerance to VBK2	T_J=25°C, $\|I_{VLDOREF}\|$ ≤ 100µA, VBK2SNS=1.2V	49.2	---	50.8	%
	T_J=25°C, $\|I_{VLDOREF}\|$ ≤ 10mA, VBK2SNS=1.2V	49	---	51	
Source Current Limit	VBK2SNS=1.2V, VLDOREF=0V	10	18	---	mA
Sink Current Limit	VBK2SNS=1.2V, VLDOREF=1.2V	10	18	---	
Discharge Current	T_J=25°C, V_{SLP_S4}=V_{VLDO_CNTL}=0V, VLDOREF=0.5V	0.8	1.3	---	mA
SLP_S4, VLDO_CNTL Logic Threshold					
SLP_S4/VLDO_CNTL High-Level Voltage	VIH	1.6	---	---	V
SLP_S4/VLDO_CNTL Low-Level Voltage	VIL	---	---	0.5	
SLP_S4/VLDO_CNTL Pull-Low Resistance		---	500	---	kΩ
Thermal Protection					
Thermal Shutdown		---	150	---	°C
Thermal Shutdown Hysteresis		---	20	---	

Pin Description

PIN	NAME	FUNCTION
1	VLDOIN	Power supply input for VLDO LDO. Connect VBK2 in typical application.
2	VLDO	VLDO 1.5A LDO output. Recommend to connect to 10μF or larger capacitance for stability.
3	AGND	Signal ground.
4	VLDOSNS	VLDO output voltage feedback.
5	VBK2SNS	VBK2 output voltage feedback.
6	VLDOREF	Buffered VLDO reference output. Recommend to connect to 0.22μF or larger capacitance for stability.
7	PVIN2	Input power supply for VBK2 buck.
8	PGOOD	Power good signal open-drain output. PGOOD goes high when VBK1 and VBK2 output voltage are within the target range.
9	PGND2	Power ground for VBK2 buck.
10	VLDO_CNTL	VLDO_CNTL signal input for VLDO LDO enable control. For detail control setup, please refer to Table 1.
11	SLP_S4	SLP_S4 signal input for VBK2 buck and VBK1 buck enable control. For detail control setup, please refer to Table 1.
12	VBK1SNS	VBK1 output voltage feedback.
13	VCC_5V	Power supply for VBK1 and VBK2 buck converter control logic circuit.
14	PVIN1	Input power supply for VBK1 buck.
15	SW1	VBK1 switching node connection to the inductor and bootstrap capacitor.
16	PGND1	Power ground for VBK1 buck.
17	SW2	VBK2 switching node connection to the inductor and bootstrap capacitor.
18	BST2	High-side MOSFET gate driver bootstrap voltage input for VBK2 buck. Connect a capacitor between the BST pin and the SW pin.

Minimum Footprint PCB Layout Section (unit: mm)

AQFN3X3-18

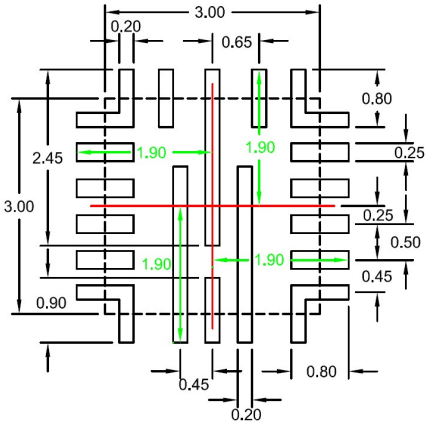


Table 1. VLDO_CNTL and SLP_S4 Control for Output State

State	VLDO_CNTL	SLP_S4	VBK1	VBK2	VLDOREF	VLDO
S0	HI	HI	ON	ON	ON	ON
S3	LO	HI	ON	ON	ON	OFF(High-Z)
S5/S4	LO	LO	OFF(discharge)	OFF(discharge)	OFF(discharge)	OFF(discharge)

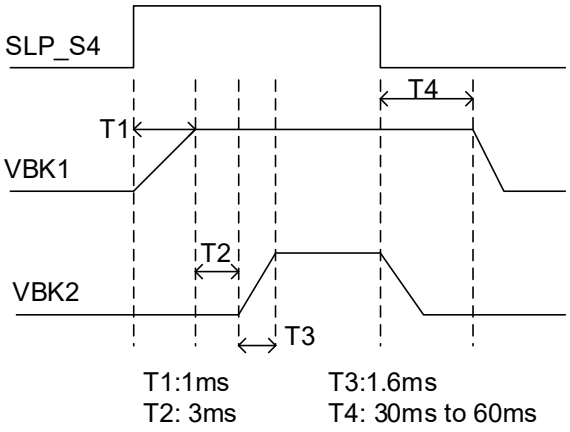


Figure 1. Power Sequence, VBK1 and VBK2 vs SLP_S4

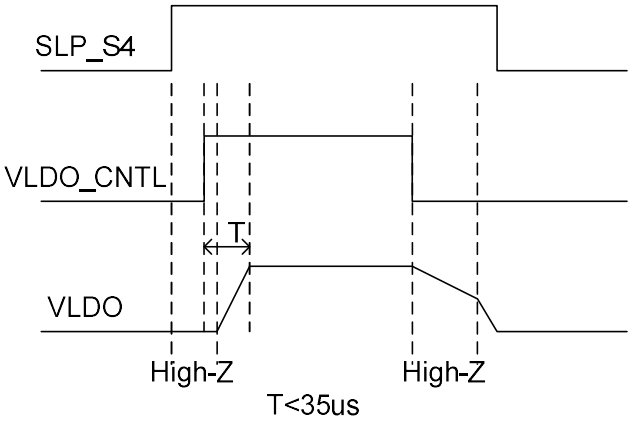


Figure 2. Power Sequence, VLDO vs VLDO_CNTL

Block Diagram

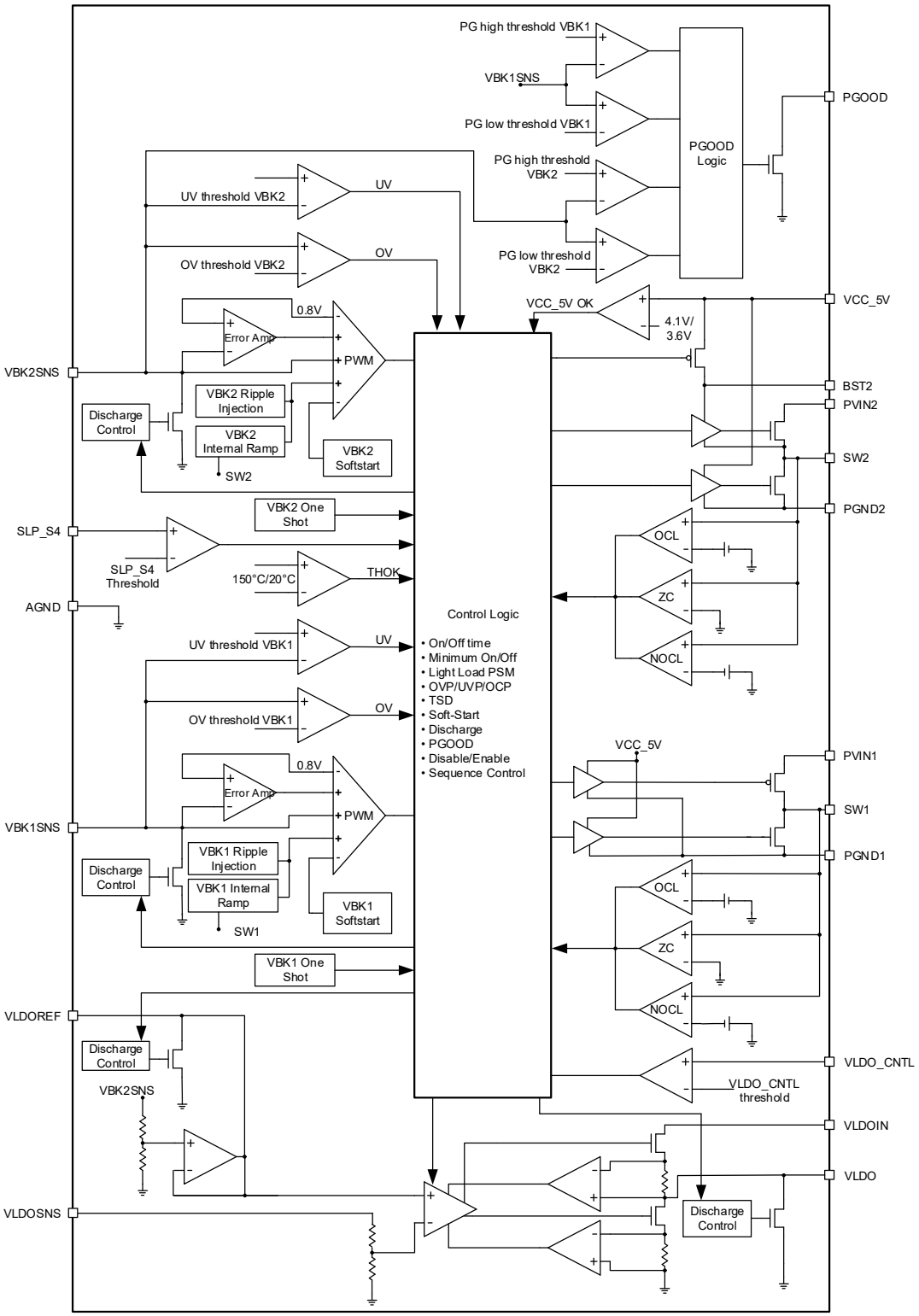


Table 2. Power Rails Name

DDR Technology	Power Rails			
	VBK1	VBK2	VLDO	VLDOREF
DDR4	VPP	VDDQ	VTT	VTTREF

Typical Application

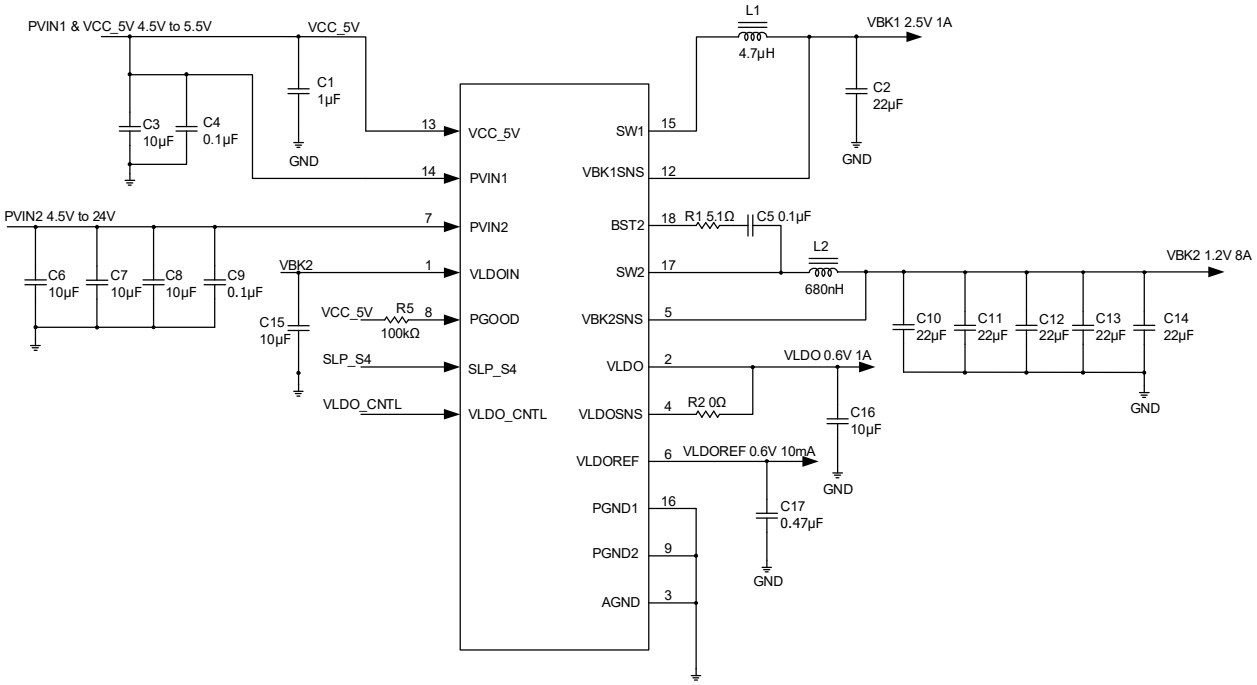
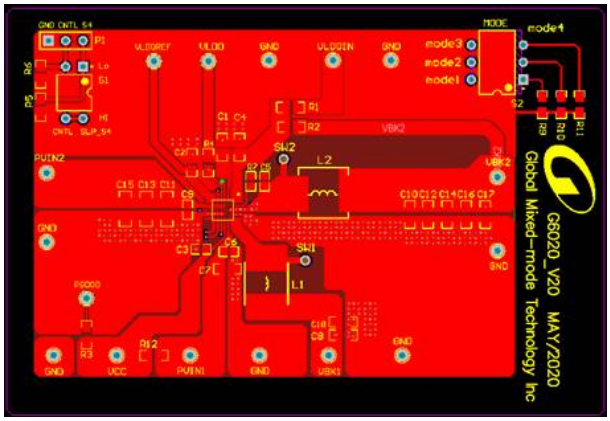


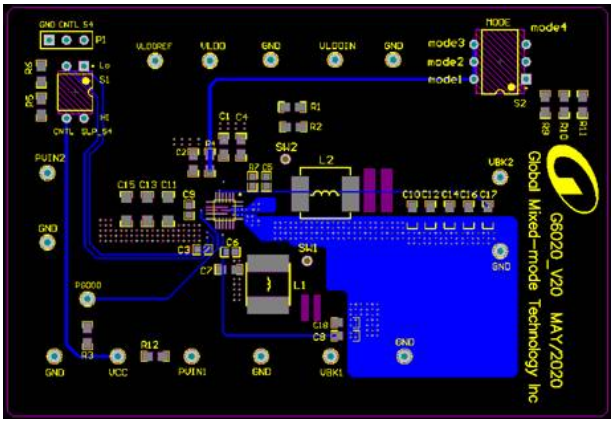
Figure 3. Application Schematic

EV Board PCB Layout Section

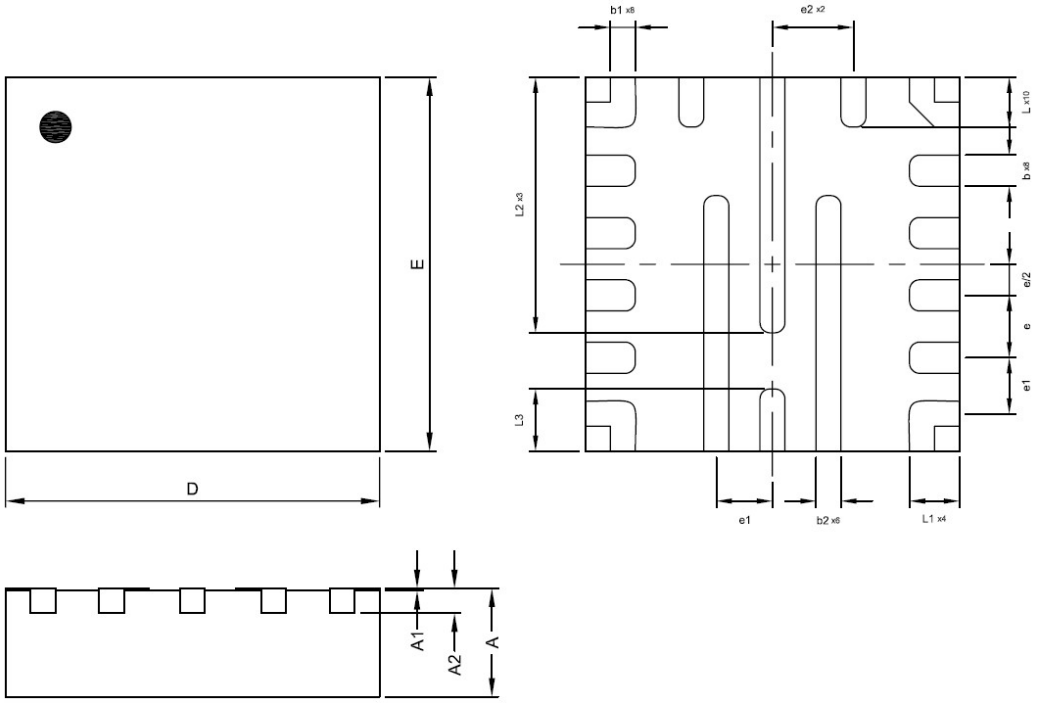
Top Layer



Bottom Layer



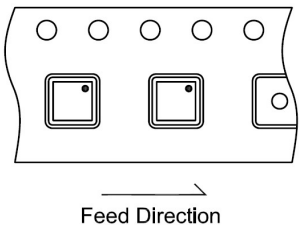
Package Information



AQFN3X3-18 Package

Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.90	1.00	0.0315	0.0354	0.0394
A1	0.00	- - -	0.05	0.0000	- - -	0.0020
A2	0.20 REF			0.0079 REF		
D	2.95	3.00	3.05	0.1161	0.1181	0.1201
E	2.95	3.00	3.05	0.1161	0.1181	0.1201
b	0.20	0.25	0.30	0.0079	0.0098	0.0118
b1	0.15	0.20	0.25	0.0059	0.0079	0.0098
b2	0.15	0.20	0.25	0.0059	0.0079	0.0098
e	0.50 BSC			0.0197 BSC		
e1	0.45 BSC			0.0177 BSC		
e2	0.65 BSC			0.0256 BSC		
L	0.35	0.40	0.45	0.0138	0.0157	0.0177
L1	0.35	0.40	0.45	0.0138	0.0157	0.0177
L2	2.00	2.05	2.10	0.0787	0.0807	0.0827
L3	0.45	0.50	0.55	0.0177	0.0197	0.0217

Taping Specification



PACKAGE	Q'TY/REEL
AQFN3X3-18	3,000 ea