Voltage Detector IC

Features

- **Internal Fixed Threshold**
- **High Accuracy ±2%**
- **Low Supply Current 16**μA
- **N-Channel Open-Drain Output**
- **Low Function Supply Voltage 2.4V**
- **Delay Time controlled by External Capacitor**
- **Used to multiple supplies application**
- **Fully Specified Over Temperature**

Applications

- **Computers**
- **Intelligent Instruments**
- **Portable/Battery-Powered Equipment**

General Description

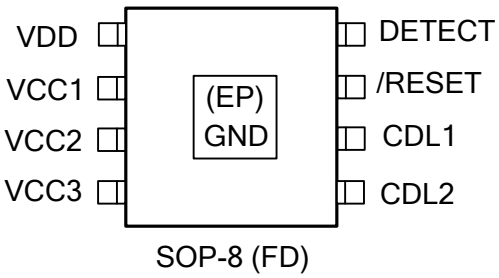
The G623A is a micro-power voltage detector IC used to monitor the multiple power supplies in microprocessor or logic system. It has high-accuracy, low current consumption and adjustable delay. It performs supervisory function by sending out a reset signal whenever the VDD voltage falls below a preset threshold level, and sending out another power detect signal whenever the VCC1, VCC2, or VCC3 power off. Once supplies recovered the threshold level, the reset and power detect signal will be released after a certain delay time controlled by external capacitor.

Ordering Information

ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE (Green)
G623AF11U	G623A	-40°C~ +125°C	SOP-8 (FD)

Note:: F1: SOP-8 (FD)
1: Bonding Code
U: Tape & Reel
Green : Lead Free / Halogen Free

Pin Configuration



SOP-8 (FD)

Absolute Maximum Ratings

VDD. . . . . .-0.3V to 6V
VCCx (VCC1, VCC2, VCC3) . . . . . .-0.3V to 6V
RESET . . . . . -0.3V to 6V
DETECT . . . . . -0.3V to 6V
CDL1 . . . . . -0.3V to 6V
CDL2 . . . . . -0.3V to 6V
Thermal Resistance Junction to Ambient, (θ_{JA})
SOP-8 (FD) . . . . . 75°C/W

Continuous Power Dissipation (T_A = +25°C)
SOP-8 (FD) . . . . .1.33°W
ESD susceptibility
HBM (Human Body Mode) 2kV
Operating Ambient Temperature. . . . .-40°C to125°C
Storage Temperature Range . . . . . .-55°C to +150°C
Reflow Temperature (soldering, 10 sec) . . . . . 260°C

1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. The device is ESD sensitive. Handling precaution recommended. The Human Body model is a 100pF capacitor discharged through a 1.5KΩ resistor into each pin.

Electrical characteristics

(Unless Otherwise Specified T_A=-25 to 125°C)

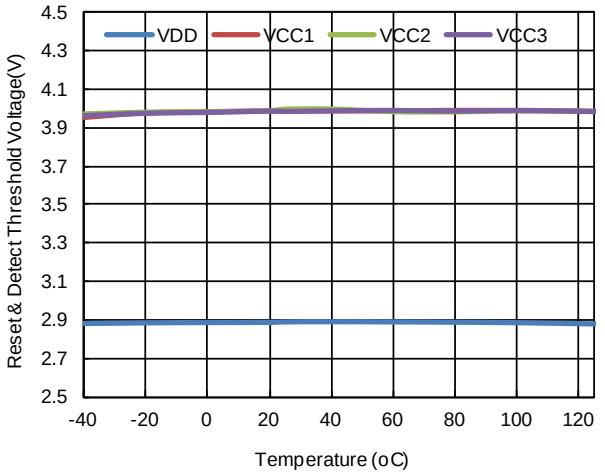
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
VDD Reset Threshold	V_{TH1}	VDD=H->L,T_A=25°C, RL=470kΩ	2.842	2.9	2.958	V
VCCx Power Detect Threshold	V_{TH2}	VCCx=H->L,T_A=25°C, RL=470kΩ	3.92	4	4.08	V
Operating Voltage Range	VOPL	Power supply VDD, VCCx	2.4	---	6	V
Supply Current when ON	I_{DD1}	VDD= V_{TH1}-0.2V=2.7V, VCCx= V_{TH2}-0.2V=3.8V	---	20	30	μA
Supply Current when OFF	I_{DD2}	VDD= V_{TH1}+2V=4.9V, VCCx= V_{TH2}+2V=6V	---	16	25	μA
RESET Output Voltage Low	$V_{RESETL\_}$	VDD=2.4V, I_{SINK}=3.6mA	---	---	0.2	V
DETECT Output Voltage Low	$V_{DETECTL\_}$	VCCx=3.7V, VDD=2.4V, I_{SINK}=3.6mA	---	---	0.2	V
V_{TH1} Hysteresis Voltage	ΔV_{HYS1}	T_A=-40 to 125°C, RL=470kΩ	0.03* V_{TH1}	0.045* V_{TH1}	0.06* V_{TH1}	V
V_{TH2} Hysteresis Voltage	ΔV_{HYS2}	T_A=-40 to 125°C, RL=470kΩ	0.03* V_{TH2}	0.045* V_{TH2}	0.06* V_{TH2}	V
RESET Output Delay Resistor	RDL1	VDD=V_{TH1}×1.1,VCDL1=0.5V, T_A=25°C	9	10	12	MΩ
DETECT Output Delay Resistor	RDL2	VCCx=V_{TH2}×1.1,VCDL2=0.5V,, T_A=25°C	10	12	15	MΩ
CDL1 pin Threshold Voltage	VCTH1	VDD=V_{TH1}×1.1,T_A=25°C, RL=470kΩ	VDD× 0.42	---	VDD ×0.65	V
CDL2 pin Threshold Voltage	VCTH2	VCCx=V_{TH2}×1.1,T_A=25°C, RL=470kΩ, VDD=V_{TH1}×1.1	VDD ×0.42	---	VDD ×0.65	V
CDL1 pin Output Discharge Current	ICDL1	VCDL1=0.1V,VDD=1V	20	400	800	μA
CDL2 pin Output Discharge Current	ICDL2	VCDL2=0.1V,VDD=1V	20	400	800	μA
RESET propagation delay time	T_{LH1}	CDL1 pin floating	50	70	200	μs
DETECT propagation delay time	T_{LH2}	CDL2 pin floating	50	70	200	μs
RESET Leak Current when OFF	Ileak1	VDS=6.5V, T_A=-40 to 85°C	---	---	0.1	μA
		VDS=6.5V, T_A=85 to 125°C	---	---	1	μA
DETECT Leak Current when OFF	Ileak2	VDS=6.5V, T_A=-40 to 85°C	---	---	0.1	μA
		VDS=6.5V, T_A=85 to 125°C	---	---	1	μA

Note 1: Production testing done at T_A=25°C, limits over temperature guaranteed by design.
RL: Pull-up resistor

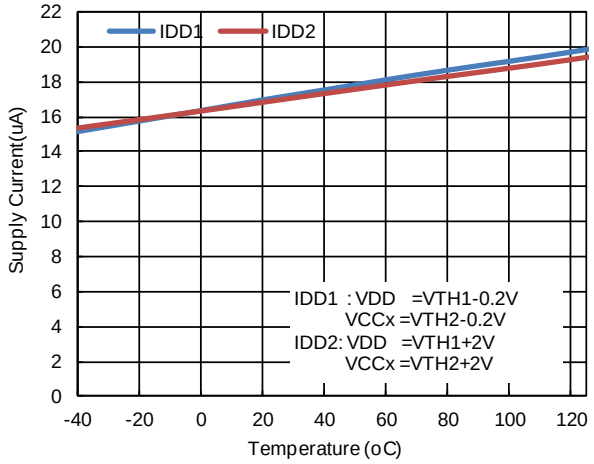
Typical Performance Characteristics

(T_A=25°C, unless otherwise specified)

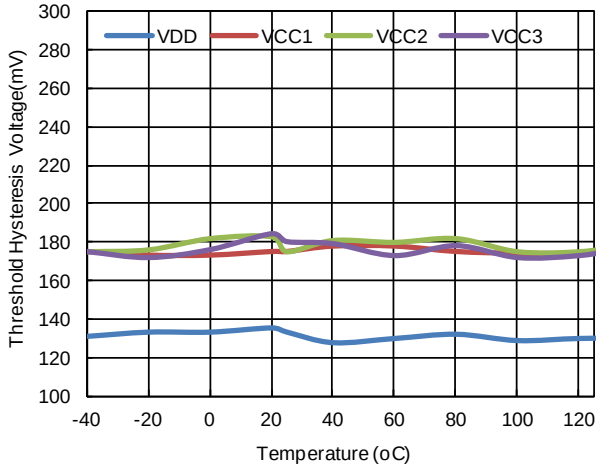
Reset & Detect Threshold Voltage vs. Temperature



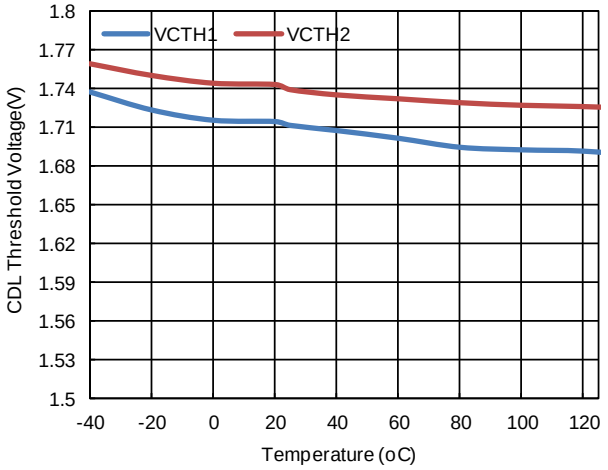
Supply Current vs. Temperature



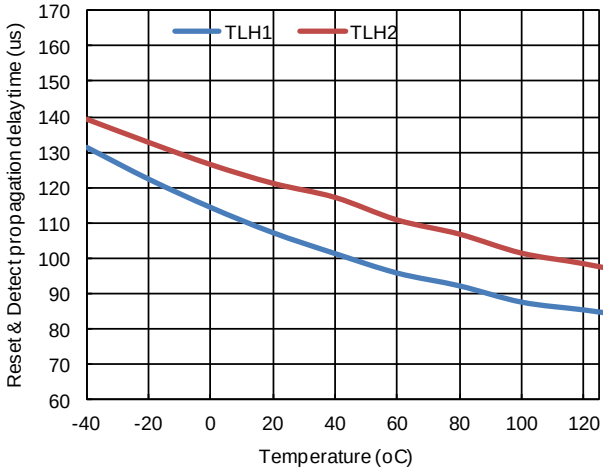
VTH Hysteresis Voltage vs. Temperature



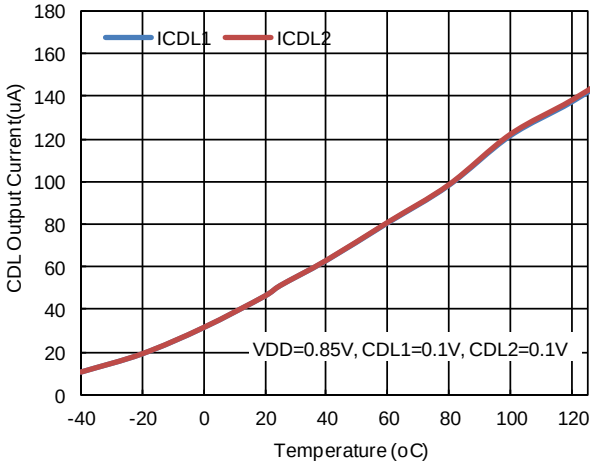
CDL Threshold Voltage vs. Temperature



Reset & Detect propagation delay time vs. Temperature



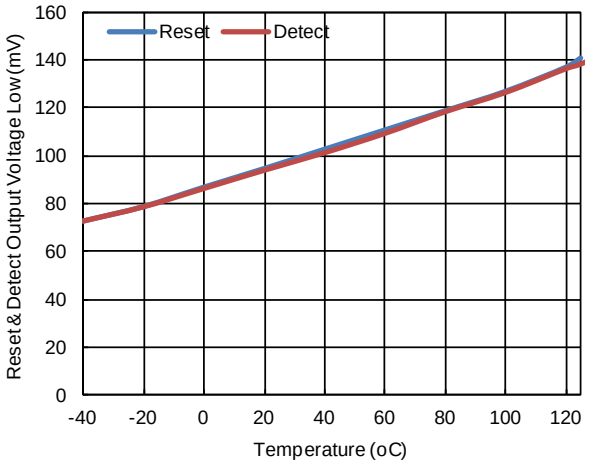
CDL Output Current vs. Temperature



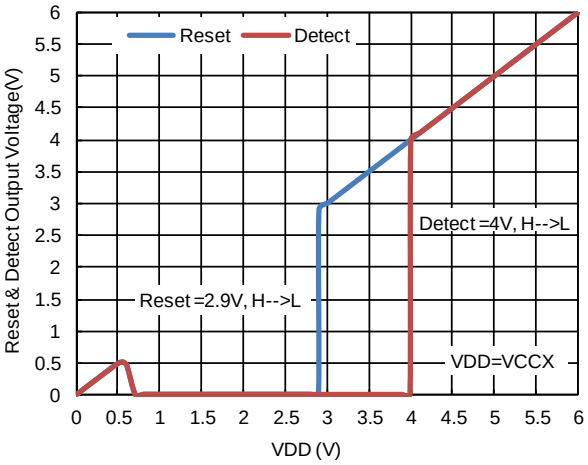
Typical Performance Characteristics

(T_A=25°C, unless otherwise specified)

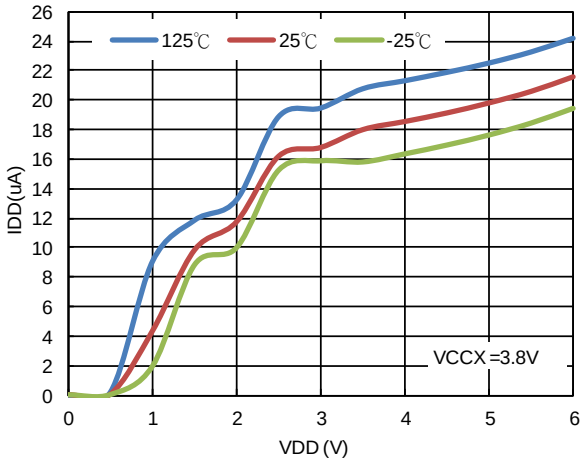
Reset & Detect Output Voltage Low vs.Temperature



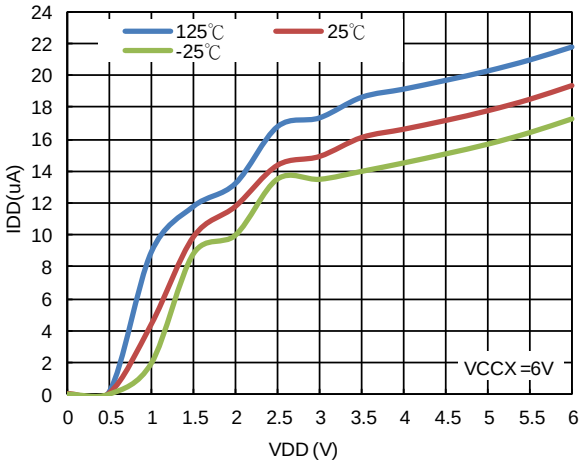
Reset & Detect Output Voltage vs. VDD



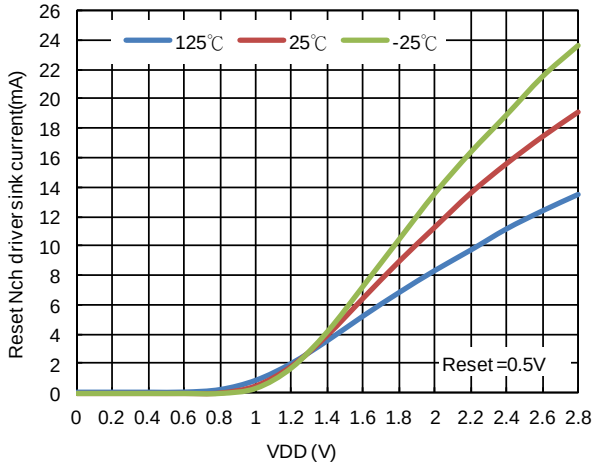
IDD vs. VDD



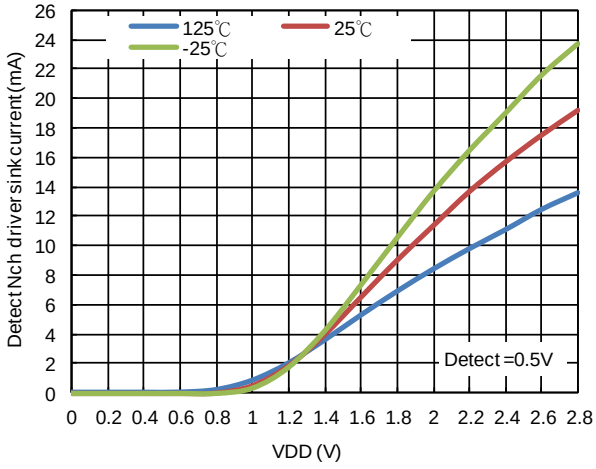
IDD vs. VDD



Reset Nch driver sink current vs. VDD



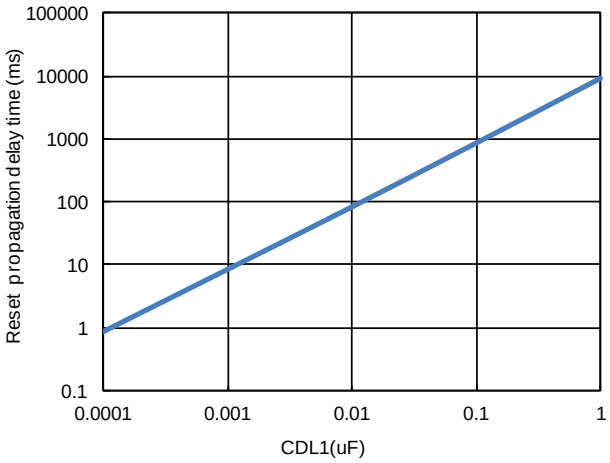
Detect Nch driver sink current vs. VDD



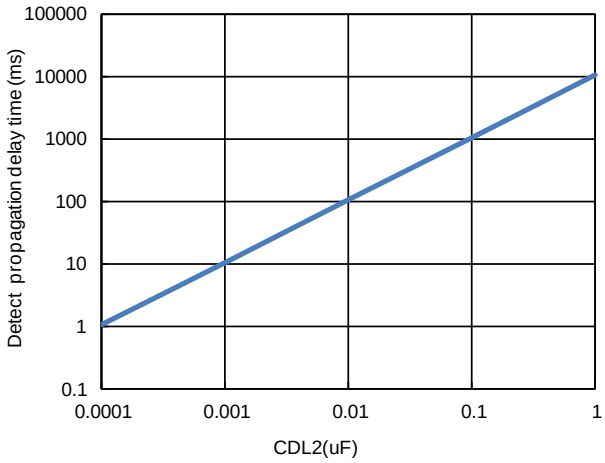
Typical Performance Characteristics

(T_A=25°C, unless otherwise specified)

Reset propagation delay time vs. CDL1



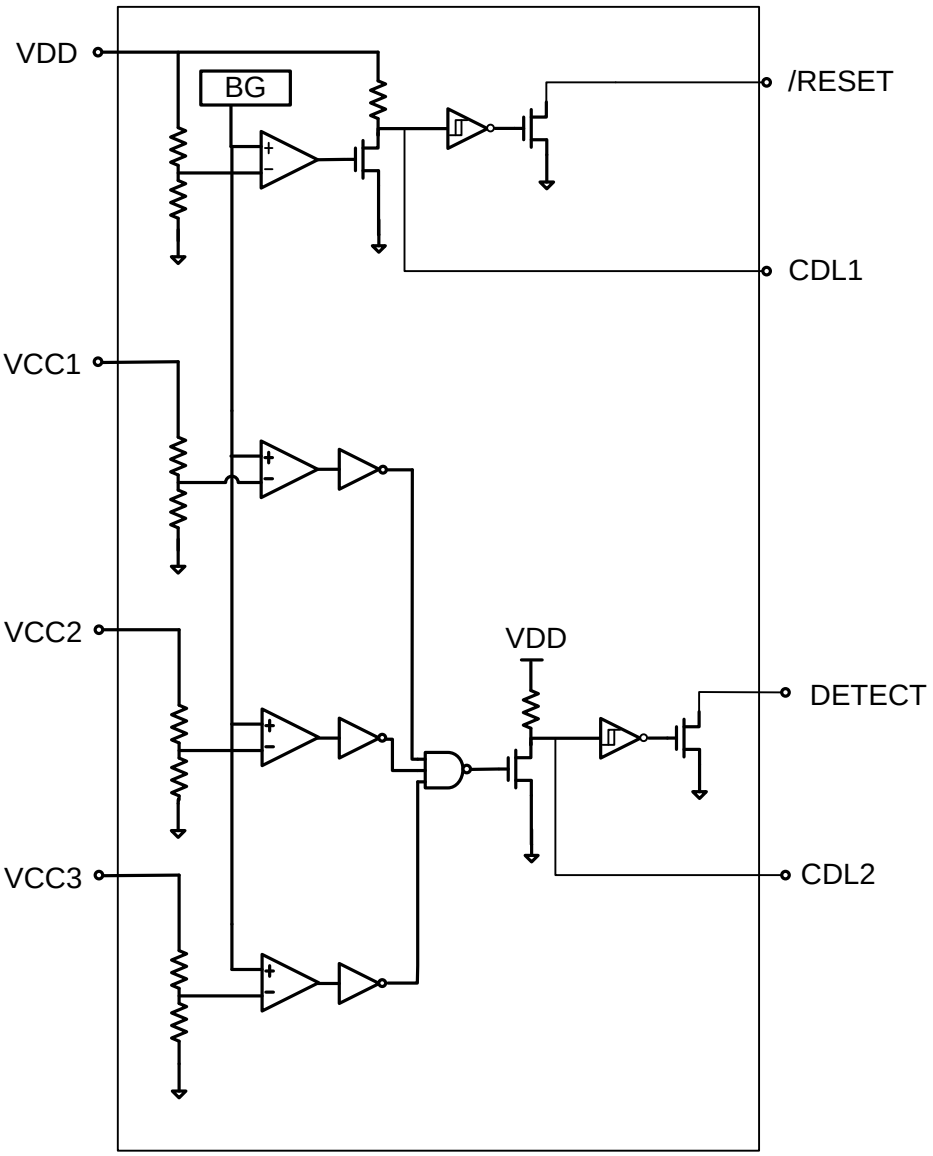
Detect propagation delay time vs. CDL2



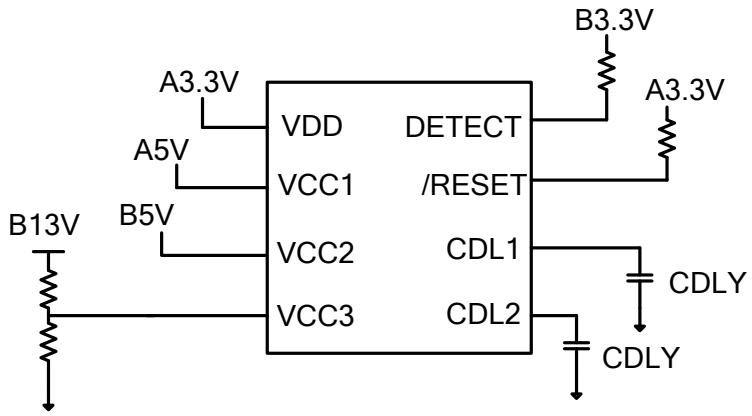
Pin Descriptions

PIN NUMBER	NAME	FUNCTION
1	VDD	Power Pin
2	VCC1	Power Pin
3	VCC2	Power Pin
4	VCC3	Power Pin
5	CDL2	External capacitor connection to set delay time
6	CDL1	External capacitor connection to set delay time
7	/RESET	Active Low Open-Drain
8	DETECT	Power detect output
EP	GND	Ground.

Block Diagram



Typical Application Circuit



When power pin VDD reaches threshold voltage (0.9*VDD) from high to low, /RESET pin goes low from high. When any power pin VCC1, VCC2, and VCC3 ramp down over the threshold voltage (0.8*VCCx), DETECT pin goes low from high. This circuit can set delay time controlled by the external capacitor at the rise of power pin.

$$T_{LH} = CT \times RCT \times \ln\left(\frac{VDD}{VDD - VCTH}\right)$$

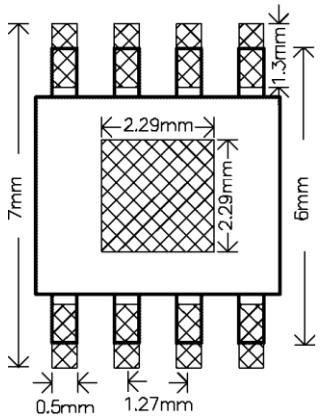
T_{LH} : time until the voltage of CDL pin rises to 0.5*VDD after VDD rises up and beyond the release voltage
CT: CDL pin external capacitor CDLY
RCT: CDL pin internal impedance

Open drain type need pull-up resistor connected to VDD or other power supply.

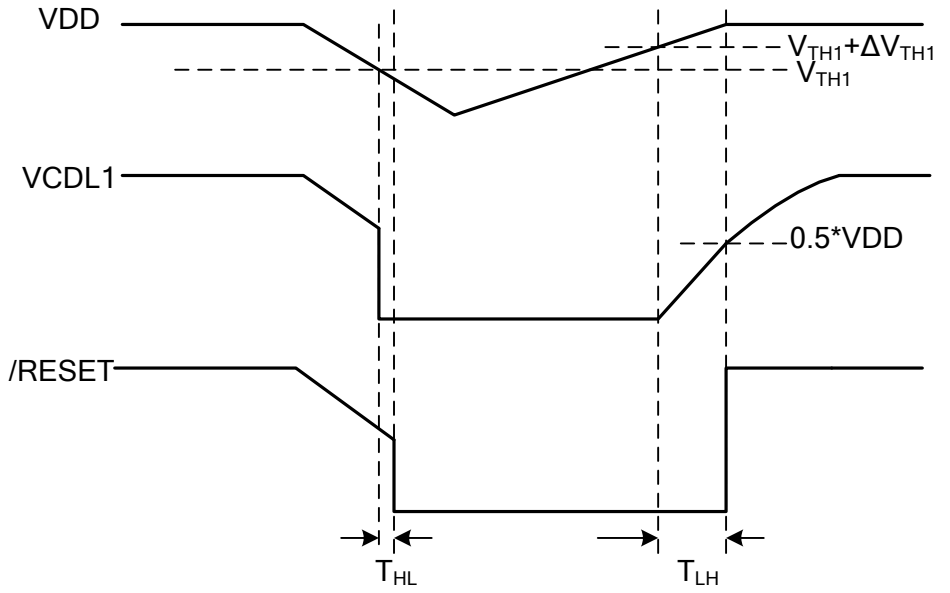
Because the resistor connected inside VCC3 pin is about 20MΩ, suggest that the low side resistor of external resistor divider is smaller than 20kΩ for accuracy.

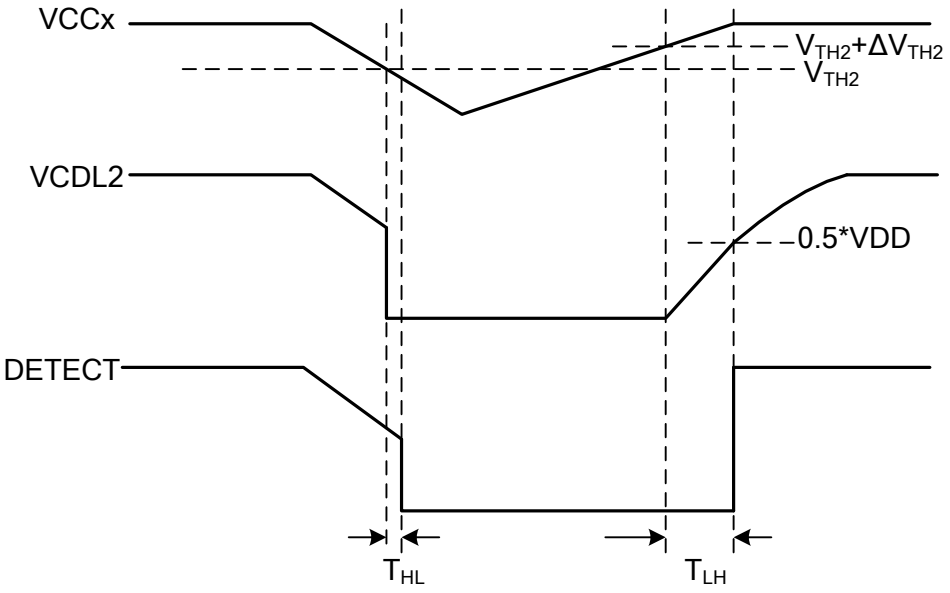
Minimum Footprint PCB Layout Section

SOP-8 (FD)



Timing Diagram

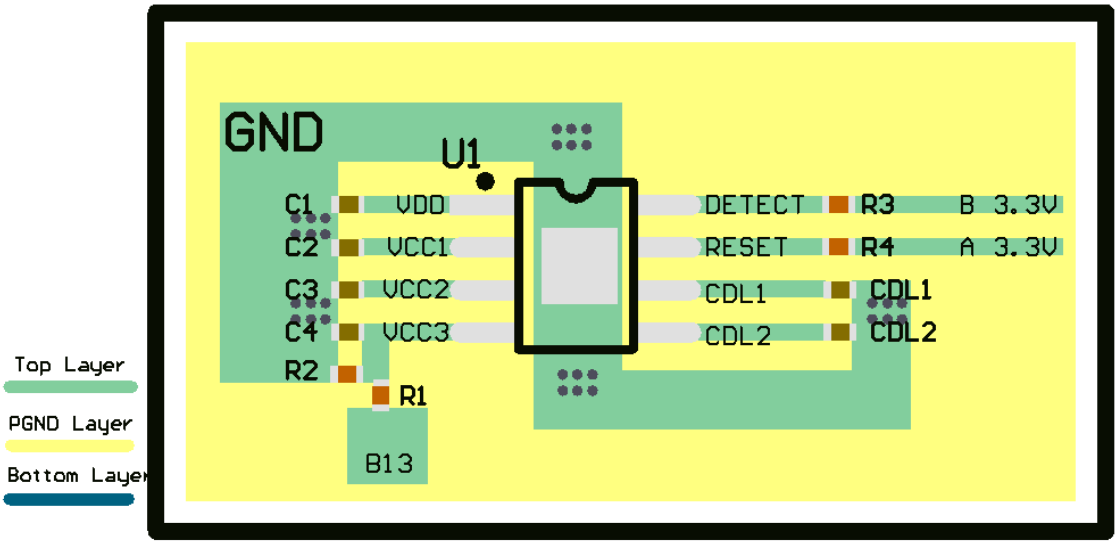




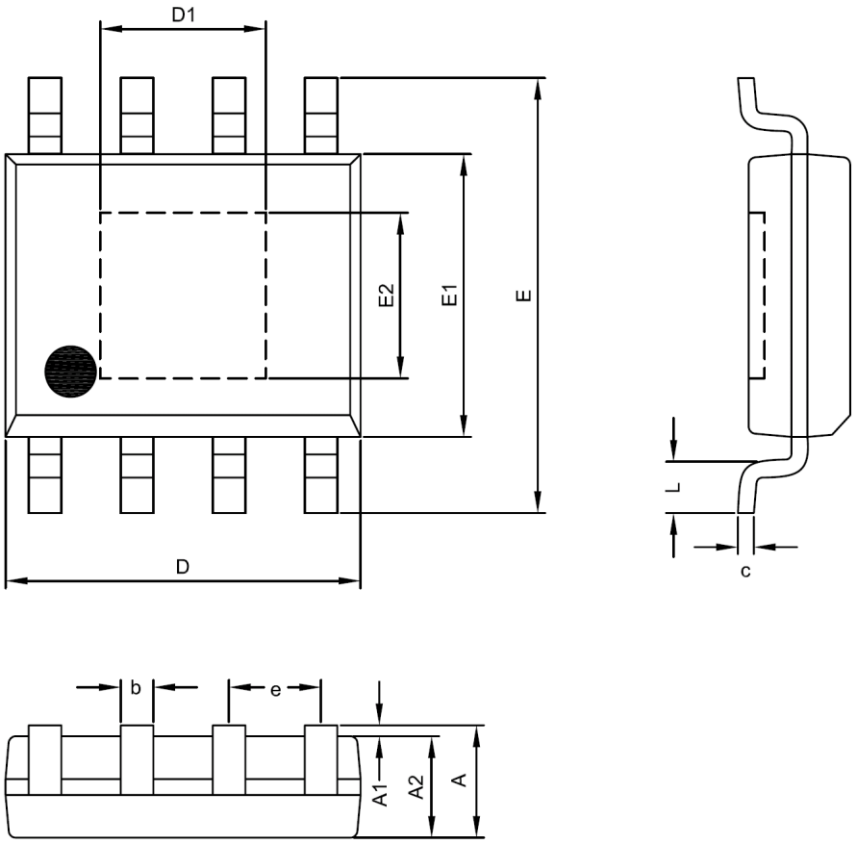
Layout guideline

Power loops of the Reset IC were considered to minimize the area. If possible, it is suggested to arrange the power loops at the top side copper plane.

(1) Connect the bypass capacitor on VDD, VCC1~3, CDL1~2 as close to the device as possible.



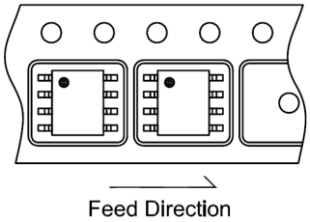
Package Information



SOP- 8 (FD) Package

Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.35	1.55	1.70	0.053	0.061	0.067
A1	0.00	- - -	0.10	0.000	- - -	0.004
A2	1.15	1.35	1.60	0.045	0.053	0.063
D	4.80	4.90	5.00	0.189	0.192	0.197
D1	2.29 BSC			0.090 BSC		
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.153	0.157
E2	2.29 BSC			0.090 BSC		
c	0.20 REF			0.008 REF		
b	0.33	0.43	0.53	0.013	0.017	0.021
e	1.27 BSC			0.050 BSC		
L	0.40	0.70	1.27	0.016	0.028	0.050

Taping Specification



PACKAGE	Q'TY/REEL
SOP-8 (FD)	2,500 ea