G660/G661/G662

Microprocessor Reset IC

Features

- **Power-On Reset Generator With Fixed Delay Time of 200ms**
- **Manual Reset Input (G660/G661)**
- **Available in three RESET Output Options**
  Push-Pull $\overline{\text{RESET}}$ Output (G660L/G662)
  Push-Pull RESET Output (G660H/G662)
  Open-Drain $\overline{\text{RESET}}$ Output (G661L)
- **Supply Voltage Supervision Range 2.5V, 3V, 3.3V, 5V**
- **Watchdog Timer (G660/G661/G662)**
- **Supply Current of 10μA at V_{CC}=3.3V**
- **SOT-23-5 Package**
- **Temperature Range . . . −40°C to 85°C**

Applications

- **Critical μP and μC Power Monitoring**
- **Industrial Equipment**
- **Programmable Controls**
- **Automotive Systems**
- **Portable/Battery-Powered Equipment**
- **Intelligent Instruments**
- **Wireless Communications Systems**
- **Notebook/Desktop Computers**

General Description

The G660/G661/G662 provide circuits initialization and timing supervision, primarily for DSP and processor-based systems. During power-on, $\overline{\text{RESET}}$ (RESET) is asserted when supply voltage VCC becomes higher than 1.1 V. Thereafter, the supply voltage supervisor monitors VCC and keeps $\overline{\text{RESET}}$ (RESET) active as long as VCC remains below the threshold voltage V_{IT+}(1).

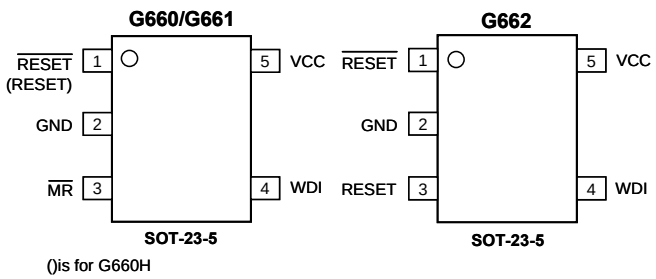
An internal timer delays the return of the output to the inactive state to ensure proper system reset. The delay time, td, starts after VCC has risen above the threshold voltage V_{IT+}. When the supply voltage drops below the threshold voltage V_{IT-}(2), the outputs becomes active again. No external components are required. All the devices have a fixed-sense threshold voltage V_{IT-} set by an internal voltage divider.

The G660/G661 incorporate a manual reset input, $\overline{\text{MR}}$. A low level at $\overline{\text{MR}}$ causes $\overline{\text{RESET}}$ (RESET) to become active. The G660/G661/G662 have WDI pin. The watchdog timer is periodically triggered by a positive or negative transition at WDI. When the supervising system fails to retrigger the watchdog circuit within the time-out interval, t_{tout}, $\overline{\text{RESET}}$ (RESET) becomes active for the time period td. This event also reinitializes the watchdog timer. Leaving WDI unconnected disables the watchdog.

The product spectrum is designed for supply voltages of 2.5V, 3V, 3.3V, and 5V. The circuits are available in a SOT-23-5 package.

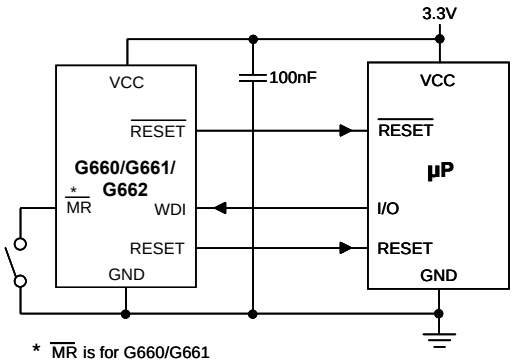
Note:
(1) V_{IT+} means the reset voltage of V_{CC} from low to high
(2) V_{IT-} means the reset voltage of V_{CC} from high to low.

Pin Configuration



()is for G660H

Typical Application Circuit



* $\overline{\text{MR}}$ is for G660/G661
** RESET is for G662

ICC may increased at high T_A, Therefore, can not connect Resistors to VCC to prevent Icc abnormal behavior at high T_A.

Ordering Information

ORDER NUMBER	RESET THRESHOLD (V)	OUTPUT TYPE	MARKING	TEMP. RANGE	PACKAGE (Green)
G660L225T11U	2.25	Push-Pull $\overline{\text{RESET}}$	660Ax	-40°C ~ +85°C	SOT-23-5
G660L263T11U	2.63	Push-Pull $\overline{\text{RESET}}$	660Bx	-40°C ~ +85°C	SOT-23-5
G660L293T11U	2.93	Push-Pull $\overline{\text{RESET}}$	660Cx	-40°C ~ +85°C	SOT-23-5
G660L455T11U	4.55	Push-Pull $\overline{\text{RESET}}$	660Dx	-40°C ~ +85°C	SOT-23-5
G660H225T11U	2.25	Push-Pull RESET	660Ex	-40°C ~ +85°C	SOT-23-5
G660H263T11U	2.63	Push-Pull RESET	660Fx	-40°C ~ +85°C	SOT-23-5
G660H293T11U	2.93	Push-Pull RESET	660Gx	-40°C ~ +85°C	SOT-23-5
G660H455T11U	4.55	Push-Pull RESET	660Hx	-40°C ~ +85°C	SOT-23-5
G661L225T11U	2.25	Open-Drain $\overline{\text{RESET}}$	661Ax	-40°C ~ +85°C	SOT-23-5
G661L263T11U	2.63	Open-Drain $\overline{\text{RESET}}$	661Bx	-40°C ~ +85°C	SOT-23-5
G661L293T11U	2.93	Open-Drain $\overline{\text{RESET}}$	661Cx	-40°C ~ +85°C	SOT-23-5
G661L455T11U	4.55	Open-Drain $\overline{\text{RESET}}$	661Dx	-40°C ~ +85°C	SOT-23-5
G662-225T11U	2.25	Push-Pull $\overline{\text{RESET}}$ & RESET	662Ax	-40°C ~ +85°C	SOT-23-5
G662-263T11U	2.63	Push-Pull $\overline{\text{RESET}}$ & RESET	662Bx	-40°C ~ +85°C	SOT-23-5
G662-293T11U	2.93	Push-Pull $\overline{\text{RESET}}$ & RESET	662Cx	-40°C ~ +85°C	SOT-23-5
G662-455T11U	4.55	Push-Pull $\overline{\text{RESET}}$ & RESET	662Dx	-40°C ~ +85°C	SOT-23-5

Note: T1: SOT-23-5
1: Bonding Code
U: Tape & Reel

Absolute Maximum Ratings

Terminal Voltage (with respect to GND)
V_{CC}. . . . . .-0.3V to +6.0V
$\overline{MR}$, WDI . . . . . .-0.3V to (V_{CC} +0.3V)
RESET, $\overline{RESET}$ (push-pull) . . . . .-0.3V to (V_{CC} + 0.3V)
$\overline{RESET}$ (open drain) . . . . . -0.3V to +6.0V
Input Current (All Pins). 10mA
Thermal Resistance Junction to Ambient, (θ_{JA})*
SOT-23-5 . . . . . .250°C/W

Continuous Power Dissipation (T_A = +25°C)*
SOT-23-5 . . . . . .0.5W
Output Current, RESET, $\overline{RESET}$ 10mA
Operating Temperature Range . . . . . .-40°C to +125°C
Storage Temperature Range . . . . . -65°C to +150°C
Reflow Temperature (soldering, 10sec) . . . . . 260°C
ESD (HBM) (1). 2kV

Note:
(1): Human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.
* Please refer to "Minimum Footprint PCB Layout Section".

Electrical Characteristics

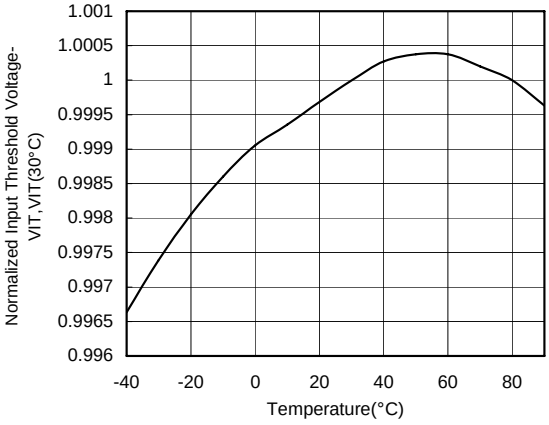
(V_{CC} =3.3V, R_L=1 MΩ , C_L=50pF, and T_A=25°C, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT
Supply Voltage Range	V_{CC}			1.1	---	5.5	V
Supply Current	I_{CC}	WDI, $\overline{MR}$, and Outputs un-connected	V_{CC}=5V	---	14	21	µA
			V_{CC}=3.3V	---	10	17	
V_{CC} Reset Threshold Accuracy (negative-going)	V_{TH-}	T_A=25°C		-2	---	2	%
Hysteresis	V_{HYST}	% of V_{TH-}		---	1	---	%
Watchdog time out	t_{tout}	V_{CC} > V_{TH-}+0.2 V		1	1.6	2.5	S
Delay time	td	V_{CC} > V_{TH-}+0.2 V		120	200	300	ms
V_{CC} to $\overline{RESET}$ (or RESET) Delay	$T_{P,Vcc}$	V_{CC} from V_{TH-}+0.2V to V_{TH}-0.2V within 1µS		---	25	40	µs
$\overline{MR}$ to $\overline{RESET}$ (or RESET) Delay	$T_{P,MR}$	$\overline{MR}$ from 0.7xV_{CC} to V_{IL}=0.3xV_{CC}, V_{CC}>V_{TH-}+0.2V		---	4	30	µs
Minimum Pulse width of WDI	$t_{w,WDI}$	WDI from 0.3xV_{CC} to 0.7xV_{CC}, V_{CC}>V_{TH-}+0.2V		---	100	---	ns
$\overline{RESET}$ (or RESET) Output Voltage LOW	V_{OL}	$\overline{RESET}$ Output, V_{CC}=V_{TH-} -0.2V	I_{SINK}=3mA	---	---	0.4	V
		RESET Output, V_{CC}=V_{TH-}+0.2V		---	---	0.4	
$\overline{RESET}$ (or RESET) Output Voltage High	V_{OH}	$\overline{RESET}$ Output, V_{CC}=V_{TH-}+0.2V	I_{Source}=150µA	0.8xV_{CC}	---	---	V
		RESET Output, V_{CC}=V_{TH-} -0.2V		0.8xV_{CC}	---	---	
$\overline{RESET}$ Output leakage (Open-drain)	I_{LKG}	V_{CC} >$V_{TH,}$ reset not asserted		---	---	1	µA
$\overline{MR}$ Input	V_{IL}	V_{CC}=3.3V		---	---	0.8	V
	V_{IH}			2.4	---	---	
$\overline{MR}$ Pullup Resistance	R_{MRB}			25	52	100	kΩ
Average high-level input current at WDI	$I_{HWDI(AVG)}$	WDI=V_{CC}=5.5V, time average (dc=88%)		---	120	---	µA
Average low-level input current at WDI	$I_{LWDI(AVG)}$	WDI=0V, V_{CC}=5.5V, time average (dc=12%)		---	-15	---	µA
WDI high-level input current	I_{HWDI}	WDI=V_{CC}=5.5V		---	140	---	µA
WDI low-level input current	I_{HWDI}	WDI=0V, V_{CC}=5.5V		---	-140	---	µA
$\overline{MR}$ high-level input current	I_{HMRB}	$\overline{MR}$ =V_{CC} x0.7, V_{CC}=5.5V		16.5	32	66	µA
$\overline{MR}$ low-level input current	I_{LMRB}	$\overline{MR}$ =0.3V, V_{CC}=5.5V		-200	-100	-50	µA
$\overline{RESET}$ Output short-circuit current	I_{OS}	V_{CC}=V_{TH-}+0.2V, V_O=0V		---	1.8	---	mA
Input capacitance at $\overline{MR}$,WDI	C_I	V_I=0V to 5.5V		---	5	---	pF

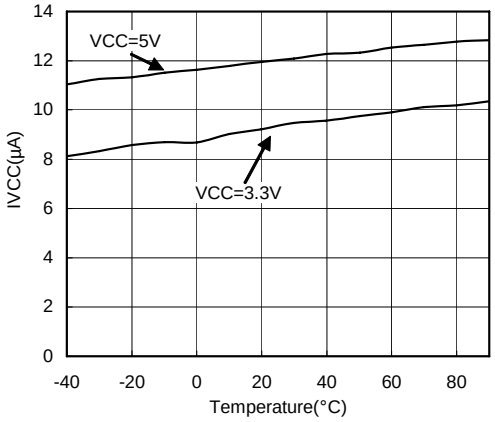
Typical Performance Characteristics

T_A=25°C, unless otherwise noted

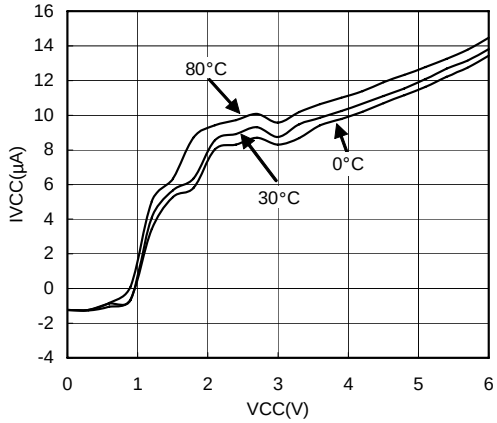
Normalized Input Threshold Voltage vs. Temperature



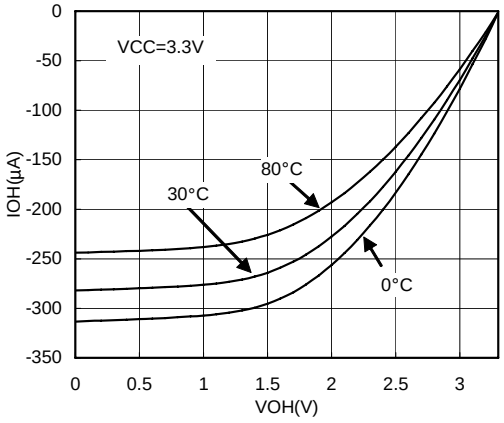
IVCC VS Temperature



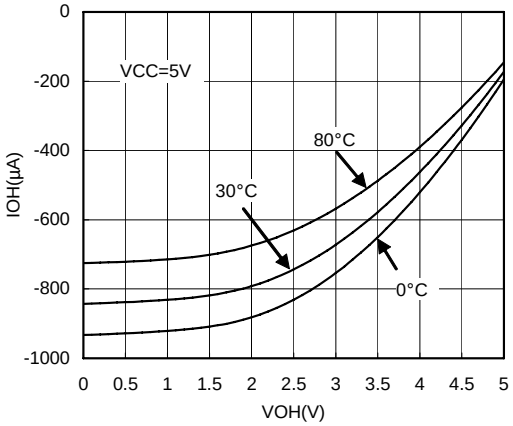
IVCC VS VCC



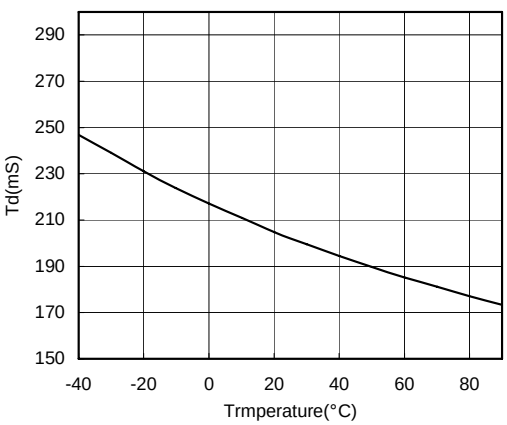
$\overline{\text{RESET}}$ Output Current vs. High Level Output Voltage



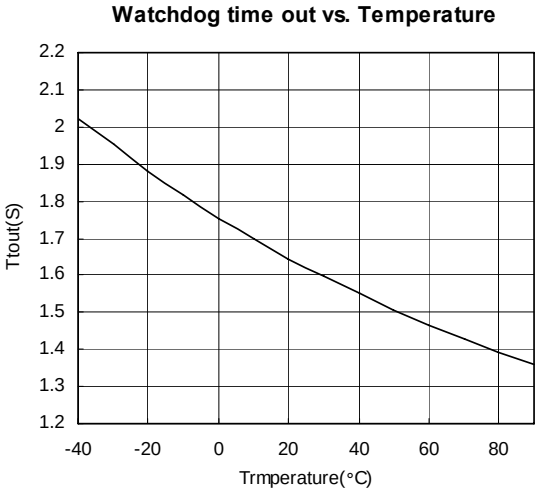
$\overline{\text{RESET}}$ Output Current vs. High Level Output Voltage



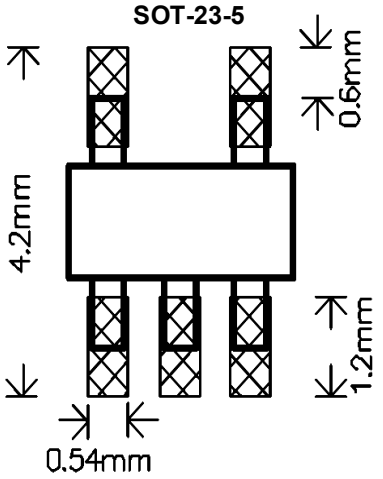
Delay time vs. Temperature



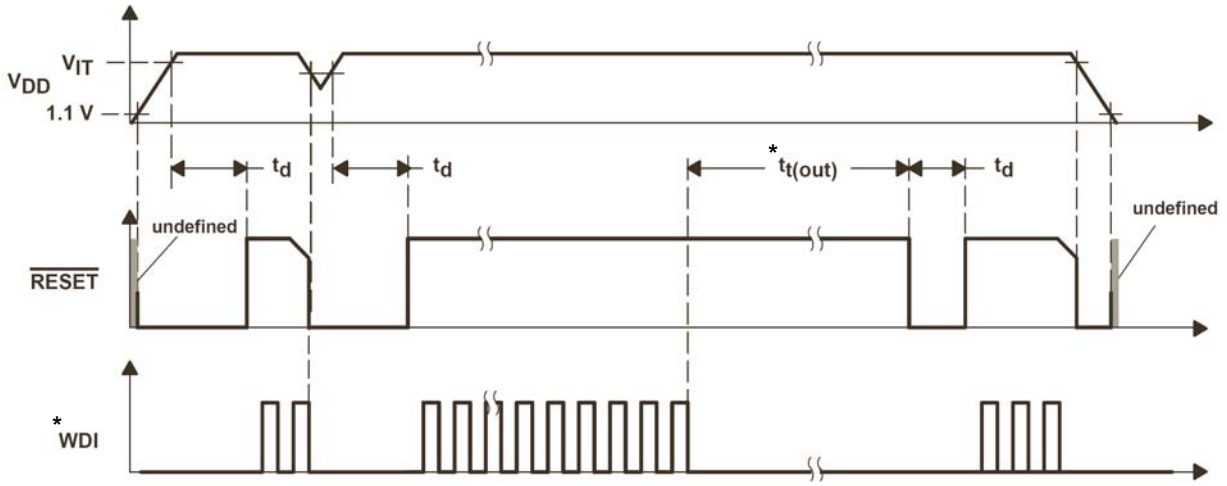
Typical Performance Characteristics (continued)



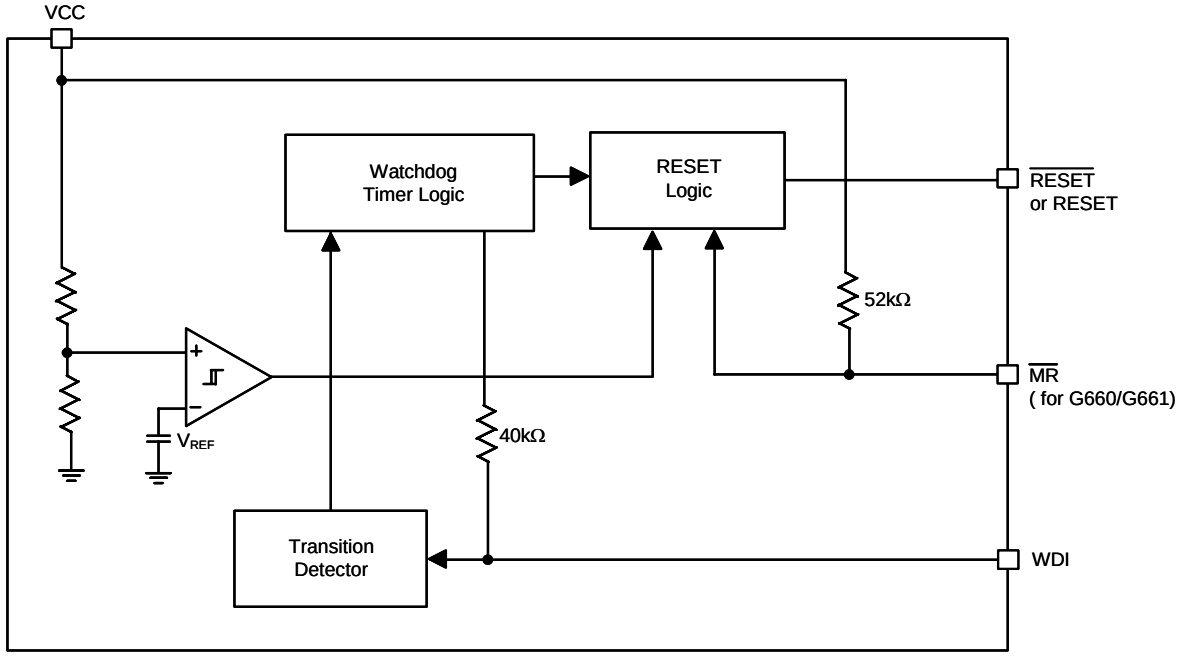
Minimum Footprint PCB Layout Section



Timing Diagram



Functional Diagram



Pin Description

PIN		NAME	FUNCTION
G660/G661	G662		
1	---	$\overline{\text{RESET}}$ (or RESET)	Active Low (or High) Reset Output
---	1	$\overline{\text{RESET}}$	Active Low Reset Output
2	2	GND	Ground
---	3	RESET	Active High Reset Output
3	---	$\overline{\text{MR}}$	Manual reset input
4	4	WDI	Watchdog timer input
5	5	VCC	Supply Voltage

Truth Table

G660/G661

INPUTS		OUTPUTS	
$\overline{\text{MR}}$	$V_{CC}>V_{IT+}$	$\overline{\text{RESET}}$	RESET
L	0	L	H
L	1	L	H
H	0	L	H
H	1	H	L

Note: WDI pin floating

G662

INPUTS	OUTPUTS	
$V_{CC}>V_{IT+}$	$\overline{\text{RESET}}$	RESET
0	L	H
1	H	L

Note: WDI pin floating

Detailed Description

A microprocessor's (µP's) reset input starts the µP in a known state. The G660/G661/G662 assert reset to prevent code-execution errors during power-up, power-down, or brownout conditions. They assert a reset signal whenever the V_{CC} supply voltage declines below a preset threshold, keeping it asserted for 200ms (TYP) after V_{CC} has risen above the reset threshold. The G661L uses an open-drain output, and the G660/G662 have push-pull output stages. Connect a pull-up resistor on the G661L's $\overline{RESET}$ output to any supply between 0 and 5.5V.

Manual Reset Input

The manual reset input ($\overline{MR}$) of G660/G661 can also initiate a reset.

Many µP-based products require manual reset capability, allowing the operator, a test technician, or external logic circuitry to initiate a reset. A logic low on $\overline{MR}$ asserts reset. Reset remains asserted while $\overline{MR}$ is low, and for the Reset Active Timeout Period (t_{RP}) after $\overline{MR}$ returns high. This input has an internal 52kΩ pull-up resistor, so it can be left open if it is not used. $\overline{MR}$ can be driven with TTL or CMOS-logic levels, or with open-drain / collector outputs. Connect a normally open momentary switch from $\overline{MR}$ to GND to create a manual-reset function; external debounce circuitry is not required. If $\overline{MR}$ is driven from long cables or if the device is used in a noisy environment, connecting a 0.1µF capacitor from $\overline{MR}$ to ground provides additional noise immunity.

Watchdog Timer Input

The G660/G661/G662 have watchdog timer input (WDI). The watchdog timer is periodically triggered by a positive or negative transition at WDI. When the supervising system fails to retrigger the watchdog circuit within the time-out interval, t_{tout}, $\overline{RESET}$ (RESET) becomes active for the time period td as shown in Timing Diagram. This event also reinitializes the watchdog timer. If the fail retrigger continuously exists, the $\overline{RESET}$ (RESET) becomes active (t_d) and inactive (t_{tout}) periodically. Leaving the WDI unconnected disable the watchdog function.

Applications Information

Ensuring a Valid Reset Output Down to V_{CC} = 0

When V_{CC} falls below 1V, the G660/G662 $\overline{RESET}$ output no longer sinks current—it becomes an open circuit. Therefore, high-impedance CMOS logic inputs connected to $\overline{RESET}$ can drift to undetermined voltages. This presents no problem in most applications since most µP and other circuitry is inoperative with VCC below 1V. However, in applications where $\overline{RESET}$ must be valid down to 0V, adding a pull-down resistor to $\overline{RESET}$ causes any stray leakage currents to flow to ground, holding $\overline{RESET}$ low (Figure 1). R1's value is not critical; 100kΩ is large enough not to load $\overline{RESET}$ and small enough to pull $\overline{RESET}$ to ground.

A 100kΩ pull-up resistor to VCC is also recommended for the G661L if $\overline{RESET}$ is required to remain valid for V_{CC} < 1V.

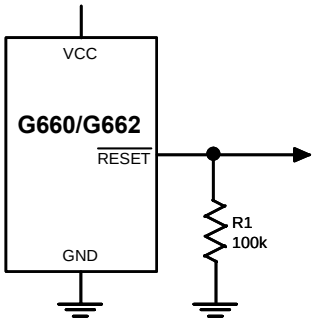


Figure 1. $\overline{RESET}$ Valid to V_{CC} = Ground Circuit

G661L Open-Drain $\overline{\text{RESET}}$ Output Allows Use with Multiple Supplies

Generally, the pull-up connected to the G661L will connect to the supply voltage that is being monitored at the IC's V_{CC} pin. However, some systems may use the open-drain output to level-shift from the monitored supply to reset circuitry powered by some other supply (Figure 2). Note that as the G661L's V_{CC} decreases below 1V, so does the IC's ability to sink current at $\overline{\text{RESET}}$. Also, with any pull-up, $\overline{\text{RESET}}$ will be pulled high as V_{CC} decays toward 0. The voltage where this occurs depends on the pull-up resistor value and the voltage to which it is connected.

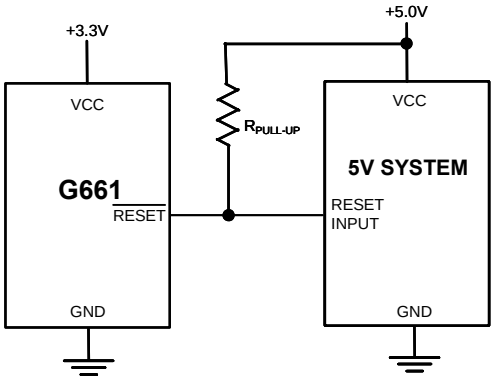


Figure 2. G661L Open-Drain $\overline{\text{RESET}}$ Output Allows Use with Multiple Supplies

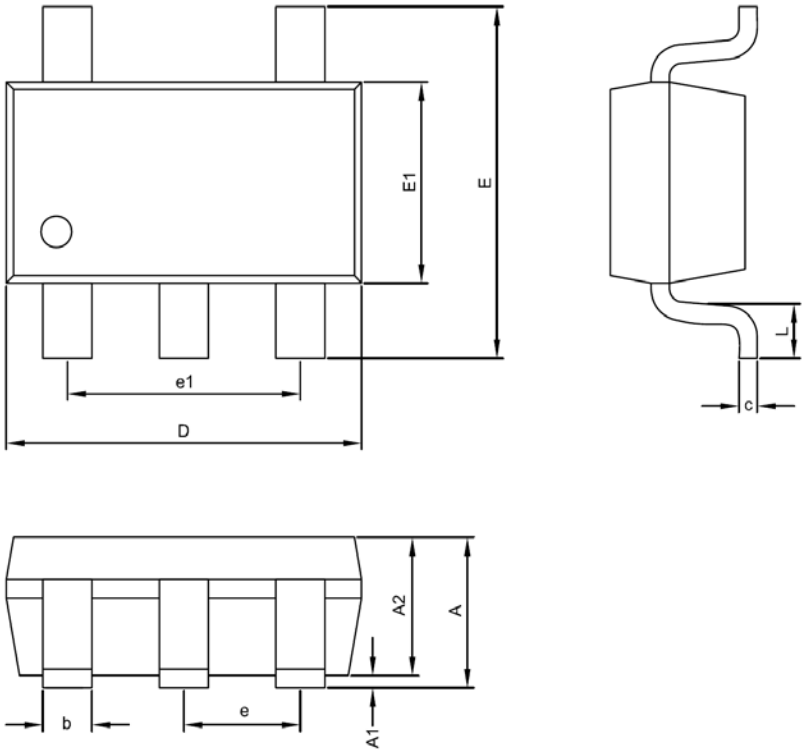
Benefits of Highly Accurate Reset Threshold

Most µP supervisor ICs have reset threshold voltages between 5% and 10% below the value of nominal supply voltages. This ensures a reset will not occur within 5% of the nominal supply, but will occur when the supply is 10% below nominal.

When using ICs rated at only the nominal supply ±5%, this leaves a zone of uncertainty where the supply is between 5% and 10% low, and where the reset may or may not be asserted.

The G660/G661/G662 use highly accurate circuitry to ensure that reset is asserted close to the 5% limit, and long before the supply has declined to 10% below nominal.

Package Information



SOT-23-5 (T1) Package

Symble	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00	1.10	1.45	0.039	0.043	0.057
A1	0.00	- - -	0.15	0.000	- - -	0.006
A2	1.00	1.10	1.30	0.039	0.043	0.051
D	2.70	2.90	3.10	0.106	0.114	0.122
E	2.60	2.80	3.00	0.102	0.110	0.118
E1	1.50	1.60	1.70	0.059	0.063	0.067
c	0.08	0.15	0.25	0.003	0.006	0.010
b	0.30	0.40	0.50	0.012	0.016	0.020
e	0.95 BSC			0.037 BSC		
e1	1.90 BSC			0.075 BSC		
L	0.30	0.45	0.60	0.012	0.018	0.024

Taping Specification

PACKAGE	Q'TY/REEL
SOT-23-5	3,000 ea