High Accuracy Digital Temperature Sensor and Thermal Watchdog with Two-Wire Interface

Features

- **SMBus interface**
- **Hardware Power-on Setting & Programmable over temperature limit**
- **Separate open-drain output pin operates as interrupt or comparator at output**
- **Register readback capability**
- **Power up defaults permit stand-alone operation as thermostat**
- **Shutdown mode to minimize power consumption**

Applications

- **System Thermal Management**
- **Personal Computers**
- **Office Electronics**
- **Electronic Test Equipment**

General Description

The G756 is a temperature sensor, analog-to-digital converter, and digital over- temperature detector with SMBus interface. The host can query the G756 at any time to read temperature.

Key Specifications

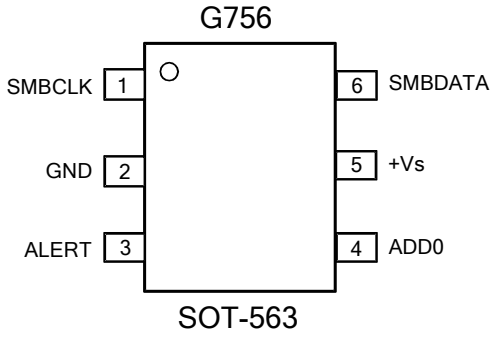
- **Supply Voltage** **1.6V to 3.6V**
- **Supply Current at 0.25 Conv/s** **7.5 µA (typ)**
  15µA (max)
  shutdown **0.5µA (max)**
- **Temperature Accuracy**
  -10°C to 100°C, +Vs=1.8V **±2°C (max)**
  -40°C to 125°C, +Vs=1.8V **±3°C (max)**

Ordering Information

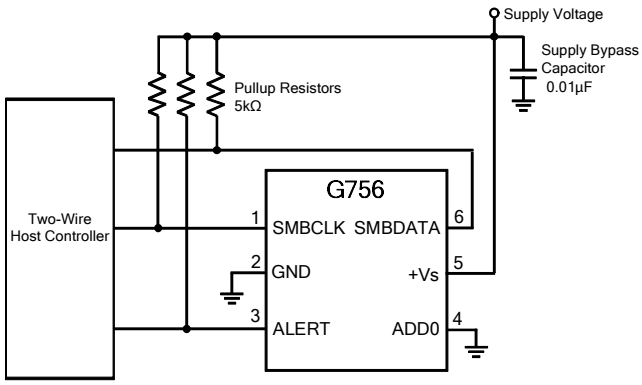
ORDER NUMBER	MARKING	PACKAGE (Green)
G756TR1G	76x	SOT-563

Note: TR: SOT-563
1: Bonding Code
G: Tape & Reel
Green : Lead Free / Halogen Free.

Pin Configuration



Typical Application Circuit



Absolute Maximum Ratings

$+V_S$ to GND.. . . . . .-0.3V to +4V
SMBCLK, SMBDAT., to GND. . . . . -0.3V to +4V
SMBDATA Current. . . . . -1mA to +50mA
ESD Protection (human body model). 2000V
Operating Temperature Range . . . . . -55°C to +125°C
Junction Temperature. . . . . +150°C
Storage temperature Range. . . . . .-60°C to +150°C
Reflow Temperature (soldering,10sec) . . . . . .+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Information

THERMAL METRIC		SOT-563	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance	130.5	°C/W
$R_{\theta JC\_top}$	Junction to case top thermal resistance	60.7	°C/W
$R_{\theta JB}$	Junction to board thermal resistance	34.1	°C/W
Ψ_{JT}	Junction to top characterization parameter	1.6	°C/W
Ψ_{JB}	Junction to board characterization parameter	35.1	°C/W

Package thermal metric were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board.

Temperature-to-Digital Converter Characteristics

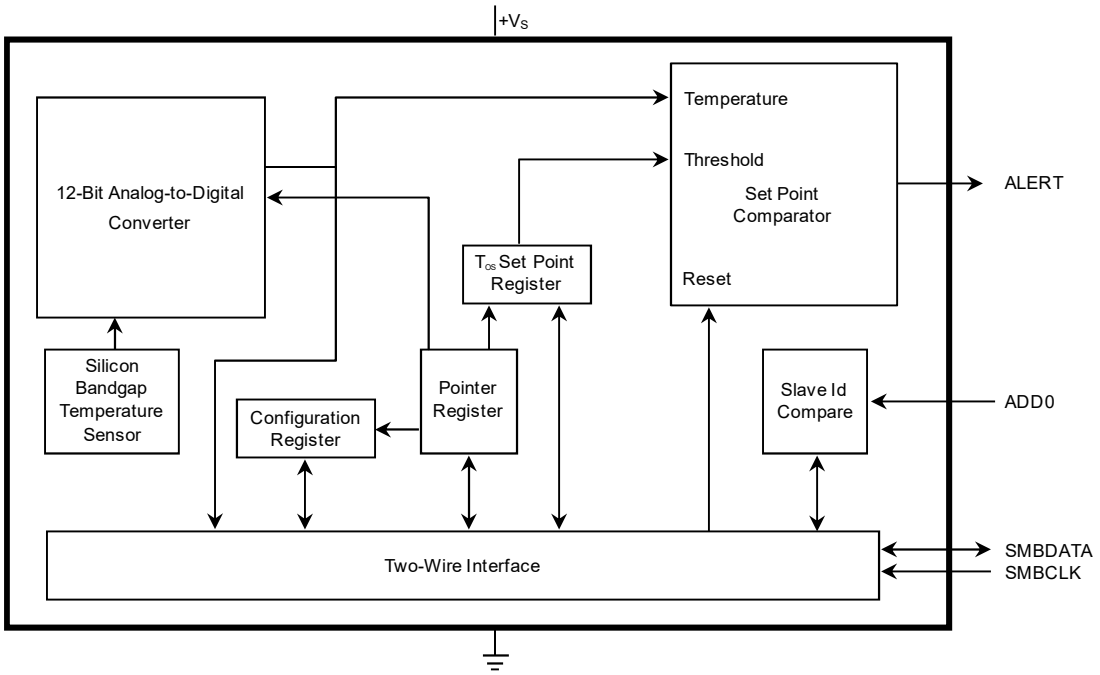
Unless otherwise noted, these specifications apply for +Vs=+1.8V Vdc. **Boldface limits apply for $T_A=T_J=T_{MIN}$ to T_{MAX}**; all other limits $T_A=T_J$= +25°C, unless otherwise noted.

PARAMETER	CONDITIONS	TYPICAL	LIMITS	UNITS
Accuracy	T_A=-10°C to +100°C, +Vs=1.8V	±0.5	±2	°C
	T_A=-40°C to +125°C, +Vs=1.8V	±1	±3	
v.s. Supply		±0.2	±0.5	°C/V
Resolution		12	---	Bits
Conversion mode	CR1 = 0, CR0 = 0	0.25	---	Conv/s
	CR1 = 0, CR0 = 1	1	---	Conv/s
	CR1 = 1, CR0 = 0 (default)	4	---	Conv/s
	CR1 = 1, CR0 = 1	8	---	Conv/s
Average Quiescent Current	Serial Bus Inactive, +Vs=1.8V CR1=1,CR0=0	17.5	25	µA
Quiescent Current	Serial Bus Inactive, +Vs = 1.8V	7.5	15	µA
	Serial Bus Active, SMBCLK Frequency = 400kHz	15	---	µA
	Serial Bus Active, SMBCLK Frequency = 2.85MHz	45	---	µA
Shutdown Current	Serial Bus Inactive, +Vs = 1.8V	0.2	0.5	µA
	Serial Bus Active, SMBCLK Frequency = 400kHz	10	---	µA
	Serial Bus Active, SMBCLK Frequency = 2.85MHz	40	---	µA

Pin Description

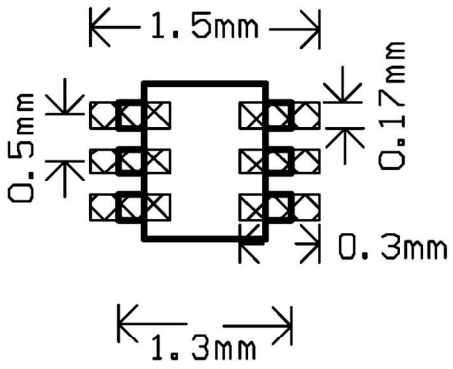
PIN	LABEL	FUNCTION	TYPICAL CONNECTION
1	SMBCLK	Serial clock.	From Controller
2	GND	Ground	Ground
3	ALERT	Overtemperature alert. Open-drain output; requires a pullup resistor	Pull up to +Vs
4	ADD0	Address select.	Connect to GND or +Vs or SMBCLK or SMBDATA
5	+Vs	Supply voltage,	DC Voltage
6	SMBDATA	Serial data. Open-drain output; requires a pullup resistor.	From Controller

Block Diagram



Minimum Footprint PCB Layout Section

SOT-563



Logic Electrical Characteristics

Digital DC Characteristics

Unless otherwise noted, these specifications apply for +Vs=+3.3 Vdc. **Boldface limits apply for T_A=T_J=T_{MIN} to T_{MAX}**; all other limits T_A=T_J=+25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	LIMITS	UNITS
$V_{IN\ (1)}$	Logical "1" Input Voltage		---	+Vs× 0.7	V (min)
			---	+Vs + 0.5	V (max)
$V_{IN\ (0)}$	Logical "0" Input Voltage		---	-0.5	V (min)
			---	+Vs×0.3	V (max)
$I_{IN\ (1)}$	Logical "1" Intput Current	V_{IN}=3.3V	0.005	1.0	µA
$I_{IN\ (0)}$	Logical "0" Intput Current	V_{IN}=0V	-0.005	-1.0	µA
C_{IN}	All Digital Inputs		20	---	pF
V_{OL}	Low Level Output Voltage	I_{OL}=2mA	---	0.4	V (max)

SMBus Digital Switching Characteristics

Unless otherwise noted, these specifications apply for +Vs = +3.3 Vdc and C_L (load capacitance) on output lines = 80pF unless otherwise specified. **Boldface limits apply for T_A = T_J = T_{MIN} to T_{MAX}**; all other limits T_A = T_J = +25°C, unless otherwise noted.

PARAMETER	CONDITIONS	FAST MODE			HIGH-SPEED MODE			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
SMBus Clock Frequency		0.001	---	0.4	0.001	---	2.85	MHz
SMBus Timeout	SMBCLK time for interface reset	---	30	---	---	30	---	ms
SMBCLK Clock Low Time	t_{LOW} , 10% to 10% points	1300	---	---	210	---	---	ns
SMBCLK Clock High Time	t_{HIGH} , 90% to 90% points	600	---	---	60	---	---	ns
SMBus Start-Condition Setup Time		600	---	---	160	---	---	ns
SMBus Repeated Start-Condition Setup Time	$t_{SU\ :\ STA}$, 90% to 90% points	600	---	---	160	---	---	ns
SMBus Start-Condition Hold Time	$t_{HD:\ STA}$, 10% of SMBDATA to 90% of SMBCLK	600	---	---	160	---	---	ns
SMBus Stop-Condition Setup Time	$t_{SD:\ STO}$, 90% of SMBCLK to 10% of SMBDATA	600	---	---	160	---	---	ns
SMBus Data Valid to SMBCLK Rising-Edge Time	$t_{SU:\ DAT}$, 10% or 90% of SMBDATA to 10% of SMBCLK	100	---	---	25	---	105	ns
SMBus Data-Hold Time	$t_{HD\ :\ DAT}$	100	---	900	25	---	---	ns

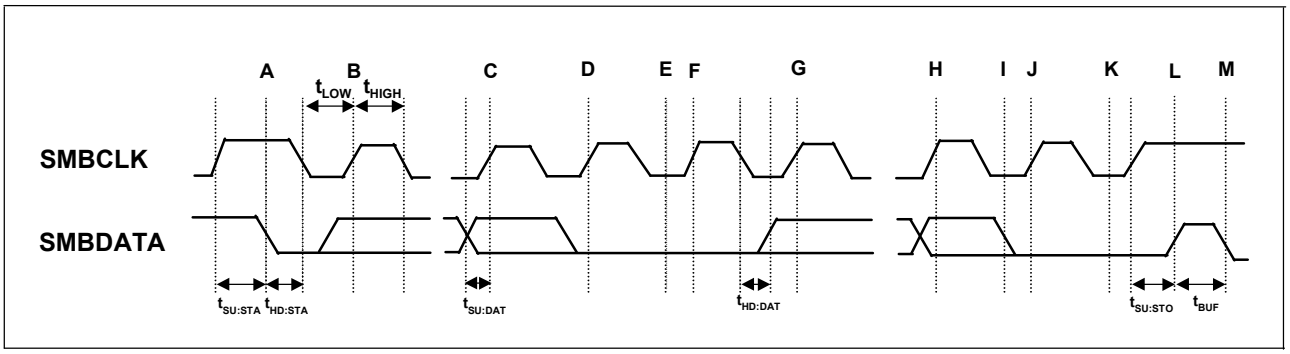


Figure 1. SMBus Write Timing Diagram

A = start condition
B = MSB of address clocked into slave
C = LSB of address clocked into slave
D = R/W bit clocked into slave
E = slave pulls SMBDATA line low
F = acknowledge bit clocked into master
G = MSB of data clocked into slave
H = LSB of data clocked into slave
I = slave pulls SMBDATA line low
J = acknowledge clocked into master
K = acknowledge clocked pulse
L = stop condition data executed by slave
M = new start condition

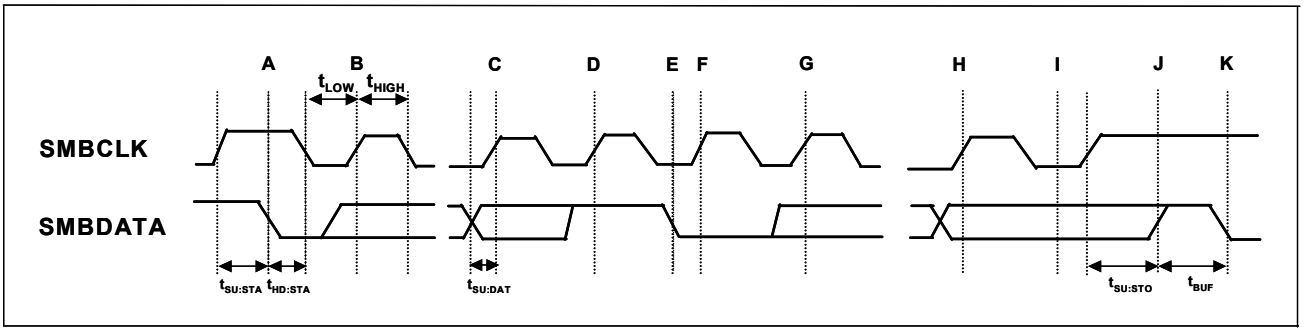


Figure 2. SMBus Read Timing Diagram

A = start condition
B = MSB of address clocked into slave
C = LSB of address clocked into slave
D = R/$\overline{W}$ bit clocked into slave
E = slave pulls SMBDATA line low
F =acknowledge bit clocked into master
G = MSB of data clocked into master
H = LSB of data clocked into master
I = acknowledge clocked pulse
J = stop condition
K= new start condition

Functional Description

The G756 temperature sensor incorporates a band-gap type temperature sensor and 12-bit ADC (Analog-to-Digital Converter). The temperature data output of the G756 is available at all times via the SMBus. If a conversion is in progress, it will be stopped and restarted after the read. A digital comparator is also incorporated that compares a series of readings, the number of which is user-selectable, to user-programmable setpoint.

SMBus Digital Interface

From a software perspective, the G756 appears as a set of word-wide registers that contain temperature data, alarm threshold values, or control bits, A standard SMBus 2-wire serial interface is used to read temperature data and write control bits and alarm threshold data.

Each A/D channel within the device responds to the same SMBus slave address for normal reads and writes.

Serial Bus Address

slave address byte consists of seven address bits, and a direction bit indicating the intent of executing a read or write operation. The G756 features an address pin to allow up to four devices to be addressed on a single bus. Table 1 describes the pin logic levels used to properly connect up to four devices

Table 1. Address Pin and Slave Addresses

Device Two-Wire Address	A0 Pin Connection
1001000	Ground
1001001	+Vs
1001010	SMBDATA
1001011	SMBCLK

Writing/Reading Operation

Accessing a particular register on the G756 is accomplished by writing the appropriate value to the Pointer Register. The value for the Pointer Register is the first byte transferred after the slave address byte with the $R/\overline{W}$ bit low. Every write operation to the G756 requires a value for the Pointer Register (see Figure 4).

When reading from the G756, the last value stored in the Pointer Register by a write operation is used to determine which register is read by a read operation. To change the register pointer for a read operation, a new value must be written to the Pointer Register. This action is accomplished by issuing a slave address byte with the $R/\overline{W}$ bit low, followed by the Pointer Register byte. No additional data are required. The master can then generate a START condition and send the slave address byte with the $R/\overline{W}$ bit high to initiate the read command. See Figure 5 for details of this sequence. If repeated reads from the same register are desired, it is not necessary to continually send the Pointer Register bytes; the G756 remembers the Pointer Register value until it is changed by the next write operation, or the G756 is reset.

Slave Mode Operations

The G756 can operate as a slave receiver or slave transmitter. As a slave device, the G756 never drives the SMBCLK line.

Slave Receiver Mode

The first byte transmitted by the master is the slave address, with the $R/\overline{W}$ bit low. The G756 then acknowledges reception of a valid address. The next byte transmitted by the master is the Pointer Register. The G756 then acknowledges reception of the Pointer Register byte. The next byte is written to the register addressed by the Pointer Register. The G756 acknowledges reception of the data byte. The master can terminate data transfer by generating a START or STOP condition.

Slave Transmitter Mode

The first byte transmitted by the master is the slave address, with the $R/\overline{W}$ bit high. The slave acknowledges reception of a valid slave address. The next byte is transmitted by the slave of the register indicated by the Pointer Register. The master acknowledges reception of the data byte. The master can terminate data transfer by generating a *Not-Acknowledge* on reception of the data byte, or generating a START or STOP condition.

General Call

The G756 responds to a two-wire General Call address (0000000) if the eighth bit is '0'. The device acknowledges the General Call address and responds to commands in the second byte. If the second byte is 00000110, the G756 internal registers are reset to power-up values. The G756 does not support the General Address acquire command.

High-Speed (Hs) Mode

In order for the two-wire bus to operate at frequencies above 400kHz, the master device must issue an Hs-mode master code (00001xxx) as the first byte after a START condition to switch the bus to high-speed operation. The G756 does not acknowledge this byte, but switches its input filters on SMBDATA and SMBCLK and its output filters on SMBDATA to operate in Hs-mode, allowing transfers at up to 2.85MHz. After the Hs-mode master code has been issued, the master transmits a START condition followed by a two-wire slave address to initiate a data transfer operation. The bus continues to operate in Hs-mode until a STOP condition occurs on the bus. Upon receiving the STOP condition, the G756 switches the input and output filters back to the default fast-mode operation.

Timeout Function

The G756 resets the serial interface if a SM BUS command continues over 30ms(typ). The G756 releases the bus if it is pulled low and waits for a START condition. To avoid activating the timeout function, it is necessary to maintain a communication speed of at least 1kHz for SMBCLK operating frequency.

SMBus Alert Function

The G756 device supports the SMBus alert function. When the G756 device operates in Interrupt Mode (TM=1), the ALERT pin can be connected as an SMBus alert signal. When a master senses that an ALERT condition is present on the ALERT line, the master sends an SMBus alert command (0001 1001) to the bus. If the ALERT pin is active, the device acknowledges the SMBus alert command and responds by returning the slave address on the SMBDATA line. The eighth bit (LSB) of the slave address byte indicates if the ALERT condition was caused by the temperature exceeding T_{HIGH} or falling below T_{LOW}. For POL=0, the LSB is low if the temperature is greater than or equal to T_{HIGH}; this bit is high if the temperature is less than T_{LOW}. The polarity of this bit is inverted if POL=1. See Figure 6 for details of this sequence. If multiple devices on the bus respond to the SMBus alert command, arbitration during the slave address portion of the SMBus alert command determines which device clears the ALERT status. The device with the lowest twowire address wins the arbitration. If the G756 device wins the arbitration, its ALERT pin inactivates at the completion of the SMBus alert command. If the G756 device loses the arbitration, its ALERT pin remains active

Extended Mode (EM)

The Extended-Mode bit configures the device for Normal mode operation (EM=0) or Extended mode operation (EM=1). In Normal mode, the Temperature Register and high- and low-limit registers use a 12-bit data format. Normal mode is used to make the G756 device compatible with the G756 device. Extended mode (EM=1) allows measurement of temperatures above 128°C by configuring the Temperature Register, and high- and low-limit registers for 13-bit data format. See Table 2, Table 3 for detail.

Table 2. 12-Bit Temperature Data Format (1)

Temperature (°C)	Digital Output (BINARY)	HEX
127.9375	0111 1111 1111	7FF
100	0110 0100 0000	640
25	0001 1001 0000	190
0.25	0000 0000 0100	004
0	0000 0000 0000	000
–0.25	1111 1111 1100	FFC
–25	1110 0111 0000	E70
–55	1100 1001 0000	C90

Table 3. 13-Bit Temperature Data Format

Temperature (°C)	Digital Output (BINARY)	HEX
150	0 1001 0110 0000	0960
128	0 1000 0000 0000	0800
127.9375	0 0111 1111 1111	07FF
100	0 0110 0100 0000	0640
25	0 0001 1001 0000	0190
0.25	0 0000 0000 0100	0004
0	0 0000 0000 0000	0000
–0.25	1 1111 1111 1100	1FFC
–25	1 1110 0111 0000	1E70
–55	1 1100 1001 0000	1C90

Thermostat Mode (TM)

The thermostat-mode bit indicates to the device whether to operate in comparator mode (TM=0) or Interrupt mode (TM=1).

Comparator Mode (TM=0)

In Comparator mode (TM=0), the Alert pin is activated when the temperature equals or exceeds the value in the $T_{(HIGH)}$ register and it remains active until the temperature falls below the value in the $T_{(LOW)}$ register. For more information on the comparator mode, see the *High- and Low-Limit Registers* section.

Interrupt Mode (TM=1)

In Interrupt mode (TM=1), the Alert pin is activated when the temperature exceeds $T_{(HIGH)}$ or goes below $T_{(LOW)}$ registers. The Alert pin is cleared when the host controller reads the temperature register. For more information on the interrupt mode, see the *High- and Low-Limit Registers* section.

Table 4. Pointer Addresses

P1	P0	REGISTER
0	0	Temperature Register (Read Only)
0	1	Configuration Register (Read/Write)
1	0	T_{LOW} Register (Read/Write)
1	1	T_{HIGH} Register (Read/Write)

Temperature Register

The Temperature Register of the G756 is configured as a 12-bit, read-only register (Configuration Register EM bit=0, see the *Extended Mode* section), or as a 13-bit, read-only register (Configuration Register EM bit=1) that stores the output of the most recent conversion. Two bytes must be read to obtain data, and are described in Table 5 and Table 6. Note that byte 1 is the most significant byte, followed by byte 2, the least significant byte. The first 12 bits (13 bits in Extended mode) are used to indicate temperature. The least significant byte does not have to be read if that information is not needed.

Table 5. Byte 1 of Temperature Register (1)

D7	D6	D5	D4	D3	D2	D1	D0
T11	T10	T9	T8	T7	T6	T5	T4
(T12)	(T11)	(T10)	(T9)	(T8)	(T7)	(T6)	(T5)

Table 6. Byte 2 of Temperature Register (1)

D7	D6	D5	D4	D3	D2	D1	D0
T3	T2	T1	T0	0	0	0	0
(T4)	(T3)	(T2)	(T1)	(T0)	(0)	(0)	(1)

(1) Extended mode 13-bit configuration shown in parenthesis.

Configuration Register
The Configuration Register is a 16-bit read/write register used to store bits that control the operational modes of the temperature sensor. Read/write operations are performed MSB first. Table 7 and Table 8 list the format and the power-up or reset value of the configuration register. For compatibility, Table 7 and Table 8 correspond to the configuration register in the G756 device. All registers are updated byte by byte.

Table 7. Byte 1 of Configuration and Power-Up or Reset Format

D7	D6	D5	D4	D3	D2	D1	D0
OS	R1	R0	F1	F0	POL	TM	SD
0	1	1	0	0	0	0	0

Table 8. Byte 2 of Configuration and Power-Up or Reset Format

D7	D6	D5	D4	D3	D2	D1	D0
CR1	CR0	AL	EM	0	0	0	0
1	0	1	0	0	0	0	0

Shutdown Mode (SD)
The Shutdown-mode bit saves maximum power by shutting down all device circuitry other than the serial interface, reducing current consumption to typically less than 0.5μA. Shutdown mode enables when the SD bit is 1; the device shuts down when current conversion is completed. When SD is equal to 0, the device maintains a continuous conversion state

Thermostat Mode (TM)
The Thermostat mode bit indicates to the device whether to operate in Comparator mode (TM=0) or Interrupt mode (TM=1). For more information on comparator and interrupt modes, see the *High- and Low-Limit Registers* section.

Polarity (POL)
The polarity bit allows the user to adjust the polarity of the ALERT pin output. If the POL bit is set to 0 (default), the ALERT pin becomes active low . When the POL bit is set to 1, the ALERT pin becomes active high and the state of the ALERT pin is inverted. The operation of the ALERT pin in various modes is shown in Figure 3.

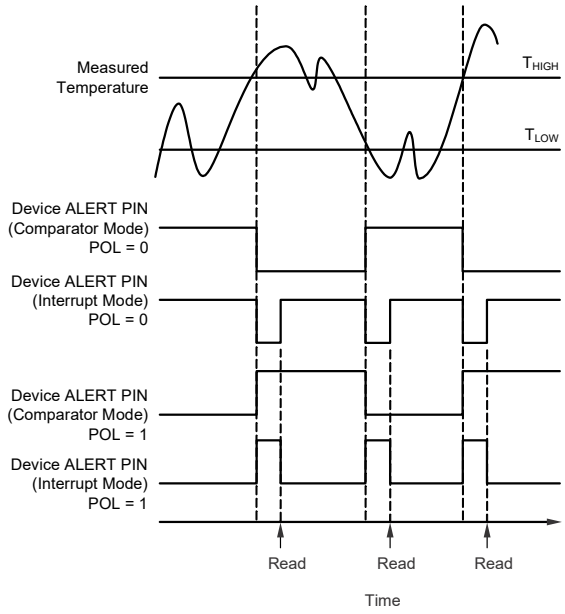


Figure 3. Output Transfer Function Diagrams

Fault Queue (F1/F0)
A fault condition exists when the measured temperature exceeds the user-defined limits set in the T_{HIGH} and T_{LOW} registers. Additionally, the number of fault conditions required to generate an alert may be programmed using the fault queue. The fault queue is provided to prevent a false alert as a result of environmental noise. The fault queue requires consecutive fault measurements in order to trigger the alert function. Table 9 defines the number of measured faults that may be programmed to trigger an alert condition in the device. For T_{HIGH} and T_{LOW} register format and byte order, see the *High- and Low-Limit Registers* section.

Table 9. Fault Settings

F1	F0	CONSECUTIVE FAULTS
0	0	1
0	1	2
1	0	4
1	1	6

One-Shot (OS)
When the device is in Shutdown Mode, writing a 1 to the OS bit starts a single temperature conversion. During the conversion, the OS bit reads '0'. The device returns to the shutdown state at the completion of the single conversion. For more information on the one-shot conversion mode, see the *One-Shot/Conversion Ready (OS)* section.

EM Bit
The Extended-Mode bit configures the device for Normal Mode operation (EM=0) or Extended Mode operation (EM=1). In normal mode, the temperature register, high-limit register, and low-limit register use a 12-bit data format. For more information on the extended mode, see the *Extended Mode (EM)* section.

Alert (AL Bit)

The AL bit is a read-only function. Reading the AL bit provides information about the comparator mode status. The state of the POL bit inverts the polarity of data returned from the AL bit. When the POL bit equals 0, the AL bit reads as 1 until the temperature equals or exceeds $T_{(HIGH)}$ for the programmed number of consecutive faults, causing the AL bit to read as 0. The AL bit continues to read as 0 until the temperature falls below $T_{(LOW)}$ for the programmed number of consecutive faults, when it again reads as 1. The status of the TM bit does not affect the status of the AL bit..

Conversion Rate

The conversion rate bits, CR1and CR0 located in the Configuration Register, configure the G756 for conversion rates of 8Hz, 4Hz (default), 1Hz, or 0.25Hz. The G756 has a typical conversion time of 26ms. To achieve different conversion rates, the G756 performs a single conversion and then powers down and waits for the appropriate delay set by CR1 and CR0. Table 10 shows the settings for CR1 and CR0.

Table 10. Conversion Rate Settings

CR1	CR0	CONVERSION RATE
0	0	0.25Hz
0	1	1Hz
1	0	4Hz (default)
1	1	8Hz

High- and Low-Limit Registers

The temperature limits are stored in the $T_{(LOW)}$ and $T_{(HIGH)}$ registers in the same format as the temperature result, and their values are compared to the temperature result on every conversion. The outcome of the comparison drives the behavior of the ALERT pin, which operates as a comparator output or an interrupt, and is set by the TM bit in the configuration register.

In Comparator mode (TM=0), the ALERT pin becomes active when the temperature equals or exceeds the value in T_{HIGH} and generates a consecutive number of faults according to fault bits F1 and F0. The ALERT pin remains active until the temperature falls below the indicated T_{LOW} value for the same number of faults.

In Interrupt mode (TM=1), the ALERT pin becomes active when the temperature equals or exceeds the value in T_{HIGH} for a consecutive number of fault conditions (as shown in Table 9). The ALERT pin remains active until a read operation of any register occurs, or the device successfully responds to the SMBus Alert Response address. The ALERT pin will also be cleared if the device is placed in Shutdown mode. Once the ALERT pin is cleared, it becomes active again only when temperature falls below T_{LOW}, and remains active until cleared by a read operation of any register or a successful response to the SMBus Alert Response address. Once the ALERT pin is cleared, the above cycle repeats, with the ALERT pin becoming active when the temperature equals or exceeds T_{HIGH}. The ALERT pin can also be cleared by resetting the device with the General Call Reset command. This action also clears the state of the internal registers in the device, returning the device to Comparator mode (TM=0).

Both operational modes are represented in Figure 1. Table 11 through Table 14 describe the format for the T_{HIGH} and T_{LOW} registers. Note that the most significant byte is sent first, followed by the least significant byte. Power-up reset values for T_{HIGH} and T_{LOW} are: T_{HIGH} = +80°C and T_{LOW} = +75°C. The format of the data for T_{HIGH} and T_{LOW} is the same as for the Temperature Register.

Table 11. Byte 1 Temperature Register HIGH(1)

D7	D6	D5	D4	D3	D2	D1	D0
H11	H10	H9	H8	H7	H6	H5	H4
(H12)	(H11)	(H10)	(H9)	(H8)	(H7)	(H6)	(H5)

(1) Extended mode 13-bit configuration shown in parenthesis.

Table 12. Byte 2 Temperature Register HIGH

D7	D6	D5	D4	D3	D2	D1	D0
H3	H2	H1	H0	0	0	0	0
(H4)	(H3)	(H2)	(H1)	(H0)	(0)	(0)	(0)

Table 13. Byte 1 Temperature Register LOW(1)

D7	D6	D5	D4	D3	D2	D1	D0
L11	L10	L9	L8	L7	L6	L5	L4
(L12)	(L11)	(L10)	(L9)	(L8)	(L7)	(L6)	(L5)

Table 14. Byte 2 Temperature Register LOW

D7	D6	D5	D4	D3	D2	D1	D0
L3	L2	L1	L0	0	0	0	0
(L4)	(L3)	(L2)	(L1)	(L0)	(0)	(0)	(0)

Bus Overview

The device that initiates the transfer is called a *master*, and the devices controlled by the master are *slaves*. The bus must be controlled by a master device that generates the serial clock (SMBCLK), controls the bus access, and generates the START and STOP conditions.

To address a specific device, a START condition is initiated, indicated by pulling the data line (SMBDATA) from a high to low logic level while SMBCLK is high. All slaves on the bus shift in the slave address byte on the rising edge of the clock, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the slave being addressed responds to the master by generating an Acknowledge and pulling SMBDATA low.

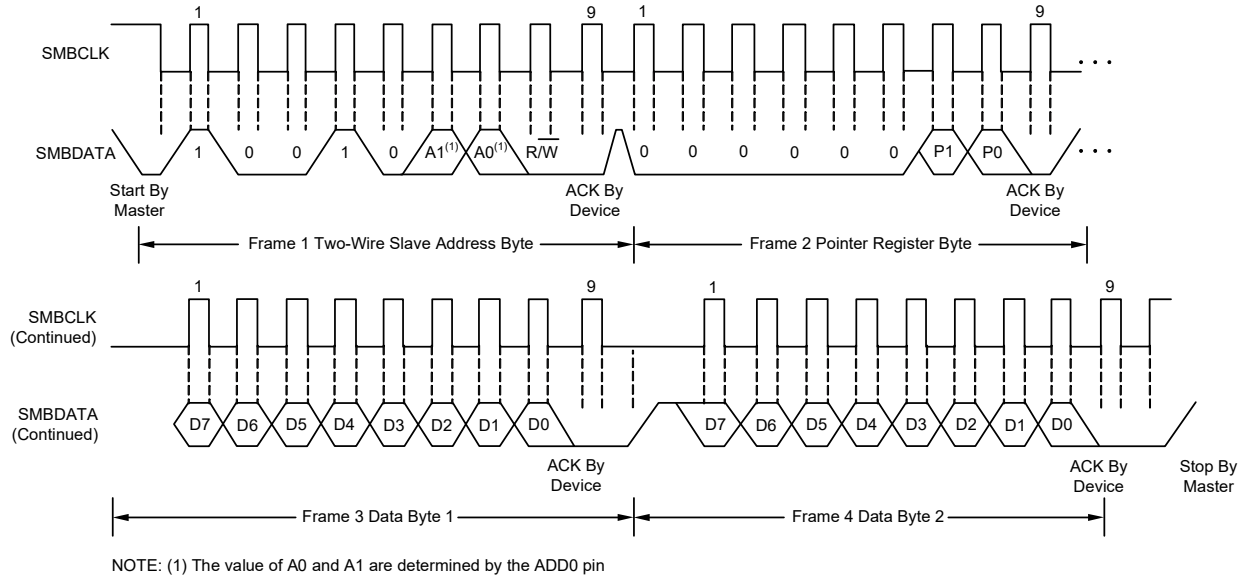
Data transfer is then initiated and sent over eight clock pulses followed by an Acknowledge Bit. During data transfer, SMBDATA must remain stable while SMBCLK is high, because any change in SMBDATA

while SMBCLK is high is interpreted as a START or STOP signal.

Once all data have been transferred, the master generates a STOP condition indicated by pulling SMBDATA from low to high , while SMBCLK is high.

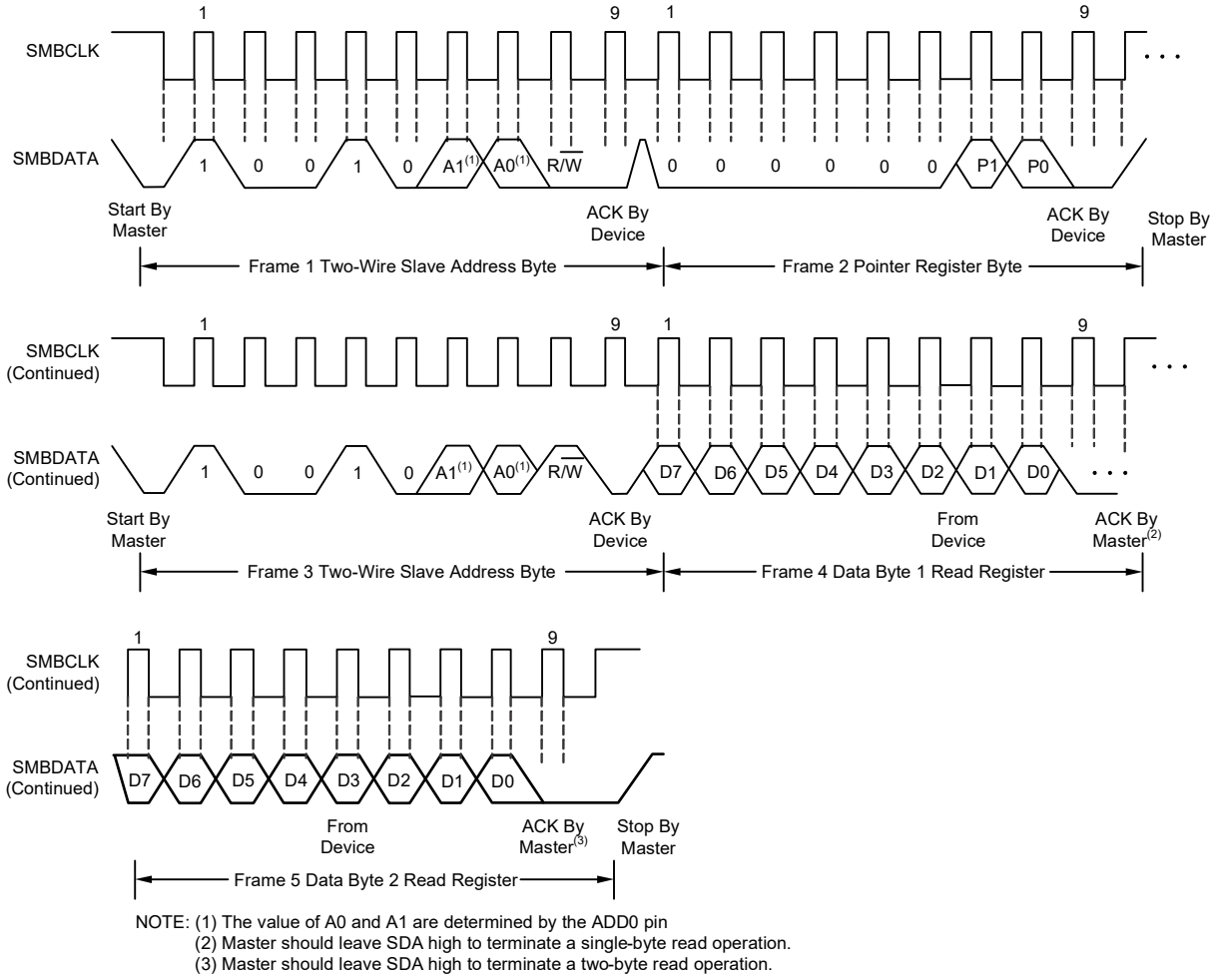
Serial Interface

The G756 operates as a slave device only on the two-wire bus and SMBus. Connections to the bus are made via the open-drain I/O lines SMBDATA and SMBCLK. The SMBDATA and SMBCLK pins feature integrated spike suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. The G756 Supports the transmission protocol for both fast (1kHz to 400kHz) and high-speed (1kHz to 2.85MHz) modes. All data bytes are transmitted MSB first.



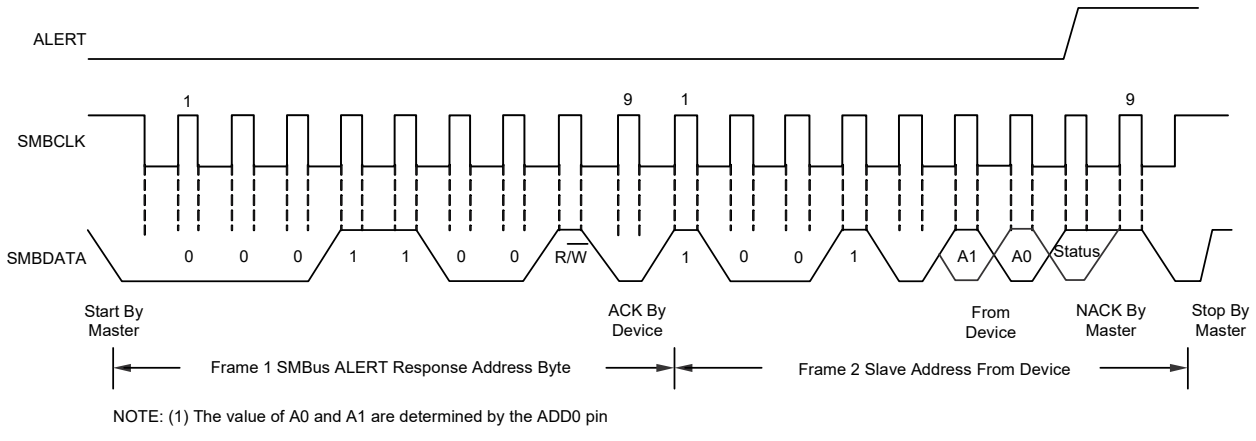
NOTE: (1) The value of A0 and A1 are determined by the ADD0 pin

Figure 4. Two-Wire Timing Diagram for Write Word Format



NOTE: (1) The value of A0 and A1 are determined by the ADD0 pin
(2) Master should leave SDA high to terminate a single-byte read operation.
(3) Master should leave SDA high to terminate a two-byte read operation.

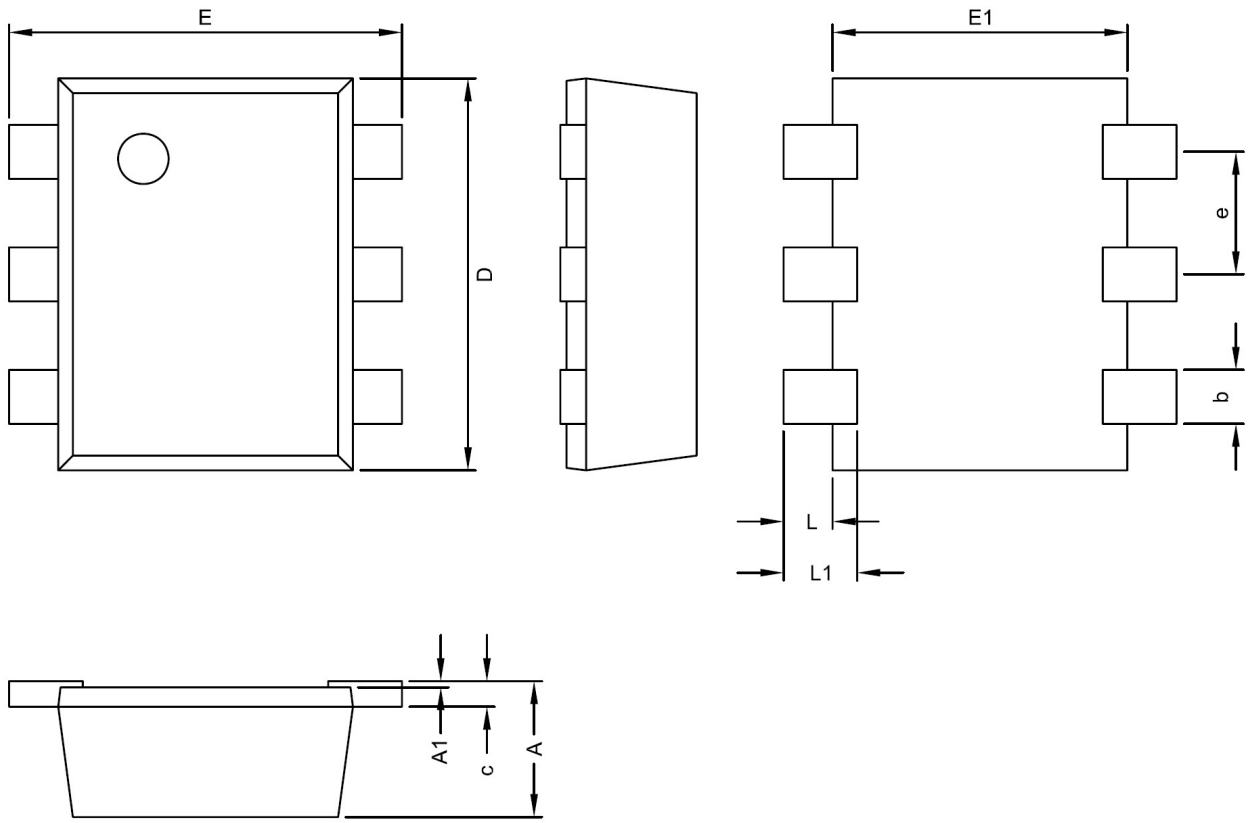
Figure 5. Two-Wire Timing Diagram for Read Word Format



NOTE: (1) The value of A0 and A1 are determined by the ADD0 pin

Figure 6. Timing Diagram for SMBus Alert

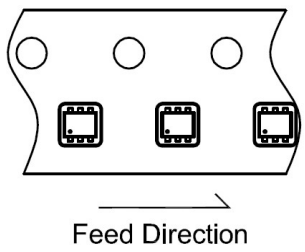
Package Information



SOT-563 Package

Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.525	- - -	0.600	0.021	- - -	0.024
A1	0.00	- - -	0.05	0.000	- - -	0.002
e	0.500 BSC			0.0197 BSC		
c	0.090	- - -	0.180	0.004	- - -	0.007
D	1.500	1.600	1.700	0.059	0.063	0.067
b	0.170	0.220	0.270	0.007	0.009	0.011
E1	1.100	1.200	1.300	0.043	0.047	0.051
E	1.500	1.600	1.700	0.059	0.063	0.067
L	0.100	0.200	0.300	0.004	0.008	0.012
L1	0.200	0.300	0.400	0.008	0.012	0.016

Taping Specification



PACKAGE	Q'TY/REEL
SOT-563	3,000 ea