

Fan Speed Controller with Linear or PWM Mode

Features

- SMBus Interface
- Linear or PWM Mode Speed Control
- Open or Close Loop Fan Speed Control
- Supply Voltage Range 3V~5.5V
- ADD0 Pin to Select 3 Different SMBus Addresses
- SMBus Alert # for G761
- G761 has Built-in Inverter for Crystal Oscillator
- Internal 32kHz clock generator, +/- 1% accuracy
- MSOP-10 for G761

Applications

- Notebook PC
- Industrial PC
- LAN Switch
- Servers
- Telecom equipment
- Industrial Control

General Description

The G761 is a single chip solution for fan speed control. It can be directly connected to the fan and performs close-loop or open-loop control. And there are two modes, PWM and linear, to drive the fan. It determined the current fan speed based on the fan rotation pulses and an externally supplied clock. The desired fan speed is programmed via the SMBus. The actual fan speed and fan status can be read via the SMBus. Short-circuit protection is implemented to prevent damages to the fan and the IC itself.

Ordering Information

ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE (Green)
G761P71U	G761	-55°C to +125°C	MSOP-10

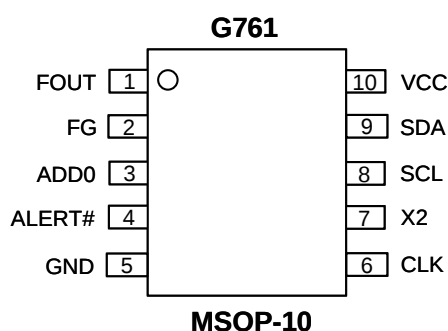
Note: P7:MSOP-10

1: Bonding Code

U: Tape & Reel

Green : Lead Free / Halogen Free.

Pin Configuration



Absolute Maximum Ratings

VCC to GND -0.3V to +6V
 SCL, SDA, FG, ADD0, CLK, FOUT -0.3V to +6V
 X2 ALERT# to GND
 SDA ALERT# Current -1mA to +50mA
 FOUT Current. -100mA to current limit
 ESD(HBM)2KV
 Thermal Resistance Junction to Ambient, (θ_{JA})
 MSOP-10 190°C/W

Continuous Power Dissipation ($T_A = +25^\circ\text{C}$)
 MSOP-10. 0.65W
 Thermal Resistance Junction to Case, (θ_{JC})
 MSOP-10. 70°C/W
 Operating Temperature Range -55°C to +125°C
 Junction Temperature +150°C
 Storage temperature Range -65°C to +165°C
 Reflow Temperature (soldering, 10sec) 260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

($V_{CC} = +5\text{V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.)

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Fan Controller					
FOUT Driver MOS On-resistance	SET_OUT=FFh, $I_{FOUT}=5\text{mA}$	---	1	---	Ω
FOUT Driver Current Limit	SET_OUT=FFh	---	1	---	A
FOUT Drive Current		---	500	---	mA
Fan Open Loop Output Differential Nonlinearity	$V_{CC}=5\text{V}$, I_{FAN} =Without Load	-1	---	1	LSB
Fan Open Loop Output Nonlinearity		-1	---	1	LSB
Fan Open Loop Output "code 1" Error		-2	---	2	LSB
Fan Open Loop Output Full Scale Error		-2	---	2	LSB
OUT PWM High-level Impedance	$I_{FOUT}=5\text{mA}$	---	1	---	Ω
OUT PWM Low-level Impedance	$I_{FOUT}=-160\mu\text{A}$	---	400	---	Ω
CLK Pin Input Clock Frequency	CLK	---	32768	---	kHz
FG Input High Threshold, V_{IH}	$V_{CC}=5\text{V}$	3	---	---	V
FG Input Low Threshold, V_{IL}	$V_{CC}=5\text{V}$	---	---	1	V
SMBus Interface					
Logic Input High Voltage	SMBCLK, SMBDATA; $V_{CC} = 4.5\text{V}$ to 5.5V	---	2.4	---	V
Logic Input Low Voltage	SMBCLK, SMBDATA; $V_{CC} = 4.5\text{V}$ to 5.5V	---	---	0.8	V
SMBDATA V_{OL} Logic Low Level Output Voltage	$I_{OL}=4\text{mA}$	---	---	0.4	V
ALERT Logic Output Low Current	ALERT, SMBDATA forced to 0.4V	6	---	---	mA
ALERT Output High Leakage Current	ALERT forced to 5.5V	---	1	---	μA
Logic Input Current	Logic inputs forced to V_{CC} or GND	-2	---	2	μA
SMBus Input Capacitance	SMBCLK, SMBDATA	---	5	---	pF
SMBus Clock Frequency		100	---	100k	Hz
SMBCLK Clock Low Time	t_{LOW} , 10% to 10% points	4.7	---	---	μs
SMBCLK Clock High Time	t_{HIGH} , 90% to 90% points	4	---	---	μs
SMBus Start-Condition Setup Time		4.7	---	---	μs
SMBus Repeated Start-Condition Setup Time	$t_{SU:STA}$, 90% to 90% points	4.7	---	---	μs
SMBus Start-Condition Hold Time	$t_{HD:STA}$, 10% of SMBDATA to 90% of SMBCLK	4	---	---	μs
SMBus Start-Condition Setup Time	$t_{SD:STO}$, 90% of SMBDATA to 10% of SMBDATA	4	---	---	μs
SMBus Data Valid to SMBCLK Rising- Edge Time	$t_{SU:DAT}$, 10% or 90% of SMBDATA to 10% of SMBCLK	800	---	---	ns
SMBus Data-Hold Time	$t_{HD:DAT}$	0	---	---	μs
SMBCLK Falling Edge to SMBus Data-Valid Time	Master clocking in data	---	---	1	μs

Note 1: Guaranteed but not 100% tested.

Note 2: Quantization error is not included in specifications for temperature accuracy.

SMBus Timing Diagram

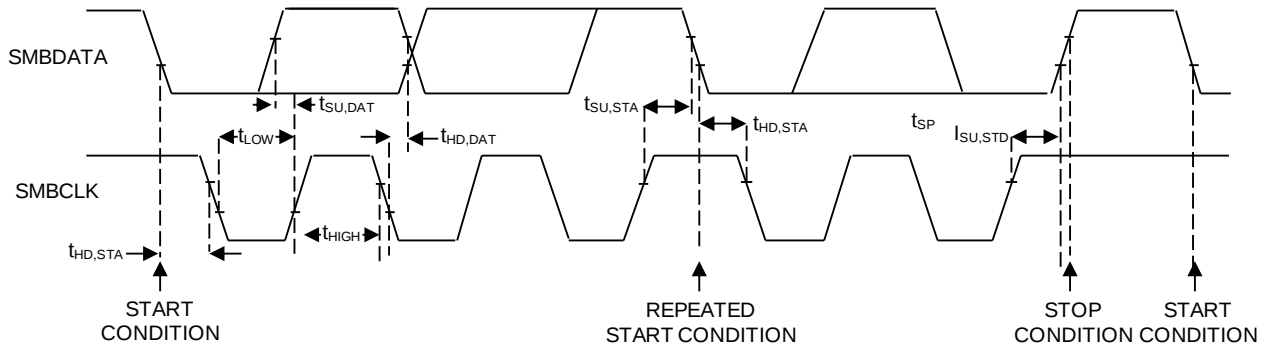


Figure 1. SMBus Timing Diagram

Function Description

FAN Speed Measurement

The fan speed is measured by counting the number of the CLK pin period between the rising edges of two fan speed pulses on FG pin. In this way, we are actually measuring the period of the fan speed. This number is stored in FAN_ACT_CNT register. This count number, N, is used in the FAN control algorithm, thus, the desired fan speed should be programmed by reading the corresponding count number. The count number is given by:

$$N = (\text{CLK} \times 15) / \text{RPM}$$

N : Count Number

RPM: FAN rotation speed, rotation per minute

For CLK = 32768Hz

$$\Rightarrow N = 491520 / \text{rpm}$$

For CLK = 16384Hz

$$\Rightarrow N = 245760 / \text{rpm}$$

Some selected count numbers are shown below

Table 1. Count numbers for different clock frequency

RPM	CLK=32768Hz	CLK=16384Hz
968	---	254
1935	254	127
2000	246	123
3000	164	82
4000	123	61
5000	98	49
6000	82	41
7000	70	35
8000	61	31
9000	55	27
10000	49	25
20000	25	12
30000	16	8

The formula of RPM versus FG_CLK_ID, FG_GEAR_MODE, FG_PLS_ID and SET_CNT (ACT_CNT) is

FG_CLK_ID: FG counting frequency

FG_GEAR_MODE: High speed fan setting factor

FG_PLS_ID: FG pulses number per revolution

Before setting the FAN_SET_CNT, make sure the FG_PLS_ID is fit the fan characteristic. Default FG_PLS_ID data bit is 0 for 2 pulses/ revolution.

FAN_SET_CNT (FAN_ACT_CNT) = N: Count Number

If FG_GEAR_MODE = 0 (default)

$$\text{FG_CLK_ID} = 0 \Rightarrow N = 491520 / \text{rpm}$$

$$\text{FG_CLK_ID} = 1 \Rightarrow N = 245760 / \text{rpm}$$

$$\text{FG_CLK_ID} = 2 \Rightarrow N = 122880 / \text{rpm}$$

Some FAN_SET_CNT selected count number are listed below. (Table 2)

Table 2. RPM vs. Count Number at different FG_CLK_ID data bits

RPM	CLK_ID=00	CLK_ID=01	CLK_ID=10
500	N/A	N/A	246
1000	N/A	246	123
2000	246	123	61
3000	164	82	41
4000	123	61	31
5000	98	49	25
6000	82	41	20
7000	70	35	18
8000	61	31	15
9000	55	27	14
10000	49	25	12
20000	25	12	N/A
30000	16	N/A	N/A

FAN Gear-Mode

As to high rotation speed type fan, the FG counting number is smaller than lower speed one and the speed controlling accuracy is less than 2% when rotation speed is over 9500rpm(FG_CLK_ID=0). To increase the accuracy of the speed controlling we designed the Gear-Mode to solve this problem.

Table 3. RPM vs. Count Number at different FG_GEAR_MODE data bits

RPM	FG_GEAR_MODE =00	FG_GEAR_MODE =01	FG_GEAR_MODE =10
2000	246	N/A	N/A
3000	164	N/A	N/A
4000	123	246	N/A
5000	98	197	N/A
6000	82	164	N/A
7000	70	140	N/A
8000	61	123	246
9000	55	109	218
10000	49	98	197
20000	25	49	98
30000	16	32	66

If FG_CLK_ID = 0 (default)

FG_GEAR_MODE = 0 => N = 491520 / rpm

FG_GEAR_MODE = 1 => N = 983040 / rpm

FG_GEAR_MODE = 2 => N = 1966080 / rpm

Some FAN_SET_CNT selected count number are listed below. (Table 3.)

Fan Protection and Fan Fail Detections

There are fan fail detection circuits for the fan. Setting bit 7 of FAN_CMD1 registers high to activate the detection of fan failure. G761 defines fan failure as no transition on FG pin for about 0.7sec if FAN_SET_DAC is not set to 00h in open-loop control mode (or FAN_SET_CNT is not set to FFh in closed-loop control mode). Bit 7~bit0 of status1 registers record the fan fail event. If fan failure events occur, ALERT pin goes low. To disable the fan-failure detection, set bit 7 of FAN_CMD1 register low.

In closed-loop control mode, if FAN actual RPM is 25% out of the programmed value for over 4 seconds (typical), bit in STATUS register is set low to indicate FAN out of control event. After the status of the 'Fan Out of Control' event is cleared by read, wait for over 4 seconds to read again to ensure that the OOC status is right. ALERT pin also goes low if this condition occurs. To disable the out of control detection, set bit 6 in FAN_CMD1 registers low.

FAN ACTUATION

FAN Driving Mode

G761 drives the FOUT pin with linear mode or PWM mode by setting register FAN_CMD1 bit 5 0 or 1, respectively, Default is linear mode.

Linear Mode

In linear driving mode, the OUT pin voltage is determined by an internal DAC which voltage range is from 1/5VCC to VCC voltage with 500mA output current capacity.

$$\frac{V_{cc}}{5} + (FAN_SET_DAC) \times \frac{1}{256} \times \frac{4}{5} V_{cc}$$

The DAC voltage is 512 levels in close-loop control mode and 256 levels in open-loop control mode.

PWM Mode

In PWM driving mode, the FOUT pin will output PWM waveform with 25kHz and amplitude from GND to VCC voltage. The duty is 512 levels in close-loop control mode and 256 levels in open-loop control mode.

FAN Control Mode

By setting register 04h[4] to 1, it enters close-loop control mode. Write it with 0, it enters open-loop control mode. Default value is 1, i.e., close-loop control mode.

Close-Loop Control

When it enters close-loop control mode, the driving voltage or duty is determined by the difference of register SET_CNT and ACT_CNT so that these two values become equal or 1 LSB error.

The SET_CNT is set by users. The ACT_CNT is obtained by counting FG rising edges using CLK pin frequency.

To stop the fan, program the fan speed register SET_CNT to 255.

Open-Loop Control

When it enters open-loop control mode, the driving voltage or duty is determined by FAN_SET_OUT register which makes a $2^8=256$ levels of output voltage or output duty. The SET_CNT is set by users. The ACT_CNT is obtained by counting FG rising edges using CLK pin frequency.

In open-loop mode, the ACT_CNT register is kept on updated by the FG counting value as in close-loop mode. In open-loop mode, the ACT_CNT won't be taken into account for output voltage or duty.

Fan Start up Voltage setting

To reduce the fan start up acoustic noise and fit the fan start up voltage G761 provide a register can select 4 kind of start up voltage. User set FAN_CMD2 register data bit1 and bit0 to determine the start up voltage.(Table 4.)

Table 4. Fan Start Up Voltage Vs. Code

FAN_CMD2 bit 1,0	Start Up Voltage (VCC=5)
00	1.0V(Code=0)
01	1.5V(Code=32)
10	2.0V(Code=64)
11	2.5V(Code=96)

Controlling Fan at Lower Speed

For stably controlling fans at lower rotation speed, three schemes are recommended as below:

- 1.Use larger decoupling capacitors between FOUT and GND.
- 2.Shunt a capacitor of 1μF-2μF on FG pin to GND.
- 3.Use fans with open-collector FG outputs.

When controlling fans under lower rotation speed, the output voltage of FOUT would be too low for fan to generate recognizable FG signals.

Using decouple capacitors on FOUT and FG is to increase the SNR on FG pins. While using fans with open_collector FG outputs can thoroughly solve the problem, because the logic high level of FG would be fixed to 5V.

Over Temperature for Output Driver

G761 provide over temperature protection function. When the chip temperature exceeds the high temperature threshold, 150°C typical, G761 will turn off the FOUT driving capacity.

SMBus Digital Interface

A standard SMBus 2-wire serial interface is used to read data or control the chip. The G761 employs standard SMBus protocols: Write Byte, Read Byte, which are depicted in SMBus Timing chart.

SMBus Slave Address Selection

G761 can be set to 3 different SMBus slave address by tying ADD0 pin to VCC, GND or let it be floating. The selection is as Table. 5 describes

Table. 5 ADD0 Slave Address Selection

ADD0	SMBus Slave Address						
	A6	A5	A4	A3	A2	A1	A0
VCC	0	1	1	1	1	1	0
Floating	1	0	0	1	0	0	0
GND	1	0	0	1	0	0	1

The G761 supports SMBus clock timeout function. When SMBCLK are held low for more than 30ms (typical) during an SMBus communication the G761 will reinitiate its bus interface and be ready for a new transmission.

Alert Function and Status Registers

Any changing of bits of STATUS registers which indicate alarm, ALERT pin outputs low. The ALERT interrupt signal is latched and can only be cleared by reading the Alert Response address (Table 6). ALERT function can be disable by setting MASK bit in FAN_CMD2 registers. The ALERT pin is open-drain output. Connect a 10kΩ resister from ALERT pin to V_{CC}.

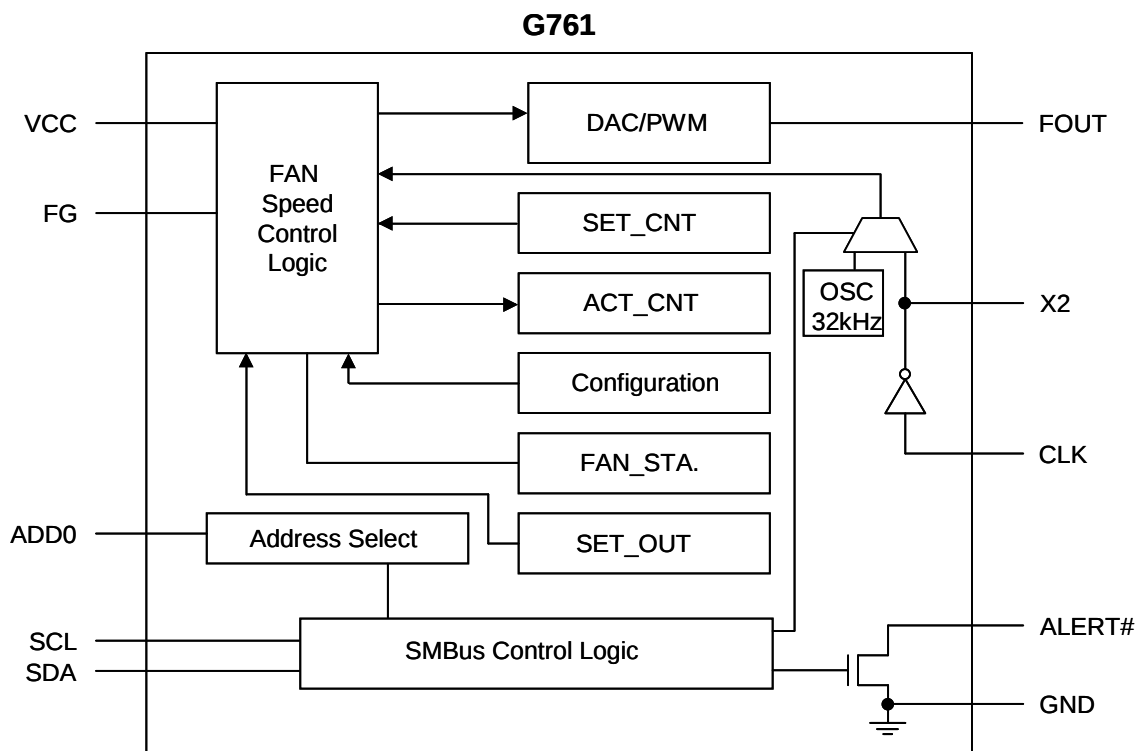
Table 6. Read Format for Alert Response Address (0001 100)

BIT	NAME
7(MSB)	ADD7
6	ADD6
5	ADD5
4	ADD4
3	ADD3
2	ADD2
1	ADD1
0(LSB)	1

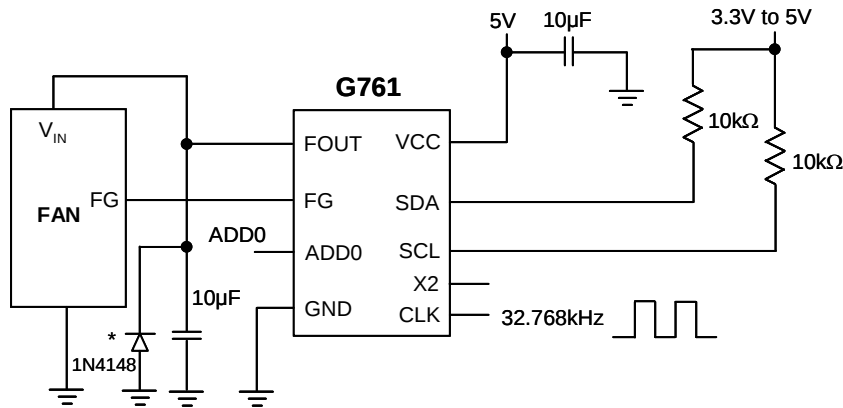
Pin Description

PIN	NAME	DIRECTION	FUNCTION
1	FOUT	Output	Output connected to fan driver circuit
2	FG	Input	Fan pulse input
3	ADD0	In/Out	SMBus slave address selection pin. VCC : 7'b0111_110 Float : 7'b1001_000 GND : 7'b1001_001
4	Alert#	Output	SMBus Alert output, open drain (no forward diode to VCC)
5	GND	Supply	Ground
6	CLK	Input	The input terminal of the built-in inverter for driving crystal.
7	X2	Output	The output terminal of the built-in inverter for driving crystal.
8	SCL	Input	SMBus serial clock input
9	SDA	In/Out	SMBus serial data input/output, open drain (no forward diode to VCC)
10	VCC	Supply	Supply Voltage

Block Diagram

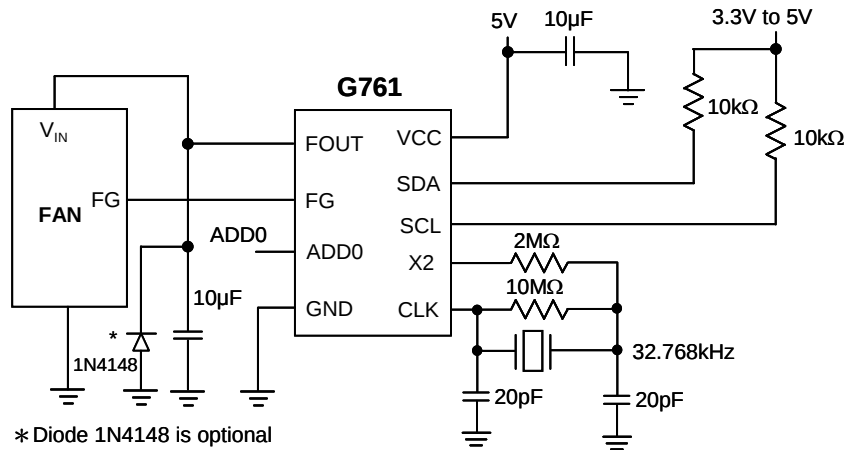


Application Circuit (Linear Mode)



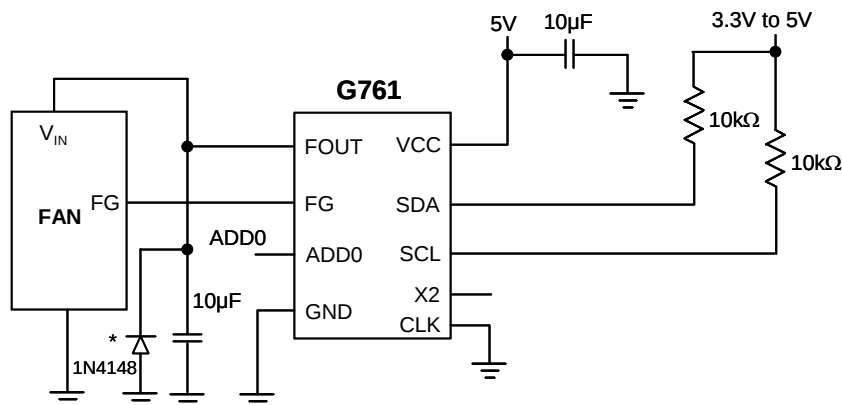
* Diode 1N4148 is optional
* CAP 10µF for linear mode

Use external oscillator



* Diode 1N4148 is optional
* CAP 10µF for linear mode

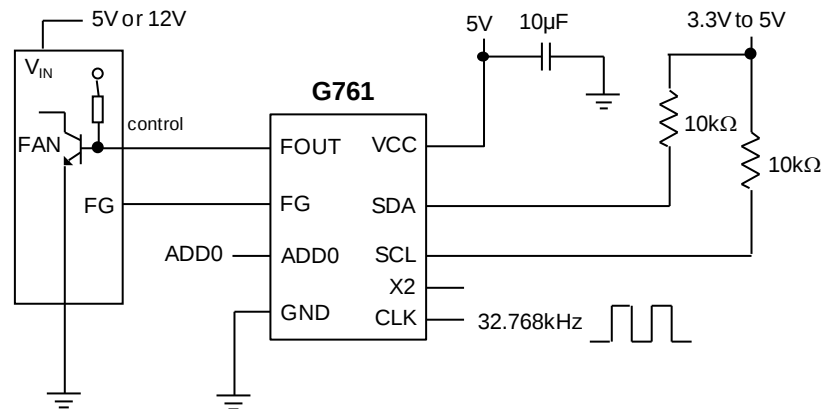
Use external crystal



* Diode 1N4148 is optional
* CAP 10µF for linear mode

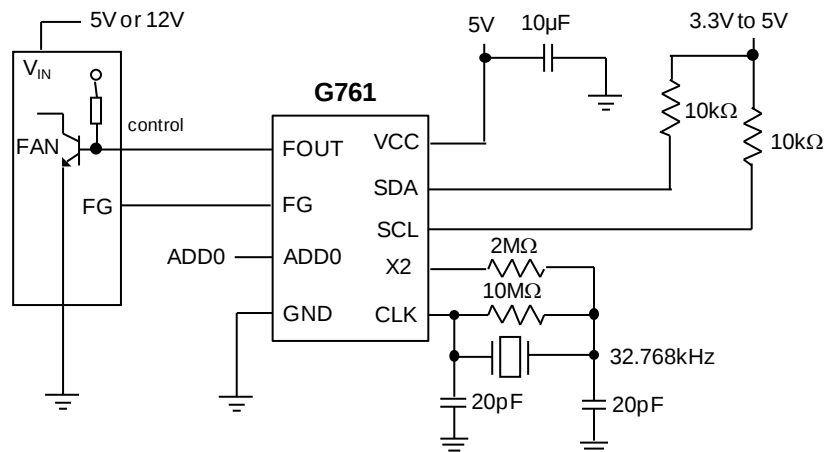
Use internal clock

Application Circuit (PWM Mode)



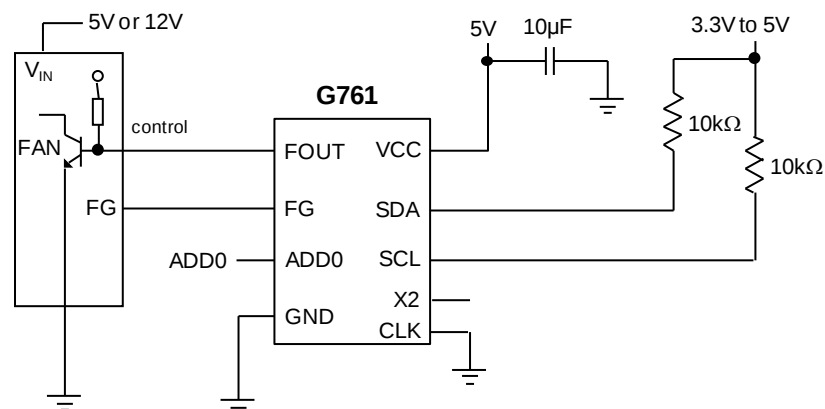
* FOUT, FG voltage must not be higher than G761's VCC

Use external oscillator



* FOUT, FG voltage must not be higher than G761's VCC

Use external crystal



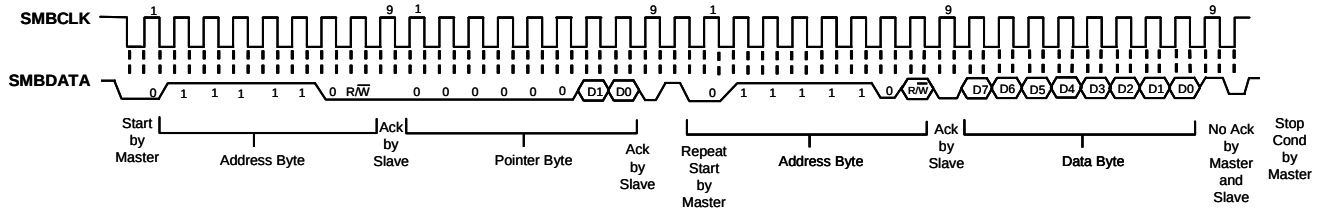
* FOUT, FG voltage must not be higher than G761's VCC

Use internal clock

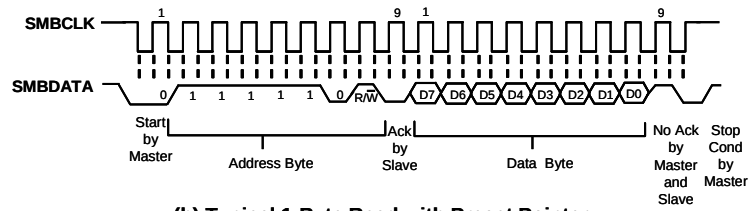
Registers Description

REGISTERS	COMMAND	POR	FUNCTION	R/W
FAN_SET_CNT	00h	11111111	Set FAN RPM in close loop control.	[7:0]R/W
FAN_ACT_CNT	01h	11111111	Read FAN RPM.	[7:0]R
STATUS	02h	xxxxxx01	Read status registers. bit 1: FAN_FAIL: FAN fail bit 0: FAN_OOC#: FAN out of control	[1:0]R
FAN_SET_OUT	03h	00000000	Set FAN output voltage/PWM duty in open loop control.	[7:0]R/W
FAN_CMD1	04h	00010000	Read/Write FAN Configuration registers. bit 7: DET_FAN_FAIL . bit 6: DET_FAN_OOC bit 5: OUT_MODE 1: PWM mode 0: linear mode bit 4: FAN_MODE 1:close-loop 0:open-loop. ID of clock which to count FG. bit 3: FG_CLK_ID1, bit 2: FG_CLK_ID0, [FG_CLK_ID1, FG_CLK_ID0] 00: Divide fan clock by 1 01: Divide fan clock by 2 10: Divide fan clock by 4 11: Divide fan clock by 8 PWM output palarity bit 1: PWM_PLARITY,1:negative duty, 0:positive duty FG pulses count per revolution bit 0: FG_PLS_ID, 0:2 Pulses count per revolution. 1:4 Pulses count per revolution.	[7:0]R/W
FAN_CMD2	05h	xx000001	Bit 5: 1 -> Use internal 32kHz clock. 0 -> Use external 32kHz clock. Bit 4: Mask ALERT# for G761. Bit 3,2: FG_GEAR_MODE. 0,1,2 -> $dT=T_{fg}/2$, $dT=T_{fg}$, $dT=2T_{fg}$ Bit 1,0: FAN_STARTV 0,1,2,3 -> 0,32,64,96 dac_code	[5:0]R/W

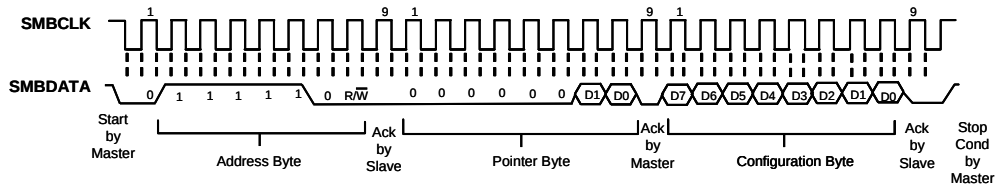
SMBus Timing



(a) Typical Pointer Set Followed by Immediate Read

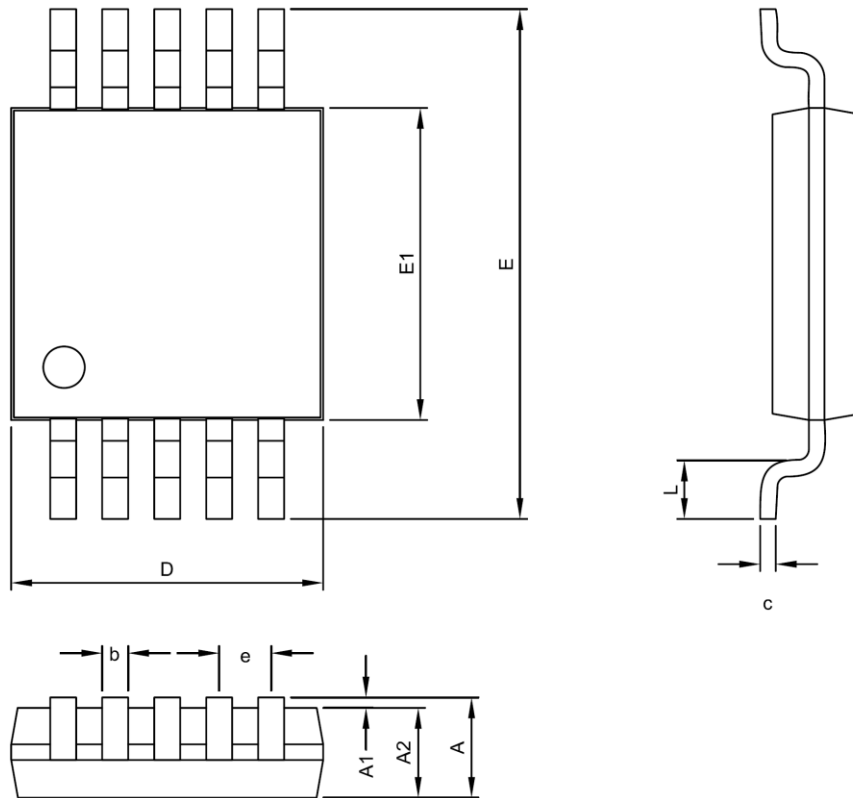


(b) Typical 1-Byte Read with Preset Pointer



(c) Register Write

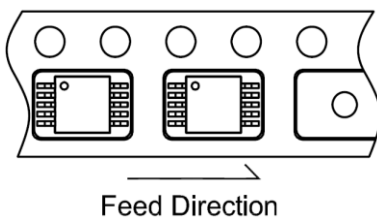
Package Information



MSOP-10 Package

Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.81	0.95	1.10	0.032	0.037	0.043
A1	0.00	---	0.15	0.000	---	0.006
A2	0.75	0.86	0.96	0.030	0.034	0.038
D	2.90	3.00	3.10	0.114	0.118	0.122
E	4.80	4.90	5.00	0.189	0.193	0.197
E1	2.90	3.00	3.10	0.114	0.118	0.122
b	0.15	0.25	0.35	0.006	0.010	0.014
c	0.15 REF			0.006 REF		
e	0.50 BSC			0.020 BSC		
L	0.4	0.53	0.8	0.016	0.021	0.031

Taping Specification



PACKAGE	Q'TY/REEL
MSOP-10	3,000 ea

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