1A Low Dropout Regulator with Enable

Features

- **Adjustable Output Low to 0.9V**
- **Input Voltage as Low as 1.0V and VPP Voltage 5V**
- **300mV Dropout @ 1A, VO 1.8V**
- **Over Current and Over Temperature Protection**
- **Enable Pin**
- **Low Reverse Leakage (Output to Input)**
- **SOP-8 (FD) Package**
- **0.9V/1.05V/1.2V/1.5V/1.8V/2.5V/3.3V Options by Setting ADJ Pin Below 0.2V and Adjustable Externally Using Resistors**
- **VO Pull Low Resistance when Disable**
- **VO Soft Start when Enable**

Applications

- **Battery-powered Device**
- **Portable Equipment**
- **Notebook Computers**

General Description

The G943 is a high performance positive voltage regulator designed for use in applications requiring very low Input voltage and very low dropout voltage at up to 1 amps. It operates with a V_{IN} as low as 0.9V and VPP voltage 5V with output voltage programmable as low as 0.9V. The G943 features ultra low dropout, ideal for applications where V_{OUT} is very close to V_{IN}. Additionally, the G943 has an enable pin to further reduce power dissipation while shutdown. The G943 provides excellent regulation over variations in line, load and temperature. A open-drain POK pin (G943F12U) indicates the output voltage status.

The G943 is available in the power SOP-8 (FD) package. It is available with 0.9V/1.05V/1.2V/1.5V/1.8V/2.5V/3.3V internally preset outputs that are also adjustable using external resistors.

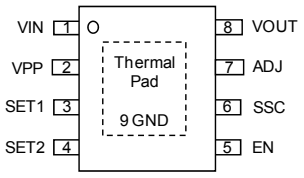
Ordering Information

ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE (Green)
G943F11U	G943A	-40°C~+85°C	SOP-8 (FD)
G943F12U	G943B	-40°C~+85°C	SOP-8 (FD)

Note: F1: SOP-8 (FD)
1&2: Bonding Code
U: Tape & Reel
Green: Lead Free / Halogen Free.

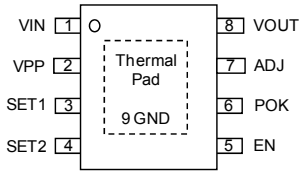
Pin Configuration

G943F11U



SOP-8 (FD)

G943F12U



SOP-8 (FD)

Note: Must connect the thermal pad to the ground.

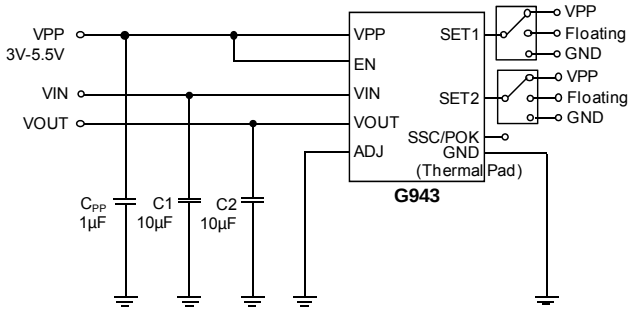
Fixed V_O Setting Table

SET1	SET2	VOUT
0	0	0.9
0	F	1.05
0	1	1.2
F	0	1.5
F	F	ADJ mode
F	1	1.5
1	0	1.8
1	F	2.5
1	1	3.3

0: pin voltage low, 1: pin voltage high, F:pin floating

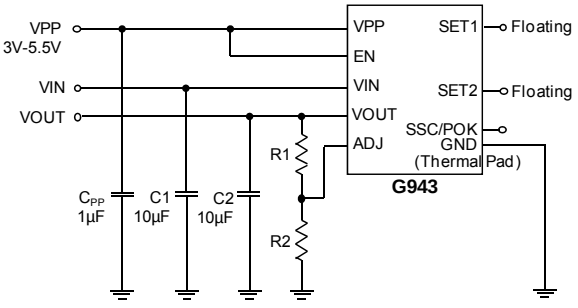
Typical Application Circuit

Pre-set Output Mode



Note: ADJ needs to be connected to ground under pre-set output mode.
Output voltage options are demonstrated in fixed Vo setting table.

ADJ Output Mode



$$VO = \frac{0.8\,(R1+R2)}{R2} \text{ Volts}$$

R2<120kΩ is recommended

Note: Both SET1 and SET2 need to be floating under ADJ mode.

Absolute Maximum Ratings (Note 1)

VPP, VIN, EN, ADJ, VOUT, SSC, SET1, SET2 Input Voltage 7V
Power Dissipation Internally Limited (Note 2)
Maximum Junction Temperature . . . . 150°C
Storage Temperature Range. . . . . -65°C ≤T_J ≤ +150°C
Reflow Temperature (soldering, 10sec) . . . . . 260°C
Thermal Resistance Junction to Ambient, (θ_{JA})
SOP-8 (FD) . . . . . 42°C/W (Note 3)
Continuous Power Dissipation (T_A = +25°C)
SOP-8 (FD) . . . . . 3.0W (Note 3)
Thermal Resistance Junction to Case, (θ_{JC})
SOP-8 (FD) . . . . . 12°C/W

Operation Conditions

VIN Voltage . . . . . 1V~5.5V
VPP Voltage . . . . . .3V~5.5V
(VPP ≥ VIN for normal operation)
Temperature Range. . . . . -40°C ≤T_A ≤ +85°C

Electrical Characteristics

V_{PP}=5V, V_{IN} =3.3V, V_{EN}=V_{PP}, I_O=10mA, C_{IN}=10µF, C_{OUT} =10µF, T_A=T_J=25°C.

The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified.

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
VIN						
Input Voltage Range	V_{IN}	V_{IN} > V_O	1.0	---	5.5	V
VPP						
V_{PP} Voltage Range	V_{PP}	V_{PP}>Vo+1V and V_{PP}>3V V_{PP}>Vo+1.7V for Io=1A	3	---	5.5	V
V_{PP} Current	I_{PPH}	V_O=1.2V	---	60	90	µA
	I_{PPL}	EN=0V	---	0.1	1	µA
VOUT						
Output Voltage	V_O	Internally set voltage V_{IN}=V_O+0.5V	0.882	0.9	0.918	V
			1.029	1.05	1.071	
			1.176	1.2	1.224	
			1.47	1.5	1.53	
			1.764	1.8	1.836	
			2.45	2.5	2.55	
			3.234	3.3	3.366	
		Externally set voltage V_{IN}=V_O+0.5V $V_{O(S)}$: V_O voltage setting	$V_{O(S)}$ -2%	$V_{O(S)}$	$V_{O(S)}$ +2%	V
Line Regulation		V_{IN}=(V_O+0.5V) to 5.5V, I_{OUT}=100mA ($\Delta V_{OUT}/\Delta V_{IN}$*$V_{OUT}$)	---	0.05	0.2	%/V
Ripple Rejection		f=1kHz	---	70	---	db
Load Regulation		10mA≤I_O≤1A	---	0.2	1	%
Dropout Voltage	V_D	I_O=1A, V_O=1.8V	---	300	---	mV
Short Circuit Current			---	200	---	mA
Current Limit	I_{LIM}		1.2	---	---	A
V_O Pull Low Resistance		V_{EN}=0V	---	35	---	Ω
Soft Start Time	T_{SS}	Css: Capacitor on SSC pin V_{IN}=V_O+1V, I_{OUT}=1A Css=3nF Time period when V_{SSC} rises from 0V to 0.8V	---	2	---	mS
		Css: Capacitor on SSC pin V_{IN}=V_O+1V, I_{OUT}=1A Css=0nF Time period when V_{SSC} rises from 0V to 0.8V	---	0.2	---	
ADJ						
Reference Voltage	V_{REF}	V_{ADJ}=V_O	0.784	0.8	0.816	V
Adjust Pin Current	I_{ADJ}		---	20	100	nA
Adjust Pin Threshold			0.15	0.2	0.25	V

Electrical Characteristics (continued)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
EN						
EN Pin Voltage High	V_{ENH}		1.2	---	---	V
EN Pin Voltage Low	V_{ENL}		---	---	0.4	V
EN Pin Pull Down Resistor	R_{EN}		---	2.5	---	MΩ
SET1, SET2						
SET1, SET2 Pin Voltage High	V_{SET1H},V_{SET2H}		V_{PP}-0.5	---	---	V
SET1, SET2 Pin Voltage Low	V_{SET1L},V_{SET2L}		---	---	0.5	V
Over Temperature Protection						
Over Temperature	T_{OT}		---	150	---	°C
Over Temperature Hysteresis	T_{OTHY}		---	30	---	°C

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Conditions are conditions under which the device functions but the specifications might not be guaranteed. For guaranteed specifications and test conditions see the Electrical Characteristics.

Note 2: The maximum power dissipation is a function of the maximum junction temperature, T_{Jmax}; total thermal resistance, θ_{JA}, and ambient temperature T_A. The maximum allowable power dissipation at any ambient temperature is $(T_{jmax}-T_A)/\theta_{JA}$. If this dissipation is exceeded, the die temperature will rise above 150°C and IC will go into thermal shutdown.

Note 3: The package is placed on a 2-layer PCB (1oz/1oz) with 3vias.Please refer to Demo Board Footprint section.

Output Voltage Setting Option

Fixed V_O Setting Table:

SET1	SET2	VOUT	Recommended VIN
0	0	0.9	1.5~1.8
0	F	1.05	1.5~1.8
0	1	1.2	1.8~3.3
F	0	1.5	2.5~3.3
F	F	ADJ mode	NA
F	1	1.5	2.5~3.3
1	0	1.8	2.5~3.3
1	F	2.5	3.3
1	1	3.3	5

*0: pin voltage low, 1: pin voltage high, F: pin floating

External V_O Setting:

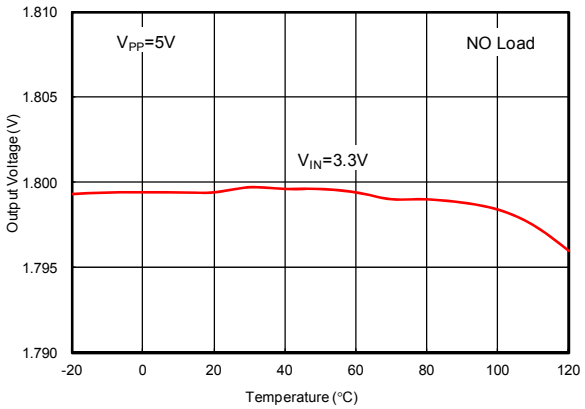
$Vo=\{(R1+R2)/R2\}*V_{ADJ}$

*If ADJ pin is connected to ground, V_O follows internal V_O setting.
*ADJ pin has the priority than SET1 pin and SET2 pin.

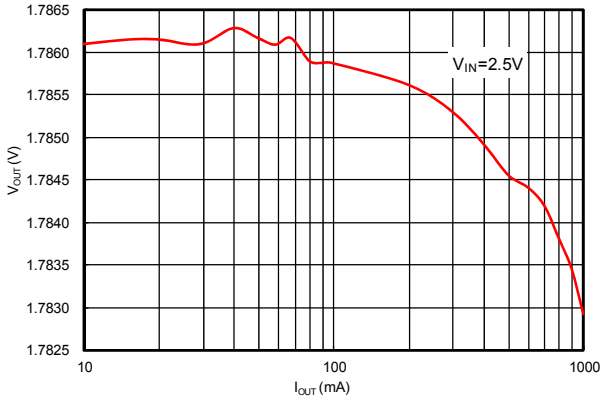
Typical Performances Characteristics

V_{PP}=5V, V_{IN} =3.3V, V_{EN}=V_{PP}, I_O=10mA, C_{IN}=10µF, C_{OUT}=10µF, T_A=25°C.

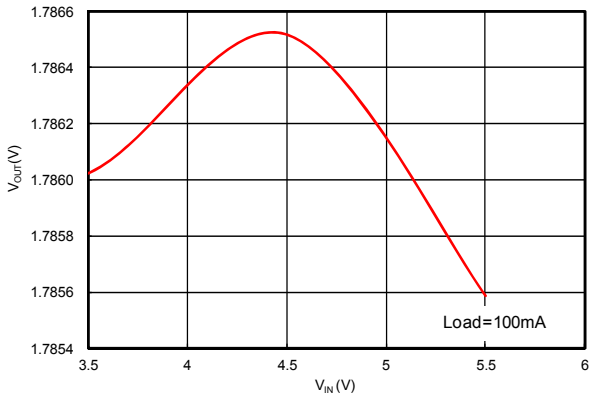
Output Voltage vs. Temperature



V_{OUT} vs. I_{OUT}

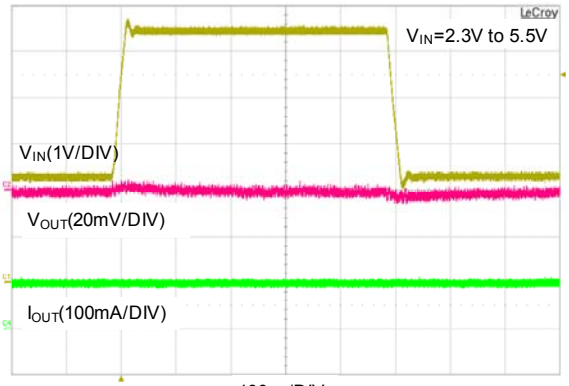


V_{OUT} vs. V_{IN}

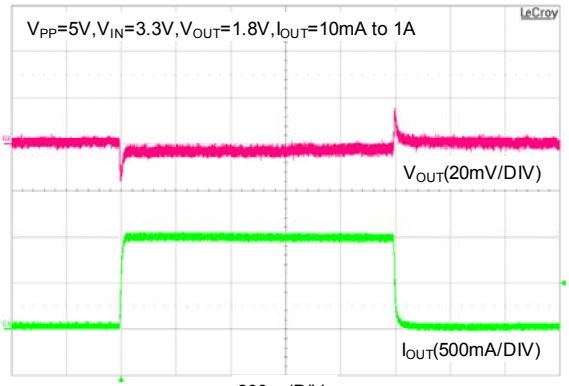


Typical Performances Characteristics (continued)

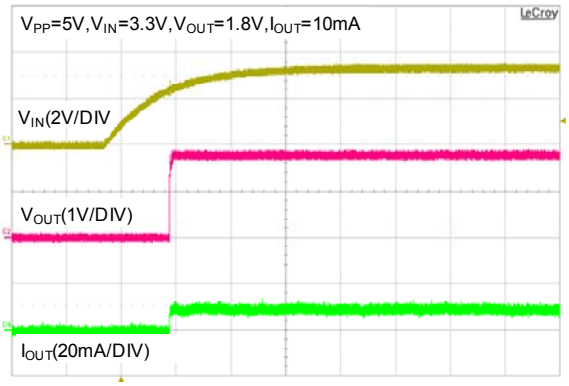
Line Transient



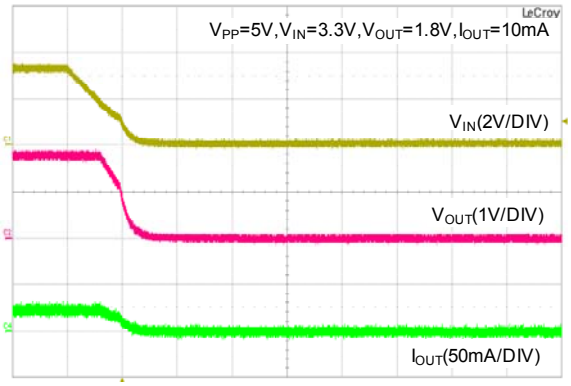
Load Transient



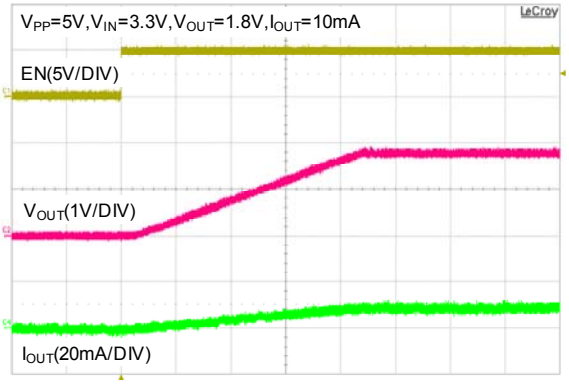
VIN Power On



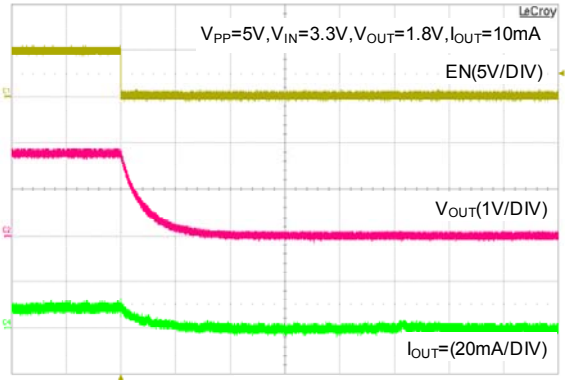
VIN Power Off



EN Power On

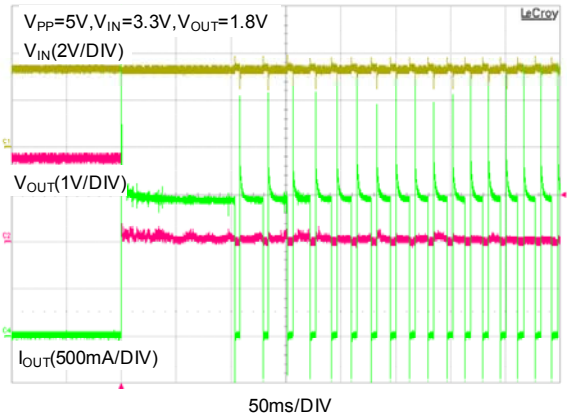


EN Power Off

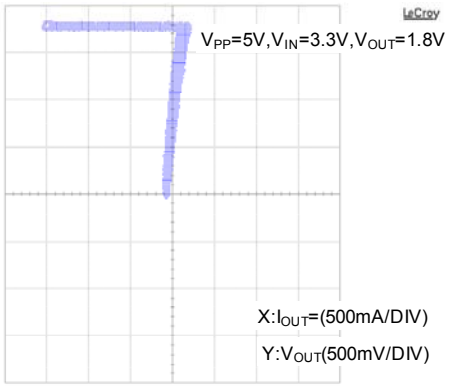


Typical Performances Characteristics (continued)

Short Circuit

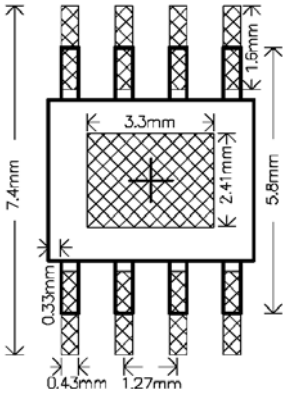


OC Protection Waveform



Minimum Footprint PCB Layout Section

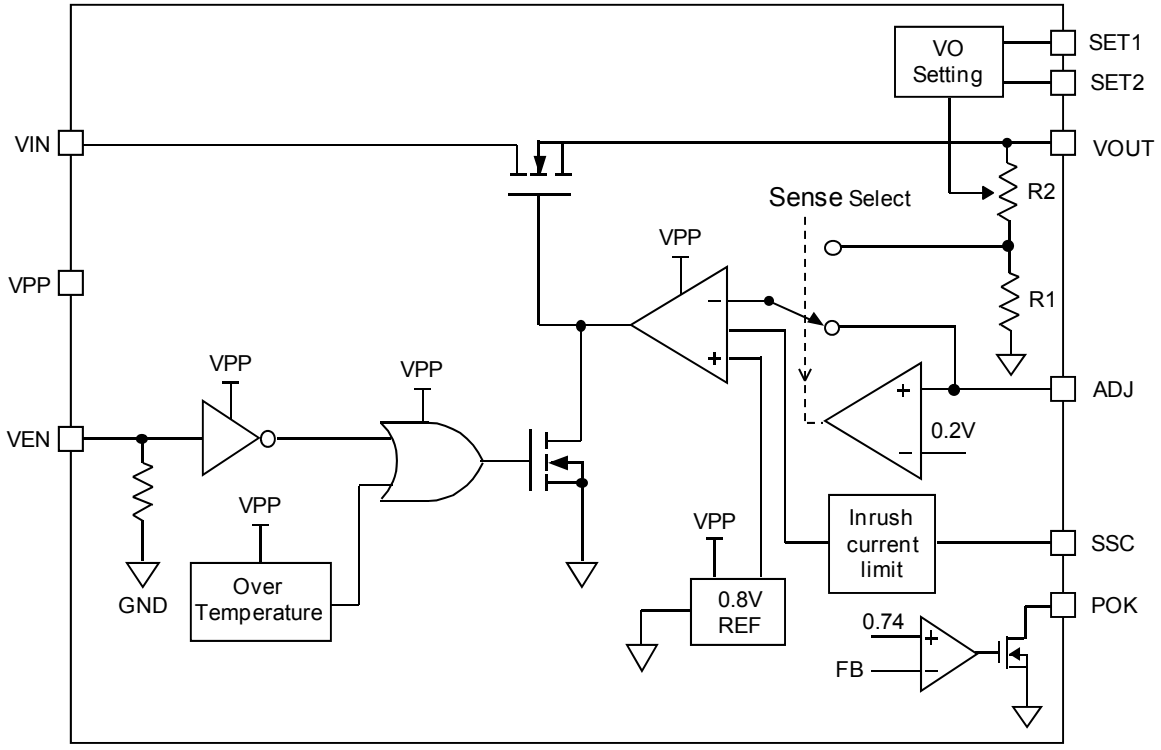
SOP-8 (FD)



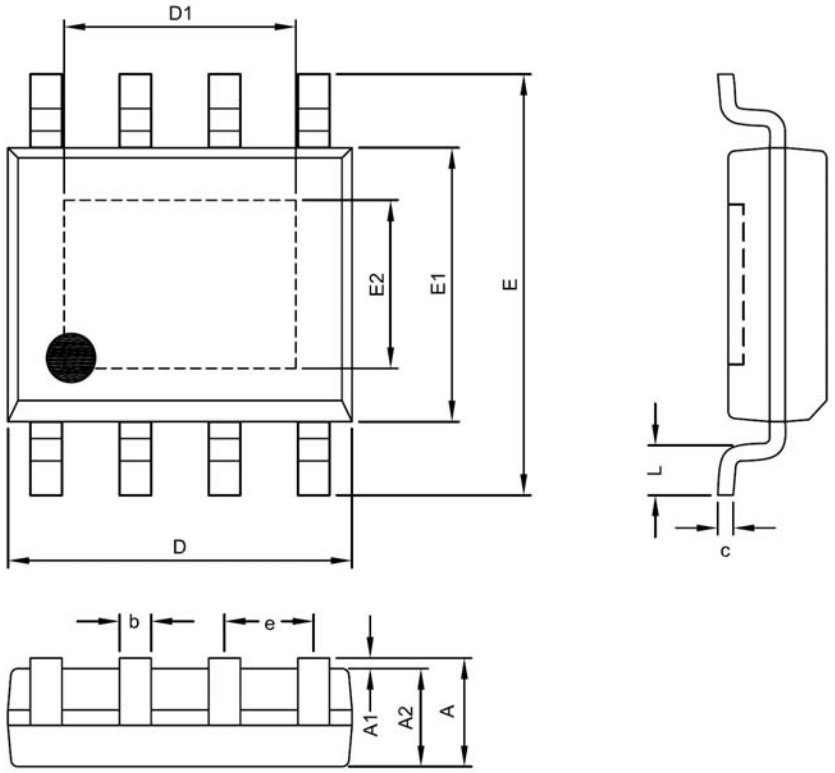
Pin Description

PIN		NAME	FUNCTION
G943F11U	G943F12U		
1	1	VIN	Input voltage. Large bulk capacitance should be placed closely to this pin. A 10μF ceramic capacitor is recommended at this pin.
2	2	VPP	Input voltage for controlling circuit.
3	3	SET1	Output voltage setting pin. Pull-high:1,Pull-Low;0
4	4	SET2	Output voltage setting pin. Pull-high:1,Pull-Low;0
5	5	EN	Enable Input. Pulling this pin below 0.4V turns the regulator off, reducing the quiescent current to a fraction of its operating value. The device will be disabled if this pin is left open.
6	---	SSC	Inrush current limit pin.
---	6	POK	Open-drain Power Good. Use a 10kΩ resistor to connect POK pin to VPP. When V_{ADJ} rises beyond 0.74V, POK will be high(closed to VPP). When V_{ADJ} falls below 0.7V, POK will be low(closed to ground).
7	7	ADJ	Resistor ratio of external feedback for output voltage by VO = 0.8*(R1+R2)/R2 Volts
8	8	VOUT	The power output of the device. A pull low resistance exists when device deactivated by EN pin.
Thermal PAD		GND	

Block Diagram



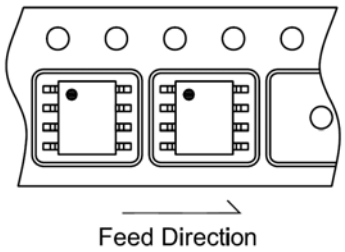
Package Information



SOP- 8 (FD) Package

Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.35	1.55	1.70	0.053	0.061	0.067
A1	0.00	- - -	0.10	0.000	- - -	0.004
A2	1.15	1.35	1.60	0.045	0.053	0.063
D	4.80	4.90	5.00	0.189	0.193	0.197
D1		3.30 BSC			0.130 BSC	
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
E2		2.41 BSC			0.095 BSC	
c		0.20 REF			0.008 REF	
b	0.33	0.43	0.53	0.013	0.017	0.021
e		1.27 BSC			0.050 BSC	
L	0.40	0.70	1.27	0.016	0.028	0.050

Taping Specification



PACKAGE	Q'TY/REEL
SOP-8 (FD)	2,500 ea