4X Linear Fan Driver for 12V DC Fan

Features

- **VO Follows 4.0 Times of VSET**
- **0.5V Dropout @ 0.5A**
- **Over Current and Over Temperature Protection**
- **Enable Pin**
- **100µA Quiescent Current in Shutdown**
- **Power TO-252-5, SOP-8, SOP-8 with power pad Package**

Applications

- **Notebook Computer Fan Driver**
- **Projector Cooling Fan**
- **Battery Powered Systems**
- **Motherboards**
- **Peripheral Cards**

General Description

The G994 is a high performance positive voltage regulator designed for use in applications requiring very low dropout voltage at up to 0.5 Amps. The G994 VO output voltage follows the 4.0 times of VSET voltage until it reaches VIN voltage. The VSET voltage must be larger than 1V to guarantee VO 4.0 times of VSET. An enable pin further reduces power dissipation while shut down. The G994 provides excellent regulation over variations in line, load and temperature.

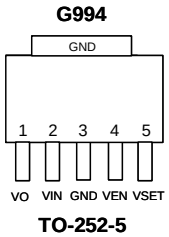
The G994 is available in the power TO-252-5, SOP-8 and SOP-8 with power pad package.

Ordering Information

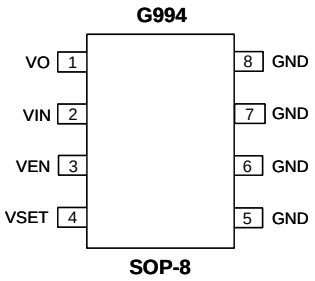
ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE (Pb free)
G994TJU	994	-40°C ~ +85°C	TO-252-5
G994P1U	G994	-40°C ~ +85°C	SOP-8
G994F1U	G994	-40°C ~ +85°C	SOP-8 (FD)

Note: TJ: TO-252-5 P1: SOP-8 F1:SOP (FD)
U: Tape & Reel

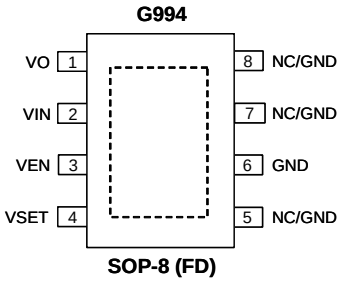
Pin Configuration



TO-252-5

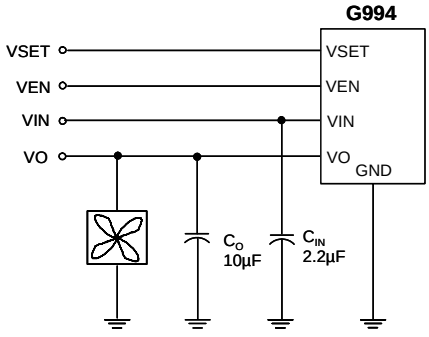


SOP-8

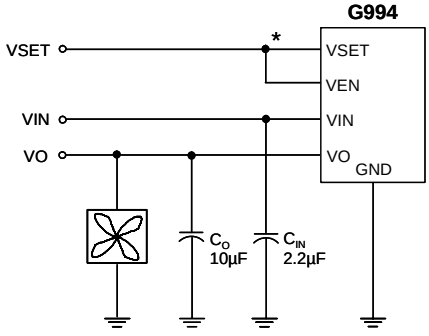


SOP-8 (FD)

Typical Application Circuit



VO =4 X VSET



VO =4 X VSET

* : V_{SET} < 0.3V Disable; V_{SET} >1V Enable

Absolute Maximum Ratings (Note 1)

Input Voltage 24V
V_{SET}, V_{EN} Voltage. 6V
Power Dissipation Internally Limited (Note 2)
Maximum Junction Temperature . . . . . .150°C
Storage Temperature Range . . . . -65°C ≤T_J ≤ +150°C
Reflow Temperature (soldering, 10sec). . . . . .260°C
Thermal Resistance Junction to Ambient, (θ_{JA}) (Note 3)
TO-252-5 . . . . . 100°C/W
SOP-8 . . . . . 125°C/W
SOP-8 (FD) . . . . . 110°C/W
Thermal Resistance Junction to Case, (θ_{JC})
TO-252-5 . . . . . .12°C/W
SOP-8 . . . . . 39°C/W
SOP-8 (FD) . . . . . .12°C/W
ESD Rating (Human Body Model) 2kV
Input Voltage . . . . . .10V ~20V
Temperature Range . . . . . -40°C ≤T_A ≤ +85°C

Electrical Characteristics

V_{SET}=2V, V_{EN}=5V, V_{IN}=15V, I_O=0.5A, C_{IN}=2.2µF, C_{OUT}=10µF, T_A=T_J=25°C unless otherwise specified (Note 4)

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
VIN					
Supply Voltage Range		10	---	20	V
Quiescent Current	V_{EN} = 5V	---	3	--	mA
	V_{EN} = 0V	---	100	--	µA
VO					
Output Voltage/V_{SET} voltage	V_{SET} = 2V	7.76	8	8.24	V/V
Line Regulation	V_{IN} = 10V to 20V	---	0.1	0.5	%
Load Regulation	V_{SET} = 3V 10mA ≤ I_O ≤ 0.5A	---	0.5	2	%
Output Resistance	I_O = 0.5A,V_{SET} = 4V	---	0.7	2	Ω
Short Circuit Current		---	0.2	---	A
VSET					
Minimum V_{SET} voltage		---	1	5.5	V
V_{SET} pin Current		---	100	300	nA
VEN					
V_{EN} Voltage High		1	---	---	V
V_{EN} Voltage Low		---	---	0.3	V
V_{EN} pin Bias Current	V_{EN} = 0V	---	3	10	µA
Over Temperature Protection					
Over Temperature		---	150	---	°C
Over Temperature Hysteresis		---	25	---	°C

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Conditions are conditions under which the device functions but the specifications might not be guaranteed. For guaranteed specifications and test conditions see the Electrical Characteristics.

Note2: The maximum power dissipation is a function of the maximum junction temperature, T_{Jmax} ; total thermal resistance, θ_{JA}, and ambient temperature T_A. The maximum allowable power dissipation at any ambient temperature is (T_{jmax}-T_A) / θ_{JA}. If this dissipation is exceeded, the die temperature will rise above 150°C and IC will go into thermal shutdown.

Note3: The package is placed on a 2-layer PCB (1oz/1oz) with minimum footprint.

Note4: Low duty pulse techniques are used during test to maintain junction temperature as close to ambient as possible.

Definitions

Line Regulation

The change in output voltage for a change in input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that average chip temperature is not significantly affected.

Load Regulation

The change in output voltage for a change in load current at constant chip temperature. The measurement is made under conditions of low dissipation or by using pulse techniques such that average chip temperature is not significantly affected.

Maximum Power Dissipation

The maximum total device dissipation for which the regulator will operate within specifications.

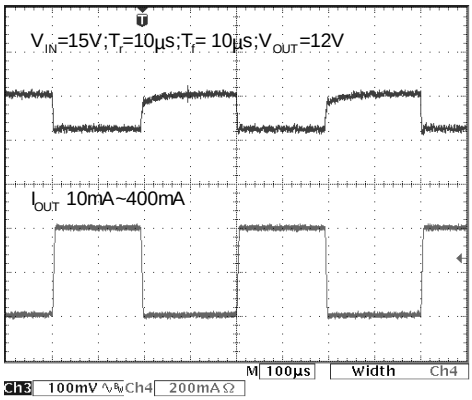
Quiescent Bias Current

Current which is used to operate the regulator chip and is not delivered to the load.

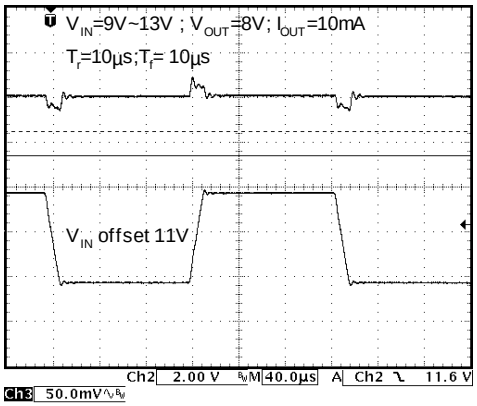
Typical Performance Characteristics

V_{SET}=2V, V_{EN}=5V, V_{IN}=15V, I_O=0.5A, C_{IN}=2.2µF, C_{OUT}=10µF, T_A=T_J=25°C.

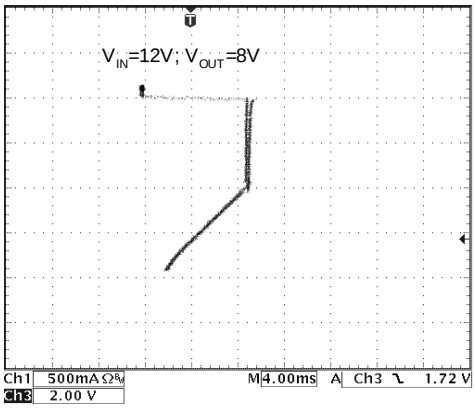
Load Transient



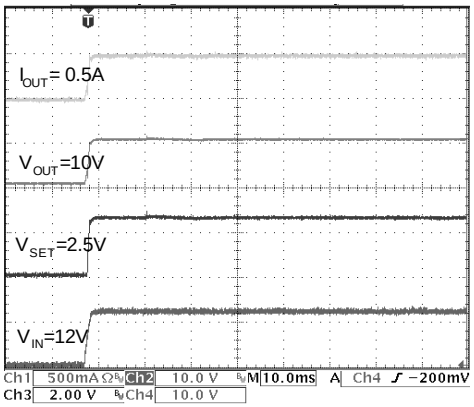
Line Transient



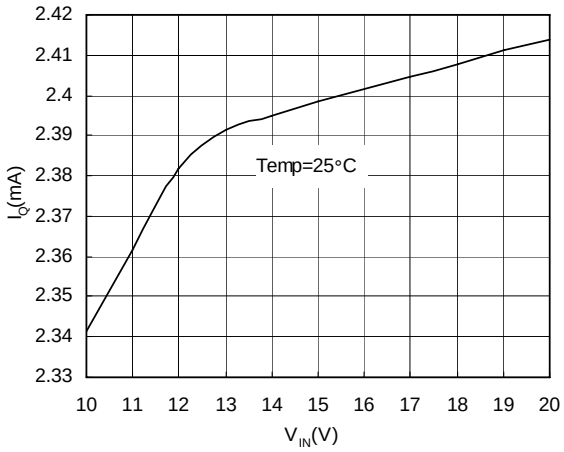
Overcurrent Protection Characteristics



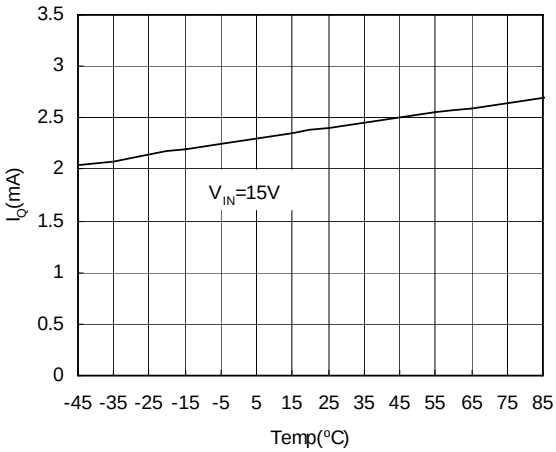
Start-UP



Quiescent Current vs. V_{IN}

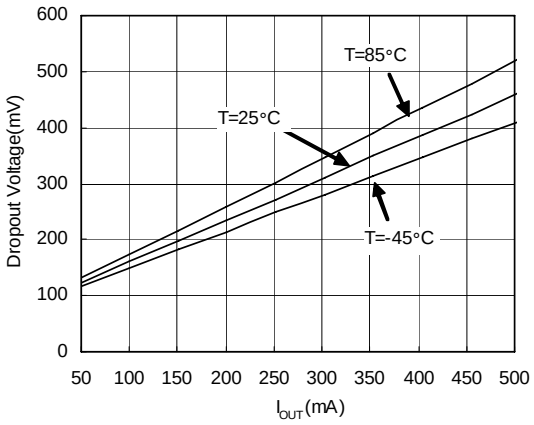


Quiescent Current vs. Temperature

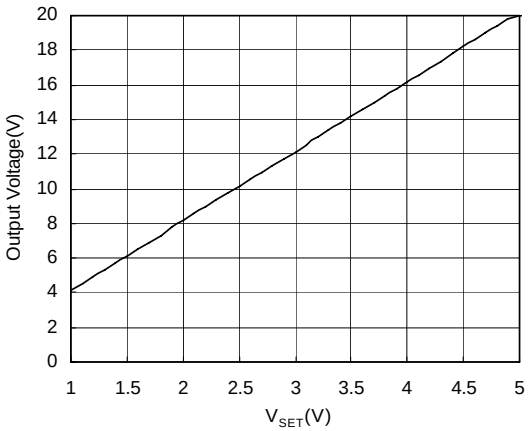


Typical Performance Characteristics (continued)

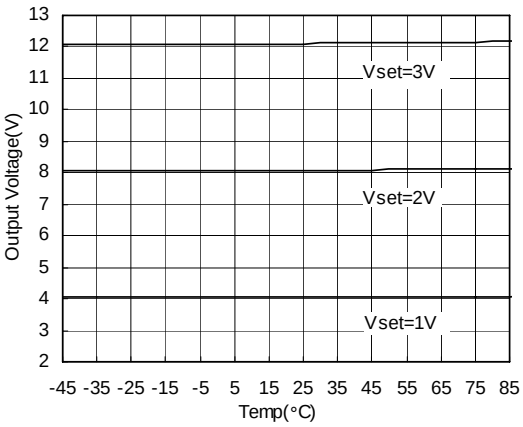
Dropout Voltage vs. I_{OUT}



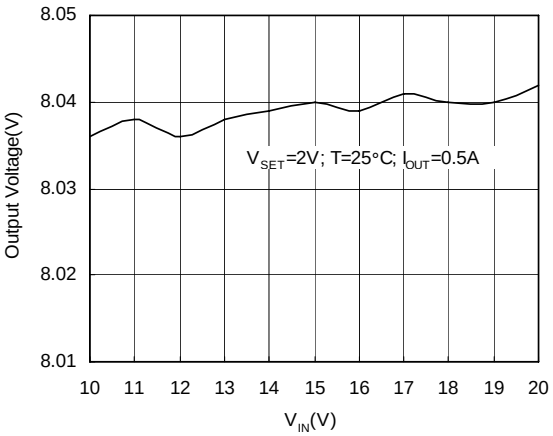
Output Voltage vs. V_{SET}



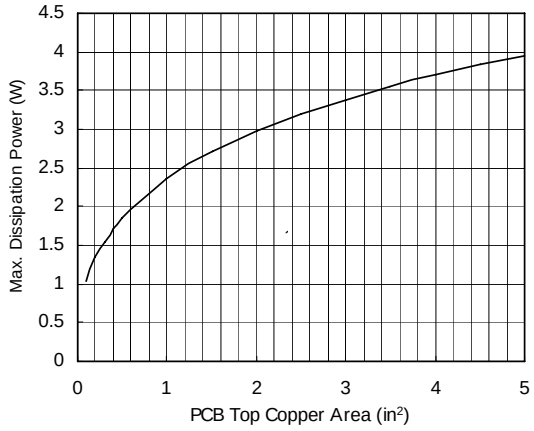
Output Voltage vs. Temperature



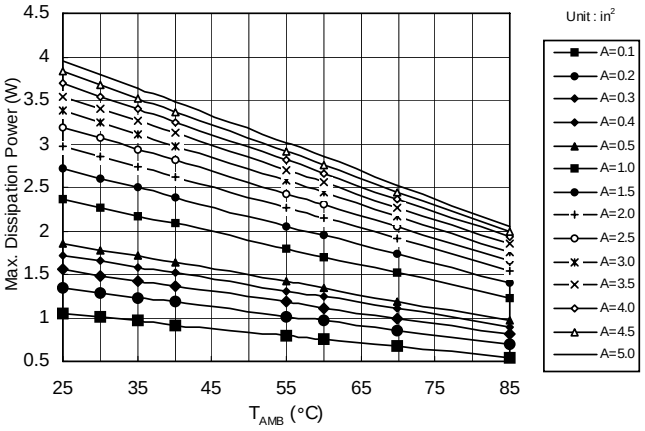
Output Voltage vs. V_{IN}



TO-252 Max. Power Dissipation vs. PCB Top Copper Area
T_{AMB} = 25°C ; Still Air

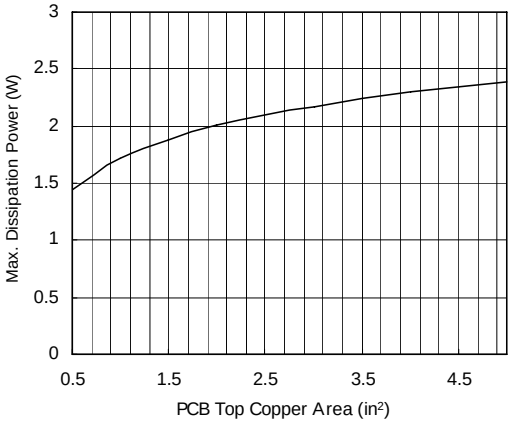


TO-252 Max. Power Dissipation vs. T_{AMB} (still air)
(Different PCB Top Copper Area)

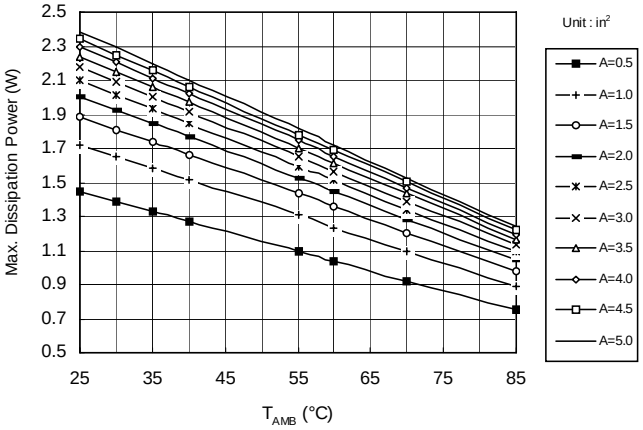


Typical Performance Characteristics (continued)

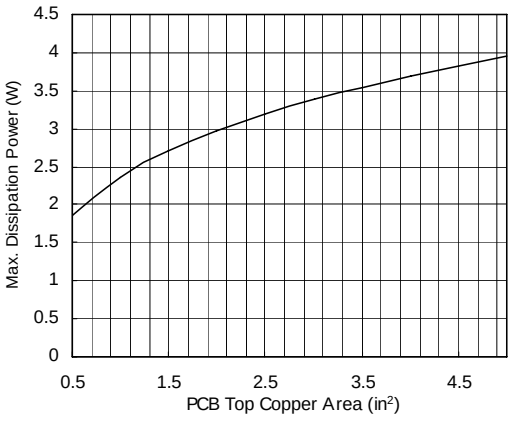
SOP-8 Max. Power Dissipation vs. PCB Top Copper Area
T_{AMB} = 25°C ; Still Air



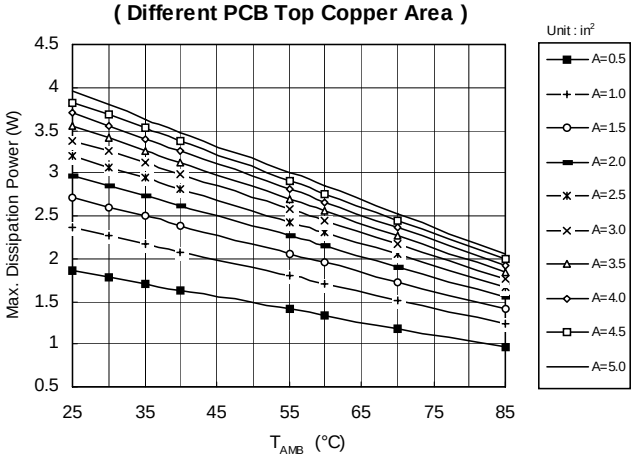
SOP-8 Max. Power Dissipation vs. TAMB (still air) (Different PCB Top Copper Area)



SOP-8 (FD) Max. Power Dissipation vs. PCB Top Copper Area
T_{AMB} = 25°C ; Still Air

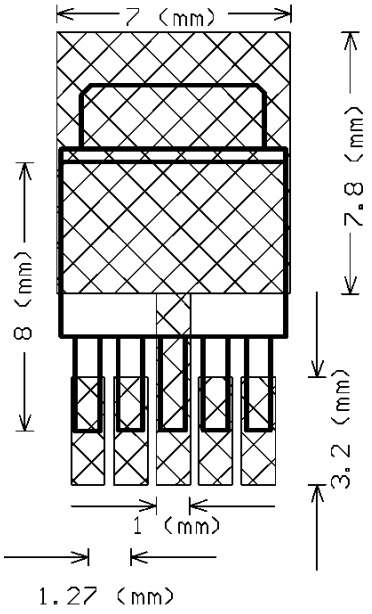


SOP-8 (FD) Max. Power Dissipation vs. TAMB (still air) (Different PCB Top Copper Area)

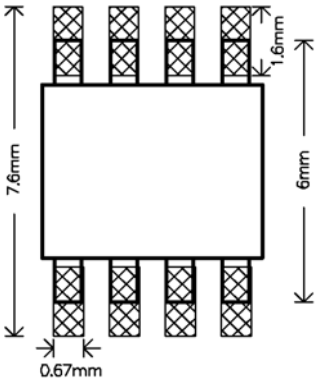


Recommended Minimum Footprint

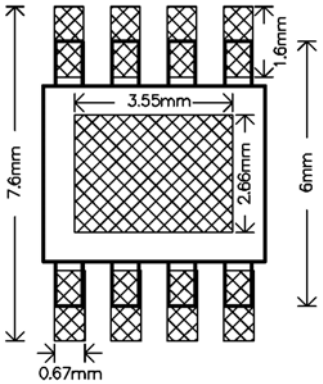
TO-252-5



SOP-8

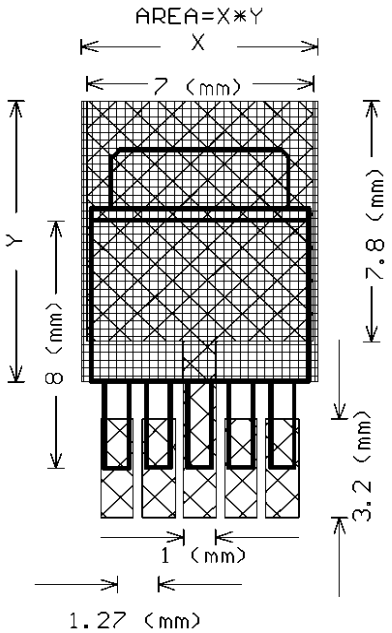


SOP-8 (FD)

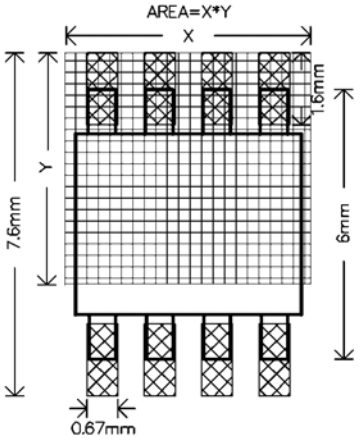


Recommended Ground Layout for Power Dissipation

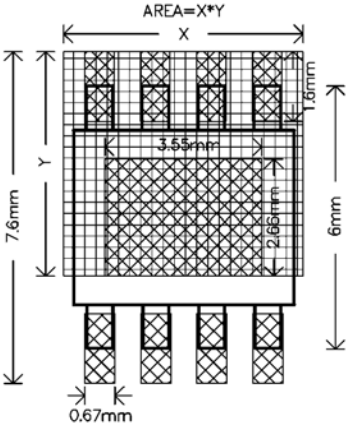
TO-252-5



SOP-8



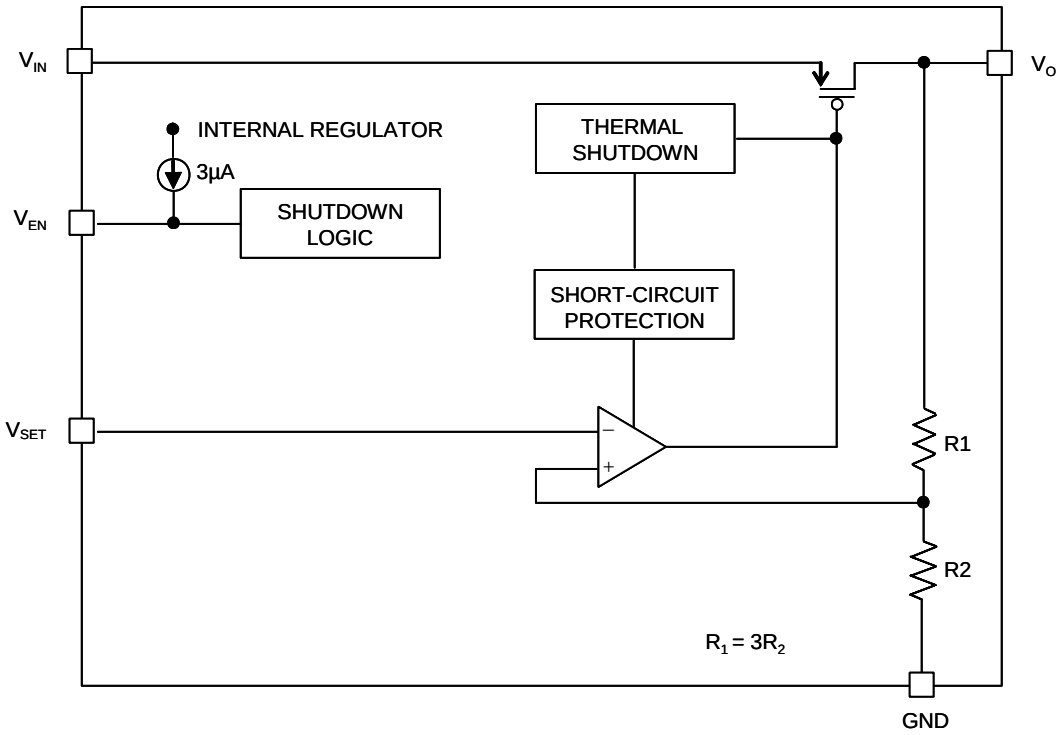
SOP-8 (FD)



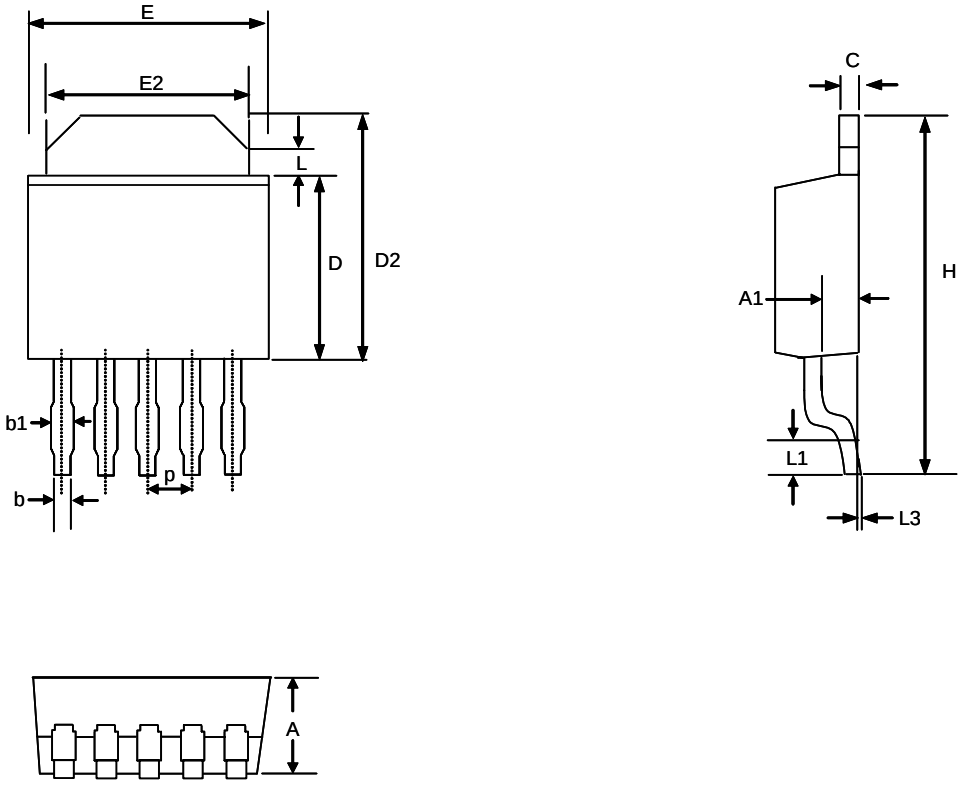
Pin Description

PIN			NAME	FUNCTION
TO-252-5	SOP-8	SOP-8 (FD)		
1	1	1	VO	The pin is the power output of the device. Its voltage is 4.0 times of VSET.
2	2	2	VIN	Input voltage.
4	3	3	VEN	Enable Input. Pulling this pin below 0.3V turns the regulator off, reducing the quiescent current to a fraction of its operating value. Internal weakly pull-high is implemented. If let this pin open, it is still activated.
5	4	4	VSET	This pin sets the output voltage. Its voltage must be larger than 1V to guarantee VO 4.0 times of VSET.
3	5~8	6	GND	Reference ground. Use all four pins on the SO-8 device for heatsinking.
		5,7,8	NC/GND	This pin is no internal connection and should connect to the Ground for power dissipation.
		Thermal Pad		Recommend connecting the Thermal Pad to the GND for excellent power dissipation.

Block Diagram

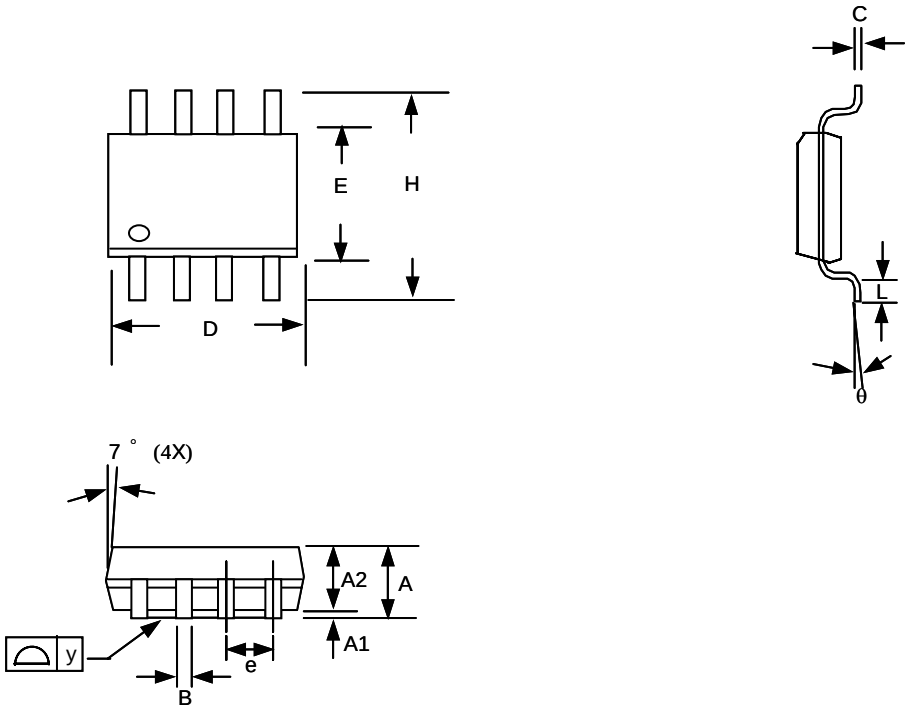


Package Information



TO-252-5 Package

SYMBOL	MILLIMETER		INCH	
	MIN.	MAX.	MIN.	MAX.
A	2.250	2.350	0.089	0.093
A1	0.950	1.050	0.037	0.041
C	0.490	0.530	0.019	0.021
E	6.400	6.600	0.252	0.260
E2	5.300	5.450	0.209	0.215
D	6.000	6.200	0.236	0.244
D2	7.100	7.300	0.280	0.287
H	9.700	10.100	0.382	0.398
L	0.600 REF		0.024 REF	
L1	1.425	1.625	0.056	0.064
L3	0.020	0.120	0.001	0.005
b	0.575	0.625	0.022	0.025
b1	0.590	0.690	0.023	0.027
P	1.270 BSC		0.050 BSC	

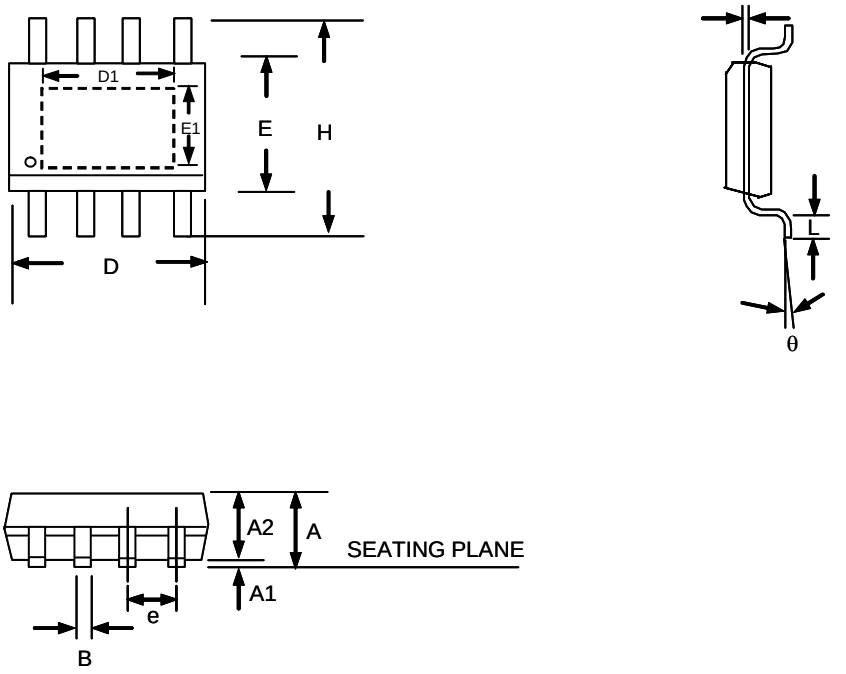


SOP-8 Package

Note:

1. Package body sizes exclude mold flash and gate burrs
2. Dimension L is measured in gage plane
3. Tolerance 0.10mm unless otherwise specified
4. Controlling dimension is millimeter converted inch dimensions are not necessarily exact.

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.35	1.60	1.75	0.053	0.063	0.069
A1	0.10	-----	0.25	0.004	-----	0.010
A2	-----	1.45	-----	-----	0.057	-----
B	0.33	-----	0.51	0.013	-----	0.020
C	0.19	-----	0.25	0.007	-----	0.010
D	4.80	-----	5.00	0.189	-----	0.197
E	3.80	-----	4.00	0.150	-----	0.157
e	-----	1.27	-----	-----	0.050	-----
H	5.80	-----	6.20	0.228	-----	0.244
L	0.40	-----	1.27	0.016	-----	0.050
y	-----	-----	0.10	-----	-----	0.004
θ	0°	-----	8°	0°	-----	8°



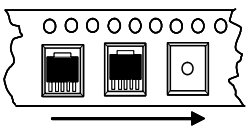
SOP-8 (FD) Package

Note:

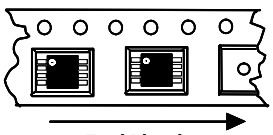
1. JEDEC Outline: MS-012 AA/E.P. Version: N/A
2. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions and gate burrs shall not exceed .15mm (.006in) per side.
3. Dimensions “E” does not include inter-lead flash, or protrusions inter-lead flash and protrusions shall not exceed .25mm (.010in) per side.

SYMBOL	DIMENSION IN MM		DIMENSION IN INCH	
	MIN.	MAX.	MIN.	MAX.
A	1.397	1.753	0.053	0.069
A1	0.00	0.13	0.000	0.005
A2	1.40 TYP		0.055 TYP	
B	0.330	0.508	0.013	0.020
D	4.801	5.004	0.189	0.197
E	3.810	3.988	0.150	0.157
e	1.27 TYP		0.05 TYP	
H	5.791	6.198	0.228	0.244
L	0.508	0.711	0.020	0.028
θ	0°	8°	0°	8°
D1	3.048	3.556.	0.120	0.140
E1	2.159	2.667	0.085	0.105

Taping Specification



Feed Direction
TO-252-5 Package Orientation



Feed Direction
Typical SOP Package Orientation

PACKAGE	Q’TY/REEL
TO-252-5	2,500 ea
SOP-8	2,500 ea
SOP-8 (FD)	2,500 ea