Three-phase motor driver

Features

- **Three-Phase Half-Bridge Drivers**
- **3V to 20V Operating Supply Voltage**
- **2A Continuous Output Current**
- **110mΩ per MOSFET On-Resistance**
- **Built-In 3.3V, 100mA LDO Regulator**
- **Under-Voltage Lockout (UVLO) and Thermal Shutdown Protection**
- **Internal Charge Pump Supports 100% Duty Cycle Operation**
- **Synchronous Rectification**
- **Over-Current Protection (OCP) with Adjustable Threshold**
- **Integrated Bi-Directional Current Sense Amplifiers**
- **Available in QFN-24 (3mm x 4mm) Package**

General Description

The M6543 is a three-phase brushless DC motor driver able to deliver up 2A continuously. It integrates three half-bridges, consisting of six N-channel Power MOSFETs. The M6543 has ENABLE and PWM inputs for each ½-H-bridge along with pre-drivers, gate drive power supplies, and current sense amplifiers. It uses an internal charge pump to generate the gate drive supply voltage for the high-side MOSFETs.

The M6543 has thermal shutdown, under-voltage lockout (UVLO) and over-current protection (OCP) for safe operation.

The M6543 are available in a 24-pin, 3mm x 4mm QFN with an exposed thermal pad.

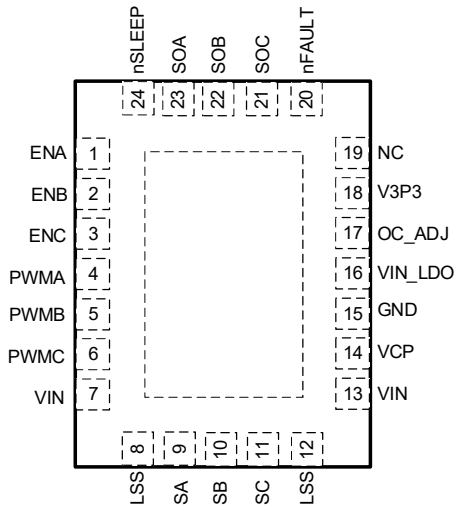
Ordering Information

ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE (Green)
M6543HK1U	6543	-40°C to +125°C	QFN3X4-24

Note: HK: QFN3X4-24
1: Bonding Code
U: Tape & Reel
Green: Lead Free / Halogen Free

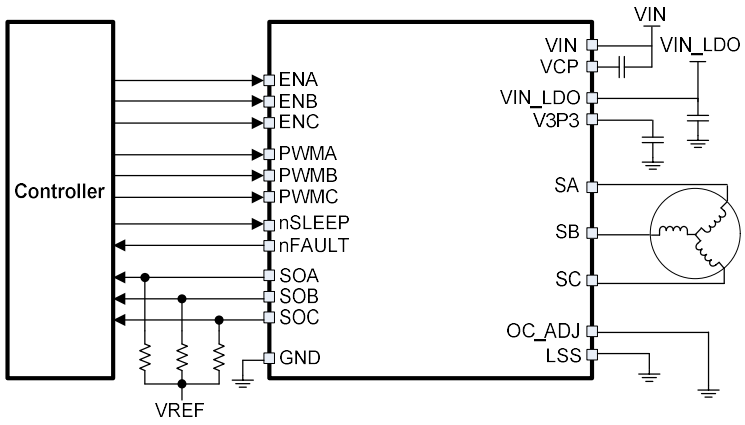
Pin Configuration

Top View



M6543 QFN3X4-24

Application Circuit



Absolute Maximum Ratings(1)

Supply Voltage VIN, VIN_LDO. . . . . -0.3V to +22V
V_{SX}. . . . . -0.3V to VIN+0.3V
VCP. . . . . .-0.3V to VIN+5V
AGND to PGND. . . . . .-0.3V to +0.3V
Voltages at all other pins. . . . . .-0.3V to +5V
Thermal Resistance of Junction to Ambient (θ_{JA})
QFN3X4-24. . . . . .44.9 °C/W
Continuous Power Dissipation (T_A = +25°C)(2)
QFN3X4-24. . . . . 2.6W
Junction Temperature. . . . . .150°C
Storage Temperature Range . . . . . -65°C to 150°C
Lead Temperature (2oldering,10 sec) . . . . . 260°C
ESD (HBM) 2kV
ESD (MM) 200V

Recommended Operating Condition(3)

Supply Voltage V_{IN}, V_{IN_LDO}. . . . . 3V to +20V
Junction Temperature Range. . . . . .-40°C to 125°C
Ambient Temperature Range . . . . . .-40°C to 85°C

Notes:

(1) Exceeding these ratings may damage the device.

(2) The maximum allowable power dissipation is a function of the maximum junction temperature TJ (MAX), the junction-toambient thermal resistance θJA, and the ambient temperature TA. The maximum allowable continuous power dissipation at any ambient temperature is calculated by PD (MAX) = (TJ (MAX)-TA)/θJA. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.

(3) The device is not guaranteed to function outside of its operating conditions.

Electrical Characteristics

(VIN=10V, LSS=GND=0V, T_A = 25°C, unless otherwise noted.)

The device is not guaranteed to function outside its operating conditions.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply						
Input supply voltage	V_{IN}, V_{IN_LDO}		3	---	20	V
Quiescent current	I_Q	nSLEEP = 1, Enx = 0	---	2.5	3.2	mA
	I_{SLEEP_VIN}		---	3	5	μA
	I_{SLEEP_VINLDO}	nSLEEP = 0	---	60	70	μA
Control Logic						
Input logic 'low' threshold	V_{IL}		---	---	0.4	V
Input logic 'high' threshold	V_{IH}		1.5	---	---	V
Logic input current	$I_{IN(H)}$	V = 5V	-20	---	20	μA
	$I_{IN(L)}$	V = 0V	-20	---	20	μA
Power up delay	t_{PUD}	At V_{IN} rising or nSLEEP rising	---	5	---	ms
Internal pull down resistance	R_{PD}	All logic Inputs	---	500	---	kΩ
nFAULT pull down RON	$R_{ON(nFAULT)}$		---	15	---	Ω
V3P3 REGULATOR						
LDO output		IOUT = 0 to 100mA	3.3	3.45	3.6	V
Protection Circuits						
UVLO threshold	V_{UVLO}	V_{IN} rising	2.5	2.7	2.9	V
UVLO hysteresis	ΔV_{UVLO}		---	150	---	mV
OCP threshold	I_{OCP_HS}	OC_ADJ pin connected to GND.	5.5	7.2	9.4	A
OCP deglitch time	t_{OCD}		---	1	---	μs
Thermal Shutdown(4)	T_{TSD}	TJ Rising	---	160	---	°C
Thermal Shutdown Hysteresis(4)	ΔT_{TSD}		---	25	---	°C

Electrical Characteristics (continued)

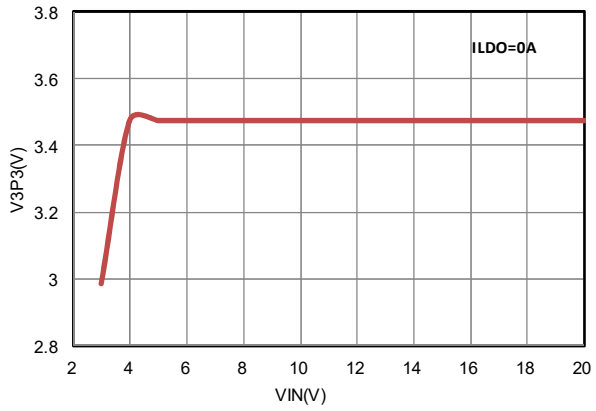
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Current sense						
Current sense ratio			1/3600	1/4000	1/4400	A/A
Current sense output		LS FET current = 1A	235	260	285	μA
		LS FET current = -1A	-285	-260	-235	μA
Current sense output		LS FET current = 100mA	20	25	30	μA
		LS FET current = -100mA	-30	-25	-20	μA
positive and negative matching (ratio of positive to negative)		LS FET current = +-1A	85%	1	115%	
positive and negative matching (ratio of positive to negative)		LS FET current = +-100mA	70%	1	130%	
Phase matching (ratio of phase to phase)		LS FET current = +-1A	85%	1	115%	
Phase matching (ratio of phase to phase)		LS FET current = +-100mA	70%	1	130%	
Current sense output voltage swing		LS FET current = +-0.25A	0	---	3.6	V
Output						
HS FET on resistance	R_{ON}(HS)	IOUT= 1A	90	110	135	mΩ
LS FET on resistance	R_{ON}(LS)	IOUT= 1A	90	110	135	mΩ
Output rise time(4)		R_{LOAD} = 50Ω	---	85	---	nS
Output fall time(4)		R_{LOAD} = 50Ω	---	85	---	nS
Dead Time(4)		R_{LOAD} = 50Ω	---	40	---	nS
PWMx to Sx Delay Time Rising(4)			---	120	---	ns
PWMx to Sx Delay Time Falling(4)			---	140	---	ns
Charge pump						
Charge pump output voltage	V_{CP}		---	V_{IN} +3.45	---	V

Note:
(4) Guaranteed by design

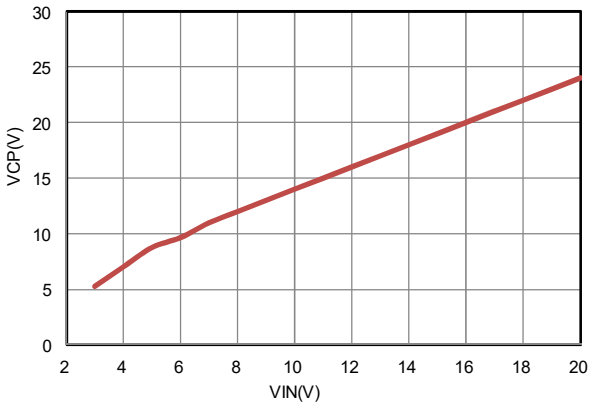
Typical Operating Characteristics

V_{IN}=V_{IN_LDO}=10V, Ambient Temperature=25°C

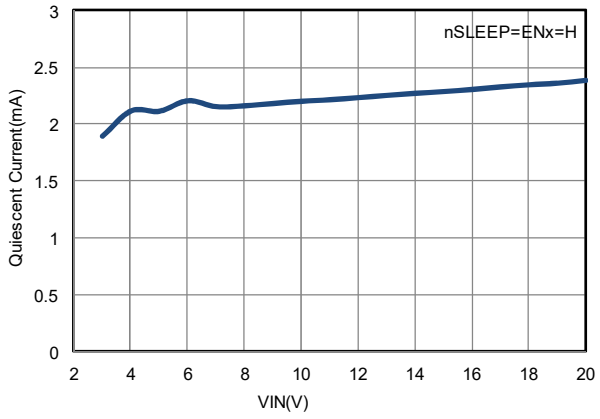
V3P3 vs. VIN



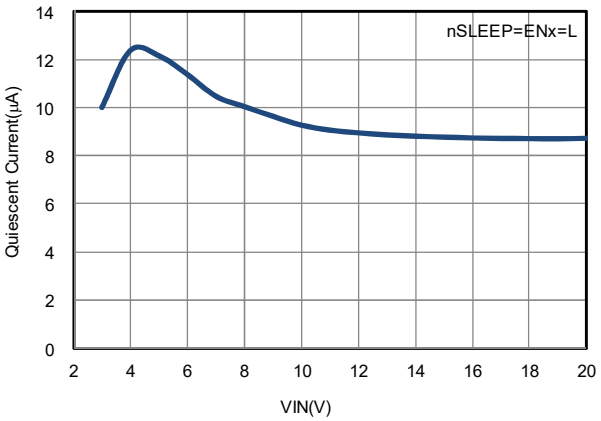
VCP vs. VIN



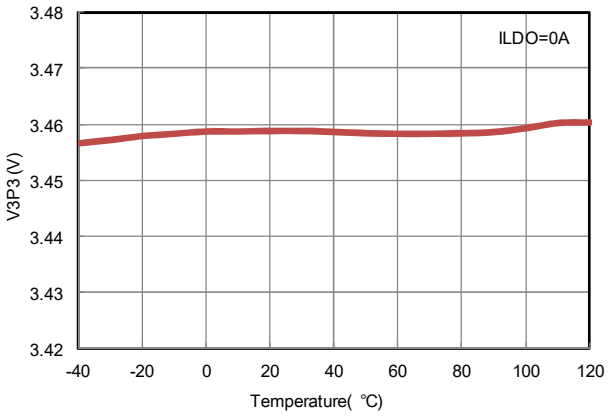
Quiescent current vs. VIN (nSLEEP =ENx = H)



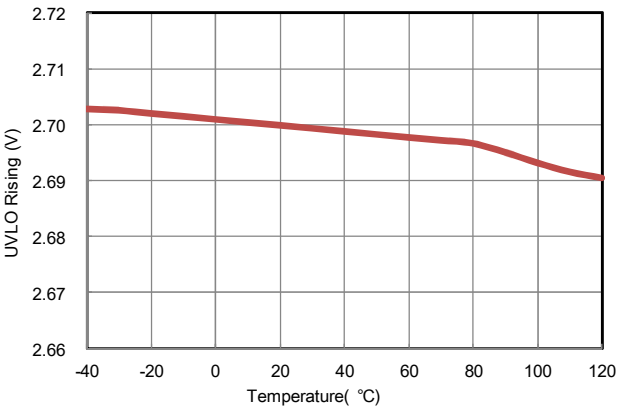
Quiescent current vs. VIN nSLEEP =ENx = L



V3P3 vs. Temperature

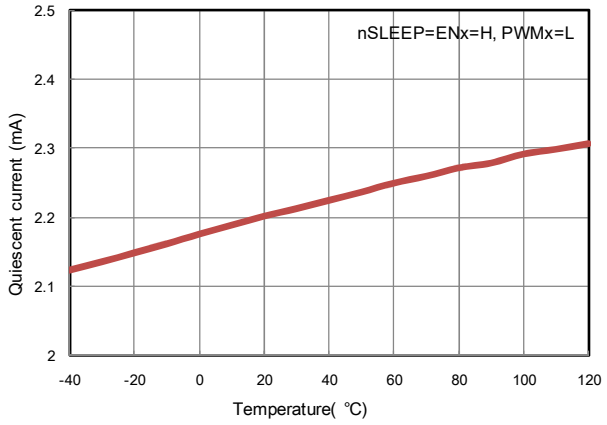


UVLO Rising Voltage vs. Temperature

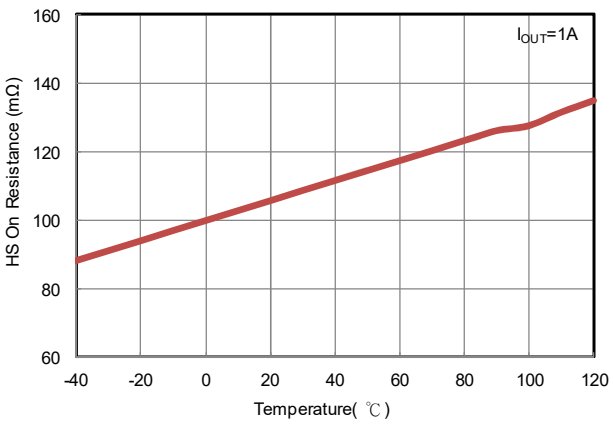


Typical Operating Characteristics (Continued)

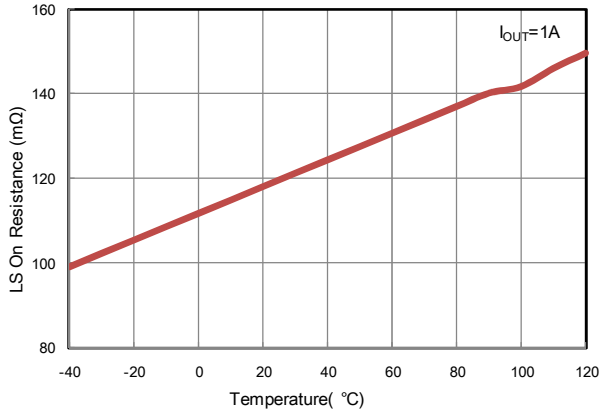
Quiescent current vs. Temperature



HS On Resistance vs. Temperature



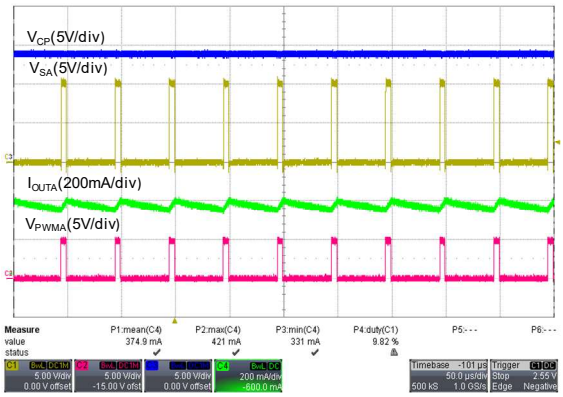
LS On Resistance vs. Temperature



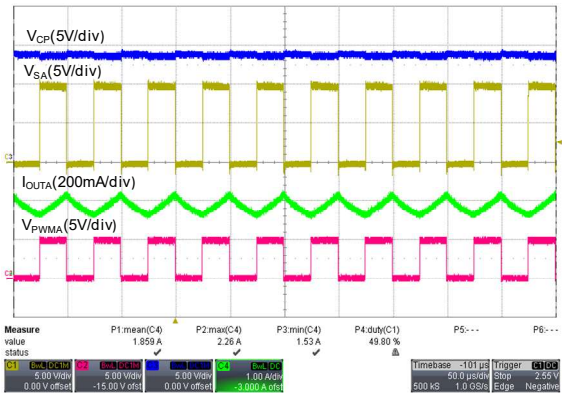
Typical Operating Characteristics

V_{IN}=V_{IN_LDO}=10V, A phase switching with 20kHz frequency, B phase LS on, C phase disable, V_{REF} = 3.3V, current sense resistor divider=1kΩ, T_A=25°C, resistor + inductor load:1Ω +0.47mH/phase with star connection, unless otherwise noted.

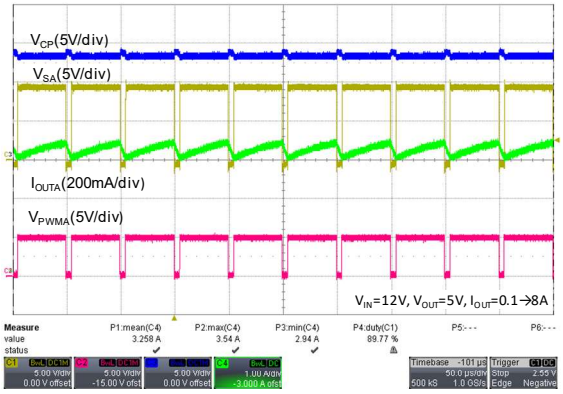
Steady State Duty=10%



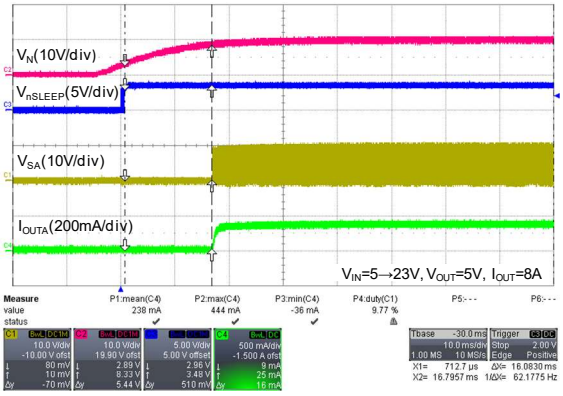
Steady State Duty=50%



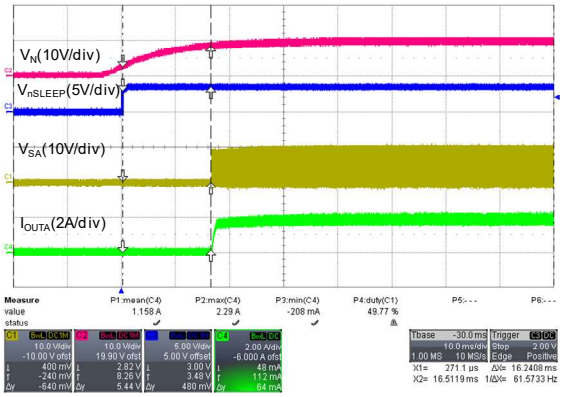
Steady State Duty=90%



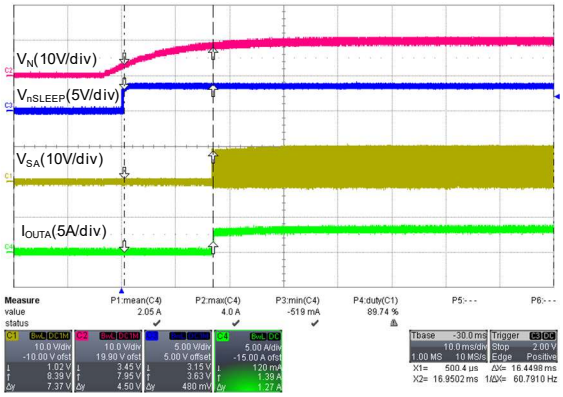
Power Ramp Up Duty=10%



Power Ramp Up Duty=50%

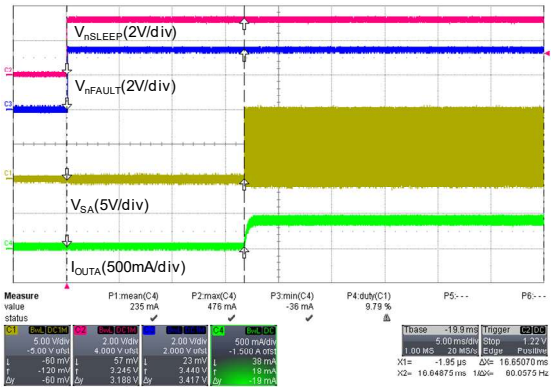


Power Ramp Up Duty=90%

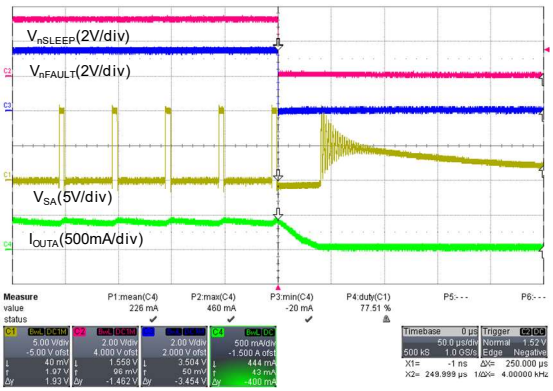


Typical Operating Characteristics (Continued)

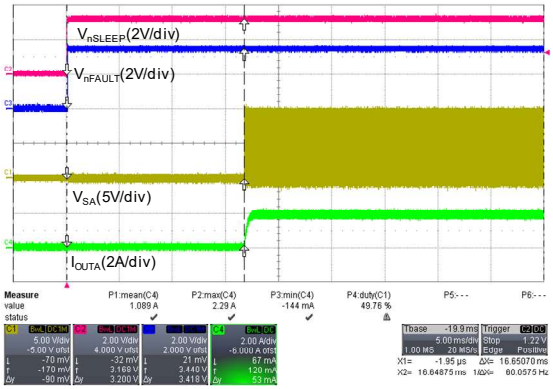
Sleep Recovery Duty=10%



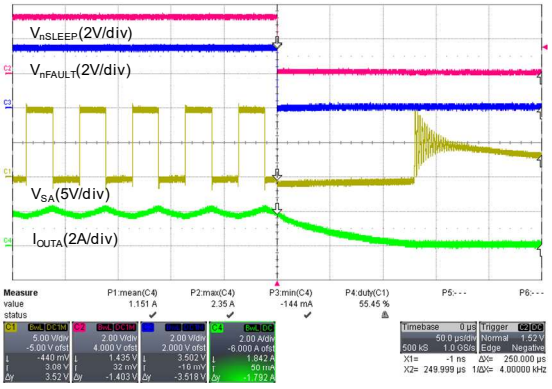
Sleep Entry Duty=10%



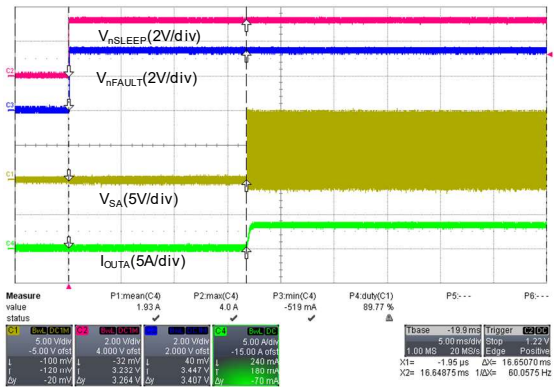
Sleep Recovery Duty=50%



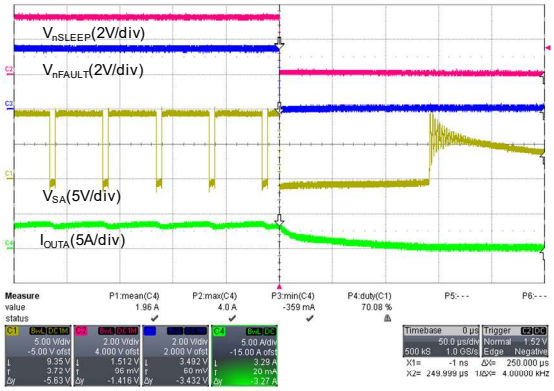
Sleep Entry Duty=50%



Sleep Recovery Duty=50%



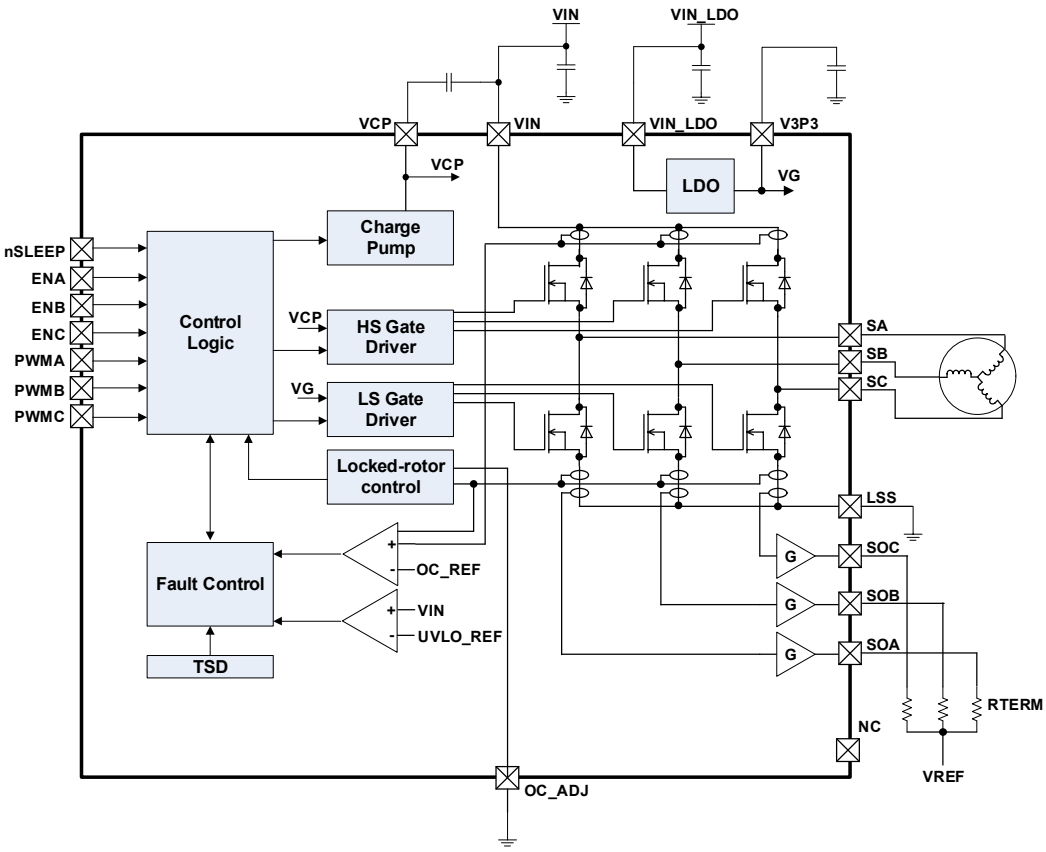
Sleep Entry Duty=90%



Pin Description

PIN	NAME	FUNCTION
1	ENA	Enable input for phase A.
2	ENB	Enable input for phase B.
3	ENC	Enable input for phase C.
4	PWMA	PWM input for phase A.
5	PWMB	PWM input for phase B.
6	PWMC	PWM input for phase C.
7	VIN	Input power.
8	LSS	Low-side source connection for phase A, B, C. Must be connected directly to GND.
9	SA	Phase A output.
10	SB	Phase B output.
11	SC	Phase C output.
12	LSS	Low-side source connection for phase A, B, C. Must be connected directly to GND.
13	VIN	Input power.
14	VCP	Charge pump output. Connect a 1uF ceramic capacitor to VIN.
15	GND	Ground.
16	VIN_LDO	LDO input.
17	OC_ADJ	OC_ADJ pin connected to GND.
18	V3P3	3.3V regulator output. Low-side gate driver supply voltage. Bypass to GND with a 0.47μF ceramic capacitor.
19	NC	NC pin must keep floating.
20	nFAULT	Fault indication. Open-drain output type, logic low when in fault condition.
21	SOC	Current sense output for phase C.
22	SOB	Current sense output for phase B.
23	SOA	Current sense output for phase A.
24	nSLEEP	Sleep mode input. Logic low to enter low-power sleep mode. Internal pull down.

Block Diagram



Operation

Input Logic

The M6543 has logic enable pins ENA, ENB, and ENC, which enables the outputs SA, SB, and SC. When ENx is low, the corresponding output is disabled and the output is high impedance. When ENx is high, the output is enabled, and the PWM input controls the state of the output. Refer to Table 1 for the logic truth table.

Table 1. Input Logic Truth Table of M6543

ENx	PWMx	Sx
H	H	VIN
H	L	GND
L	X	High Impedance

nSLEEP Operation

When nSLEEP is driving low, M6543 is into low power sleep mode. In this mode, all the internal circuits are disabled. When waking up from sleep mode, approximately 1 ms the device responds to inputs. The nSLEEP input has a weak pull-down resistor.

Current Sense Amplifiers

The current flowing in each of the three outputs is sensed by internal low-side current sensing circuits. An output pin for each phase sources or sinks a current that is proportional to the current flowing in each phase.

A termination resistor (RTERM) is connected to a reference voltage to convert the sensing current into a voltage. When current is flowing, the voltage is above or below the reference voltage according to the current flowing direction. The equation is :

$V_{SO} = V_{REF} + (R_{TERM} * I_{LOAD}) / 4000$

Automatic Synchronous Rectification

When the output MOSFETs are both turned off, inductor current must continue to flow. This current normally is passed through the MOSFET body diodes and therefore more power dissipation in the body diodes.

When both the HS and LS MOSFETSs are turned off, if the voltage on an Sx output pin is driven below ground, the LS MOSFET is turned on until the current flowing through it reaches near zero, or until the HS MOSFET is commanded to turn on. Similarly, if the voltage on the Sx pin rises above VIN, the HS MOSFET is turned on until the current reaches near zero, or the LS MOSFET is turned on.

nFAULT Output

An nFAULT output pin is driven active low for a fault condition. An over-current protection (OCP) or over-temperature protection (OTP) is driven nFAULT pin active low. This pin is an open-drain output type and must be pulled up by an external pull up resistor.

Input UVLO Protection

If the voltage on the VIN pin falls below the UVLO threshold voltage, all circuitry in the device will be disabled and internal logic will be reset. When VIN rises above the UVLO threshold, operation will resume.

Thermal Shutdown

If the die temperature exceeds safe limits, all output FETs will be disabled and the nFAULT pin will be driven low. When the die temperature has fallen to a safe level operation will automatically resume.

Over-current Protection

If the over-current threshold is reached and lasts for longer than the over-current deglitch time, all six output FETs will be disabled (outputs become high impedance) and the nFAULT pin will be driven low. During this time current will be recirculated through the body diodes. The over-current shutdown is latched in this case until either nSLEEP is reset or VIN power is cycled.

Over-current conditions on both high and low side devices; i.e., a short to ground, supply, or across the motor winding will all result in an over-current shutdown.

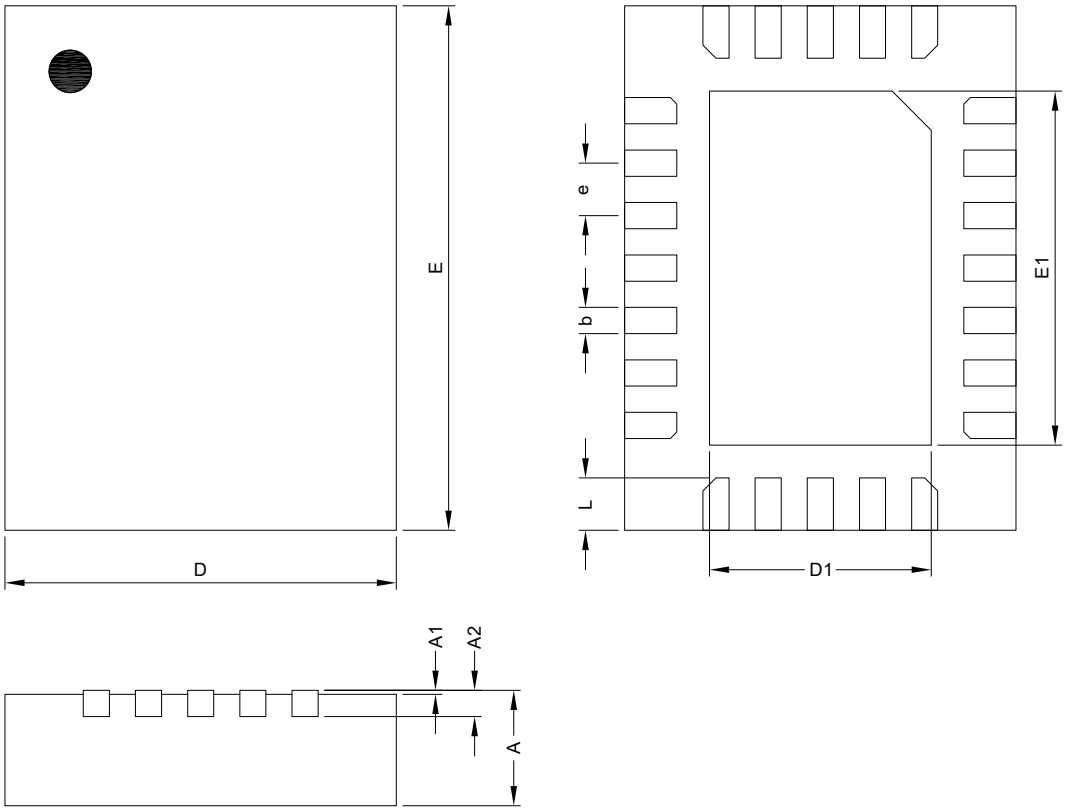
3.3V LDO output

An internal regulator generates a 3.3V voltage with 100mA capacity, which could be used to power a small low-power microcontroller. A bypass capacitor of 4.7μF~10μF is required from the V3P3 pin to ground.

Charge Pump

A charge pump is used to generate the gate drive for the high-side MOSFETs. The charge pump requires one external capacitor 1μF ceramic capacitor rated for at least 10V between VIN and VCP.

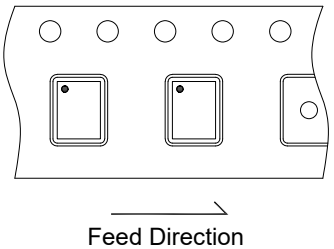
Package Information



QFN3X4-24 Package

Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.85	0.90	0.0315	0.0335	0.0354
A1	0.00	- - -	0.05	0.0000	- - -	0.0020
A2		0.203 REF			0.0080 REF	
D	2.95	3.00	3.05	0.1161	0.1181	0.1201
E	3.95	4.00	4.05	0.1555	0.1575	0.1594
D1	1.65	1.70	1.75	0.0650	0.0670	0.0689
E1	2.65	2.70	2.75	0.1043	0.1063	0.1083
b	0.15	0.20	0.25	0.0059	0.0079	0.0098
e		0.40 BSC			0.0157 BSC	
L	0.30	0.40	0.45	0.0138	0.0157	0.0177

Taping Specification



PACKAGE	Q'TY/REEL
QFN3X4-24	3,000ea